Lattice Semiconductor Data Book 1996

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Lattice™ Semiconductor Corporation

ispLSI and pLSI Product Index

Part #	Pins	Density (PLD Gates)	Tpd (ns)	Fmax (MHz)	Description	Page
ispLSI / pLSI 1016E	44	2000	7.5, 10	125, 100	64 Macrocell High-Density PLD	2-47
ispLSI / pLSI 1016	44	2000	10, 12, 15, 20	110, 90, 80, 60	64 Macrocell High-Density PLD	2-61
ispLSI / pLSI 1024	68	4000	12, 15, 20	90, 80, 60	96 Macrocell High-Density PLD	2-79
ispLSI / pLSI 1032E	84	6000	10, 12, 15	90, 80, 70	128 Macrocell High-Density PLD	2-95
ispLSI / pLSI 1032	84	6000	12, 15, 20	90, 80, 60	128 Macrocell High-Density PLD	2-111
ispLSI / pLSI 1048E	128	8000	10, 15, 20	90, 70, 50	192 Macrocell High-Density PLD	2 -129
ispLSI / pLSI 1048C	128	8000	16, 22	70, 50	192 Macrocell High-Density PLD	2 -143
ispLSI / pLSI 1048	120	8000	15, 18, 24	80, 70, 50	192 Macrocell High-Density PLD	2-159
ispLSI / pLSI 2032	44	1000	5.5, 7.5, 10, 15	150, 135, 110, 80	32 Macrocell High-Density PLD	2-175
ispLSI / pLSI 2064	84	2000	7.5, 10, 15	125, 100, 80	64 Macrocell High-Density PLD	2-191
ispLSI / pLSI 2096	128	4000	7.5, 10, 15	125, 100, 80	96 Macrocell High-Density PLD	2-207
ispLSI / pLSI 2128	160	6000	10, 15	100, 80	128 Macrocell High-Density PLD	2-221
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ispLSI / pLSI 3192	240	8000	10, 15	100, 70	192 Macrocell High-Density PLD	2-251
ispLSI / pLSI 3256	160	11000	15, 20	70, 50	256 Macrocell High-Density PLD	2-267
ispLSI / pLSI 6192	208	25000	15, 20	70, 50	192 Macrocell High-Density Cell-Based PLD with Dedicated Memory and Register/Counter Modules	2-287

GAL Product Index

Part #	Pins	Tpd (ns)	Fmax (MHz)	Icc (mA)	Isb (µA)	Description	Page
GAL16LV8	20	3.5, 5, 7.5, 10, 15	250, 166, 100, 83.3, 62.5	70, 65	—	3.3V Ultra-Fast 20-Pin PLD	3-5
GAL16LV8ZD	20	15, 25	62.5, 41.6	55	100	3.3V Zero-Power 20-Pin PLD	3-27
GAL16V8Z/ZD	20	12, 15	83.3, 62.5	55	100	Zero-Power 20-Pin PLD	3-45
GAL16V8	20	5, 7.5, 10, 15, 25	166, 100, 62.5, 41.6	115, 55, 90	—	Universal 20-Pin PLD	3-65
GAL16VP8	20	15, 25	80, 50	115	—	64mA High Output Drive 16V8	3-89
GAL18V10	20	7.5, 10, 15, 20	111, 105, 66.7, 62.5	115	—	22V10 Subset	3-107
GAL20RA10	24	7.5, 10, 15, 20, 30	83.3, 71.4, 50, 41.7, 25	100	—	Asynchronous – 10 Prog. Clocks	3-123
GAL20LV8	24	3.5, 5, 7.5	250, 166, 125	70	—	3.3V Ultra-Fast 24-Pin PLD	3-139
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GAL20V8Z/ZD	24	12, 15	83.3, 62.5	55	100	Zero-Power 24-Pin PLD	3-175
GAL20V8	24	5, 7.5, 10, 15, 25	166, 100, 62.5, 41.7	115, 55, 90	—	Universal 24-Pin PLD	3-195
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In-System Programmable Generic Digital Switch Product Index

Part #	Pins	Tpd (ns)	Fmax (MHz)	Icc (mA)	Description	Page
ispGDS22/18/14	28/24/20	7.5	50	40	11x11 / 9x9 / 7x7 Programmable Switch Matrix	4-5

Thank you for your interest in Lattice Semiconductor Corporation's programmable logic products. Lattice Semiconductor offers the world's highest performance and broadest product line of high density and low density CMOS PLDs.

This data book includes our industry leading ISP™ High Density PLDs and industry standard GAL® product line. In addition, information on our extensive line of software solutions is provided. Together, these innovative products solve every application requirement.

Lattice Semiconductor, the worldwide leader in E^2CMOS® and In-System Programmable™ (ISP) PLDs, is committed to supplying you with the optimal solution to all of your programmable logic requirements.

Sincerely,

Steven A. Laub
Vice President and General Manager
Lattice Semiconductor Corporation

Lattice Semiconductor Corporation

1996 Data Book

Lattice Semiconductor Corporation

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Section 1

Introduction

Background

Through pioneering efforts in applying E^{2}CMOS® technology to programmable logic, Lattice Semiconductor Corporation (LSC) has established the GAL® family of products as the industry standard worldwide. With the introduction of the in-system programmable Large Scale Integration (ispLSI®) devices and high-density programmable Large Scale Integration (pLSI®) devices, Lattice Semiconductor has become the world's largest supplier of low-density CMOS PLDs and the fastest growing supplier of high-density CMOS PLDs.

The Lattice Semiconductor Advantage

Time-to-Market

E^{2}CMOS PLDs enable system designers to meet ever-shrinking time-to-market constraints while avoiding the significant development costs, lead times, and dedicated inventories associated with traditional ASIC and bipolar PLD solutions.

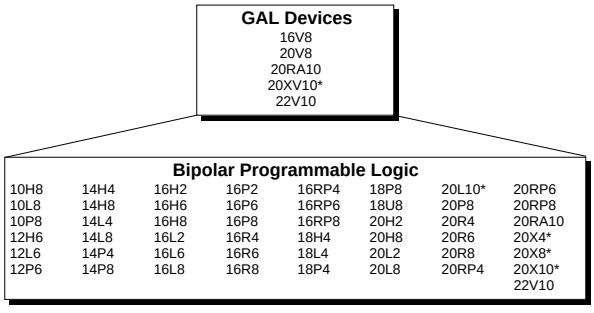
Flexibility

Programmable and reprogrammable devices enable fast and easy modifications to system designs.

Product Differentiation

LSC's programmable devices allow design engineers to easily differentiate their end-product through proprietary feature enhancements. This is particularly true when a system utilizes the non-volatile ISP™ (In-System Programmable™) technology pioneered by LSC.

Figure 1. Five GAL devices replace virtually all bipolar PAL devices.



* GAL20XV10 replaces 20L10, 20X10, 20X8 and 20X4

Inventory Reduction

A single standard part type can be used in multiple, diverse applications. Just five GAL architectures replace virtually all bipolar PAL® architectures (see Figure 1).

Products

The Lattice Semiconductor PLD product offering can be segmented into two strategic product thrusts:

Low Density: GAL Family

- 100 - 1,000 Gates
- The Highest Performance PLDs from Any Supplier
- 3.3 and 5 Volt Options
- Superior Replacements for Bipolar and CMOS PLD Architectures
- E^{2}CMOS Low-Power, Quality and Reliability
- Broadest Range of PLD Architectures Offering Features not Available in Other PLDs
- Pioneering Non-Volatile In-System Programmability (ISP)

High Density: ispLSI and pLSI Families

- 1,000 - 25,000 Gates (World's Largest)
- World's Fastest High-Density PLDs
- 3.3V and 5 Volt Options
- Superior Architectures (Flexible, Predictable Performance)
- Dedicated, On-Chip Memory (ispLSI and pLSI 6000)
- Pioneering Non-Volatile In-System Programmable (ISP) Technology
- Comprehensive Portfolio of Development Tools

Introduction

Product Features

There are three fundamental features which LSC PLDs share: E²CMOS technology, performance leadership and innovation.

E²CMOS Technology

All GAL, ispLSI and pLSI devices are manufactured using Lattice Semiconductor's proprietary high-speed UltraMOS® E²CMOS technology. LSC is unique among "fab-less" companies in that the process technology development is actually done by Lattice Semiconductor. UltraMOS technology successfully combines the best features of CMOS and NMOS process technology to yield PLDs with the following key features:

- Industry Leading Performance
- High Logic Densities
- Low Power Consumption
- Non-Volatile, In-System Programmability
- Fast Erase and Reprogram Times
- 100% Full Parametric Testability
- 100% Programming and Functional Yields

Performance Leadership

LSC continues its long track record of producing the fastest CMOS PLDs in the market. These industry-leading high-performance products are typically available to the market months ahead of any other PLD supplier. As a result, LSC customers have always been able to take full advantage of next generation microprocessor speeds and bring out industry leading end-products of their own, thus fueling their own success.

While speed continues to be a top priority, Lattice Semiconductor has also introduced PLD families which address other logic design concerns such as 3.3 Volt operation (GAL16/20LV8 and GAL22LV10), low power ("Zero-Power" GAL16/20V8Z and GAL16/20V8ZD), high output drive (GAL16/20VP8) and logic density (GAL26CV12).

Innovation

The third, and perhaps the most important attribute of Lattice Semiconductor's products is technology and architectural innovation. LSC's most far-reaching innovation may have been the decision in 1984 to combine E²CMOS technology with the PLD architecture when all other PLD suppliers were offering UV erasable EPROM technology. This marriage yielded the GAL product family — the "First Revolution in PLD Design."

LSC innovation also started the "Second Revolution in PLD Design" with the introduction of the first non-volatile in-system programmable high-density PLD family — ispLSI and reinforced with the introduction of the ispGAL22V10 and ispGDS families.

The ISP product families of ispLSI, ispGAL and ispGDS devices dramatically impact system development and manufacturing. LSC ISP solutions deliver:

Effortless Prototyping: Design iterations can be downloaded directly to the ISP device soldered onto the prototype board.

Reconfigurable Systems: A single generic board can be "personalized" to one of many system configurations at final board-level test.

Simplified Manufacturing: Eliminates all stand-alone programming steps. Device programming can be done as part of board-level testing. The result is no misprogrammed devices, no inventory headaches keeping track of patterned devices, and no PLD rework costs.

No More Bent Leads: ISP technology also solves the handling problems associated with high pin count, fine pitch packages (PQFP, TQFP etc.). Programming devices in-system eliminates bent leads and unreliable solder joints.

Summary

Lattice Semiconductor, the leader in E²CMOS PLDs, is committed to providing its customers with industry-leading programmable solutions. We realize that your system design requirements and time-to-market pressures will only get tougher in the future. LSC is committed to supporting you with state-of-the-art products with the performance, architecture, quality and reliability that satisfy your requirements.

Section 2

Introduction to ispLSI® and pLSI® Families

The ispLSI and pLSI Families

Lattice Semiconductor Corporation's (LSC) in-system programmable Large Scale Integration (ispLSI) and programmable Large Scale Integration (pLSI) families are the logical choice for your next design project. They're the first programmable logic devices to combine the performance and ease of use of PLDs with the density and flexibility of FPGAs. And at 154 MHz system speed, and up to 25,000 PLD gates, they're the world's fastest and highest density programmable logic devices!

There are five ispLSI and pLSI families to fit your specific application needs. LSC's premier ispLSI and pLSI 1000 family implements high integration functions such as controllers, LANs and encoders at high speeds. The second generation ispLSI and pLSI 1000E family increases in-system performance with enhanced logic utilization. The high performance ispLSI and pLSI 2000 family with its large number of I/Os handles timers and counters, as well as timing critical interfaces to high speed RISC/CISC microprocessors. The highest density ispLSI and pLSI 3000 family integrates complete system logic, DSP functions, and entire encryption or compression logic into a single package, while delivering superior performance. Finally, the ispLSI and pLSI 6000 family combines dedicated FIFO or RAM memory modules with programmable logic in a cell-based architecture to yield single-chip solutions to the most complex system design problems.

The ispLSI family incorporates Lattice Semiconductor's innovative in-system programmable™ (ISP™) technology. ISP technology allows for real-time programming, less expensive manufacturing and end-user feature reconfiguration.

ispLSI and pLSI 1000 and 1000E: The Premier High Density Families

- ❑ 125 MHz system performance
- ❑ 7.5 ns pin-to-pin delay (maximum)
- ❑ 2,000-8,000 PLD gates
- ❑ 44-pin to 128-pin packages

ispLSI and pLSI 2000: Unparalleled System Performance

- ❑ 154 MHz system performance (World's Fastest!)
- ❑ 5.5 ns pin-to-pin delay (maximum)
- ❑ 1,000-6,000 PLD gates
- ❑ 44-pin to 176-pin packages
- ❑ High I/O to logic ratio

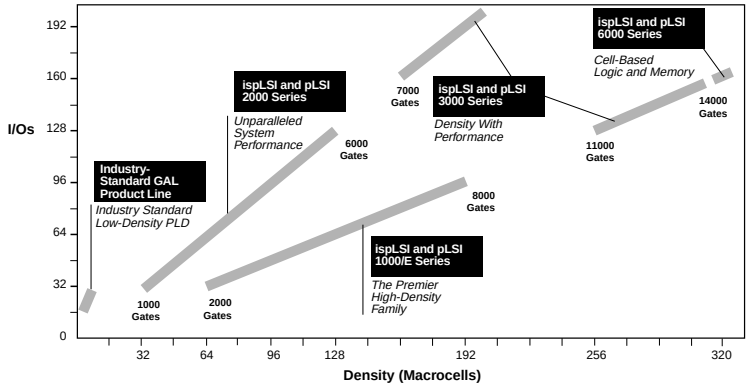
ispLSI and pLSI 3000: Density with Performance

- ❑ 100 MHz system performance
- ❑ 10 ns pin-to-pin delay (maximum)
- ❑ 8,000-14,000 PLD gates
- ❑ 208-pin to 240-pin packages
- ❑ Boundary scan for enhanced testability

ispLSI and pLSI 6000: Cell-Based Logic and Memory

- ❑ 70 MHz system performance
- ❑ 15 ns pin-to-pin delay (maximum)
- ❑ 25,000 PLD gates (including 4,000-bit dedicated memory module and eight-bank register/counter module)
- ❑ 20 ns FIFO/single-port/dual-port memory options
- ❑ 208-pin package
- ❑ Boundary scan for enhanced testability

Lattice Semiconductor's ispLSI and pLSI Families



Introduction to ispLSI and pLSI

Family Overview

From registers to counters, multiplexers to complex state machines, these families of high-density programmable logic will address your high-performance system logic needs.

Each device contains multiple Generic Logic Blocks (GLBs) designed to maximize system flexibility and performance. And a generous supply of registers and I/O cells provides the optimum balance of internal logic and external connections. A global interconnect scheme ties everything together, enabling high logic utilization.

ispLSI and pLSI Architecture

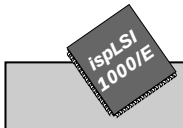
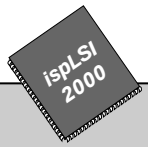
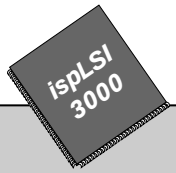
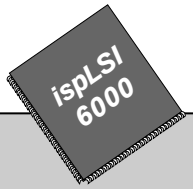
The ispLSI and pLSI architecture was constructed with real system design requirements in mind. Figure 1 shows the representation of the ispLSI 3256 architecture. This architecture provides the designer with the following advantages:

- ❑ High speed
- ❑ Predictable performance
- ❑ Low power
- ❑ Flexible architecture
- ❑ Easy to use
- ❑ Design portability across all the families
- ❑ Non-volatile in-system programmable (ispLSI)
- ❑ Advanced Global Clock Network
- ❑ Boundary Scan (3000 and 6000 families)
- ❑ Built-in memory (6000 family)

The Global Routing Pool

Central to the ispLSI and pLSI architecture is the Global Routing Pool (GRP), which connects all of the internal logic and makes it available to the designer. The GRP provides complete interconnectivity with fixed and predictable delays. This unique interconnect scheme

Table 1. ispLSI and pLSI Family Attributes

	ispLSI & pLSI 1000/E Family	ispLSI & pLSI 2000 Family	ispLSI & pLSI 3000 Family	ispLSI & pLSI 6000 Family
				
Density (PLD Gates)	2,000 - 8,000	1,000 - 6,000	8,000 - 14,000	25,000
Speed: Fmax (MHz)	125 - 60	154 - 80	100 - 50	70 - 50
Speed: Tpd (ns)	7.5 - 20	5.5 - 15	10 - 20	15 - 20
Macrocells	64 - 192	32 - 128	192 - 320	192
Registers	96 - 288	32 - 128	384 - 480	416*
Memory (Bits)	—	—	—	4608
Inputs & I/Os	36 - 110	34 - 136	128 - 192	159
Pins/Package	44-, 68-, 84-pin PLCC 44-, 100-pin TQFP 120-,128-pin PQFP 44-, 68-pin JLCC 84-, 133-pin CPGA	44-, 84-pin PLCC 44-, 100-, 128-, 176-pin TQFP 128-pin PQFP 160-pin MQFP	160-, 208-, 240-pin MQFP 167-pin CPGA	208-pin MQFP

*Includes 8 x 16 Register/Counter Module

1/2/3000-2

consistently provides high performance and allows effortless implementation of complex designs.

The Output Routing Pool (ORP)

The Output Routing Pool (ORP) is a unique ispLSI and pLSI architectural feature which provides flexible connections between the GLB outputs and the output pins. This flexibility allows for "last minute" logic design changes to be implemented without changing the external pin-out.

Generic Logic Block (GLB)

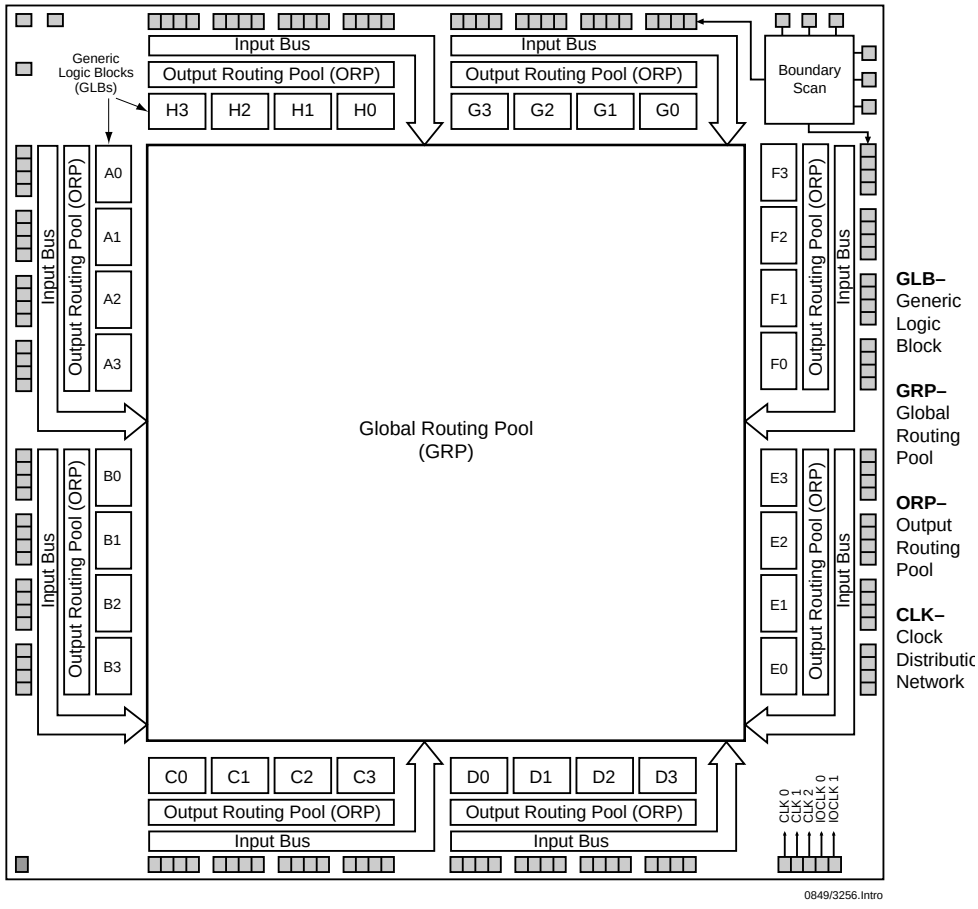
The key element in the ispLSI and pLSI architecture is the Generic Logic Block (GLB). This powerful logic block provides a high input-to-output ratio for best logic efficiency. The GLB (figure 2) used in the ispLSI and pLSI 1000/E and 2000 families feature 18 inputs which drive an array of 20 Product Terms (PTs). These product terms feed four outputs which effectively handle both wide and narrow gating functions. The ispLSI and pLSI 3000 family utilizes a Twin GLB which delivers wider logic functionality. The Twin GLB accepts 24 inputs and feeds two arrays of 20 Product Terms that ultimately drive two sets of four outputs.

The architectural flexibility of the ispLSI and pLSI GLB, combined with its optimum input-to-output ratio, allows the GLB to implement virtually all 4-bit and 8-bit MSI functions.

An additional element of architectural flexibility is the Product Term Sharing Array (PTSA). The PTSA allows the 20 PTs from the AND array to be shared with any and all of the four GLB outputs. This ability to share PTs between all of the four GLB outputs provides a highly efficient means to implement complex state machines by eliminating duplicate product term groups.

Each of the four outputs from the PTSA feeds into a flexible Output Logic Macrocell (OLMC), consisting of a D-type flip-flop with an Exclusive-OR gate on the input. The OLMC allows each GLB output to be configured as either combinatorial or registered. Combinatorial mode

Figure 1. ispLSI 3256 Functional Block Diagram



is available as AND-OR or Exclusive-OR. Registered mode is available as D, T or J-K.

The power of the GLB is further enhanced by a flexible clock distribution network. This network provides a choice of clock signals to each GLB: global synchronous clock signals or internally generated asynchronous product term clock signals.

Standard Configuration

- ❑ GLB outputs comprised of 4, 4, 5 and 7 product terms
- ❑ The PTSA can combine up to 20 product terms per GLB output to meet the needs of both wide and narrow logic functions

Figure 2. ispLSI and pLSI 1000, 1000E and 2000 Family GLB

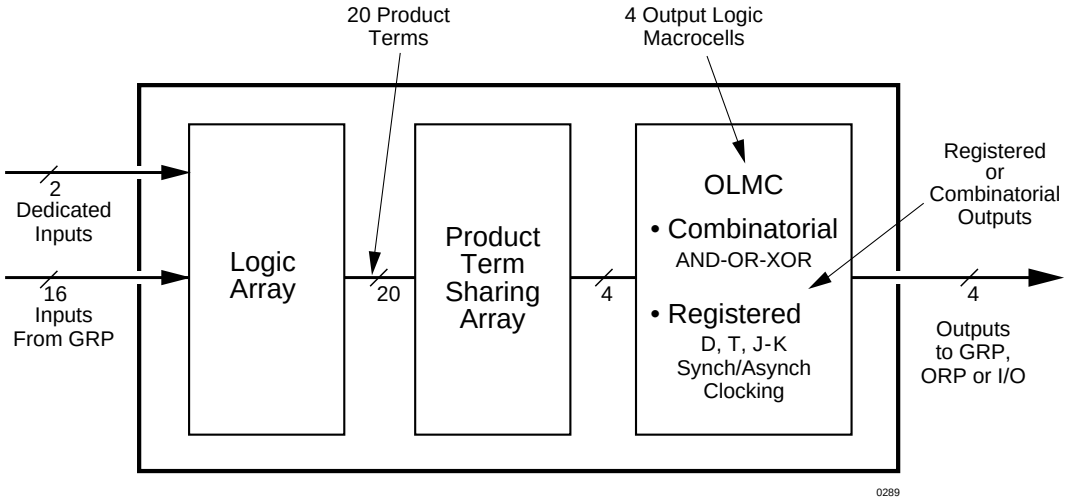
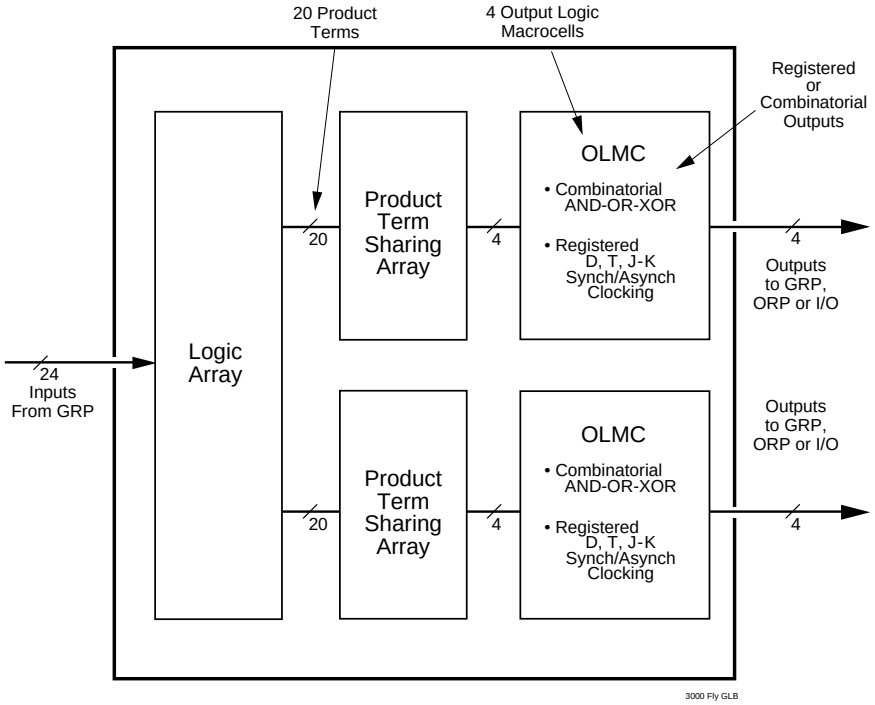


Figure 3. ispLSI and pLSI 3000 and 6000 Family "Twin GLB"



High-Speed Bypass Configuration

- ❑ For speed-critical timing paths
- ❑ Bypasses the PTSA and the Internal Exclusive-OR gate of the OLMC
- ❑ Provides four product terms per output
- ❑ Supports design of fast address decoders

Exclusive-XOR Configuration

- ❑ Utilizes powerful exclusive-XOR architecture
- ❑ Great for counters, comparators and ALU functions

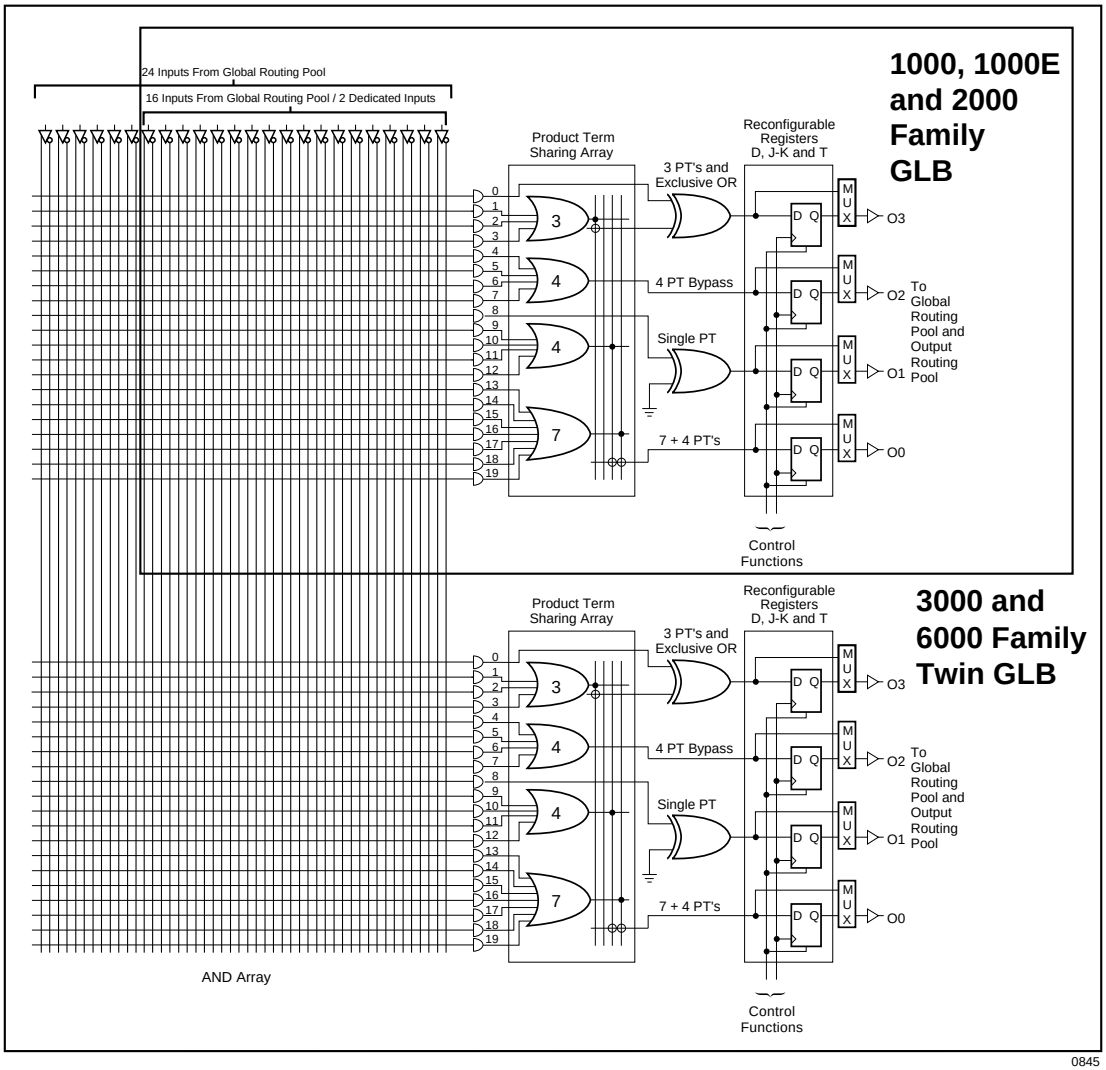
Single PT Configuration

- ❑ Small Logic Functions at Fast Speed

Multi-Mode Configuration

- ❑ Individual outputs are independently configurable
- ❑ PTSA gives flexibility in the number and selection of product terms per output

Figure 4. GLB: Multi-Mode Configuration



Security Cell

A security cell is provided in the ispLSI and pLSI devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by reprogramming the device, so the original configuration can never be examined once this cell is programmed.

Device Programming

ispLSI and pLSI devices can be programmed using a Lattice Semiconductor-approved device programmer, available from a number of third party manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is automatic and is completely transparent to the user. In-system programming is also available with ispLSI devices which allows programming on the circuit board using Lattice Semiconductor programming algorithms and standard 5V system power.

Latch-up Protection

ispLSI and pLSI devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the internal circuitry to latch-up. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

In-System Programmability

LSC's ispLSI devices (in-system programmable) are the industry's only high-density programmable logic family offering non-volatile, in-system reconfigurability.

ispLSI devices are available in all five families: 1000, 1000E, 2000, 3000 and 6000. The ispLSI devices are 100 percent functionally and parametrically compatible with their pLSI counterparts, with the added capability for 5-volt in-system programmability and reprogrammability.

Complex logic functions can be implemented in multiple ispLSI devices with complete on-board configurability. In-system programming of a multiple ispLSI chip solution is easily achieved through a proprietary in-system erase/program/verify technique.

In-system programmability can revolutionize the way you design, manufacture and service systems.

Prototype Board Designs

In-system programming allows you to program and modify your logic designs "in-system" without removing the device(s) from the board. This accelerates the system and board-level debug process and enables you to define the board layout earlier in the design process.

Fine Pitch Package Handling

When programming traditional PLDs, manual handling is required during both design/debugging and manufacturing stages. When using PQFPs or TQFPs, fragile leads as thin as 0.5 mm can easily bend in the programmer socket causing coplanarity damage. With ispLSI, you can solder these packages onto your printed circuit board and still program and reprogram the devices during debugging and manufacturing – without ever losing a single part due to bent leads.

Reconfigurable Systems

Your options become boundless when you have the ability to change the functionality of devices already soldered on a PC board. You can now implement multiple hardware configurations with the same circuit board design. A variety of protocols or system interfaces can be implemented on a generic board as the last step in the manufacturing flow.

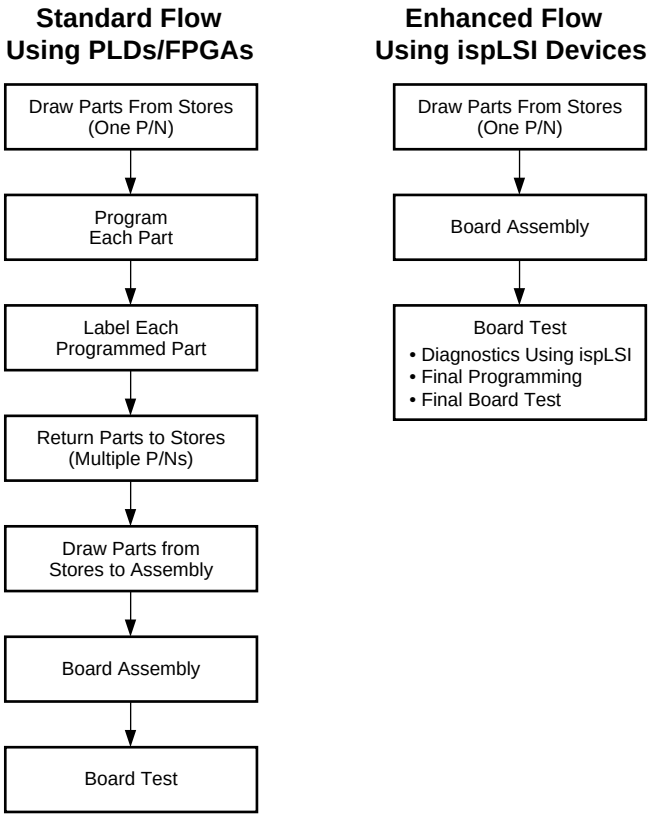
Easier Field Updates

With software reconfigurable systems, field updates are as easy as loading a new configuration from a floppy or downloading it through a modem.

Enhanced Manufacturing Flow with ispLSI

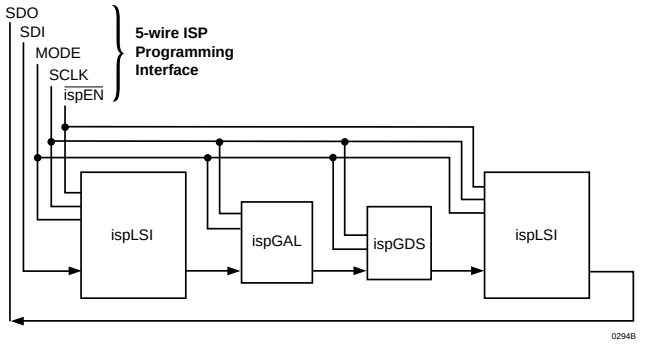
Perhaps the most exciting benefit of the ispLSI family is its potential to streamline the manufacturing process by eliminating the separate programming and labeling steps usually associated with PLDs. Quality is enhanced when product handling steps are reduced, in this case, those associated with programming, labeling and re-inventorying multiple device types. Eliminating socketing further improves quality and reduces board cost. Figure 6 shows the enhanced manufacturing with the ispLSI device.

Figure 6. Manufacturing Flow Comparison



All necessary programming is achieved via five TTL-level logic interface signals (see figure 7). These five signals control the on-chip programming circuitry, which protects against inadvertent reprogramming via on-chip state machines. The ispLSI family can also be programmed using popular third-party logic programmers.

Figure 7. In-System Programming Interface (Multi-Chip Solution)

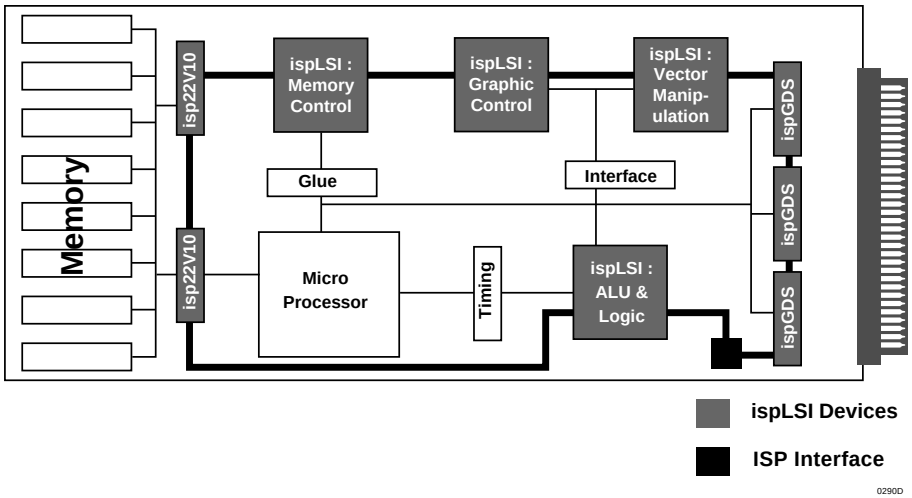


Boundary Scan

An emerging trend in board-level testing is boundary scan test, an attractive feature helping designers test system boards efficiently while lowering test and manufacturing costs. The ispLSI and pLSI 3000 and 6000 families offer dedicated IEEE 1149.1 boundary scan support for all test functions required by the standard. By using ispLSI and pLSI devices you not only eliminate expensive "bed-of-nails" testers but also simplify testing of surface-mount boards, multi-layer boards and boards using fine-pitch packages. Boundary scan is ideal wherever tight board layout limits access to logic signals.

It only takes four pins to implement the boundary scan interface. The ispLSI 3000 and 6000 devices share the four boundary scan signals with the in-system programming pins. This enhances the testability of system designs allowing logic to be reconfigured to improve controllability and observability.

Figure 5. In-System Programmable Graphics Board



Development Systems

The Lattice Semiconductor pLSI/ispLSI Development System (pDS) software is used to implement designs in ispLSI and pLSI devices. Design alternatives can be quickly implemented using LSC's low cost pDS software or the pDS+ family of Fitters that interface with third-party development software packages. This section describes the pDS and pDS+ Development Systems. Programmer support is also discussed.

pLSI/ispLSI Development System (pDS)

Features

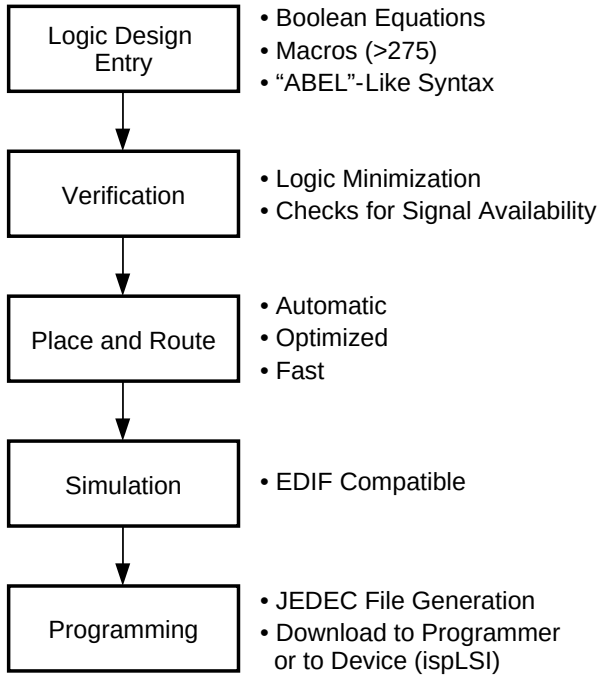
- ❑ High-performance, low-cost development environment
- ❑ Supports ispLSI and pLSI device families
- ❑ Boolean logic and text file design entry
- ❑ Windows-based graphical user interface
- ❑ Over 275 macros available
- ❑ Automatic place and route
- ❑ Static timing table
- ❑ Logic simulation with popular simulators
- ❑ JEDEC file download direct to programmer or ispLSI device

General Description

All ispLSI and pLSI families are supported by Lattice Semiconductor's low-cost pDS software. It runs on IBM-compatible (386/486/Pentium) PCs with Microsoft® Windows.

The graphical user interface employs an easy-to-use mouse and pull-down menu driven approach. Combined with Boolean logic data entry using an ABEL™-like syntax, pDS makes design entry with ispLSI and pLSI quick and straightforward (see figure 8).

Figure 8. pDS Design Flow



0292A

The pDS software supports over 275 macros to assist the design process. These macros cover most TTL functions, from gate primitives to 16-bit counters. The software also supports user-definable macros which can be modifications of existing macros or custom creations.

The pDS software automatically verifies the design, performs logic minimization and checks for signal availability.

The LSC Place and Route software assigns pins and critical speed paths while routing the design.

Quick compilation speeds the design, debug and rework process dramatically. Incremental design techniques are also supported.

Timing and functional simulation is available from Lattice Semiconductor, using Viewsim simulation software.

The Windows graphical user interface makes programming easy, using pull-down menus, intuitive point-and-click commands and self explanatory instructions. Without any up-front training, designs can be completed within hours instead of days or weeks.

pLSI/ispLSI Development System Plus (pDS+)

Features

- ❑ Supports ispLSI and pLSI device families
- ❑ Schematic capture, state machine, design entry HDL, and Boolean equations
- ❑ Expanded macro library (>300)
- ❑ Automatic logic minimization and partitioning
- ❑ Automatic place and route
- ❑ Logic and timing simulation
- ❑ EDIF compatible
- ❑ JEDEC file download direct to programmer or ispLSI device

General Description

For higher level design entry environments, LSC offers pDS+ development software packages, which expand on the core capabilities of pDS. Schematic capture, state machine, HDL and Boolean entry are supported, along with an expanded macro library.

The pDS+ software utilizes industry standard third-party design environments such as Viewlogic's Pro Series, Data I/O's Synario and others.

Running on IBM compatible (486/Pentium) PCs or workstation platforms, pDS+ software supports automatic logic minimization and partitioning as well as place and route, resulting in high logic utilization.

For logic and timing simulation, support is available from Lattice through Viewlogic Viewsim and Data I/O Synario-Sim simulation tools.

Third Party Programming Support

The ispLSI and pLSI families are supported by popular third-party logic programmers including Data I/O, Logical Devices, BP-Microsystems, Stag, System General, SMS Micro Systems and Advin. Table 2 describes each vendor's specific programmer models that support the ispLSI and pLSI devices. No proprietary, expensive, high pin-count programmers are required.

High pin-count socket adapters are available from Emulation Technology, Procon Technology, EDI Corporation and Logical Systems Corporation.

Additionally, the ispLSI family can be programmed on the board (in-system), which eliminates the need for a stand-alone programmer. For specific details refer to the LSC Programming Tools Guide available from your local Sales Representative.

Table 2. Programming Support

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30/A
System General	TURPRO-1

isp Engineering Kit

The ispLSI family may also be programmed with Lattice Semiconductor's isp Engineering Kit Model 100 for PCs. The kit is designed for engineering purposes only and is not intended for production use. By connecting an eight-wire cable to the parallel printer port of a PC, JEDEC files can be easily downloaded into the ispLSI device. Additionally, this cable can be connected directly to the circuit board facilitating on-board in-system programming.

Notes

1000 and 1000E Family Architectural Description

1000 and 1000E Family Introduction

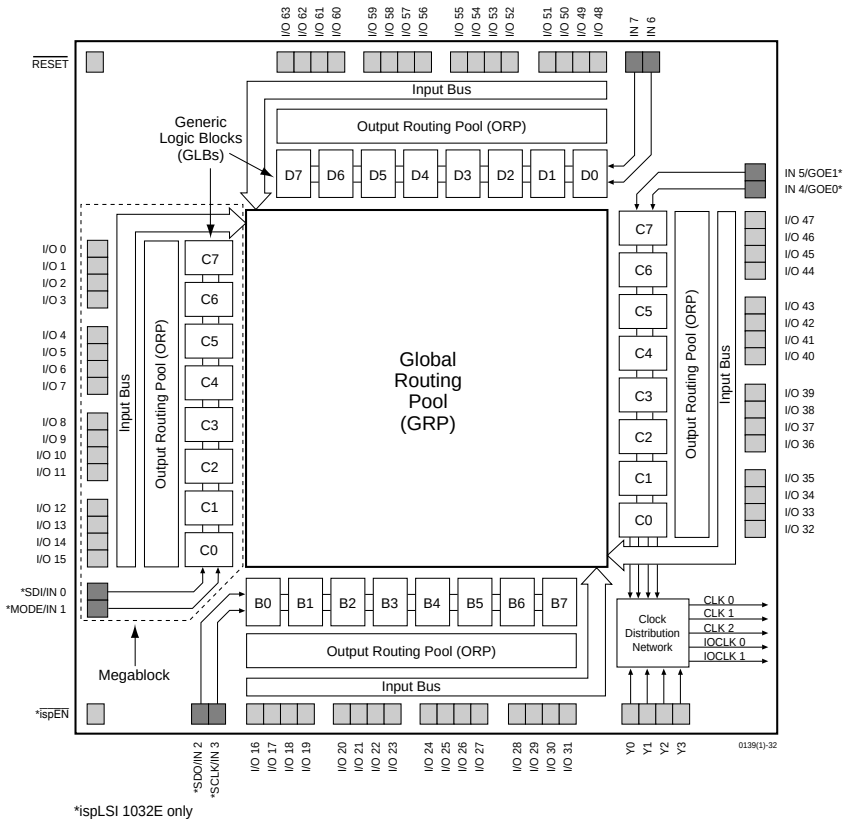
The ispLSI and pLSI 1000E devices are functional supersets of the ispLSI and pLSI 1000 devices and are architecturally similar except that the 1000E family features two new global output enable pins per device (only one for the 1016E) and programmable output slew rate control. The basic unit of logic for the ispLSI and pLSI families is the Generic Logic Block (GLB). Figure 1 illustrates the ispLSI 1032E with its 32 GLBs labeled A0, A1 .. D7. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs, which can be configured to be either combinatorial or registered. Inputs to the GLB come from the Global Routing Pool (GRP) and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

As an example, the ispLSI 1032E has 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bidirectional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. For the ispLSI and pLSI 1000E family only, each output can be programmed independently for slow output slew rate to minimize overall output switching noise.

The I/O cells are grouped into sets of 16 as shown in figure 1. Each of these I/O groups is associated with a Megablock through the use of the Output Routing Pool (ORP).

Eight GLBs, 16 I/O cells, one ORP and two dedicated inputs are connected together to make a Megablock. The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each Megablock shares a common Output Enable (OE) signal. The ispLSI 1032E device, shown in figure 1, contains four Megablocks.

Figure 1. ispLSI 1032E Functional Block Diagram



*ispLSI 1032E only

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the devices are selected using the Clock Distribution Network. The dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five outputs (CLK 0, CLK1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special GLB (C0 on the ispLSI and pLSI 1032 and 1032E devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

The ispLSI and pLSI 1000E Family is functionally identical to the 1000 Family with the exception of the addition of optional global output enable (GOE) pins. The ispLSI 1016E has one GOE pin option, while the remaining devices have two. These pins are multiplexed with dedicated inputs on the 1016E, 1024E and 1032E for pinout compatability.

Generic Logic Block

The Generic Logic Block (GLB) is the standard logic block of Lattice Semiconductor Corporation (LSC) high-density ispLSI and pLSI devices. A GLB has 18 inputs, four outputs and the logic necessary to implement most standard logic functions. The internal logic of the GLB is divided into four separate sections: the AND Array, the Product Term Sharing Array (PTSA), the Reconfigurable Registers, and the Control Functions (see figure 2). The AND array consists of 20 product terms, which can produce the logical product of any of the 18 GLB inputs. Sixteen of the inputs come from the Global Routing Pool, and are either feedback signals from any of the GLBs or inputs from the external I/O cells. The two remaining inputs come directly from two dedicated input pins. These signals are available to the product terms in both the logical true and the complemented forms which makes Boolean logic reduction more efficient.

The PTSA takes the 20 product terms and routes them to the four GLB outputs. There are four OR gates, with

Figure 2. GLB: Product Term Sharing Array Example

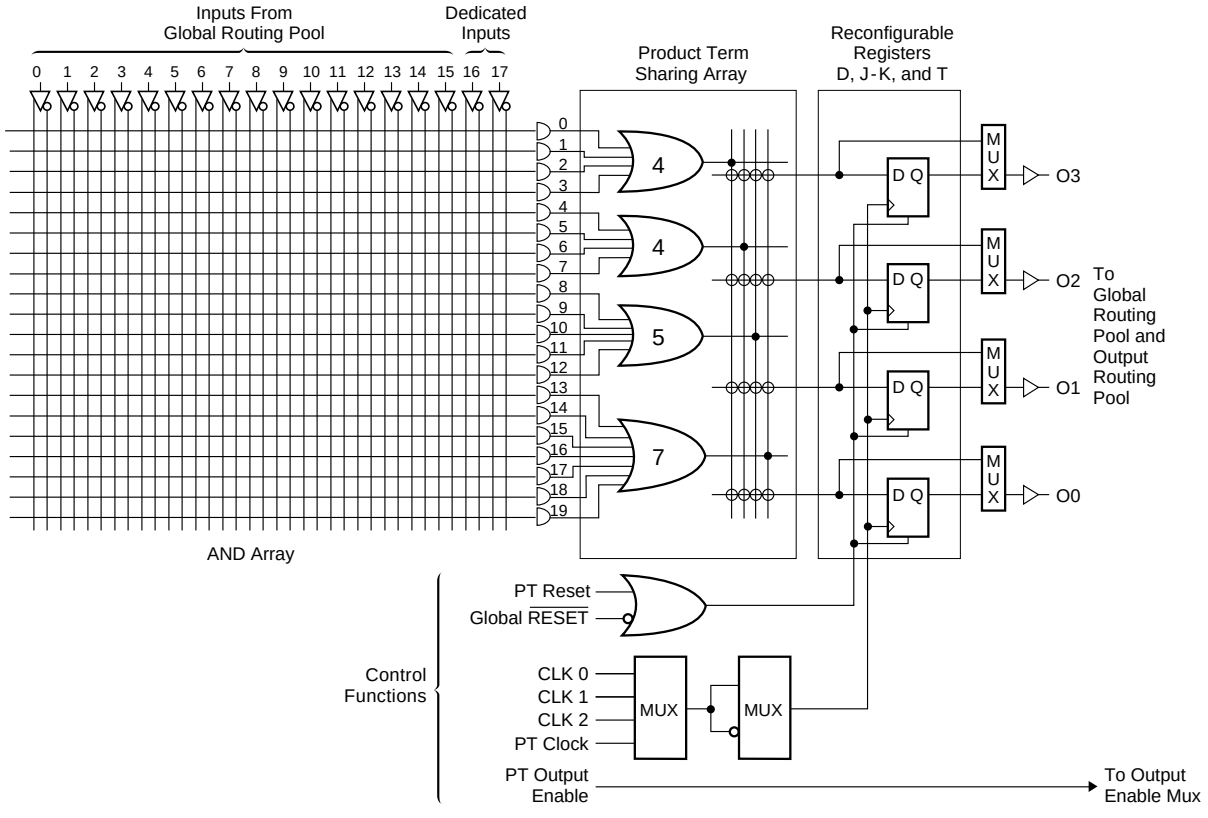


Figure 3. GLB: Four Product Term Bypass Example

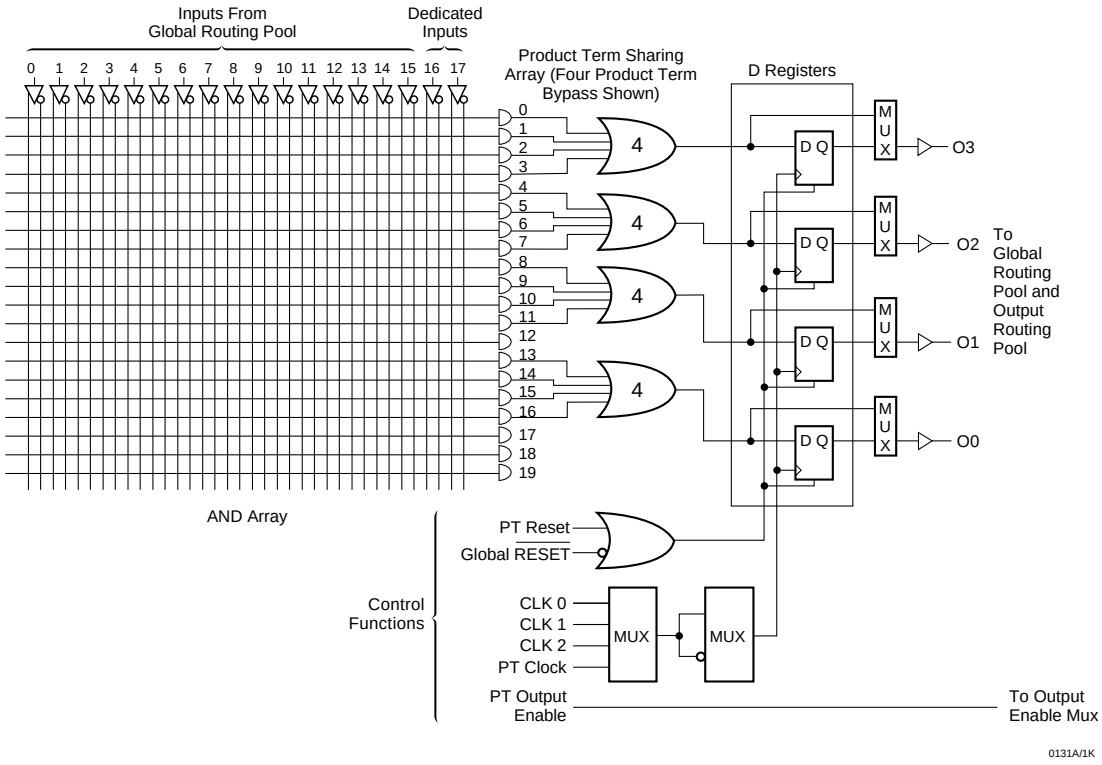
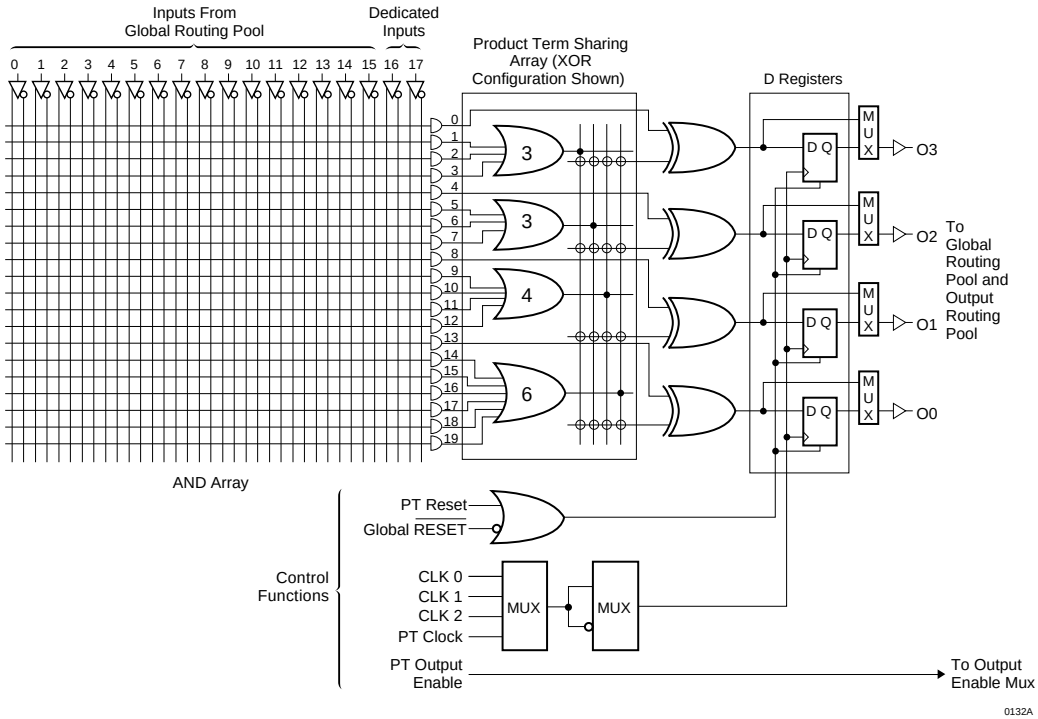


Figure 4. GLB: XOR Gate Example



Generic Logic Block (continued)

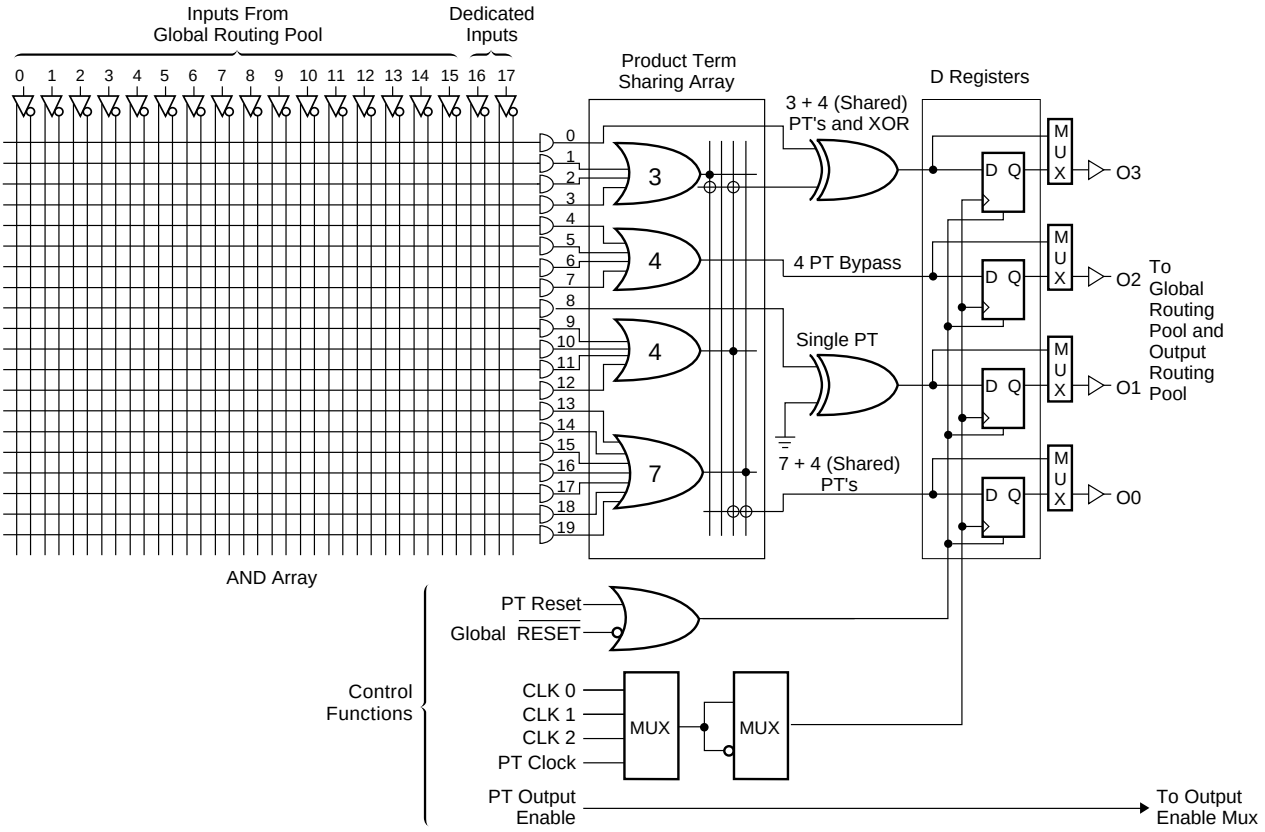
four, four, five and seven product terms each (see figure 2). The output of any of these OR gates can be routed to any of the four GLB outputs, and if more product terms are needed, the PTSA can combine them as necessary. In addition, the PTSA can share product terms similar to an FPLA device. If the user's main concern is speed, the PTSA can use a bypass circuit which provides four product terms to each output, to increase the performance of the cell (see figure 3). This can be done to any or all of the four outputs from the GLB.

The Reconfigurable Registers consist of four D-type flip-flops with an XOR gate on the input. The XOR gate in the GLB can be used either as a logic element or to reconfigure the D-type flip-flop to emulate a J-K or T-type flip-flop (see figure 4). This greatly simplifies the design of counters, comparators and ALU type functions. The registers can be bypassed if the user needs a combinatorial output. Each register output is brought back into the Global Routing Pool and is also brought to the I/O cells via the Output Routing Pool. Reconfigurable registers are not available when the four product term bypass is used.

The PTSA is flexible enough to allow these features to be used in virtually any combination that the user desires. In the GLB shown in figure 5, Output Three (O3) is configured using the XOR gate while Output Two (O2) is configured using the four Product Term Bypass. Output One (O1) uses one of the inputs from the five Product Term OR gate while Output Zero (O0) combines the remaining four product terms with all of the product terms from the seven Product Term OR gate for a total of eleven (7+4).

Various signals that control the operation of the GLB outputs are driven from the Control Functions (see figure 5). The clock for the registers can come from any of three sources developed in the Clock Distribution Network (see Clock Distribution Network section) or from a product term within the GLB. The Reset Signal for the GLB can

Figure 5. GLB: Mixed Mode Configuration Example



come from the Global Reset pin ($\overline{\text{RESET}}$) or from a product term within the GLB. The global reset pin is always connected and is logically "ORed" with the PT reset (if used). An active reset signal always sets the Q of the registers to a logic 0 state. The Output Enable for the I/O cells associated with the GLB comes from a product term within the block. Use of a product term for a control function makes that product term unavailable for use as a logic term. Refer to the Product Term Sharing Matrix (table 1) to determine which logic functions are affected.

There are many additional features in a GLB that allow implementation of logic intensive functions. These features are accessible using the Hard Macros from the software and require no intervention on the part of the user.

Product Term Sharing Matrix

This matrix describes how each of the product terms are used in the various modes. As an example, Product Term 12 can be used as an input to the five input OR gate in the standard configuration. This OR gate under standard configuration can be routed to any of the four GLB outputs. Product Term 12 is not used in the four product term bypass mode. When GLB output one is used in the XOR mode Product Term 12 becomes one of the inputs to the four input OR Gate. If Product Term 12 is not used in the logic, then it is available for use as either the Asynchronous Clock signal or the GLB Reset signal.

The Megablock

A Megablock consists of eight GLBs, an ORP, 16 I/O cells, two dedicated inputs and a common product term OE. Each of these will be explained in detail in the following sections. These elements are coupled together as shown in figure 6. The various members of the ispLSI and pLSI 1000/E families combine from one to six Megablocks on a single device (see table 2).

For the 1000 Family, the eight GLBs within the Megablock share two dedicated input pins. These dedicated input pins are not available to GLBs in any other Megablock. These pins are dedicated (non-registered) inputs only

Table 1. Product Term Sharing Matrix

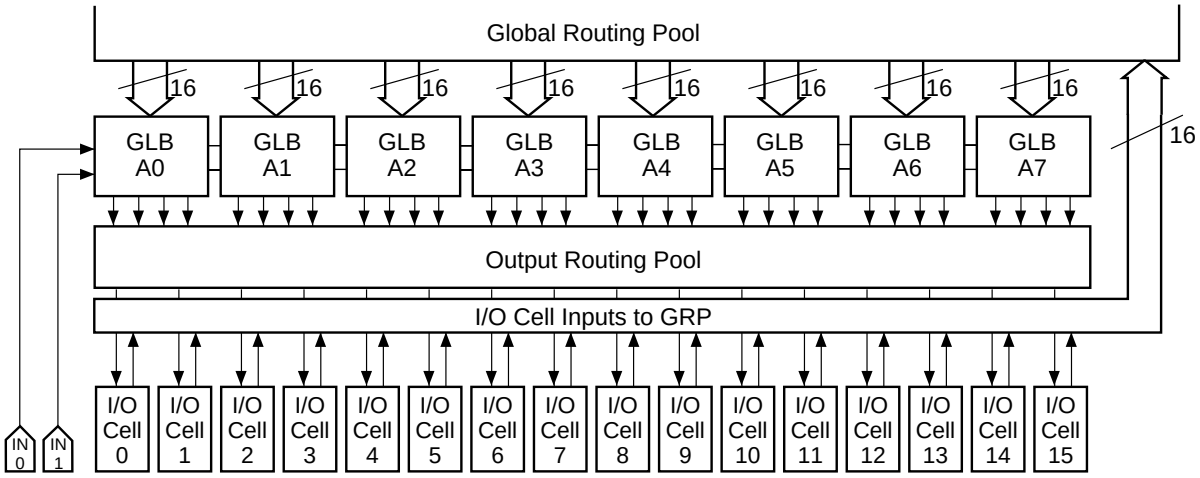
Product Term #	Standard Configuration Output Number 3 2 1 0	Four Product Term Bypass Output Number 3 2 1 0	Single Product Term Output Number 3 2 1 0	XOR Function Output Number 3 3 2 2 1 1 0 0	Alternate Function
0	■ ■ ■ ■	■	■	■	
1	■ ■ ■ ■	■		■	
2	■ ■ ■ ■	■		■	
3	■ ■ ■ ■	■		■	
4	■ ■ ■ ■	■	■	■	
5	■ ■ ■ ■	■		■	
6	■ ■ ■ ■	■		■	
7	■ ■ ■ ■	■		■	
8	■ ■ ■ ■	■	■	■	
9	■ ■ ■ ■	■		■	
10	■ ■ ■ ■	■		■	
11	■ ■ ■ ■	■		■	
12	■ ■ ■ ■	■		■	■CLK/Reset
13	■ ■ ■ ■	■	■	■	
14	■ ■ ■ ■	■		■	
15	■ ■ ■ ■	■		■	
16	■ ■ ■ ■	■		■	
17	■ ■ ■ ■			■	
18	■ ■ ■ ■			■	
19	■ ■ ■ ■			■	■ OE/Reset

Table 2. Device Resources

pLSI and ispLSI Devices	Megablocks	GLBs	I/O Cells	Dedicated Inputs
1016/1016E	2	16	32	4
1024/1024E	3	24	48	6
1032/1032E	4	32	64	8
1048/1048C/1048E	6	48	96	10/12

Table 2-0051/1k

Figure 6. The Megablock Block Diagram



and are automatically assigned by software. The product term OE signal is generated within the Megablock and is common to all 16 of the I/O cells in the Megablock. The OE signal can be generated using a product term (PT19) in any of eight GLBs within the Megablock. See Output Enable Control section for further details.

Because of the shared logic within the Megablock, signals that share a common function (counters, busses, etc.) should be grouped within a Megablock. This will allow the user to obtain the best utilization of the logic within the device and eliminate routing bottlenecks.

Input Routing

Signal inputs are handled in two ways within the device. First, each I/O cell within the device has its input routed directly to the GRP. This gives every GLB within the device access to each I/O cell input. Second, each Megablock has two dedicated inputs which are directly routed to the eight GLBs within the Megablock. Both input paths are shown in figure 6.

The Output Routing Pool

The ORP routes signals from the GLB outputs to I/O cells configured as outputs or bidirectional pins (see figure 7). The purpose of the ORP is to allow greater flexibility when assigning I/O pins. It also simplifies the job for the routing software which results in a higher degree of utilization.

By examining the ORP in figure 7, it can be seen that a GLB output can be connected to one of four I/O cells. Further flexibility is provided by using the PTSA (figures 2 through 5) which makes the GLB outputs completely interchangeable. This allows the routing program to freely interchange the outputs to achieve the best routability. This is an automatic process and requires no intervention on the part of the user.

The ORP bypass connections (see figure 8) further increase the flexibility of the device. The ORP bypass connects specific GLB outputs to specific I/O cells at a faster speed. The bypass path tends to restrict the routability of the device and should only be used for critical signals.

Figure 7. Output Routing Pool

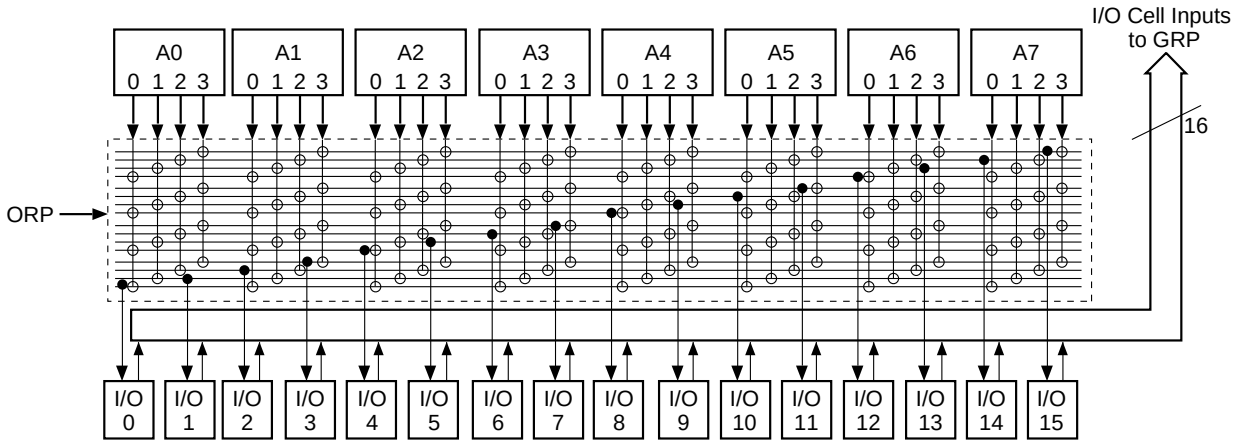
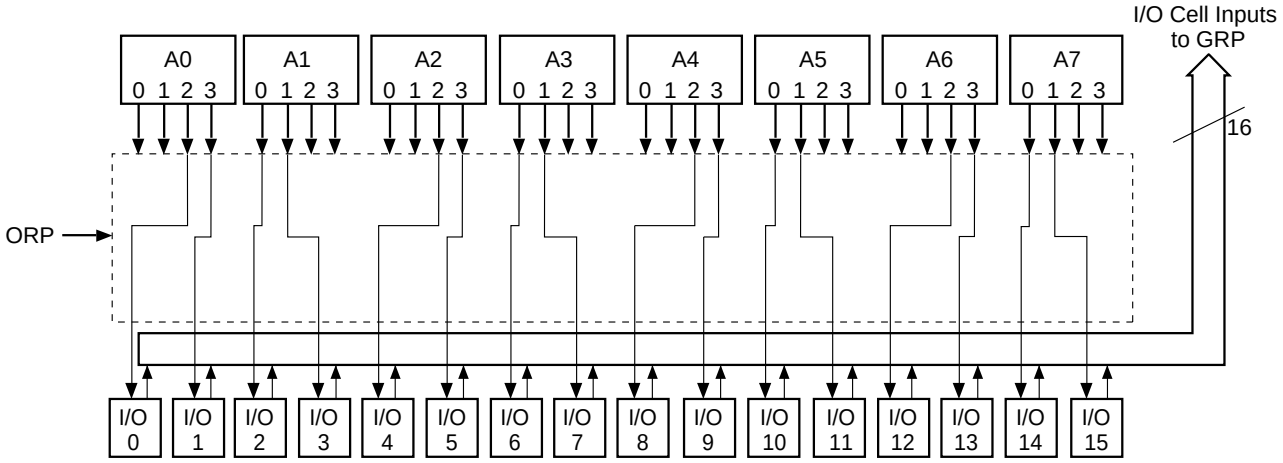


Figure 8. Output Routing Pool Showing Bypass



I/O Cell

The I/O cell (see figure 9) is used to route input, output or bidirectional signals connected to the I/O pin. One logic input comes from the ORP, and the other comes from the faster ORP bypass (see figure 9). A pair of multiplexers select which signal will be used, and its polarity. The Output Enable of the I/O cell is controlled by the OE signal generated within each Megablock.

As with the data path, a multiplexer selects the signal polarity. The Output Enable can be set to a logic high (enabled) when an output pin is desired, or logic low (disabled) when an input pin is needed. The Global Reset ($\overline{\text{RESET}}$) signal is driven by the active low chip reset pin. This reset is always connected to all GLB and I/O registers. Each I/O cell can individually select one of the two clock signals (IOCLK 0 or IOCLK 1). These clock signals are generated by the Clock Distribution Network.

Using the multiplexers, the I/O cell can be configured as an input, an output, a 3-stated output or a bidirectional I/O. The D-type register can be configured as a level sensitive transparent latch or an edge triggered flip-flop to store the incoming data. Figure 10 illustrates some of the various I/O cell configurations possible.

There is an active pull-up resistor on the I/O pins which is automatically used when the pin is not connected. An option exists to have active pull-up resistors connected to all pins. This improves the noise immunity and reduces Icc for the device.

Figure 9. I/O Cell Architecture

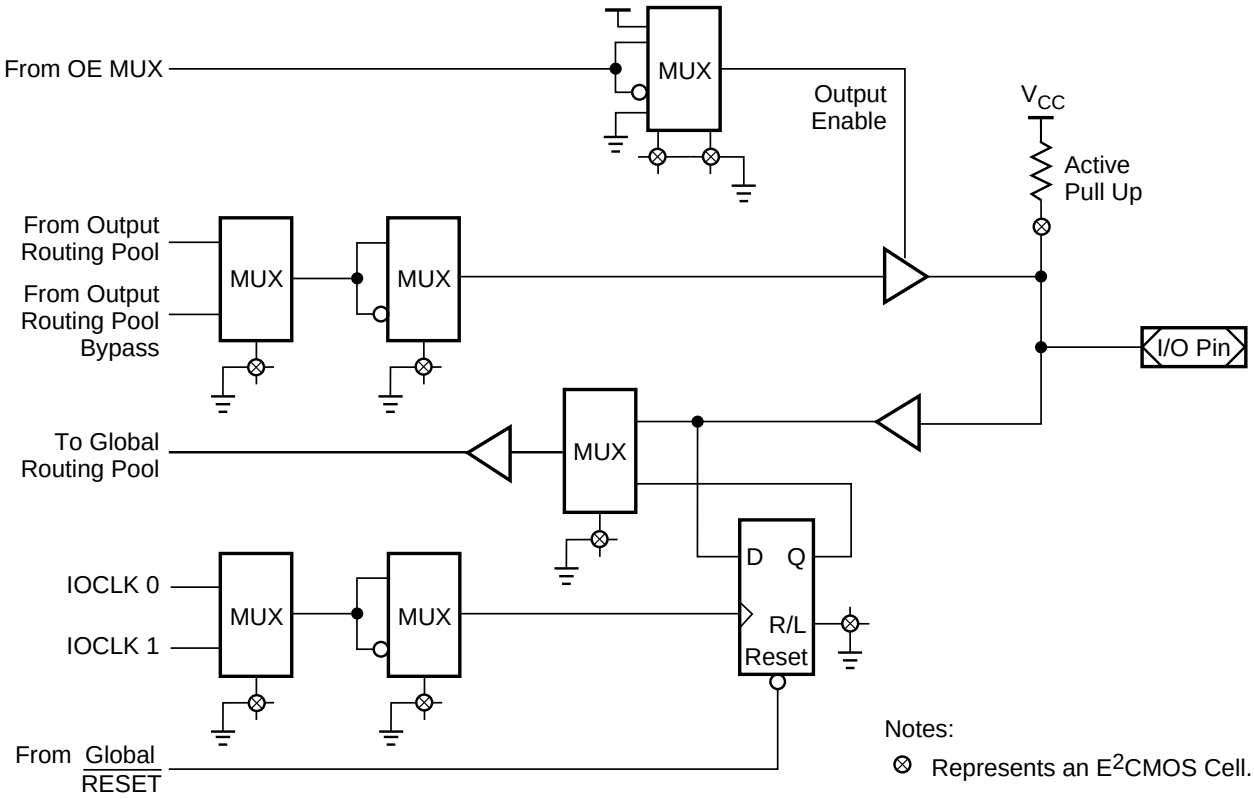
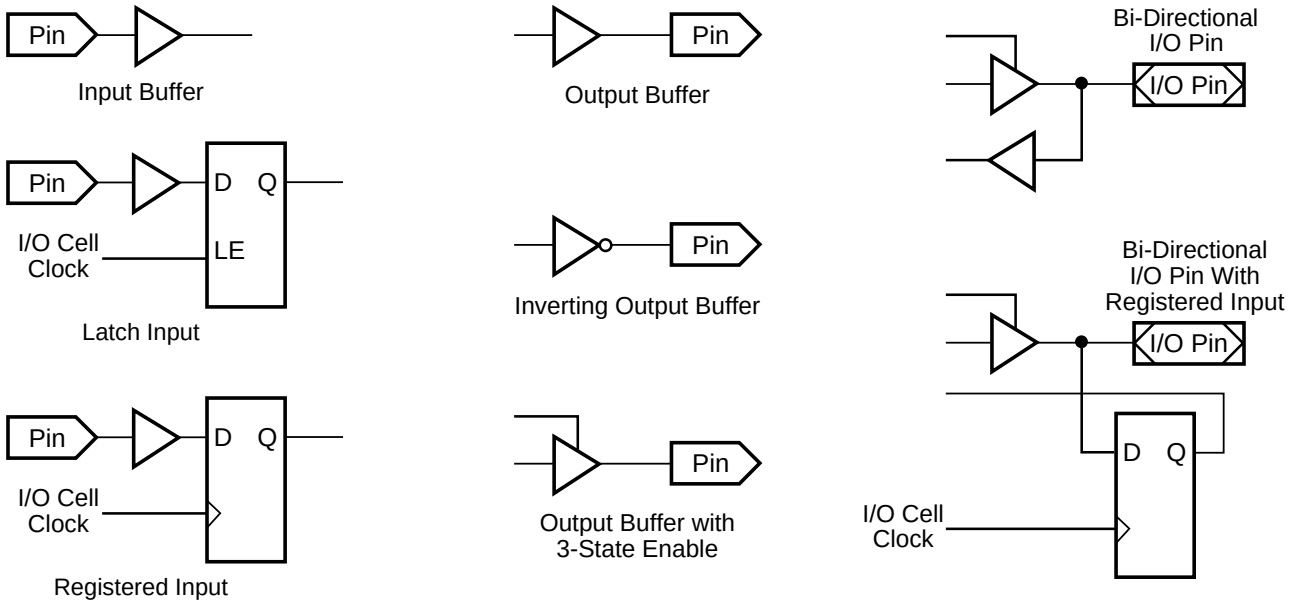


Figure 10. Examples of I/O Cell Configurations



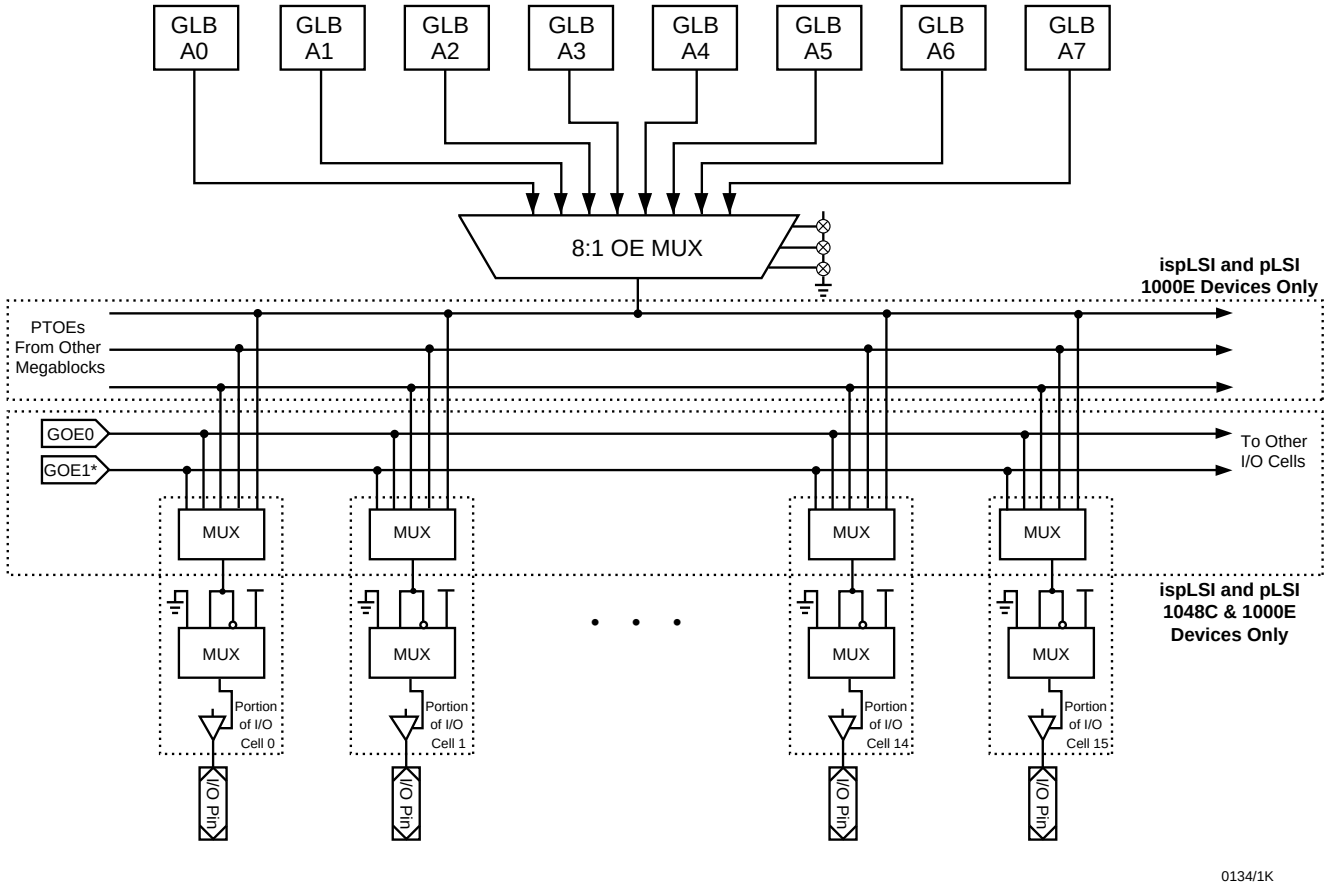
The Output Enable Control

One OE signal can be generated within each GLB using the OE Product Term (PT19). One of the eight OE signals within a Megablock is then routed to all of the I/O cells within that Megablock (see figure 11). This OE signal can simultaneously control all of the 16 I/O cells that are used in 3-state mode. Individual I/O cells also have independent control for permanently enabling or disabling the output buffer (refer to the I/O cell section). Only one OE signal is allowed per Megablock for 3-state operation.

The advantage to this approach is that the OE signal can be generated in any GLB within the Megablock that happens to have an unused OE product term. This frees up the other OE product terms for use as logic.

The 1000E and 1048C devices also have optional Global Output Enable (GOE) inputs. These provide minimum delay output enable control and are multiplexed with dedicated inputs on the 1016E, 1024E and 1032E devices.

Figure 11. Output Enable Control for a Megablock

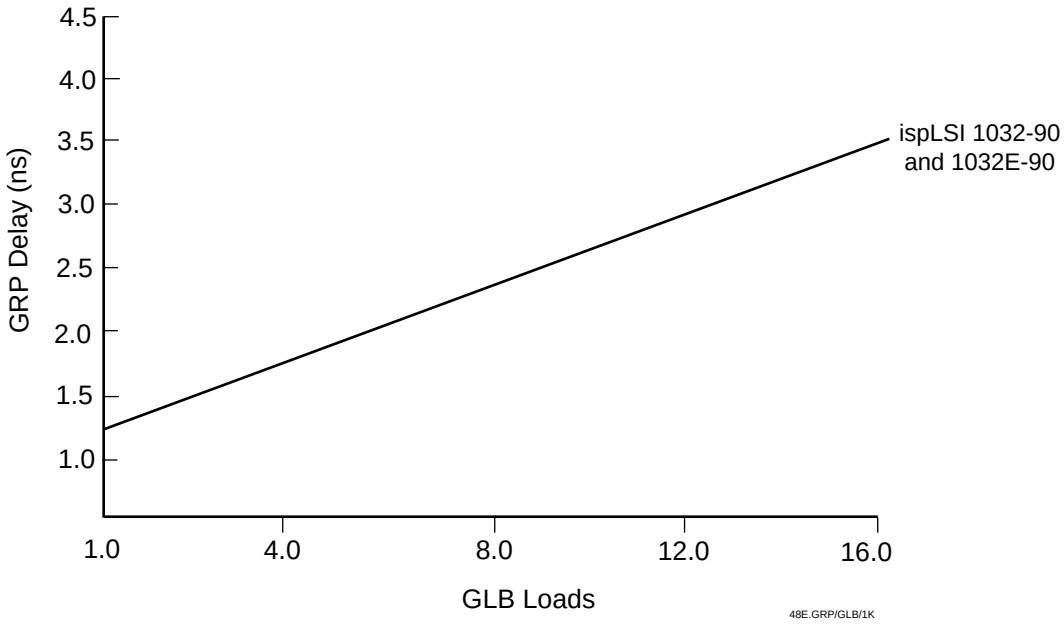


*Not available on ispLSI and pLSI 1016E.

Global Routing Pool

The GRP is a proprietary interconnect structure that offers fast predictable speeds with complete connectivity. The GRP allows the outputs from the GLBs or the I/O cell inputs to be connected to the inputs of the GLBs. Any GLB output is available to the input of all other GLBs, and similarly an input from an I/O pin is available as an input to all of the GLBs. Because of the uniform architecture of the ispLSI and pLSI devices, the delays through the GRP are both consistent and predictable. However, they are slightly affected by GLB loading as shown in figure 12.

Figure 12. GRP Delay vs GLB Loading Example



Clock Distribution Network

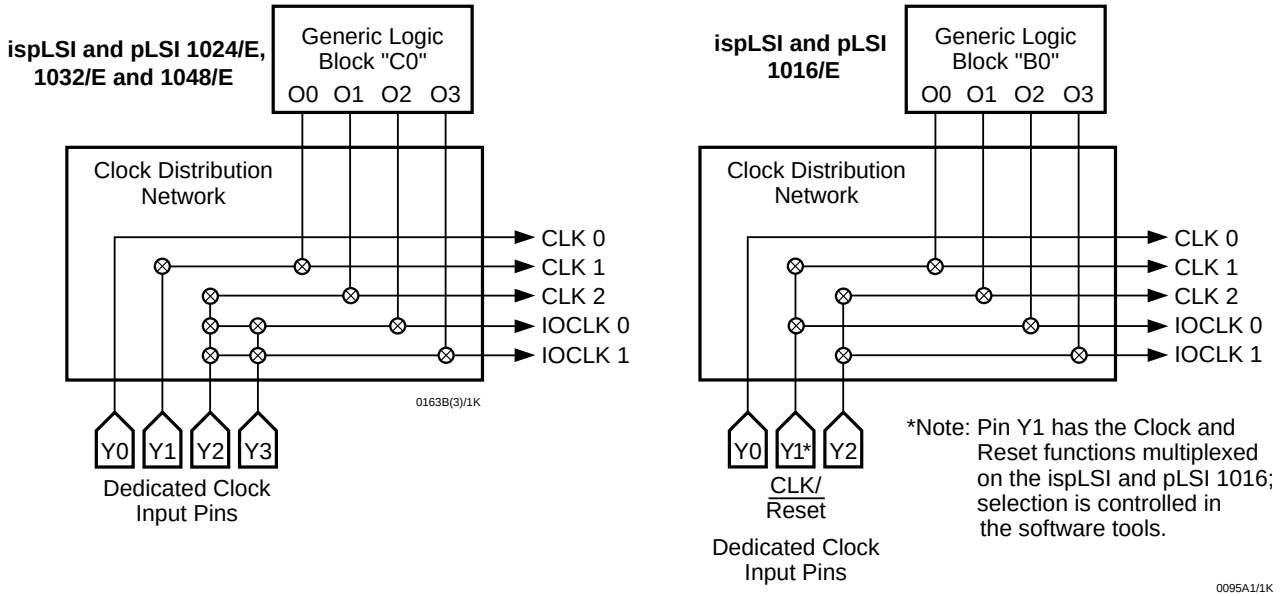
The Clock Distribution Networks are shown in figure 13. They generate five global clock signals CLK 0, CLK 1, CLK 2 , IOCLK 0 and IOCLK 1. The first three, CLK 0, CLK 1 and CLK 2 may be used for clocking all the GLBs in the device. Similarly, IOCLK 0 and IOCLK 1 signals are used for clocking all of the I/O cells in the device. There are four dedicated system clock pins (Y0, Y1, Y2, Y3), three for the ispLSI and pLSI 1016 (Y0, Y1, Y2), which can be directed to any GLB or any I/O cell using the Clock Distribution Network. The other inputs to the Clock Distribution Network are the four outputs of a dedicated clock GLB ("C0" for the ispLSI 1032 is shown in figure 1). These clock GLB outputs can be used to create a user-defined internal clocking scheme.

For example, the clock GLB can be clocked using the external main clock pin Y0 connected to global clock signal CLK 0. The outputs of the clock GLB in turn can generate a "divide by" signal of the CLK 0 which can be connected to the CLK 1, CLK 2, IOCLK 0 or IOCLK 1 global clock lines.

All GLBs have the capability of generating their own asynchronous clocks using the clock Product Term (PT12). CLK 0, CLK 1 and CLK 2 feed to their corresponding clock MUX inputs on all the GLBs (see figure 2).

The two I/O clocks generated in the Clock Distribution Network IOCLK 0 and IOCLK 1, are brought to all the I/O cells and the user programs the I/O cell to use one of the two.

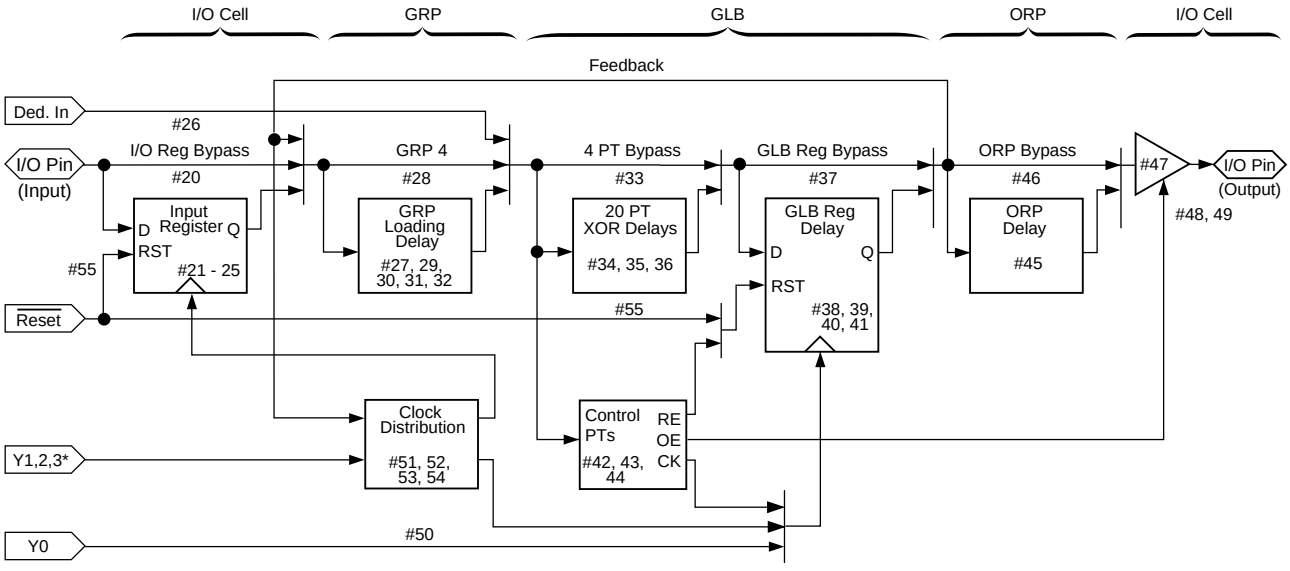
Figure 13. Clock Distribution Networks



Timing Model

The task of determining the timing through the device is simple and straightforward. A device timing model is shown in figure 14. To determine the time that it takes for data to propagate through the device, simply determine the path the data is expected to follow, and add the various delays together (figure 15). Critical timing paths are shown in figure 14, using data sheet parameters. Note that the Internal timing parameters are given for reference only, and are not tested. External timing parameters are tested and guaranteed on every device.

Figure 14. ispLSI and pLSI Timing Model[1, 2]



*Note: Y1 and Y2 only for the ispLSI and pLSI 1016 and 1016E.

Figure 15. ispLSI and pLSI Timing Model Examples[1, 2]

Combinatorial Paths

tpd1	=	tiobp	+	tgrp4	+	t4ptbp	+	t20ptxor	+	torpbp	+	tob
#1	=	#20	+	#28	+	#33	+	#37	+	#46	+	#47
tpd2	=	tiobp	+	tgrp4	+	txoradj	+	t20ptxor	+	torp	+	tob
#2	=	#20	+	#28	+	#36	+	#37	+	#45	+	#47

Registered Paths

General Form:

tsu	=	Logic	+	Regsu	-	Clock(min)
th	=	Clock(max)	+	Regh	-	Logic
tco	=	Clock(max)	+	Regco	+	Output

Specific Examples:

tsu1	=	(tiobp	+	tgrp4	+	t4ptbp)	+	tgsu	-	tgy0(min)		
#6	=	(#20	+	#28	+	#33)	+	#38	-	#50		
th1	=	tgy0(max)	+	tgh	-	(tiobp	+	tgrp4	+	t4ptbp)		
#8	=	#50	+	#39	-	(#20	+	#28	+	#33)		
tco1	=	tgy0(max)	+	tgco	+	(torpbp	+	tob)				
#7	=	#50	+	#40	+	(#46	+	#47)				
tsu2	=	(tiobp	+	tgrp4	+	txoradj)	+	tgsu	+	tgy0(min)		
#9	=	(#20	+	#28	+	#36)	+	#38	+	#50		
th2	=	tgy0(max)	+	tgh	-	(tiobp	+	tgrp4	+	txoradj)		
#11	=	#50	+	#39	-	(#20	+	#28	+	#36)		
tco2	=	tgy0(max)	+	tgco	+	(torp	+	tob)				
#10	=	#50	+	#40	+	(#45	+	#47)				

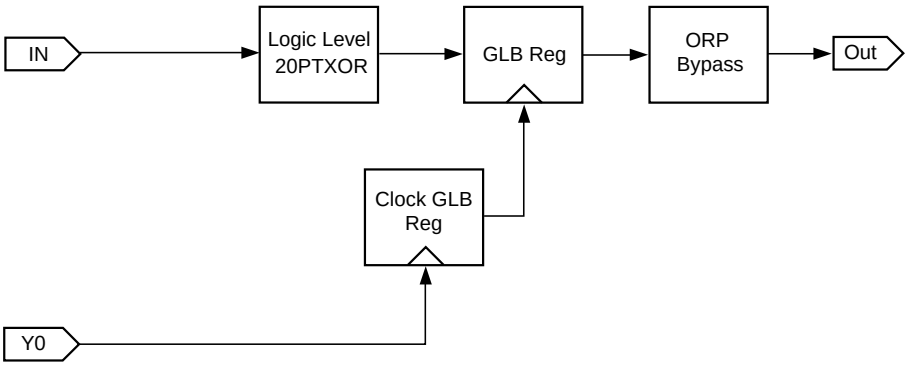
Table 2-0016/1k.eps

1. The timing parameter reference numbers refer to the Internal Timing Parameters contained in the individual data sheets.
2. The example timing model refers to the 1000 devices. For the 1000E timing model, please refer to the individual data sheets.

Circuit Timing Example

A design requires one logic level (using the 20PTXOR path). The design then uses a GLB register before exiting the device using the ORP bypass. Calculate **t**su, **t**h and **t**co.

Figure 16. Timing Calculation Example



0494/1K

Figure 16. Timing Calculation Example (continued)

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**iobp + **t**grp4 + **t**20ptxor) + (**t**gsu) – (**t**gy0(min) + **t**gco + **t**gcp(min))
	=	(#22 + #30 + #37) + (#40) – (#54 + #42 + #56)
4.5 ns	=	(0.3 + 2.3 + 6.8) + (0.2) – (1.4 + 2.9 + 0.8)
th	=	Clock (max) + Reg h - Logic
	=	(**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gh) – (**t**iobp + **t**grp4 + **t**20ptxor)
	=	(#54 + #42 + #56) + (#41) – (#22 + #30 + #37)
3.5 ns	=	(1.4 + 2.9 + 1.8) + (6.8) – (0.3 + 2.3 + 6.8)
tco	=	Clock (max) + Reg co + Output
	=	(**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#54 + #42 + #56) + (#42) + (#47 + #49)
11.7 ns	=	(1.4 + 2.9 + 1.8) + (2.9) + (1.0 + 1.7)

Table 2-0042a-32

1. Calculations are based upon timing specifications for the ispLSI and pLSI 1032E-90 device.

Notes

2000 Family Architectural Description

ispLSI and pLSI 2000 Family Introduction

The basic unit of logic of the ispLSI and pLSI 2000 family is essentially the same as that of the ispLSI and pLSI 1000/E family. However, there are some specific architectural differences: global clock, I/O Cell and OE, and ORP structures. A functional block diagram of the 2032 device is shown in figure 1. These architectural differences are described in detail below.

Global Clock Structure

The clock GLB distribution network of the 1000/E family has been eliminated and replaced by three dedicated global GLB clock input signals CLK0, CLK1, and CLK2. These three clocks are used for clocking all the GLBs configured as registers in the device. They feed directly to the GLB clock input via a clock multiplexer. CLK0 is associated with system clock pin Y0, CLK1 corresponds to system clock pin Y1, and CLK3 corresponds to system clock pin Y2. This is illustrated in figure 2. The GLB global clocks do not have inversion capability, but all GLBs continue to have the capability of generating their own asynchronous clocks using the clock product term (PT12) with inversion capability. The GLB global clocks and the GLB product term clock feed to their corresponding clock multiplexer shown in figure 3.

Figure 1. ispLSI 2032 Functional Block Diagram

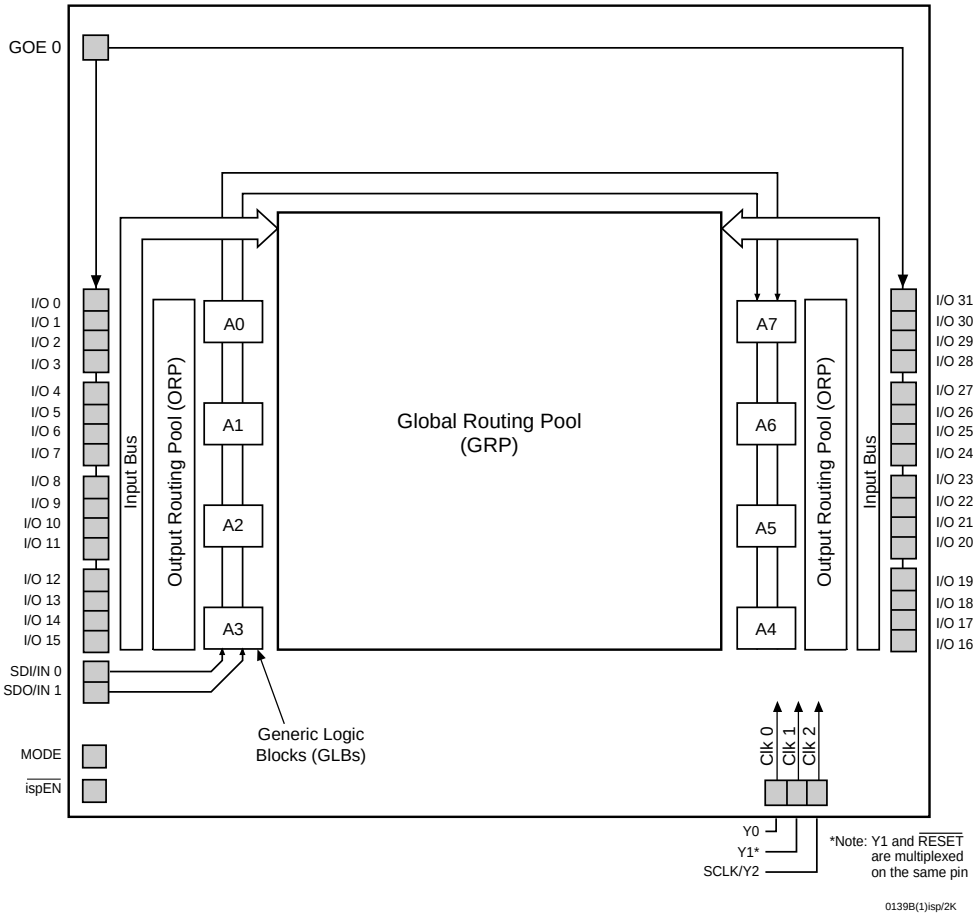


Figure 2. Global Clock Structure

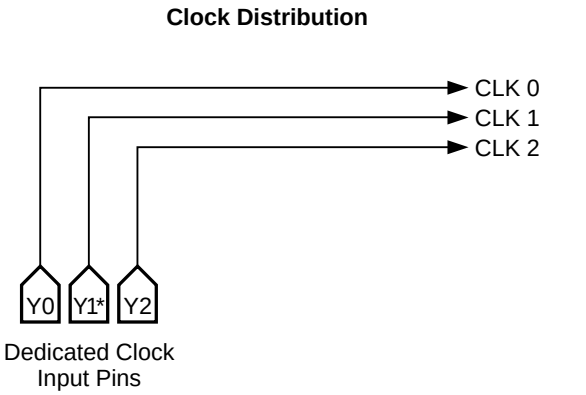
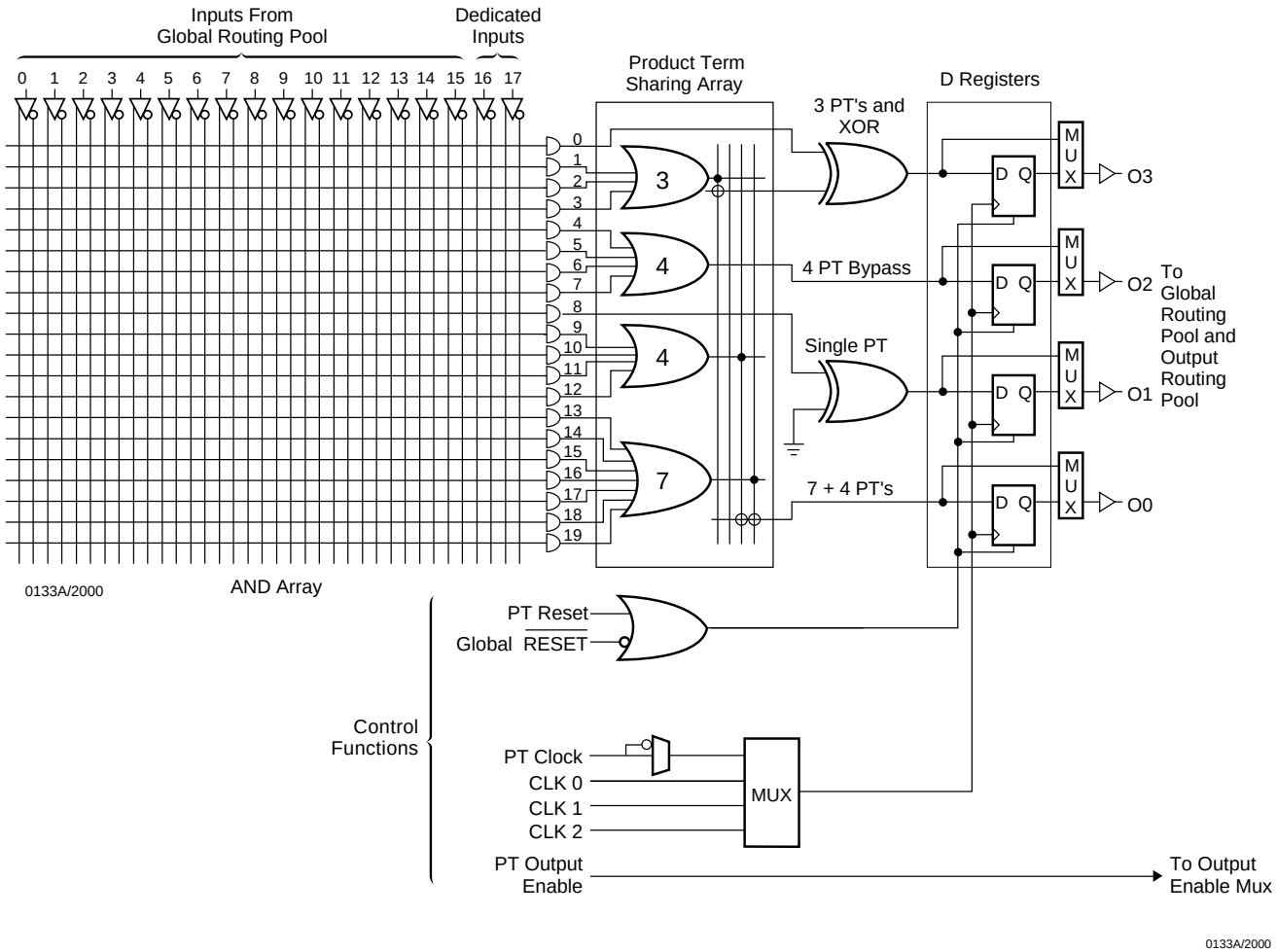


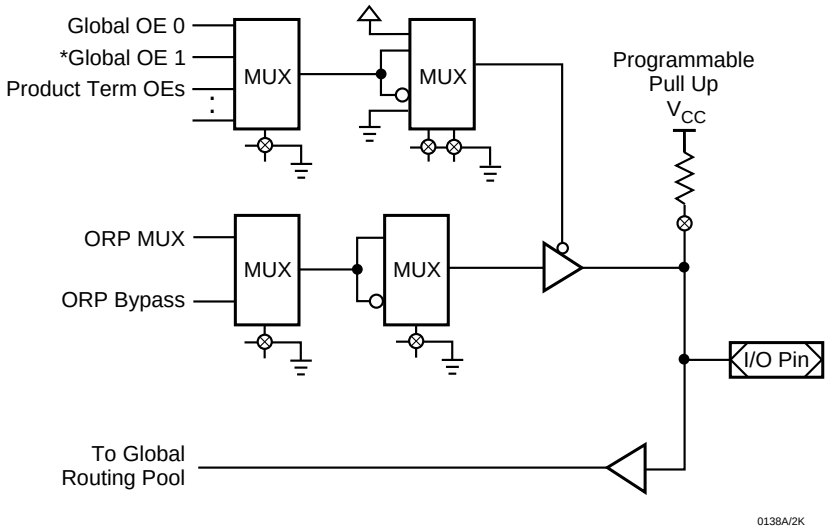
Figure 3. GLB with Clock Multiplexer Scheme



I/O Cell and OE Structure

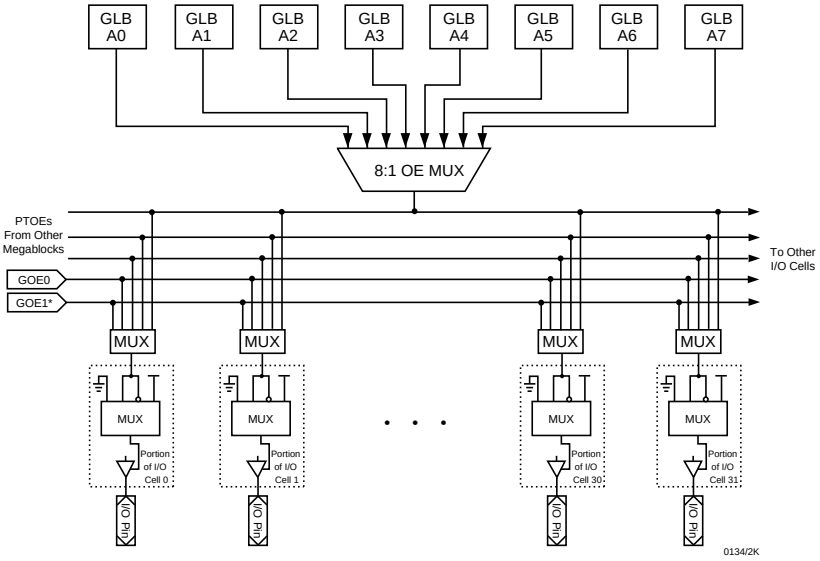
The reconfigurable input register or latch has been removed to simplify the I/O cell architecture. Each I/O cell can be individually programmed to be a combinatorial input, combinatorial output, or a bidirectional I/O pin with 3-state control. With the simplified I/O cell architecture, the I/O clocks have also been removed. This is illustrated in figure 4. The product term output enable (PTOE) signal is still generated within each GLB using product term 19. The PTOE is generated in one of the eight GLBs. In addition to the PTOE, there is a global output enable (GOE) pin which can control any of the device's 3-state output buffers. The multiplexing between the GOE and PTOE is illustrated in figure 5. The 2032 device has one GOE and the 2064, 2096 and 2128 devices each have two GOEs.

Figure 4. ispLSI and pLSI 2000 Family I/O Cell Architecture



⊗ Represents an E^2CMOS Cell.
* Except 2032

Figure 5. ispLSI and pLSI 2000 Family Output Enable Controls



* Except 2032

Output Routing Pool (ORP)

Each megablock now contains two ORPs to increase output routability. A set of four GLBs is associated with one of the two ORPs within the megablock. The 16 outputs of the four GLBs within a megablock will feed to any of the 16 associated I/O cells. In the 1000/E family, the 32 GLB outputs feed only 16 associated I/O cells. In this device family, 32 GLB outputs of a megablock can feed 32 I/O cells. Output routability has doubled. This is illustrated in figure 6. Each GLB output has an ORP bypass capability so more designs can have critical output signals. This is shown in figure 7.

Figure 6. ispLSI and pLSI 2000 Family Output Routlng Pool

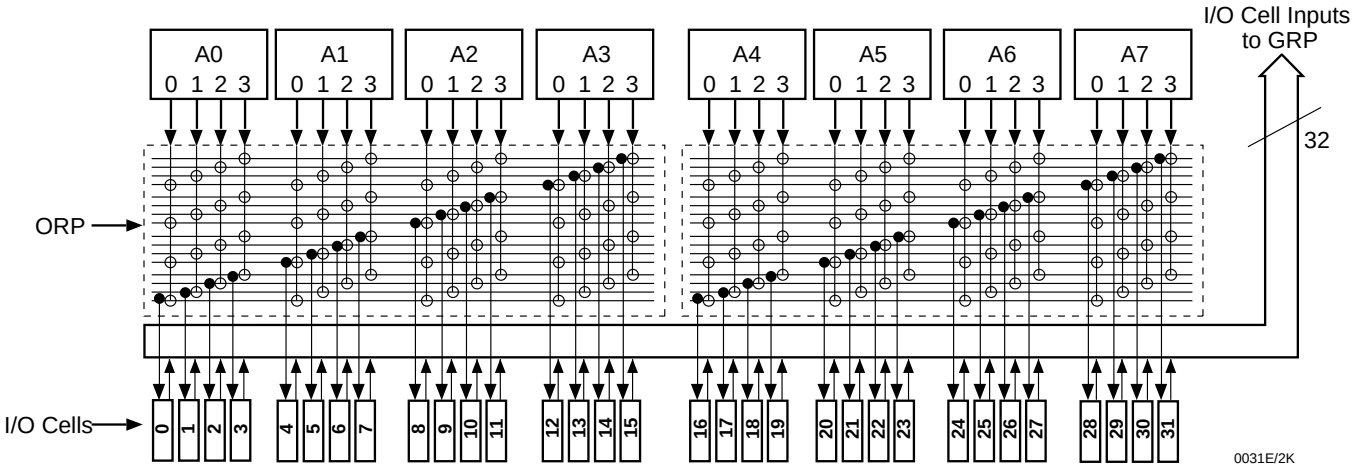
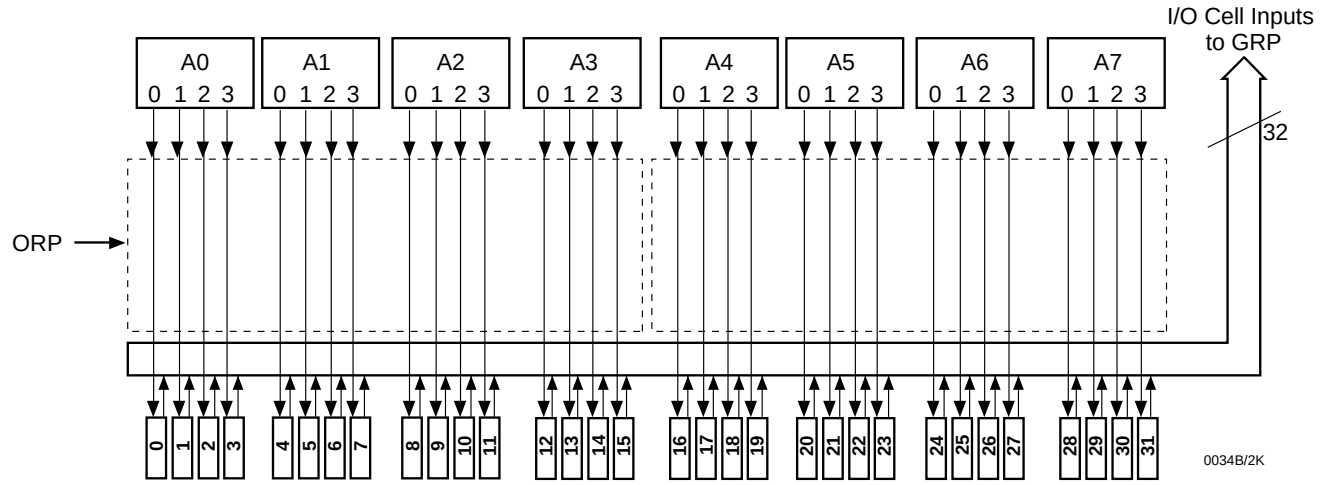


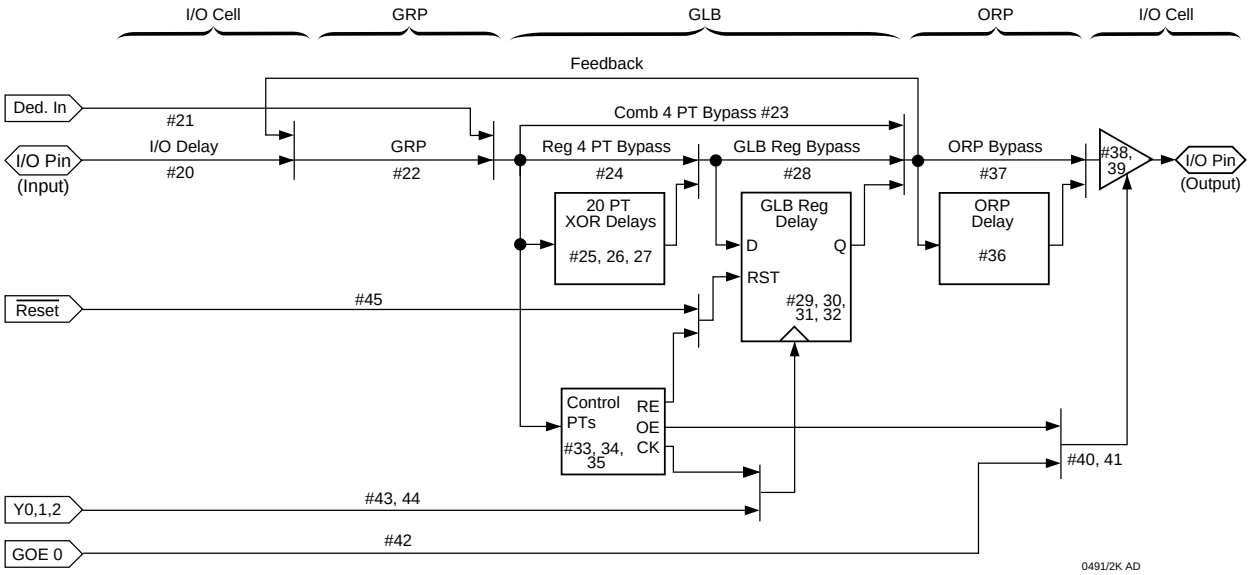
Figure 7. ispLSI and pLSI 2000 Family Output Routlng Pool Showing Bypass



Timing Model

The task of determining the timing through the device is simple and straightforward. A device timing model is shown in figure 8. To determine the time that it takes for data to propagate through the device, simply determine the path the data is expected to follow, and add the various delays together (figure 8). Critical timing paths are shown in figure 8, using data sheet parameters. Note that the Internal timing parameters are given for reference only, and are not tested. External timing parameters are tested and guaranteed on every device.

Figure 8. ispLSI and pLSI 2032 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (**t**io + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**io + **t**grp + **t**ptck(min))
= (#20+ #22+ #26) + (#29) - (#20+ #22+ #35)
1.9 ns = (1.1 + 1.3 + 5.1) + (0.3) - (1.1 + 1.3 + 2.9)

th = Clock (max) + Reg h - Logic
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**io + **t**grp + **t**20ptxor)
= (#20+ #22+ #35) + (#30) - (#20+ #22+ #26)
1.4 ns = (1.1 + 1.3 + 5.2) + (3.0) - (1.1 + 1.3 + 5.1)

tco = Clock (max) + Reg co + Output
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#20+ #22+ #35) + (#31) + (#36 + #38)
9.1 ns = (1.1 + 1.3 + 5.2) + (0.7) + (1.3 + 1.2)

Table 2-0042-16/2K AD

1. Calculations are based upon timing specifications for the ispLSI and pLSI 2032-135L.

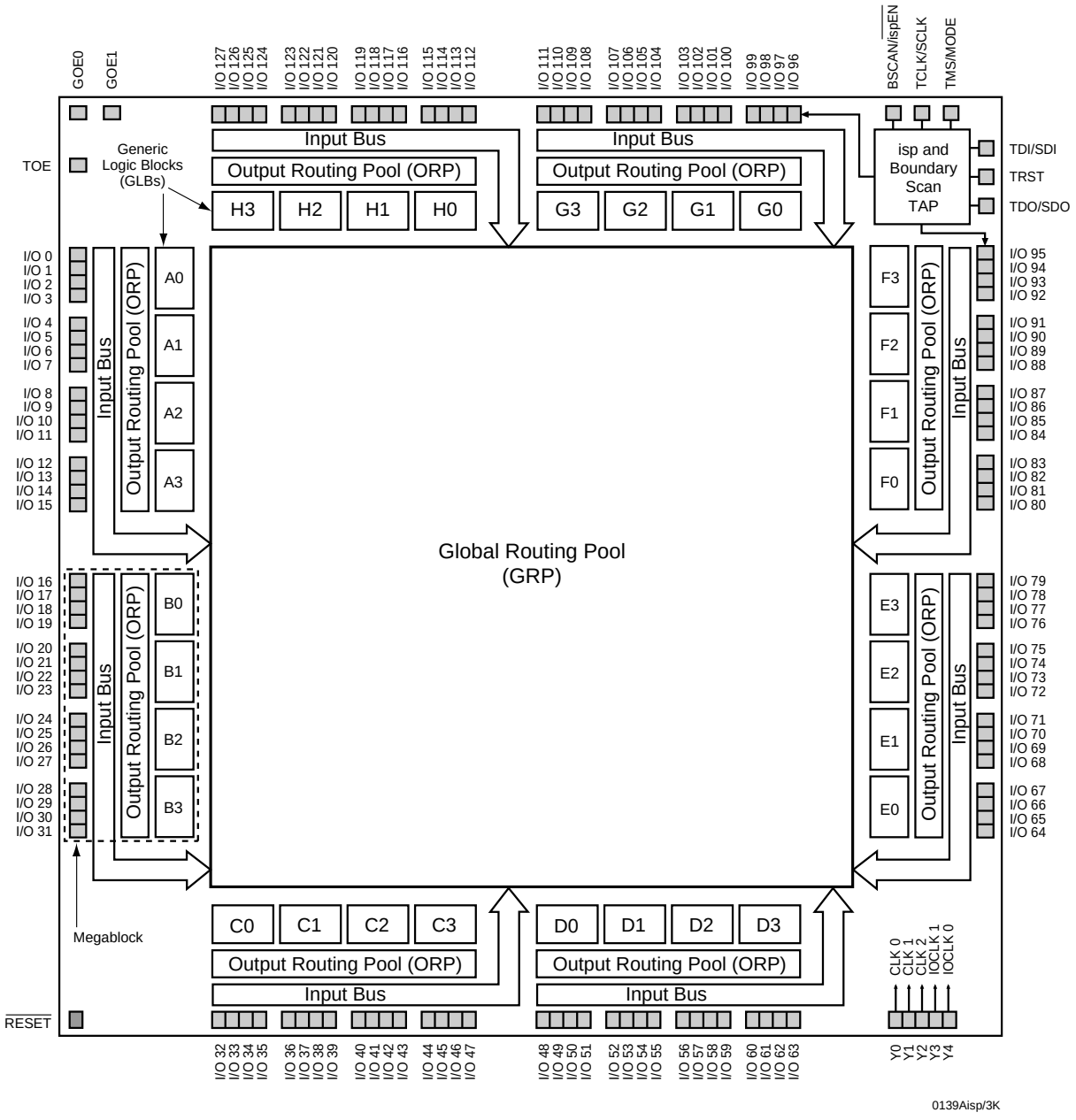
Notes

3000 Family Architectural Description

ispLSI and pLSI 3000 Family Introduction

The basic unit of logic of the ispLSI and pLSI 3000 family is closely related to that of the ispLSI and pLSI 1000/E family. However, there are some notable architectural differences: Boundary Scan, Megablock and GLB structure, Global clock structure, and I/O cell structure. A functional block diagram of the ispLSI 3256 device is shown in figure 1. The architectural differences are described in the following sections.

Figure 1. ispLSI 3256 Functional Block Diagram



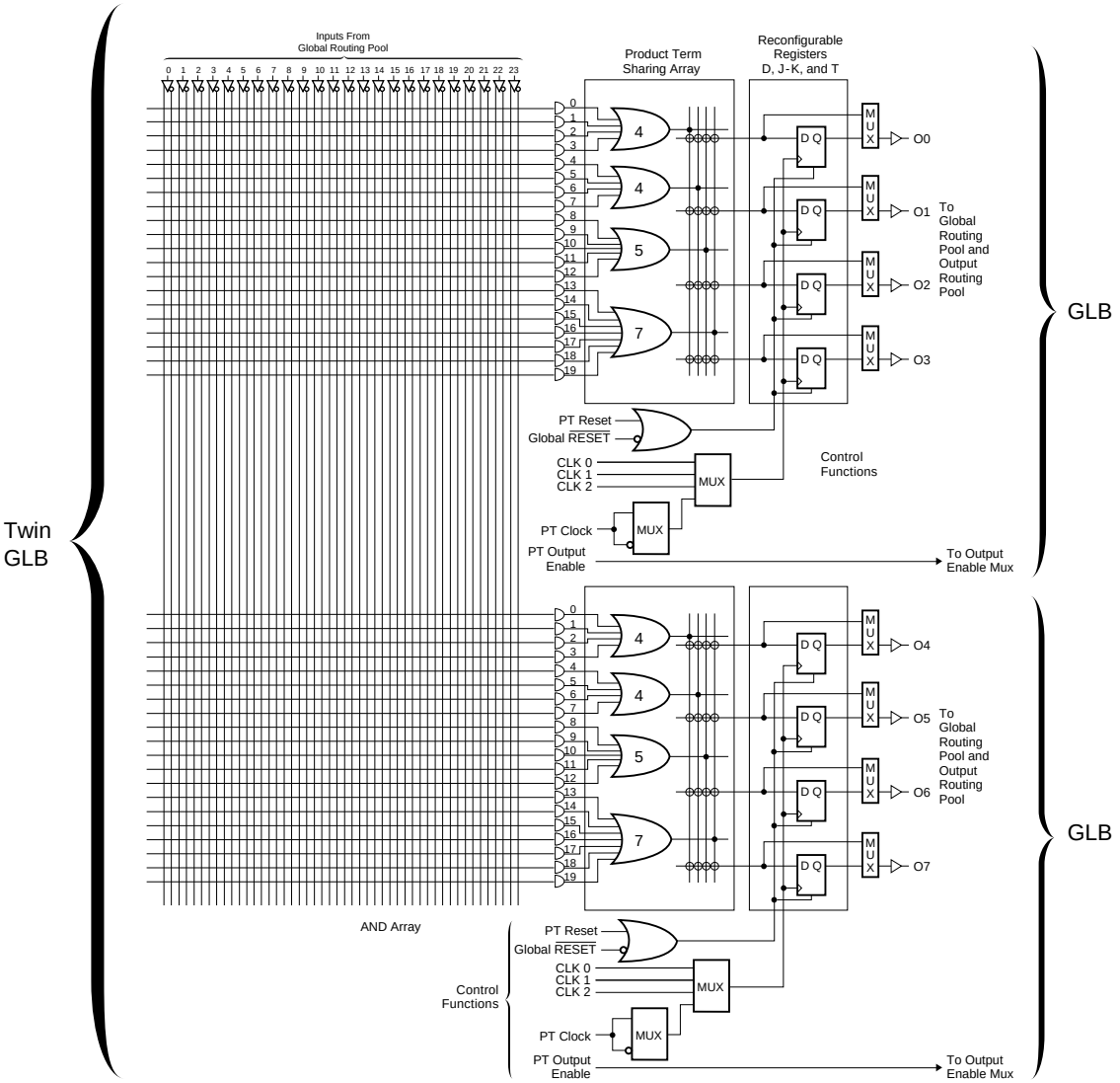
Generic Logic Block

The Twin GLB is the standard logic block of the Lattice Semiconductor ispLSI and pLSI 3000 Family. This Twin GLB has 24 inputs, eight outputs and the logic necessary to implement most standard logic functions. The internal logic of the Twin GLB is divided into four separate sections: The AND Array, the Product Term Sharing Array, the Reconfigurable Registers, and the Control section.

The AND array consists of two 20 Product Term Sharing Arrays which can produce the logical sum of any of the 24 Twin GLB inputs. These inputs all come from the GRP, and are either feedback signals from any of the 32 Twin GLBs or inputs from the external I/O Cells. All Twin GLB input signals are available to the Product Terms in both the logical true and complemented forms which makes Boolean logic reduction easier.

The two Product Term Sharing Arrays (PTSA) take the 20 Product Terms each and allocate them to four Twin GLB outputs. There are four OR gates, with four, four, five and seven inputs respectively. The output of any of these gates can be routed to any of the four Twin GLB outputs, and if more Product Terms are needed, the PTSA can combine them as necessary. If the user's main concern is speed, the PTSA can use a bypass circuit with four Product Terms to increase the performance of the cell. This can be done to any or all of the eight outputs of the Twin GLB.

Figure 2. Twin GLB: Product Term Sharing Array



Megablock Structure

Four Twin GLBs make up a Megablock. Each GLB has a maximum fan-in of 24 inputs, and no dedicated inputs associated with any Megablock. A GLB has eight associated outputs. A total of 32 GLB outputs are fed to the ORP of "single I/O" 3000 family devices (i.e., those with one I/O pin for every two GLB outputs, such as the 3256). However, only 16 out of the 32 outputs feed to 16 I/O cells. For "double I/O" 3000 family devices (those with one I/O pin for each GLB output, such as the 3192), 16 GLB outputs are fed to each ORP which drives 16 I/O cells. "Double I/O" devices, therefore, employ two ORP's per Megablock.The Megablock structure for single and double I/O devices is shown in figures 3 and 4.

Figure 3. ispLSI and pLSI 3000 Family Single I/O Megablock Block Diagram

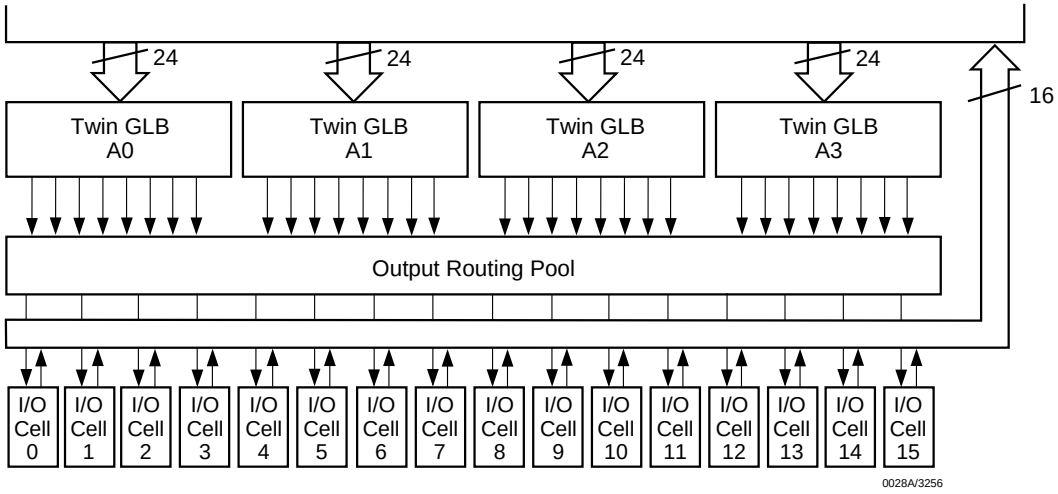
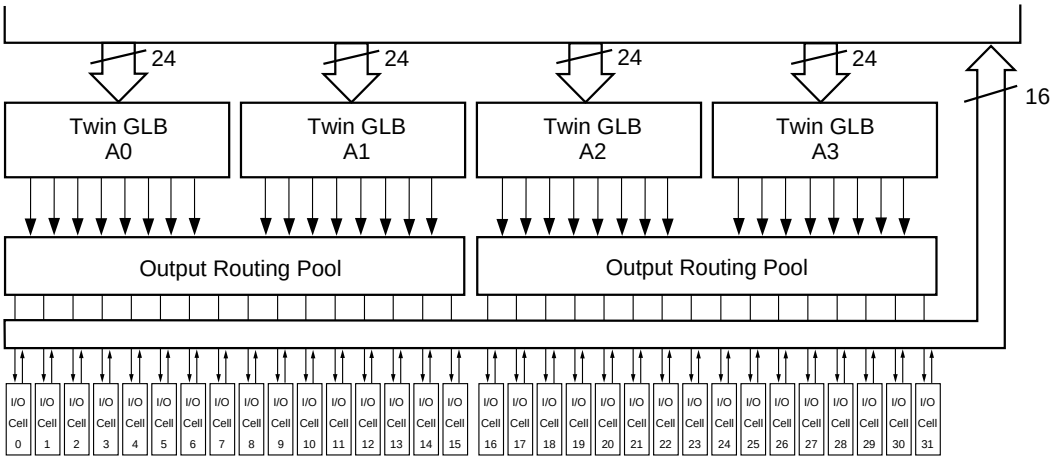


Figure 4. ispLSI and pLSI 3000 Family Double I/O Megablock Block Diagram



Global Clock Structure

The global clock structure is made up of five global clock input pins, Y0, Y1, Y2, Y3, and Y4. This is shown in figure 5. Three of the clock pins are dedicated for GLB clocks and the remaining two clock pins are dedicated for I/O register clocks. The clock GLB generation network which is designed into the 1000/E device family has been removed so all input clock signals are fed directly to the GLB clock input via a clock multiplexer. The GLB global clocks do not have inversion capability, but the product term clock does have inversion capability before it reaches the clock multiplexer.

Figure 5. ispLSI and pLSI 3000 Family Global Clock Structure

I/O Cells

The I/O cell structure architecture remains nearly the same as the 1000/E Family as illustrated in figure 6. Each I/O cell now contains Boundary Scan Registers, shown in figure 9 and discussed in detail in the next section. An input pin has only one scan register as shown in figure 10. A global test OE signal is hardwired to all I/O cells and is useful to perform static testing of all the 3-state output buffers within the device. In addition to the test OE signal, two global OEs are connected to all I/O pins. The product term OE signal and global OE signals are fed to an OE multiplexer. The OE signals, with the exception of the test OE, have inversion capability after going through the OE multiplexer as shown in figure 7.

Figure 6. ispLSI and pLSI 3000 Family I/O Cell Architecture

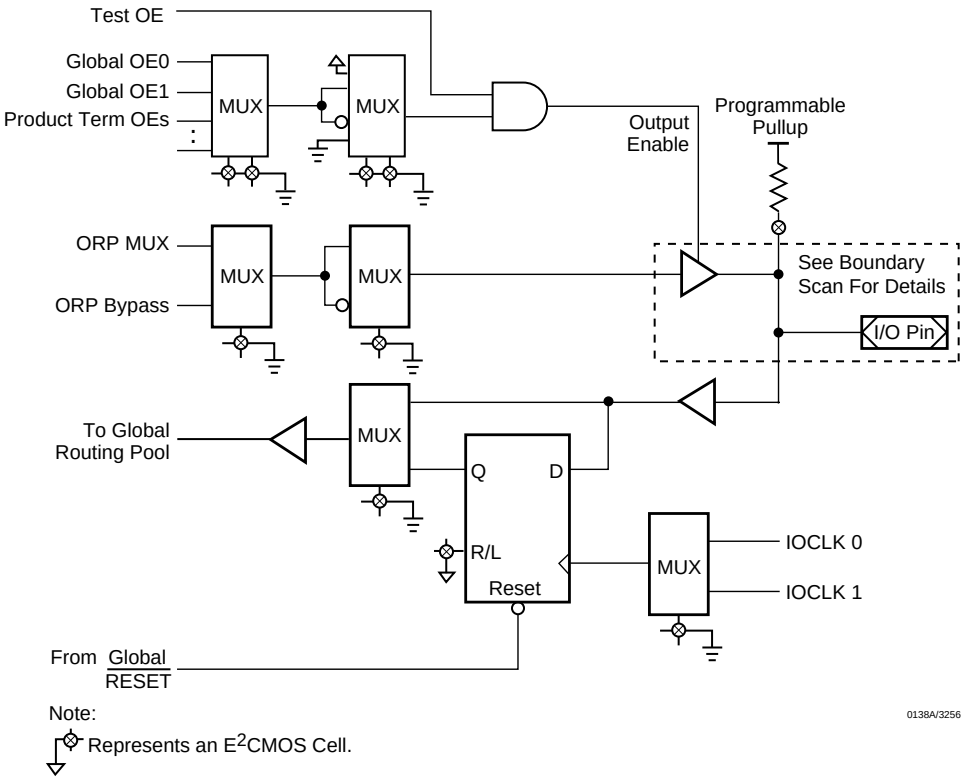
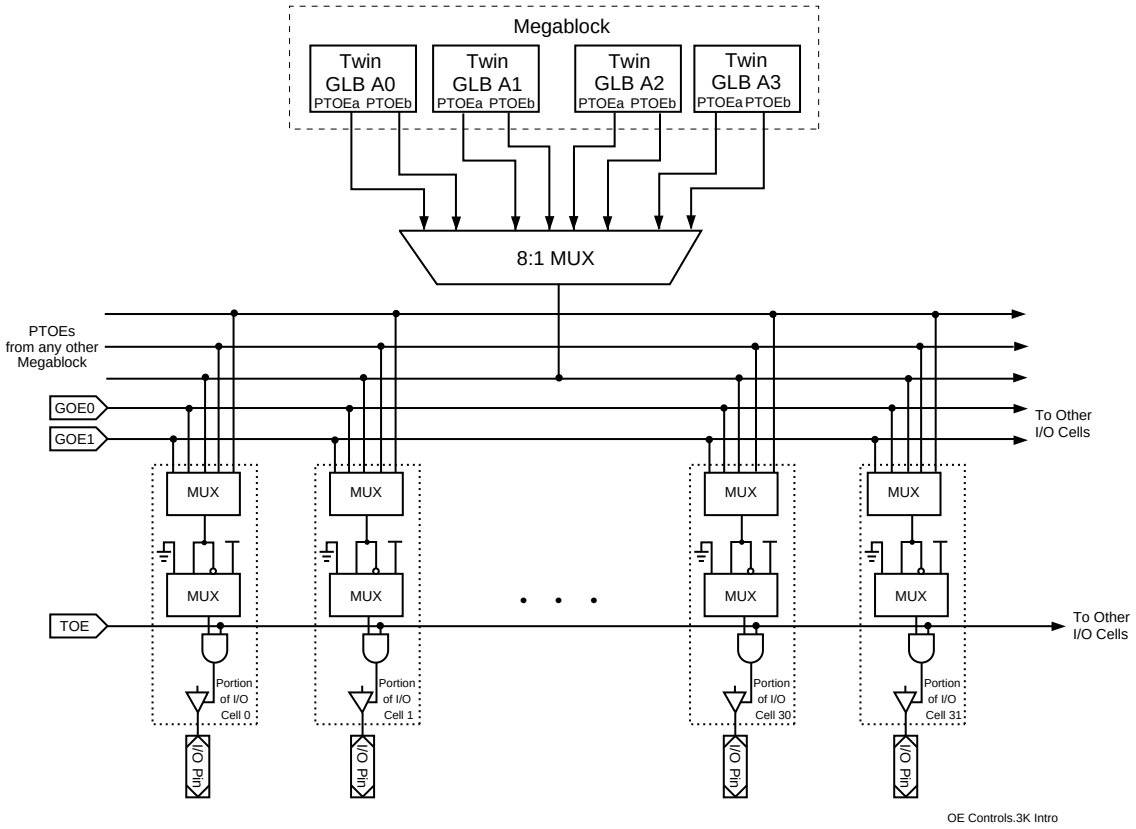


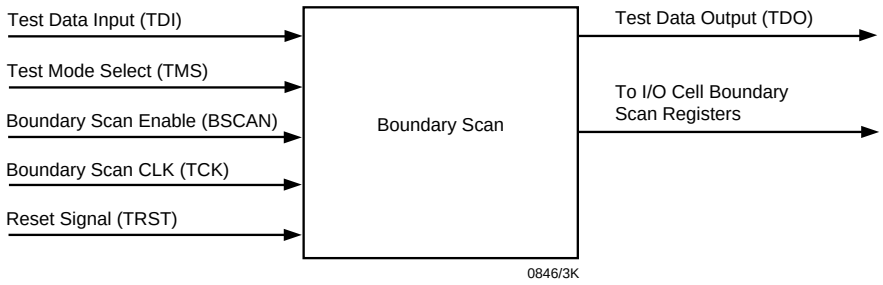
Figure 7. ispLSI and pLSI 3000 Family Output Enable Controls



Boundary Scan

Boundary Scan (IEEE 1149.1 compatible) is a test feature incorporated within the device to provide on-chip test capabilities during PCB testing. Five input signal pins, BSCAN, TDI, TCK, TMS, $\overline{\text{TRST}}$, and one output signal pin, TDO, are associated with the boundary scan logic cells. These signal pins occupy the same dedicated signal pins used for ISP programming. The signal BSCAN is associated with the ispEN pin, TDI corresponds to the SDI pin, TCK corresponds to the SCLK pin, TMS corresponds to the MODE pin, and TDO corresponds to the SDO pin. When ispEN is asserted low, the MODE, SDI, SDO, and SCLK options become active for ISP programming. Otherwise, BSCAN, TDI, TCK, TMS, TDO, and $\overline{\text{TRST}}$ options become active for boundary scan testing of the device. The boundary scan block diagram is shown in figure 8. TDI is the test data serial input, TCK is the boundary scan clock associated with the serial shift register, TMS is the test mode select input, TDO is the test data output, and $\overline{\text{TRST}}$ is the reset signal.

Figure 8. Boundary Scan Block Diagram



The user interfaces to the boundary scan circuitry through the Test Access Port (TAP). The TAP consists of a control state machine, instruction decoder and instruction register.

The TAP is controlled using the test control lines: Test Data IN (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Reset (TRST) and Test Clock (TCK).

The TAP controls the operation of the Boundary Scan Registers after decoding the instruction code sent to the instruction register (see table 1).

The Boundary Scan Registers for the I/O cells are shown in figure 9. As illustrated in the figure, each I/O cell contains three registers, two latches and five multiplexers to implement the ability to capture the state of the I/O cell or to set the state of the output path of the cell or to function as a conventional I/O cell.

The Boundary Scan Registers required for an input only cell are shown in figure 10. An input only cell can only have its state captured, which only requires one MUX and one register.

All of the input cells and I/O cells are serially connected together in a long chain. The scan out of one cell is connected to the scan in of the next cell. The cells for the 3256 are connected in the following order: TDI to IO63 through IO32 to Y4, Y3, Y2, Y1, RESET, TOE, GOE1, GOE0, Y0, IO31 through IO0 to IO64 through IO127 to TDO. The cells for the 3192 are connected in the following order: TDI to GOE0, GOE1, Y0, Y1, Y2, Y3, Y4, RESET, I/O95 through I/O0 to I/O96 through I/O191 to TDO.

Figure 9. Boundary Scan Registers for I/O Cells

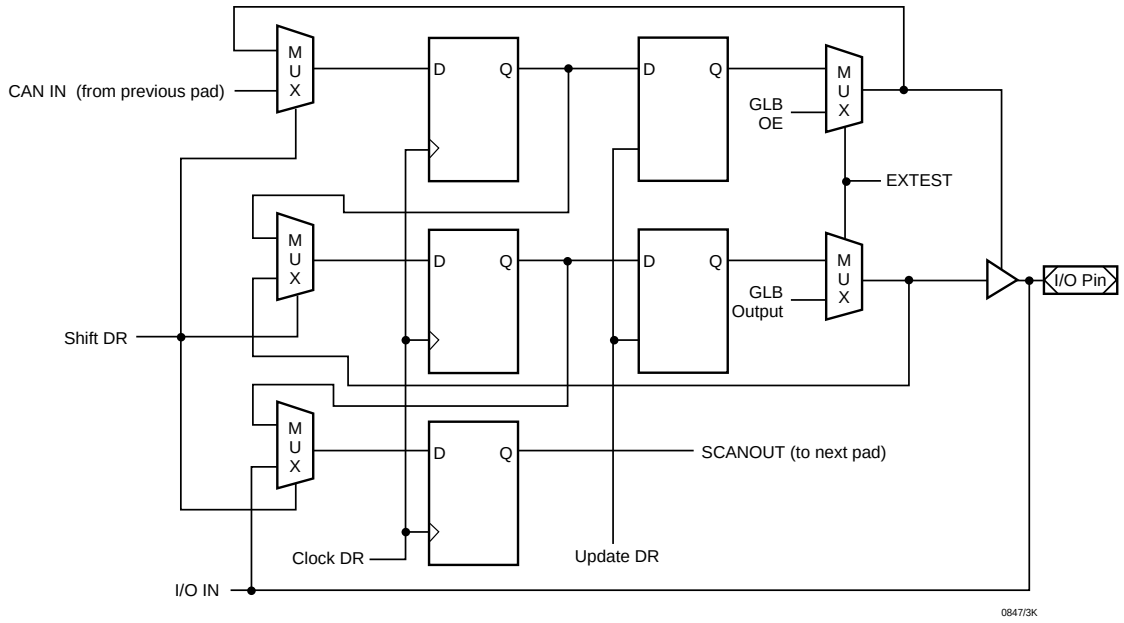


Figure 10. Boundary Scan Registers for an Input Only Cell

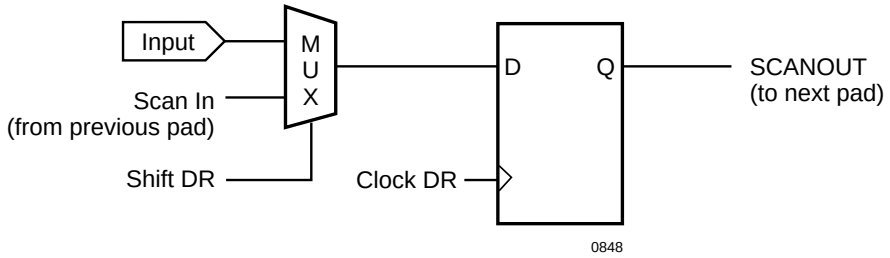


Table 1. Boundary Scan Instruction Codes

Instruction Name	Code		Description
SAMPLE/PRELOAD	10*	11100	Loads and shifts data into BSCAN registers
EXTEST	00*	00000	Drives external I/O with BSCAN registers
BYPASS	11*	11111	Bypasses registers of selected device(s)

Note: LSB shifts in 1st
*3256 only

Table 10-0006/3K

Timing Model

The task of determining the timing through the device is simple and straightforward. A device timing model is shown in figure 11. To determine the time that it takes for data to propagate through the device, simply determine the path the data is expected to follow, and add the various delays together (figure 12). Critical timing paths are shown in figure 11, using data sheet parameters. Note that the Internal timing parameters are given for reference only, and are not tested. External timing parameters are tested and guaranteed on every device.

Figure 11. ispLSI and pLSI 3256 Timing Model

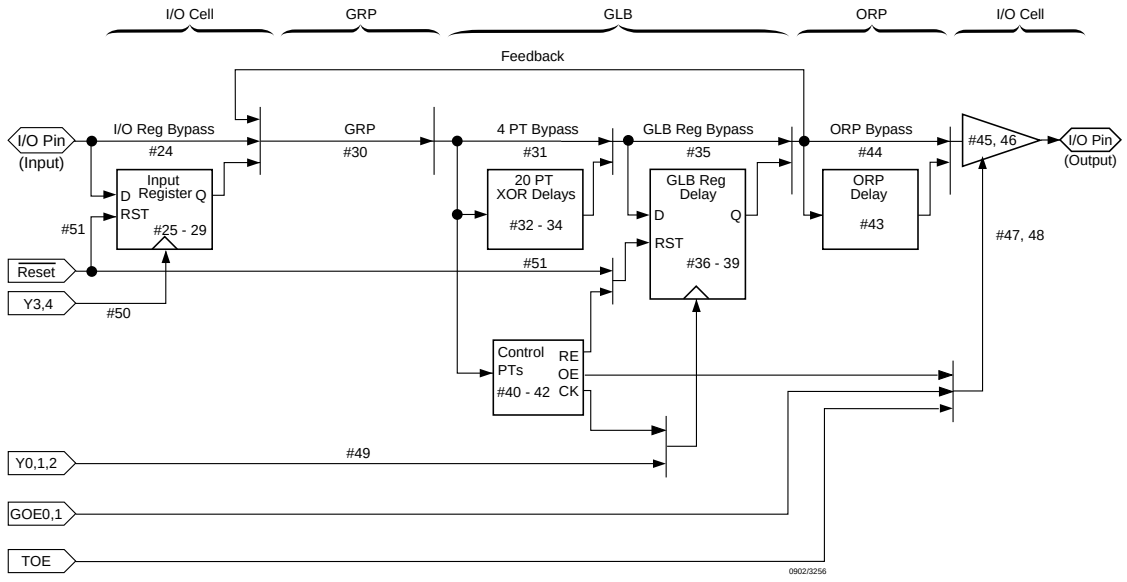


Figure 12. Timing Calculation Example

Derivations of tsu, th and tco from the Product Term Clock[1]

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**iobp + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp + **t**ptck(min))
	=	(#24+ #30+ #33) + (#36) - (#24+ #30+ #42)
8.0 ns	=	(2.4 + 3.0 + 9.4) + (1.8) - (2.4 + 3.0 + 3.2)
th	=	Clock (max) + Reg h - Logic
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp + **t**20ptxor)
	=	(#24+ #30+ #42) + (#37) - (#24+ #30+ #33)
2.9 ns	=	(2.4 + 3.0 + 6.3) + (6.0) - (2.4 + 3.0 + 9.4)
tco	=	Clock (max) + Reg co + Output
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#24 + #30 + #42) + (#38) + (#43 + #45)
2.9 ns	=	(2.4 + 3.0 + 6.3) + (1.8) + (2.7 + 2.4)

Table 2- 0042-16/3256

1. Calculations are based upon timing specifications for the ispLSI and pLSI 3256-70L.

6000 Family Architectural Description

ispLSI and pLSI 6000 Family Introduction

The ispLSI and pLSI 6192 devices are high-density, cell-based programmable logic devices that contain a dedicated Memory Module, a dedicated Register/Counter Module and an 8000-gate general-purpose Programmable Logic block. Output Routing Pools (ORP) and a Global Routing Pool (GRP) give complete interconnectivity between these elements. The dedicated modules have been added to enhance the functionality, performance and utilization of the device.

The ispLSI and pLSI 6192 is offered in three versions: the ispLSI and pLSI 6192FF (FIFO), 6192SM (Single Port RAM) and 6192DM (Dual Port RAM). All three devices employ the same general-purpose programmable logic module and register/counter module, with only the memory module functionality changing. The pinouts of the three devices are different only in the memory module control interface pins.

Memory Module

Lattice Semiconductor offers a dedicated dual-port FIFO module in the ispLSI and pLSI 6192FF devices. The FIFO is user configurable as a 256 x 18 or 512 x 9 block and is connected to the external world through dedicated FIFO I/O pins. The other data port of the FIFO goes to the GRP. A variety of FIFO control flags such as Full ($\overline{FF}$), Almost Full ($\overline{ALF}$), Almost Empty ($\overline{ALE}$) and Empty ($\overline{EF}$) are available as dedicated device outputs. These signals are also available as inputs to the GRP to facilitate use by on-chip logic.

The ispLSI and pLSI 6192SM feature a single-port memory module. The module can be organized either as a single 256 x 18 or 512 x 9 single port memory or as two smaller 128 x 18 or 256 x 9 single port memories. The external interface features memory address input pins (A0-A8), Read/Write (RWL/RWH), Chip Select ($\overline{CS}$), Output Enable ($\overline{OE}$) control lines, and 18 bidirectional data lines. The memory can be accessed from this external interface or from the internal GRP based on the user's design.

The ispLSI and pLSI 6192DM has functionality similar to the 6192SM, but access from the GRP or external pins is supported concurrently. Dedicated arbitration logic and Busy flags help to resolve issues arising from simultaneous access from both ports of the same memory location. The Busy signal from the external port ($\overline{BusyA}$) is available at a dedicated device pin.

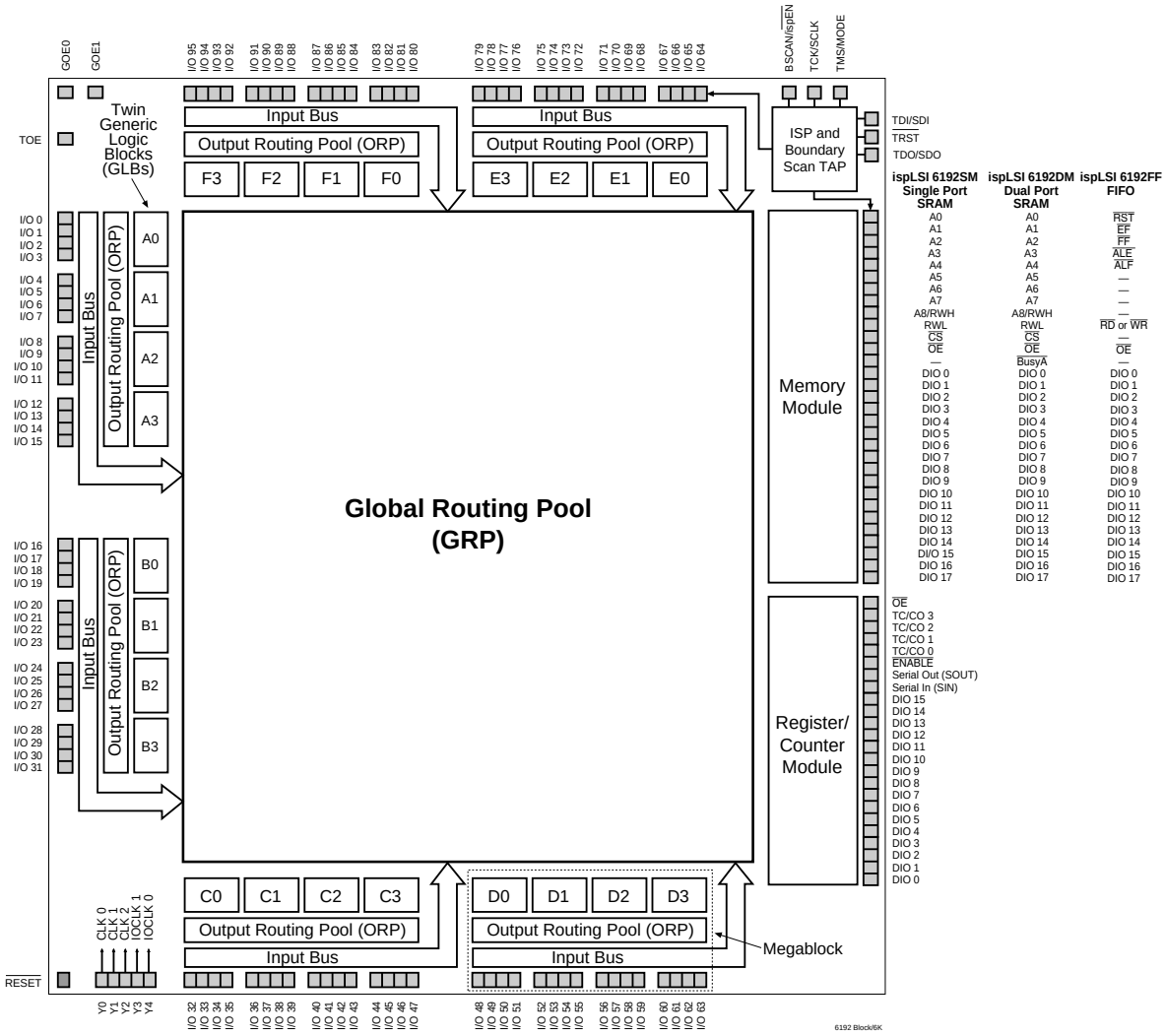
Register/Counter Module

An additional feature of the ispLSI 6192 and pLSI devices is a dedicated Register/Counter module. Eight 16-bit blocks are available to function as registers or shift registers. In addition, four of these blocks can be programmed to operate as loadable Up/Down counters. These four blocks include carry-in and carry-out connections to allow counter cascading up to 64 bits. The

Table 1. ispLSI and pLSI 6192 Device Features

	Memory Module Options			Register/Counter Module	General Programmable Logic Module
Functions	FIFO 6192FF	Single-Port SRAM 6192SM	Dual-Port SRAM 6192DM	Programmable Register / Counter / Timer / Shift Register	Universal: Registered or Combinatorial
Organization	Programmable 512 x 9 or 256 x 18			Cascadeable 8 x 16 Bit Words	192 Macrocells
External Interface	18 I/O & 13 Control Pins			16 I/O & 8 Control Pins	96 I/O / 5 Clocks / 2 Global Output Enables
Performance	20ns Memory Access Time (Tacc)			125MHz Counter Frequency (Fcnt)	15ns Logic Delay (Tpd) 70MHz Frequency (Fmax)
Programmability	In-System Programmable				
Testability	IEEE 1149.1 Boundary Scan Test				
Package	208-Pin Metal Quad Flat Pack (MQFP)				

Figure 1. ispLSI and pLSI 6192 Functional Block Diagram



Note:
Since certain signal names are duplicated on Memory Module and Register/Counter Module pins ($\overline{OE}$, DIO), the notation:
$\overline{OE}$ (RAM)
$\overline{OE}$ (RC)
DIO (RAM)
DIO (RC)
will be used periodically in this data sheet to differentiate signals.

Register/Counter block also has a 16-bit data port connected to the GRP along with a variety of control inputs and status flag outputs.

Programmable Logic Module

The basic unit of general-purpose programmable logic on the ispLSI and pLSI 6192 devices is the Twin Generic Logic Block (Twin GLB) labeled A0, A1....F3 in the block diagram. There are a total of 24 of these Twin GLBs in the ispLSI and pLSI 6192 devices. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays as well as eight outputs which can be configured independently to be combinatorial or registered. All Twin GLB logic inputs come from the GRP.

Four Twin GLBs, 16 I/O Cells and one ORP form a logic Megablock. The 16 I/O cells within a Megablock share one Product Term Output Enable and two Global Output Enable signals. The outputs of four Twin GLBs are connected to a set of 16 I/O cells by the ORP. The ispLSI and pLSI 6192 devices each contain six of these Megablocks.

The GRP has, as its inputs, the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells as well as independent bidirectional data bus ports from the FIFO and Register/Counter blocks. Flag outputs from these modules as well as control inputs are also connected to the GRP. All these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other logic block on the device. The device has 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a latched input, an output or a bidirectional I/O pin with 3-state control. Output signal levels are TTL compatible, and the output drivers can source 4mA and sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. The devices are packaged in space saving 208-pin Metal Quad Flat Pack (MQFP) packages.

Clocks in the ispLSI and pLSI 6192 devices are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

In-System Programmability

The ispLSI 6192 devices also feature 5-Volt in-system programmability and in-system diagnostic capabilities. Consequently, the devices offer non-volatile “on-the-fly” reprogrammability of logic and memory to support truly reconfigurable systems.

Boundary Scan

The ispLSI and pLSI 6192 family also has Boundary Scan capability, consisting of dedicated cells connected between the on-chip system logic and the device’s input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one. The device supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

For More Information

For full details on the ispLSI and pLSI 6000 cell-based architecture, see the ispLSI and pLSI 6192 data sheet in this Data Book.

Notes

Introduction to ispLSI® and pLSI®1000/E Families

Introduction

Lattice Semiconductor Corporation's (LSC) ispLSI and pLSI families are high-density and high-performance E^2CMOS® programmable logic devices. They provide design engineers with a superior system solution for integrating high-speed logic on a single chip.

The ispLSI and pLSI 1000 and 1000E families combine the performance and ease of use of PLDs with the density and flexibility of FPGAs.

The ispLSI and pLSI 1000 and 1000E families are ideal for designs requiring high speeds with highly integrated logic.

The ispLSI family incorporates Lattice Semiconductor's innovative in-system programmable™ (ISP™) technology. ISP technology allows for real-time programming, less expensive manufacturing and end-user feature reconfiguration.

E^2CMOS technology features reprogrammability, the ability to program the device again and again to easily incorporate any design modifications. This same capability allows full parametric testability during manufacturing, which guarantees 100 percent programming and functional yield.

All necessary development tools are available from LSC and third-party vendors. Development tools offered range from LSC's low cost pDS® software, featuring Boolean entry in a graphical Windows™ based environment, to the pDS+™ family of Fitters that interface with third party development software packages. Design systems interfacing with pDS+ Fitters feature schematic capture, state machine and HDL design entry. Designs can now be completed in hours as opposed to days or weeks.

ispLSI and pLSI 1000 and 1000E Families

- ❑ 125 MHz System Performance
- ❑ 7.5 ns Pin-to-Pin Delay
- ❑ Deterministic Performance
- ❑ High Density (2,000-8,000 PLD Gates)
- ❑ 44-Pin to 133-Pin Package Options
- ❑ Flexible Architecture
- ❑ Easy-to-Use
- ❑ In-System Programmable (ispLSI)

ispLSI and pLSI Technology

- ❑ UltraMOS E^2CMOS — the PLD Technology of Choice
- ❑ Electrically Erasable/Programmable/ Reprogrammable
- ❑ 100% Tested During Manufacture
- ❑ 100% Programming Yield
- ❑ Fast Programming

ispLSI and pLSI Development Tools

- ❑ Low Cost, Fully Integrated pDS Design System for the PC
- ❑ pDS+ Support for Industry-Standard Third-Party Design Environments and Platforms
- ❑ HDL, VHDL, Boolean Equation, State Machine and Schematic Capture Entry
- ❑ Timing and Functional Simulation
- ❑ PC and Workstation Platforms

Introduction to ispLSI and pLSI 1000/E Families

1000 and 1000E Families Overview

The ispLSI and pLSI 1000 and 1000E families of high-density devices address high-performance system logic needs, ranging from registers, to counters, to multiplexers, to complex state machines.

With PLD densities ranging from 2,000 to 8,000 gates, the ispLSI and pLSI 1000 and 1000E families provide a wide range of programmable logic solutions which meet tomorrow's design requirements today.

Each device contains multiple Generic Logic Blocks (GLBs), which are designed to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provides the optimum combination of internal logic and external connections. A global interconnect scheme ties everything together, enabling utilization of up to 80% of available logic. Table 1 describes the family attributes.

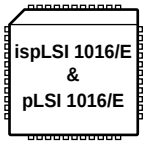
Table 1. ispLSI and pLSI 1000E Family Attributes

Family Member	1016/1016E	1024/1024E	1032/1032E	1048/1048C/1048E
Density (PLD Gates)	2,000	4,000	6,000	8,000
Speed: **f**max (MHz)	125	125	90	90
Speed: **t**pd (ns)	7.5	7.5	10	10
GLBs	16	24	32	48
Registers	96	144	192	288
Inputs + I/O	36	54	72	106*/110
Pin/Package	44-pin PLCC 44-pin TQFP 44-pin JLCC	68-pin PLCC 100-pin TQFP 68-pin JLCC	84-pin PLCC 100-pin TQFP 84-pin CPGA	120-pin PQFP* 128-pin PQFP 133-pin CPGA

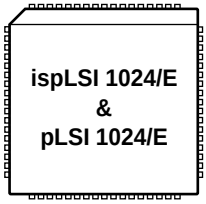
Table 1/1K Intro

* ispLSI/pLSI 1048 Only

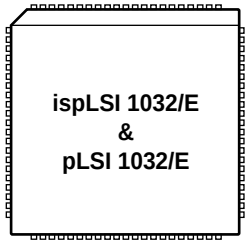
Figure 1. 1000/E Family Packages



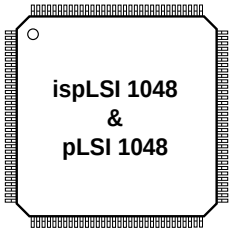
44-Pin PLCC



68-Pin PLCC



84-Pin PLCC

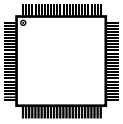


120-Pin PQFP

ispLSI 1016/E
&
pLSI 1016

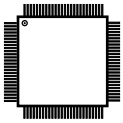
44-Pin TQFP

ispLSI 1024/E

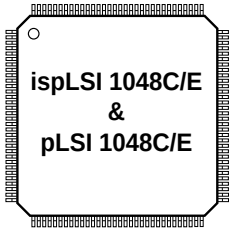


100-Pin TQFP

ispLSI 1032/E
&
pLSI 1032

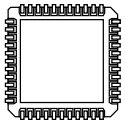


100-Pin TQFP



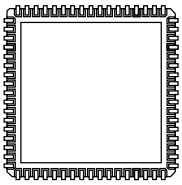
128-Pin PQFP

ispLSI 1016/883
&
pLSI 1016/883



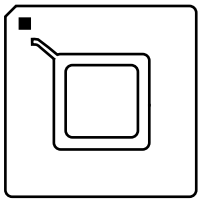
44-Pin JLCC

ispLSI 1024/883
&
pLSI 1024/883



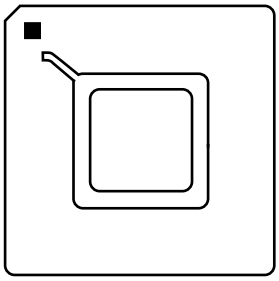
68-Pin JLCC

ispLSI 1032/883
&
pLSI 1032/883



84-Pin CPGA

ispLSI 1048C/883
&
pLSI 1048C/883



133-Pin CPGA

Pkgs.1K Intro/2

Notes

ispLSI® and pLSI® 1016E

High-Density Programmable Logic

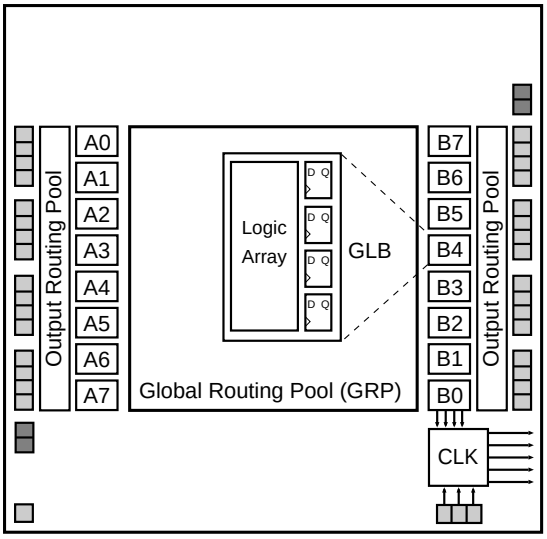
Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **— 2000 PLD Gates**
  - **— 32 I/O Pins, Four Dedicated Inputs**
  - **— 96 Registers**
  - **— High-Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 125 MHz Maximum Operating Frequency**
  - **— t_{pd} = 7.5 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **— Reprogram Soldered Device for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Enhanced Pin Locking Capability**
  - **— Three Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **pLSI/ispLSI DEVELOPMENT TOOLS**

  pDS® Software
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning**
  - **— Automatic Place and Route**
  - **— Static Timing Table**

  pDS+™ Software
  - **— Industry Standard, Third-Party Design Environments**
  - **— Schematic Capture, State Machine, HDL**
  - **— Automatic Partitioning and Place and Route**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

Functional Block Diagram



Description

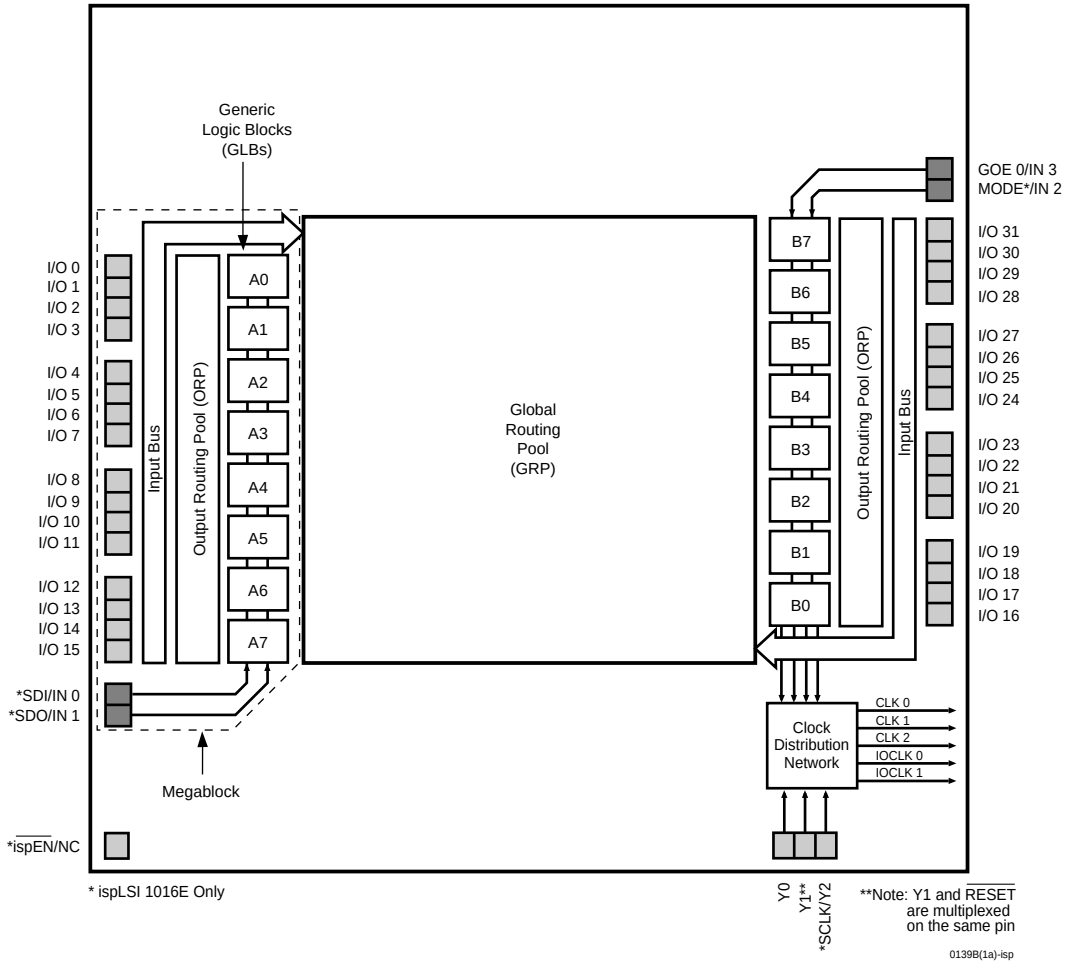
The ispLSI and pLSI 1016E are High Density Programmable Logic Devices containing 96 Registers, 32 Universal I/O pins, four Dedicated Input pins, three Dedicated Clock Input pins, one Global OE input pin and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1016E features 5-Volt in-system programming and in-system diagnostic capabilities. The ispLSI 1016E offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1016E device, but multiplexes four input pins to control in-system programming. A functional superset of the ispLSI and pLSI 1016 architecture, the ispLSI and pLSI 1016E devices add a new global output enable pin.

The basic unit of logic on the ispLSI and pLSI 1016E devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1...B7 (see figure 1). There are a total of 16 GLBs in the ispLSI and pLSI 1016E devices. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Functional Block Diagram

Figure 1. ispLSI and pLSI 1016E Functional Block Diagram



The devices also have 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each ispLSI and pLSI 1016E device contains two Megablocks.

The GRP has, as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 1016E devices are selected using the Clock Distribution Network. Three dedicated clock pins (Y0, Y1 and Y2) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (B0 on the ispLSI and pLSI 1016E devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2-0005/2000

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input, I/O, Y1, Y2 Clock Capacitance	8	pf	V_{CC} = 5.0V, V_{PIN} = 2.0V
C_2	Y0 Clock Capacitance	12	pf	V_{CC} = 5.0V, V_{PIN} = 2.0V

1. Guaranteed, but not 100% tested.

Table 2 - 0006a

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2-0008A-isp

Switching Test Conditions

Input Pulse Levels	GND to 3.0V	
Input Rise and Fall Time 10% to 90%	-125	≤ 2 ns
	-100	≤ 3 ns
Input Timing Reference Levels	1.5V	
Ouput Timing Reference Levels	1.5V	
Output Load	See figure 2	

Table 2 - 0003/1016

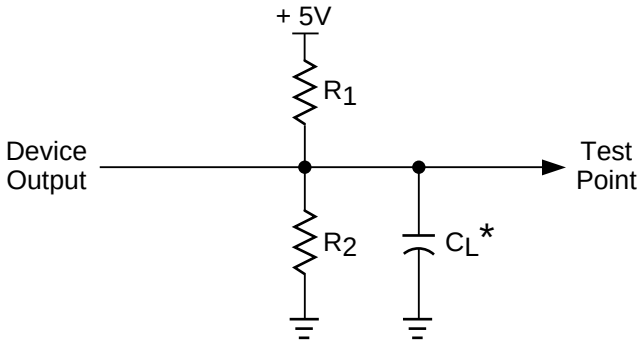
3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2-0004a

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213a

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
I_{IL-isp}	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V, f_{CLOCK} = 1 MHz	–	90	–	mA

Table 2-0007a-16-isp

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using four 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-125		-100		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	7.5	–	10.0	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	10.0	–	13.0	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	125	–	100	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	100	–	77.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle $\left(\frac{1}{twh + tw1}\right)$	167	–	125	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	5.0	–	7.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	4.5	–	5.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	5.5	–	8.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	5.5	–	6.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	10.0	–	13.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	5.0	–	6.5	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	12.0	–	15.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	12.0	–	15.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	7.0	–	9.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	7.0	–	9.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	3.0	–	4.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	3.0	–	4.0	–	ns
t_{su3}	–	20	I/O Reg. Setup Time before Ext. Sync Clock (Y2, Y3)	3.0	–	3.5	–	ns
t_{h3}	–	21	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	0.0	–	0.0	–	ns

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Table 2-0030-16/125,100

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-125		-100		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
tiobp	22	I/O Register Bypass	–	0.3	–	0.4	ns
tiolat	23	I/O Latch Delay	–	1.8	–	2.4	ns
tiosu	24	I/O Register Setup Time before Clock	3.0	–	3.5	–	ns
tioh	25	I/O Register Hold Time after Clock	-0.3	–	-0.4	–	ns
tioco	26	I/O Register Clock to Out Delay	–	4.0	–	5.0	ns
tior	27	I/O Register Reset to Out Delay	–	4.0	–	5.0	ns
tdin	28	Dedicated Input Delay	–	2.2	–	2.6	ns
GRP							
tgrp1	29	GRP Delay, 1 GLB Load	–	1.8	–	1.9	ns
tgrp4	30	GRP Delay, 4 GLB Loads	–	1.9	–	2.2	ns
tgrp8	31	GRP Delay, 8 GLB Loads	–	2.1	–	2.5	ns
tgrp16	32	GRP Delay, 16 GLB Loads	–	2.4	–	3.1	ns
GLB							
t4ptbpc	34	4 Product Term Bypass Path Delay (Combinatorial)	–	3.9	–	5.7	ns
t4ptbpr	35	4 Product Term Bypass Path Delay (Registered)	–	3.9	–	5.6	ns
t1ptxor	36	1 Product Term/XOR Path Delay	–	4.4	–	6.1	ns
t20ptxor	37	20 Product Term/XOR Path Delay	–	4.4	–	6.1	ns
txoradj	38	XOR Adjacent Path Delay[3]	–	4.4	–	6.6	ns
tgbp	39	GLB Register Bypass Delay	–	1.0	–	1.6	ns
tgsu	40	GLB Register Setup Time before Clock	0.2	–	0.2	–	ns
tgh	41	GLB Register Hold Time after Clock	1.5	–	2.5	–	ns
tgco	42	GLB Register Clock to Output Delay	–	1.8	–	1.9	ns
tgro	43	GLB Register Reset to Output Delay	–	4.4	–	6.3	ns
tptre	44	GLB Product Term Reset to Register Delay	–	3.5	–	5.1	ns
tptoe	45	GLB Product Term Output Enable to I/O Cell Delay	–	5.5	–	7.1	ns
tptck	46	GLB Product Term Clock Delay	3.2	3.5	4.8	5.3	ns
ORP							
torp	47	ORP Delay	–	1.0	–	1.0	ns
torpbp	48	ORP Bypass Delay	–	0.0	–	0.0	ns

Table 2-0036-16/125,100

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

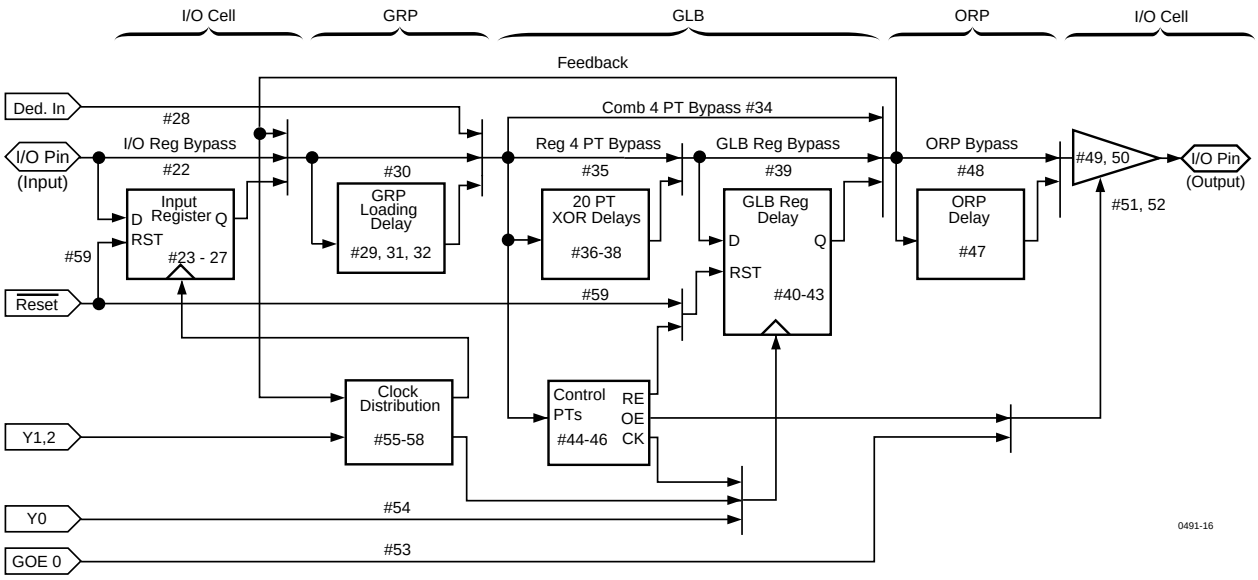
Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-125		-100		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	49	Output Buffer Delay	–	1.4	–	1.7	ns
t_{sl}	50	Output Slew Limited Delay Adder	–	10.0	–	10.0	ns
t_{oen}	51	I/O Cell OE to Output Enabled	–	4.3	–	5.3	ns
t_{odis}	52	I/O Cell OE to Output Disabled	–	4.3	–	5.3	ns
t_{goe}	53	Global Output Enable	–	2.7	–	3.7	ns
Clocks							
t_{gy0}	54	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	1.3	1.3	1.4	1.4	ns
$t_{gy1/2}$	55	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.3	2.7	2.4	2.9	ns
t_{gcp}	56	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	1.8	0.8	1.8	ns
$t_{ioy1/2}$	57	Clock Delay, Y1 or Y2 to I/O Cell Global Clock Line	0.0	0.3	0.0	0.4	ns
t_{iocp}	58	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	1.8	0.8	1.8	ns
Global Reset							
t_{gr}	59	Global Reset to GLB and I/O Registers	–	3.2	–	4.5	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

Table 2-0037-16/125,100

ispLSI and pLSI 1016E Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**iobp + **t**grp4 + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp4 + **t**ptck(min))
	=	(#22 + #30 + #37) + (#40) - (#22 + #30 + #46)
1.4 ns	=	(0.3 + 1.9 + 4.4) + (0.2) - (0.3 + 1.9 + 3.2)
th	=	Clock (max) + Reg h - Logic
	=	(**t**iobp + **t**grp4 + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp4 + **t**20ptxor)
	=	(#22 + #30 + #46) + (#41) - (#22 + #30 + #37)
0.6 ns	=	(0.3 + 1.9 + 3.5) + (1.5) - (0.3 + 1.9 + 4.4)
tco	=	Clock (max) + Reg co + Output
	=	(**t**iobp + **t**grp4 + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#22 + #30 + #46) + (#42) + (#47 + #49)
9.9 ns	=	(0.3 + 1.9 + 3.5) + (1.8) + (1.0 + 1.4)

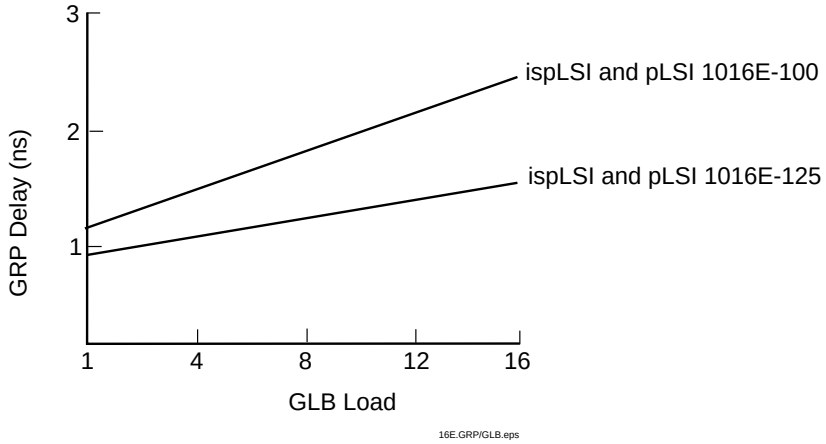
Derivations of tsu, th and tco from the Clock GLB[1]

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**iobp + **t**grp4 + **t**20ptxor) + (**t**gsu) - (**t**gy0(min) + **t**gco + **t**gcp(min))
	=	(#22 + #30 + #37) + (#40) - (#54 + #42 + #56)
2.9 ns	=	(0.3 + 1.9 + 4.4) + (0.2) - (1.3 + 1.8 + 0.8)
th	=	Clock (max) + Reg h - Logic
	=	(**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gh) - (**t**iobp + **t**grp4 + **t**20ptxor)
	=	(#54 + #42 + #56) + (#41) - (#22 + #30 + #37)
-0.2 ns	=	(1.3 + 1.8 + 1.8) + (1.5) - (0.3 + 1.9 + 4.4)
tco	=	Clock (max) + Reg co + Output
	=	(**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#54 + #42 + #56) + (#42) + (#47 + #49)
9.1 ns	=	(1.3 + 1.8 + 1.8) + (1.8) + (1.0 + 1.4)

Table 2-0042-16

1. Calculations are based upon timing specifications for the ispLSI and pLSI 1016E-125

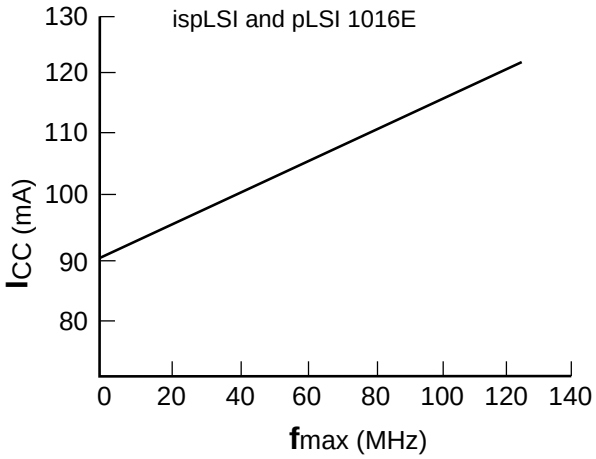
Maximum GRP Delay vs GLB Loads



Power Consumption

Power Consumption in the ispLSI and pLSI 1016E device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of four 16-bit counters
Typical current at 5V, 25°C

I_{CC} can be estimated for the ispLSI and pLSI 1016E using the following equation:

I_{CC}(mA) = 23 + (# of PTs * 0.52) + (# of nets * max freq * 0.004)

Where:
- # of PTs = Number of product terms used in design
- # of nets = Number of signals used in device
- Max freq = Highest clock frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of four GLB loads on average exists and the device is filled with four 16-bit counters. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

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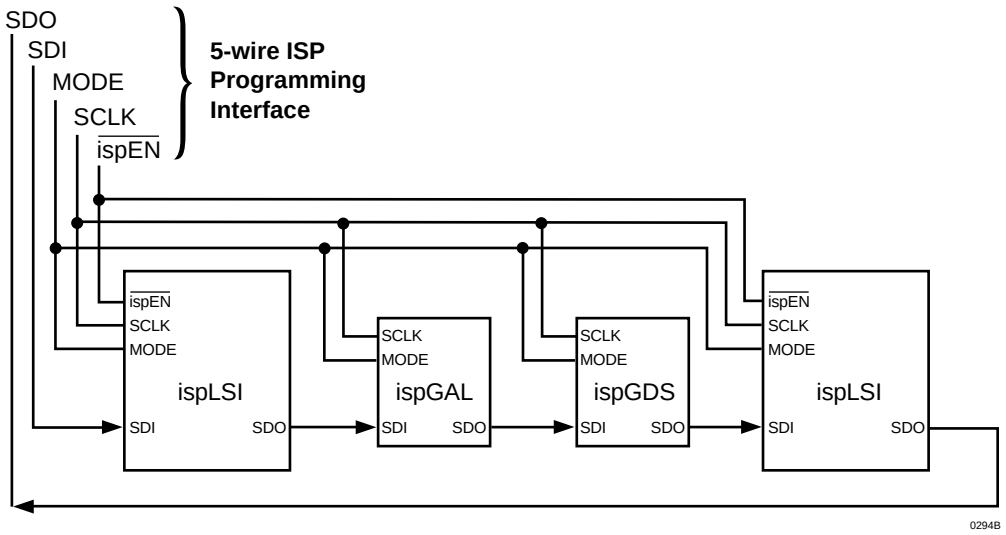
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor High-Density Programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

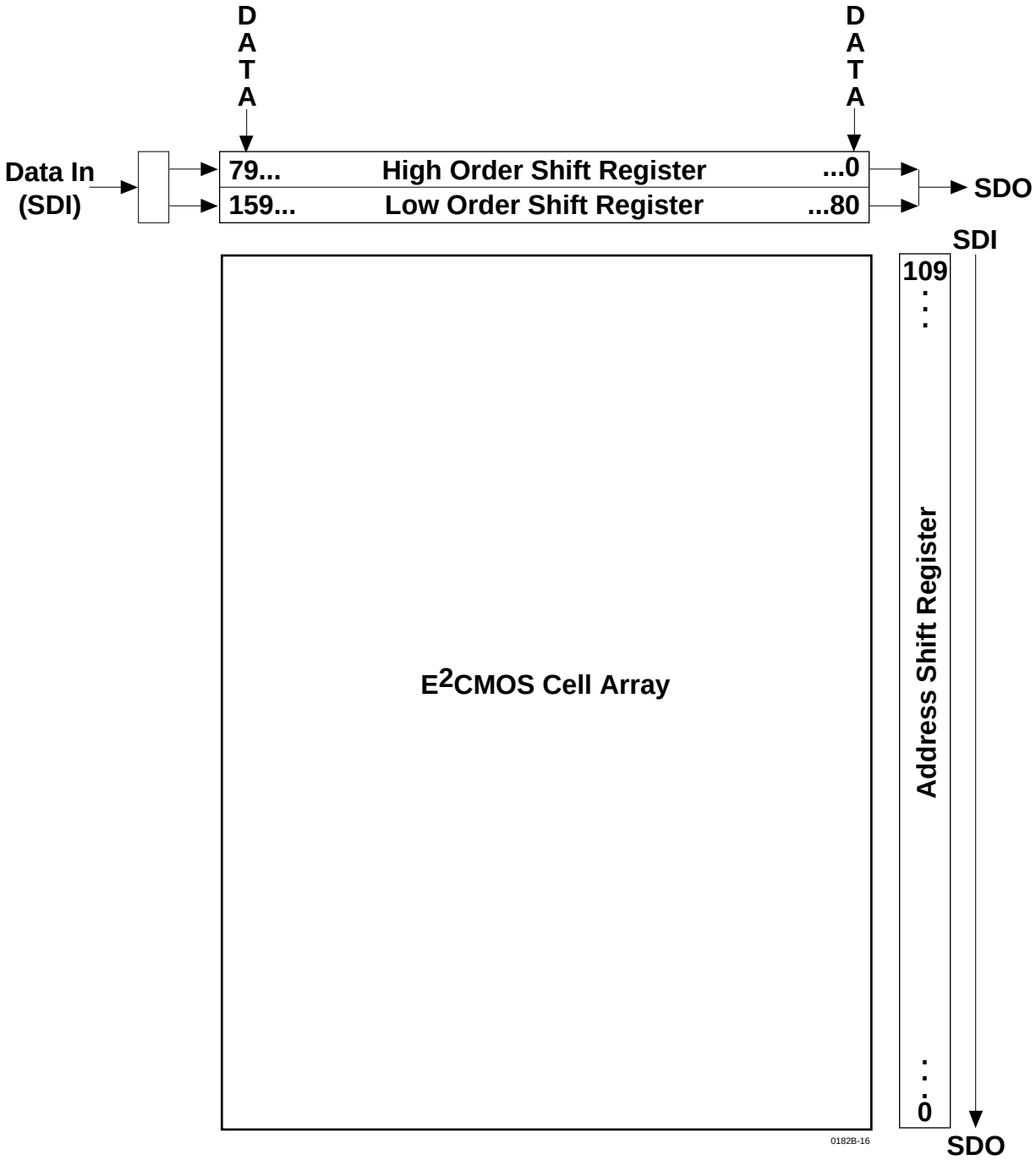
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for the interface include isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device, please refer to the ISP Architecture and Programming section of this Data Book.

The device identifier for the ispLSI 1016E is 0000 1011 (0B hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 1016E Shift Register Layout



Note: A logic “1” in the Address Shift Register bit position enables the row for programming or verification. A logic “0” disables it.

Pin Description

NAME	PLCC PIN NUMBERS	TQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	9, 10, 11, 12, 13, 14, 15, 16, 19, 20, 21, 22, 23, 24, 25, 26, 31, 32, 33, 34, 35, 36, 37, 38, 41, 42, 43, 44, 1, 2, 3, 4	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0/IN 3	2	40	This is a dual function pin. It can be used either as Global Output Enable for all I/O cells or it can be used as a dedicated input pin.
$\overline{\text{ispEN}}$**/NC	13	7	Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK controls become active.
SDI*/IN 0	14	8	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high.SDI/IN0 also is used as one of the two control pins for the isp state machine.
MODE*/IN 2	36	30	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high.
SDO*/IN 1	24	18	Output/Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an ouput pin to read serial shift register data. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high.
SCLK*/Y2	33	27	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. It is a dedicated clock input when $\overline{\text{ispEN}}$ is logic high. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device.
Y0	11	5	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs on the device.
Y1/$\overline{\text{RESET}}$	35	29	This pin performs two functions: - Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. - Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
GND	1, 23	17, 39	Ground (GND)
VCC	12, 34	6, 28	Vcc

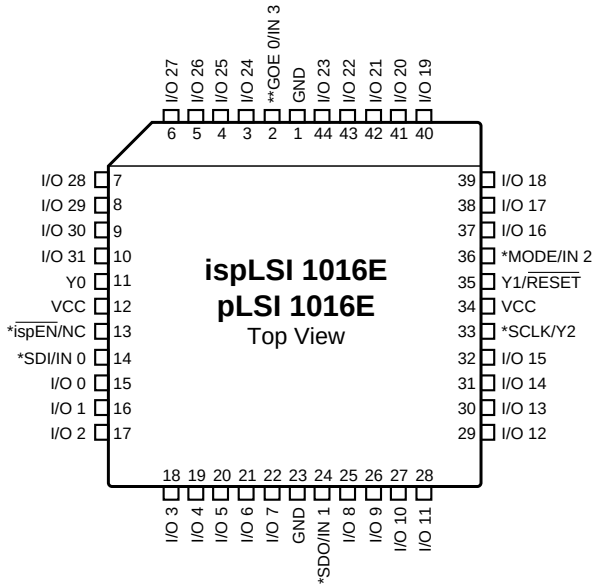
Table 2-0002C-16-isp

* ispLSI 1016E only

** $\overline{\text{ispEN}}$ for ispLSI 1016E; NC for pLSI 1016E must be left floating or tied to Vcc, must not be grounded or tied to any other signal.

Pin Configurations

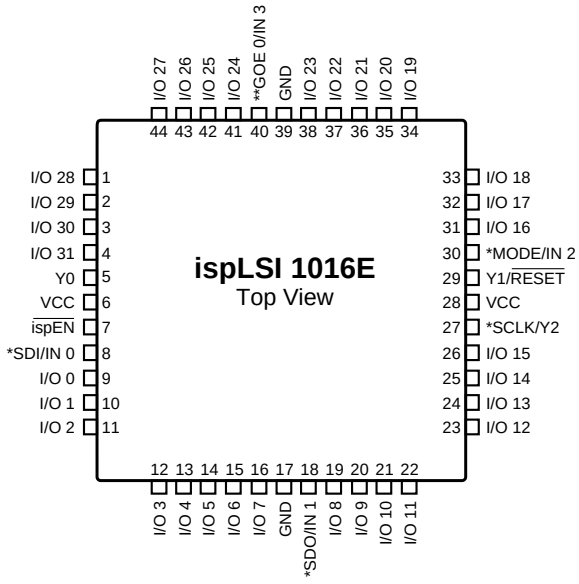
ispLSI and pLSI 1016E 44-pin PLCC Pinout Diagram



* Pins have dual function capability for ispLSI 1016E only (except pin 13, which is $\overline{\text{ispEN}}$ only).
** Pins have dual function capability which is software selectable.

0123A-isp1016

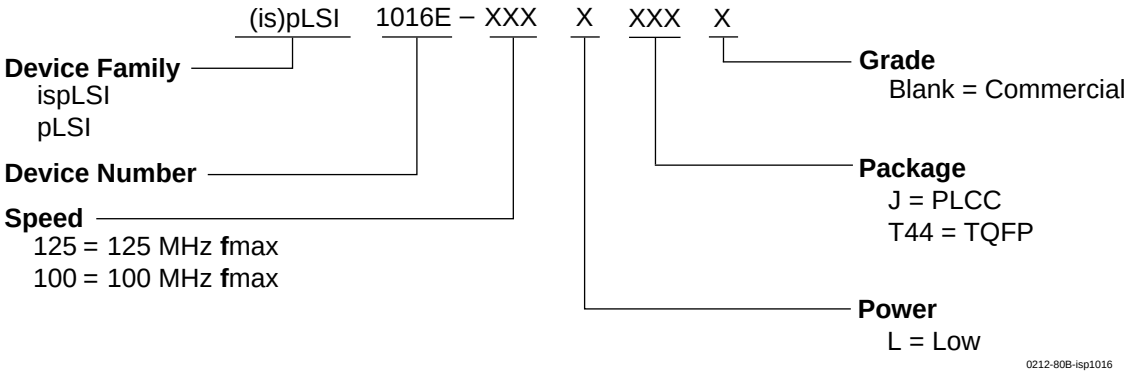
ispLSI 1016E 44-pin TQFP Pinout Diagram



* Pins have dual function capability.
** Pins have dual function capability which is software selectable.

0851-16E/TQFP

Part Number Description



ispLSI and pLSI 1016E Ordering Information

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	125	7.5	ispLSI 1016E-125LJ	44-Pin PLCC
	125	7.5	ispLSI 1016E-125LT44	44-Pin TQFP
	100	10	ispLSI 1016E-100LJ	44-Pin PLCC
	100	10	ispLSI 1016E-100LT44	44-Pin TQFP
pLSI	125	7.5	pLSI 1016E-125LJ	44-Pin PLCC
	100	10	pLSI 1016E-100LJ	44-Pin PLCC

Table 2 - 0041A-16-isp1016

ispLSI® and pLSI® 1016

High-Density Programmable Logic

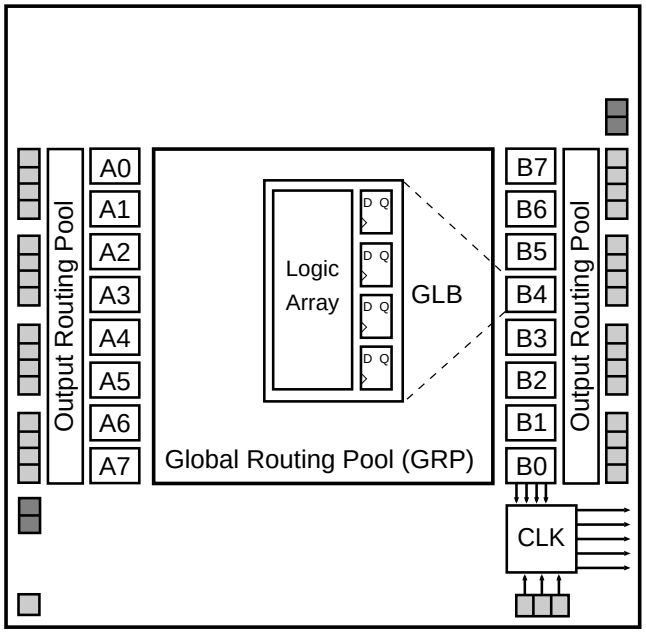
Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— High-Speed Global Interconnect**
  - **— 2000 PLD Gates**
  - **— 32 I/O Pins, Four Dedicated Inputs**
  - **— 96 Registers**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
  - **— Security Cell Prevents Unauthorized Copying**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 110 MHz Maximum Operating Frequency**
  - **— f_{max} = 60 MHz for Industrial and Military/883 Devices**
  - **— t_{pd} = 10 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile E²CMOS Technology**
  - **— 100% Tested**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Three Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI AND pLSI DEVELOPMENT TOOLS**

  pDS® Software
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning**
  - **— Automatic Place and Route**
  - **— Static Timing Table**

  pDS+™ Software
  - **— Industry Standard, Third Party Design Environments**
  - **— Schematic Capture, State Machine, HDL**
  - **— Automatic Partitioning**
  - **— Automatic Place and Route**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

Functional Block Diagram



Description

The ispLSI and pLSI 1016 are High-Density Programmable Logic Devices containing 96 Registers, 32 Universal I/O pins, four Dedicated Input pins, three Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1016 features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1016 device, but multiplexes four input pins to control in-system programming.

The basic unit of logic on the ispLSI and pLSI 1016 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. B7 (see figure 1). There are a total of 16 GLBs in the ispLSI and pLSI 1016 devices. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

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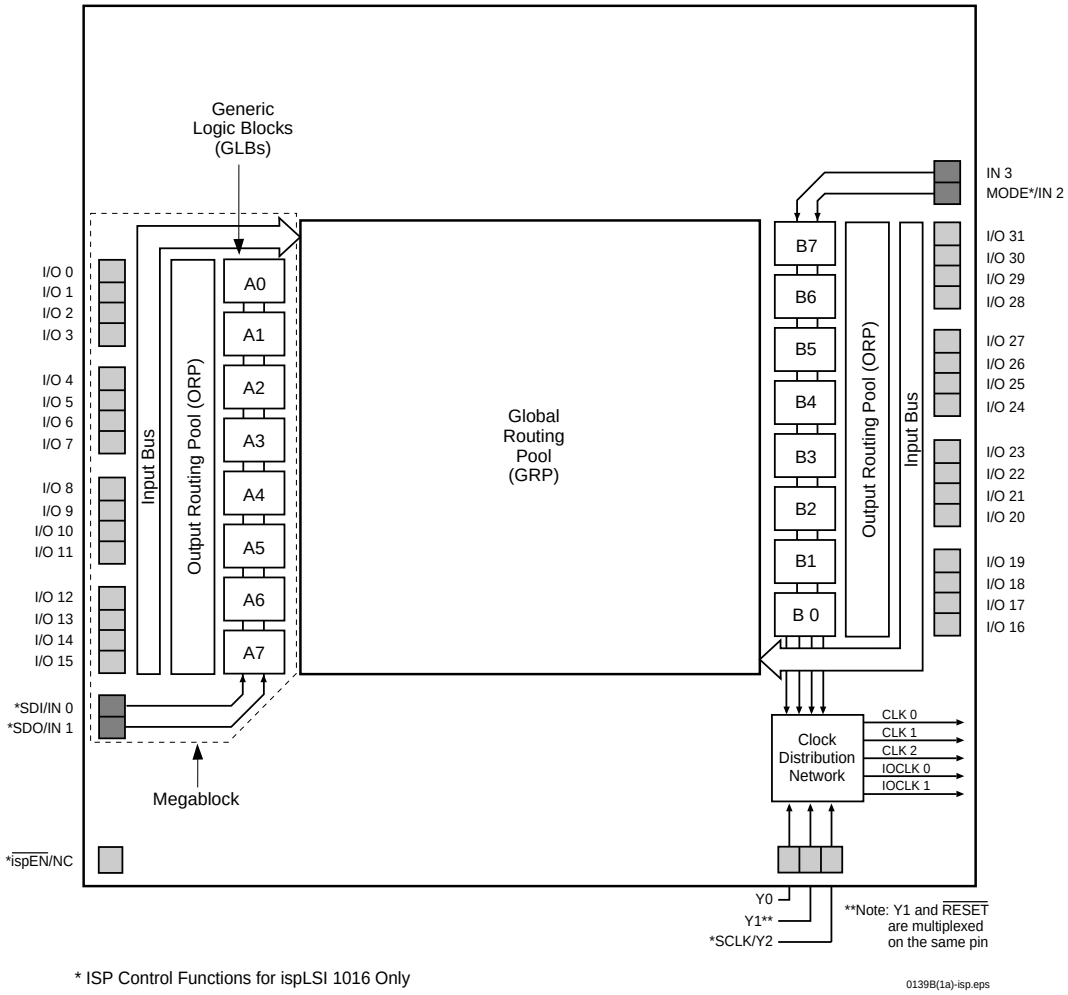
Functional Block Diagram

Figure 1. ispLSI and pLSI 1016 Functional Block Diagram



The devices also have 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The ispLSI and pLSI 1016 devices contain two of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 1016 devices are selected using the Clock Distribution Network. Three dedicated clock pins (Y0, Y1 and Y2) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (B0 on the ispLSI and pLSI 1016 devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to +70°C	4.75	5.25	V
		Industrial	T_A = -40°C to +85°C	4.5	5.5	
		Military/883	T_C = -55°C to +125°C	4.5	5.5	
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V

Table 2- 0005Aisp w/mil.eps

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER		MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	Commercial/Industrial	8	pf	V_{CC}=5.0V, V_{IN}=2.0V
		Military	10	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance		10	pf	V_{CC}=5.0V, $V_{I/O}$, V_Y=2.0V

1. Guaranteed but not 100% tested.

Table 2- 0006

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2- 0008B

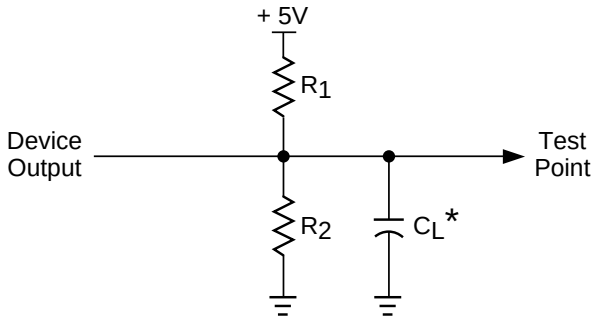
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

Table 2- 0003

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

Table 2- 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$		–	–	10	µA
$I_{IL\text{-}isp}$	isp Input Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		–	–	-150	µA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	$0V \le V_{IN} \le V_{IL}$		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V	Commercial	–	100	150	mA
		f_{TOGGLE} = 1 MHz	Industrial/Military	–	100	170	mA

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using four 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[5]	#[2]	DESCRIPTION[1]	-110		-90		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	10	–	12	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	14.5	–	17	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	111	–	90.9	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	70.1	–	58.8	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	125	–	125	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	4.5	–	6	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	–	7	–	8	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	7.5	–	9	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	8.5	–	10	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	14	–	15	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10	–	10	–	ns
t_{en}	B	14	Input to Output Enable	–	15	–	15	ns
t_{dis}	C	15	Input to Output Disable	–	15	–	15	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	4	–	4	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	4	–	4	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y1, Y2)	2	–	2	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y1, Y2)	5.5	–	6.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit loadable counter using GRP feedback.
4. **f**max (Toggle) may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[5]	#[2]	DESCRIPTION[1]	-80		-60		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	15	–	20	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	20	–	25	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	80	–	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	50	–	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	100	–	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	7	–	9	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	–	10	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	10	–	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	12	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	17	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10	–	13	–	ns
t_{en}	B	14	Input to Output Enable	–	18	–	24	ns
t_{dis}	C	15	Input to Output Disable	–	18	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	5	–	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	5	–	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y1, Y2)	2	–	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y1, Y2)	6.5	–	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. f_{max} (Toggle) may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-110		-90		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{iobp}	20	I/O Register Bypass	–	0.8	–	1.0	ns
t_{iolat}	21	I/O Latch Delay	–	1.7	–	2.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	4.1	–	4.5	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	1.8	–	2.0	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	1.7	–	2.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	2.1	–	2.5	ns
t_{din}	26	Dedicated Input Delay	–	1.7	–	2.0	ns
GRP							
t_{grp1}	27	GRP Delay, 1 GLB Load	–	0.6	–	0.7	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	0.8	–	1.0	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	1.5	–	1.8	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	2.1	–	2.6	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	2.8	–	3.4	ns
GLB							
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	5.3	–	6.5	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	6.1	–	7.0	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	6.6	–	8.0	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	8.2	–	9.5	ns
t_{gbp}	37	GLB Register Bypass Delay	–	0.5	–	0.5	ns
t_{gsu}	38	GLB Register Setup Time before Clock	0.3	–	1.0	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	2.9	–	3.5	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	1.6	–	1.5	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	2.1	–	2.5	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	8.2	–	10.0	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.0	–	9.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	2.8	6.2	3.5	7.5	ns
ORP							
t_{orp}	45	ORP Delay	–	2.0	–	2.5	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.4	–	0.5	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-110		-90		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	47	Output Buffer Delay	–	2.1	–	2.5	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	3.3	–	4.0	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	3.3	–	4.0	ns
Clocks							
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.9	2.9	3.5	3.5	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.1	3.8	2.5	4.5	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	4.2	1.0	5.0	ns
$t_{ioy1/2}$	53	Clock Delay, Y1 or Y2 to I/O Cell Global Clock Line	2.1	3.8	2.5	4.5	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	4.2	1.0	5.0	ns
Global Reset							
t_{gr}	55	Global Reset to GLB and I/O Registers	–	7.9	–	7.5	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{iobp}	20	I/O Register Bypass	–	2.0	–	2.7	ns
t_{iolat}	21	I/O Latch Delay	–	3.0	–	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	5.5	–	7.3	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	1.0	–	1.3	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	3.0	–	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	2.5	–	3.3	ns
t_{din}	26	Dedicated Input Delay	–	4.0	–	5.3	ns
GRP							
t_{grp1}	27	GRP Delay, 1 GLB Load	–	1.5	–	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	2.0	–	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	3.0	–	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	3.8	–	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	4.5	–	6.0	ns
GLB							
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	6.5	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	7.0	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	8.0	–	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	9.5	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	1.0	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.0	–	1.3	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	4.5	–	6.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	2.0	–	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	2.5	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	10.0	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	9.0	–	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	3.5	7.5	4.6	9.9	ns
ORP							
t_{orp}	45	ORP Delay	–	2.5	–	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.5	–	0.7	ns

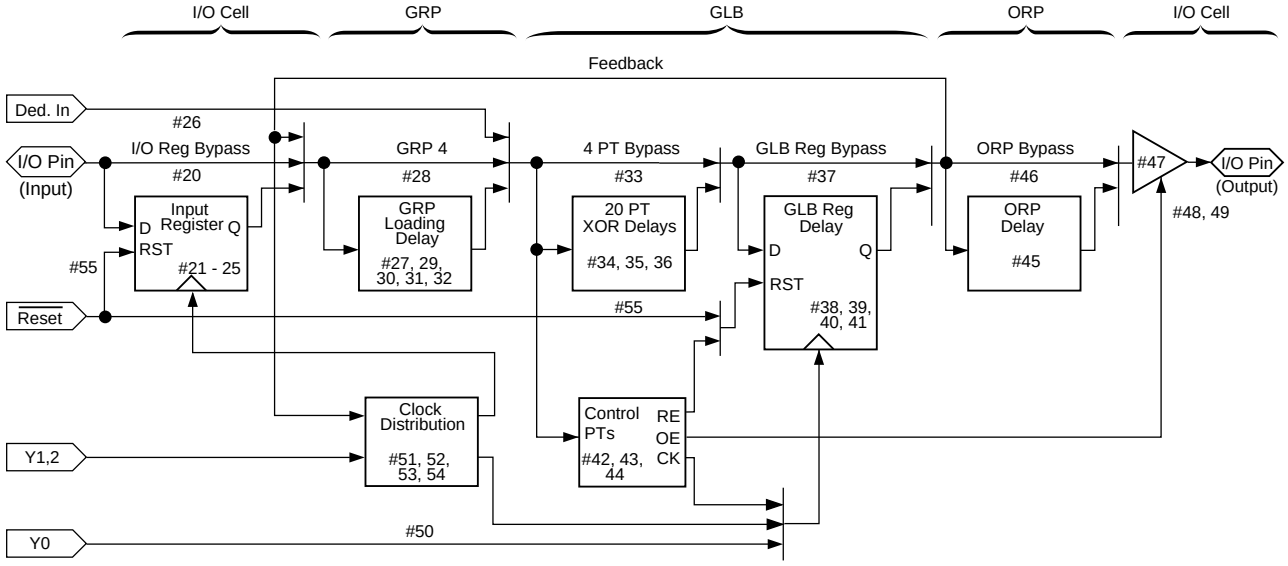
1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	47	Output Buffer Delay	–	3.0	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	5.0	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	5.0	–	6.7	ns
Clocks							
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	4.5	4.5	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	3.5	5.5	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	1.0	5.0	1.3	6.6	ns
$t_{ioy1/2}$	53	Clock Delay, Y1 or Y2 to I/O Cell Global Clock Line	3.5	5.5	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.0	5.0	1.3	6.6	ns
Global Reset							
t_{gr}	55	Global Reset to GLB and I/O Registers	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI and pLSI 1016 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (tiobp + tgrp4 + t20ptxor) + (tgsu) - (tiobp + tgrp4 + tptck(min))
= (#20 + #28 + #35) + (#38) - (#20 + #28 + #44)
5.5 ns = (1.0 + 1.0 + 8.0) + (1.0) - (1.0 + 1.0 + 3.5)

th = Clock (max) + Reg h - Logic
= (tiobp + tgrp4 + tptck(max)) + (tgh) - (tiobp + tgrp4 + t20ptxor)
= (#20 + #28 + #44) + (#39) - (#20 + #28 + #35)
3.0 ns = (1.0 + 1.0 + 7.5) + (3.5) - (1.0 + 1.0 + 8.0)

tco = Clock (max) + Reg co + Output
= (tiobp + tgrp4 + tptck(max)) + (tgco) + (torp + tob)
= (#20 + #28 + #44) + (#40) + (#45 + #47)
16.0 ns = (1.0+ 1.0 +7.5) + (1.5) + (2.5 + 2.5)

Derivations of tsu, th and tco from the Clock GLB[1]

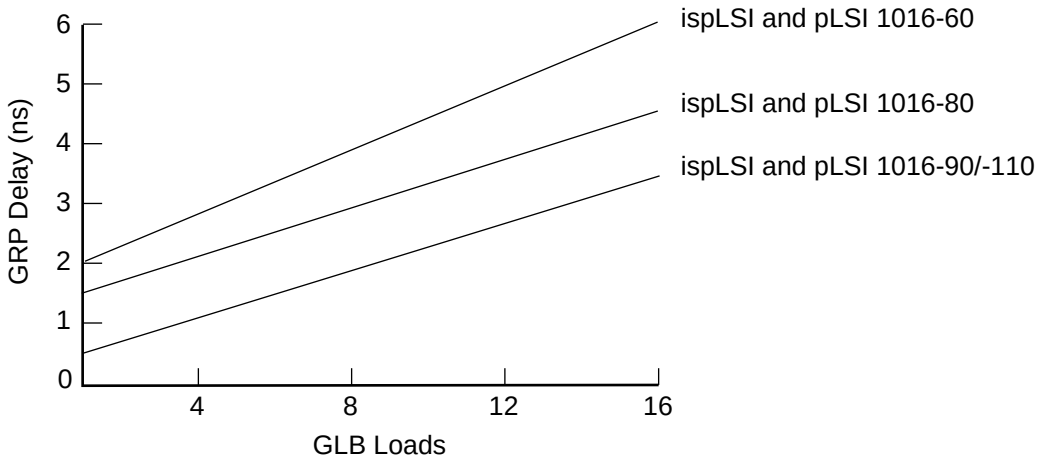
tsu = Logic + Reg su - Clock (min)
= (tiobp + tgrp4 + t20ptxor) + (tgsu) - (tgy0(min) + tgco + tgcp(min))
= (#20 + #28 + #35) + (#38) - (#50 + #40 + #52)
5.0 ns = (1.0 + 1.0 + 8.0) + (1.0) - (3.5 + 1.5 + 1.0)

th = Clock (max) + Reg h - Logic
= (tgy0(max) + tgco + tgcp(max)) + (tgh) - (tiobp + tgrp4 + t20ptxor)
= (#50 + #40 + #52) + (#39) - (#20 + #28 + #35)
3.5 ns = (3.5 + 1.5 + 5.0) + (3.5) - (1.0 + 1.0 + 8.0)

tco = Clock (max) + Reg co + Output
= (tgy0(max) + tgco + tgcp(max)) + (tgco) + (torp + tob)
= (#50 + #40 + #52) + (#40) + (#45 + #47)
16.5 ns = (3.5 + 1.5 + 5.0) + (1.5) + (2.5 + 2.5)

1. Calculations are based upon timing specifications for the ispLSI and pLSI 1016-90.

Maximum GRP Delay vs GLB Loads

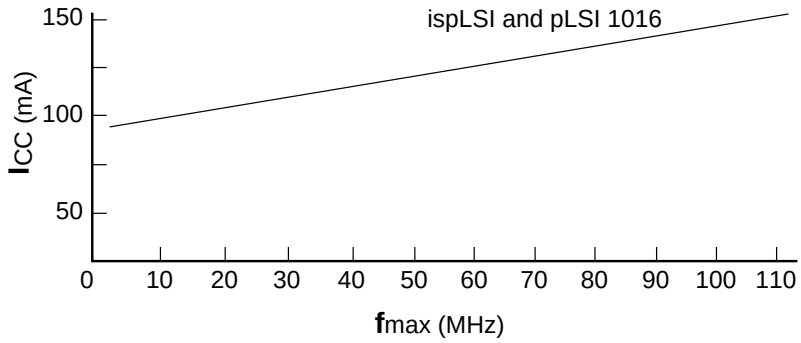


0126A-80-16-isp.eps

Power Consumption

Power consumption in the ispLSI and pLSI 1016 device depends on two primary factors: the speed at which the device is operating, and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of Four 16-bit Counters
Typical Current at 5V, 25°C

I_{CC} can be estimated for the ispLSI and pLSI 1016 using the following equation:

I_{CC} = 31 + (# of PTs * 0.45) + (# of nets * Max. freq * 0.009) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

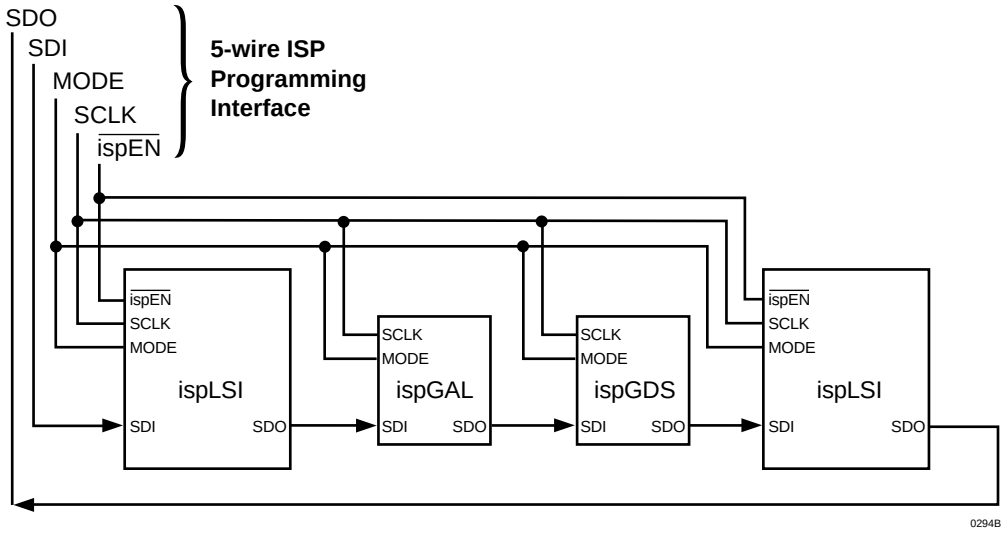
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

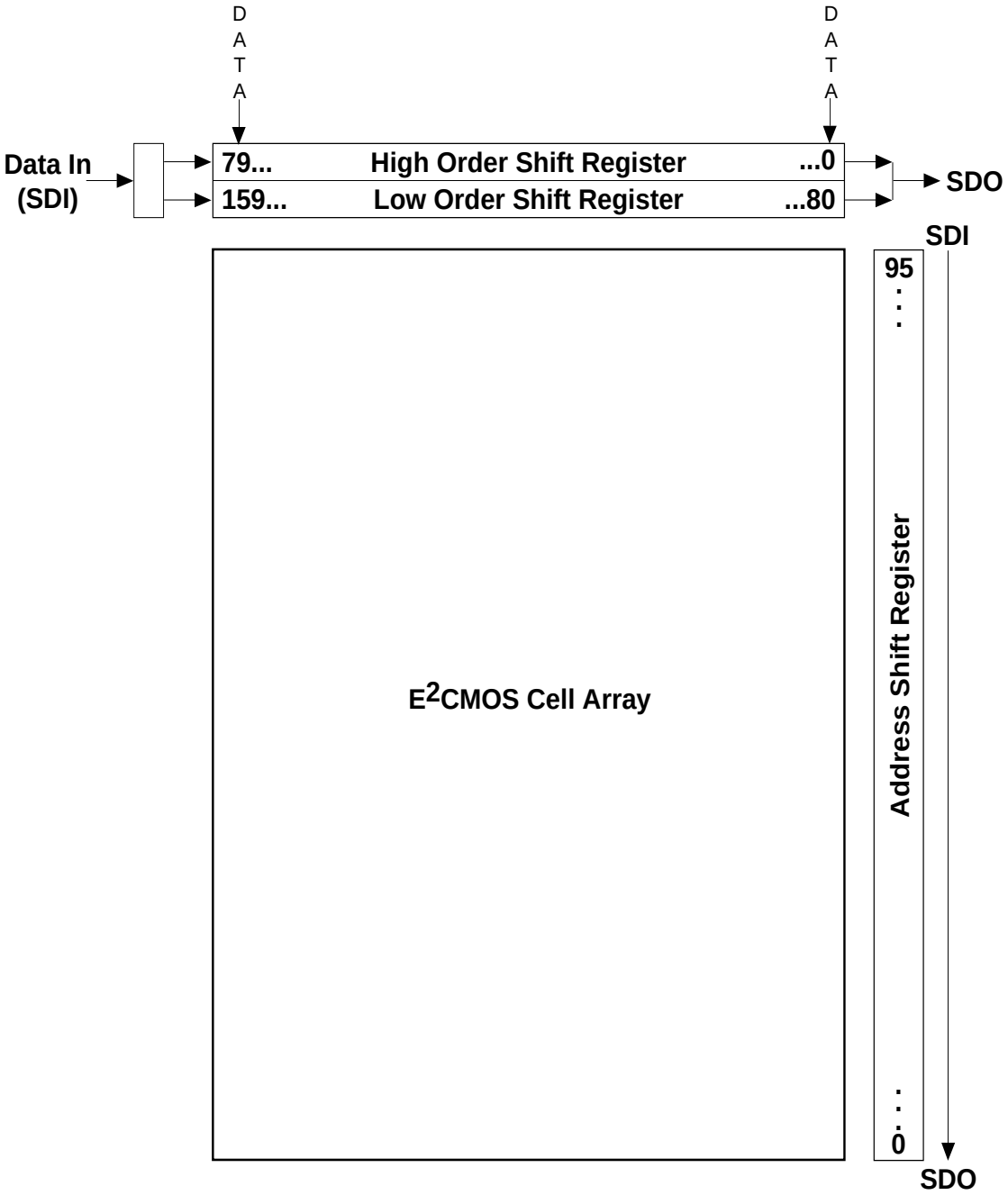
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section in this Data Book.

The device identifier for the ispLSI 1016 is 0000 0001 (01 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 1016 Shift Register Layout



Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

Pin Description

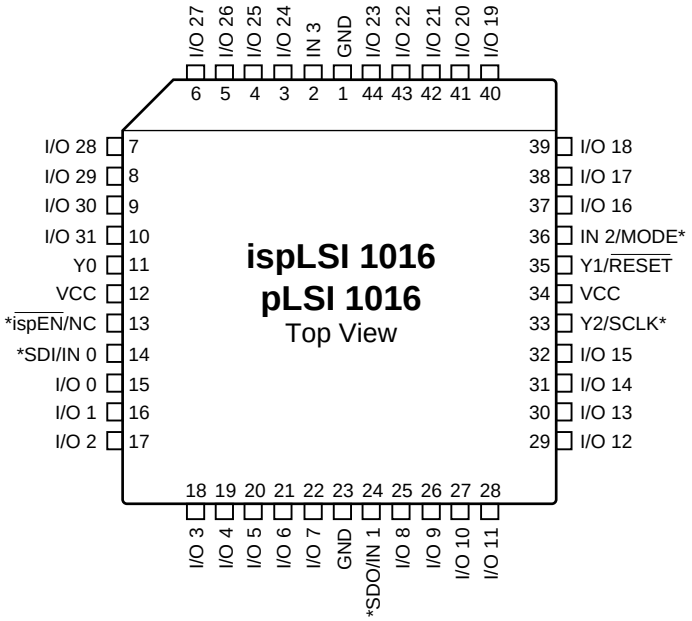
NAME	PLCC PIN NUMBERS	TQFP PIN NUMBERS	JLCC PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	9, 10, 11, 12, 13, 14, 15, 16, 19, 20, 21, 22, 23, 24, 25, 26, 31, 32, 33, 34, 35, 36, 37, 38, 41, 42, 43, 44, 1, 2, 3, 4	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 3	2	40	2	Dedicated input pins to the device.
$\overline{\text{ispEN}}$*/NC	13	7	13	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	14	8	14	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE*/IN 2	36	30	36	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO*/IN 1	24	18	24	Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK*/Y2	33	27	33	Input – This pin performs two functions. It is a dedicated clock input when $\overline{\text{ispEN}}$ is logic high. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
Y0	11	5	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1/$\overline{\text{RESET}}$	35	29	35	This pin performs two functions: – Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. – Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
GND VCC	11, 23 12, 34	7, 39 6, 28	1, 23 12, 34	Ground (GND) V_{CC}

* For ispLSI 1016 Only

Table 2 - 0002C-16-isp

Pin Configuration

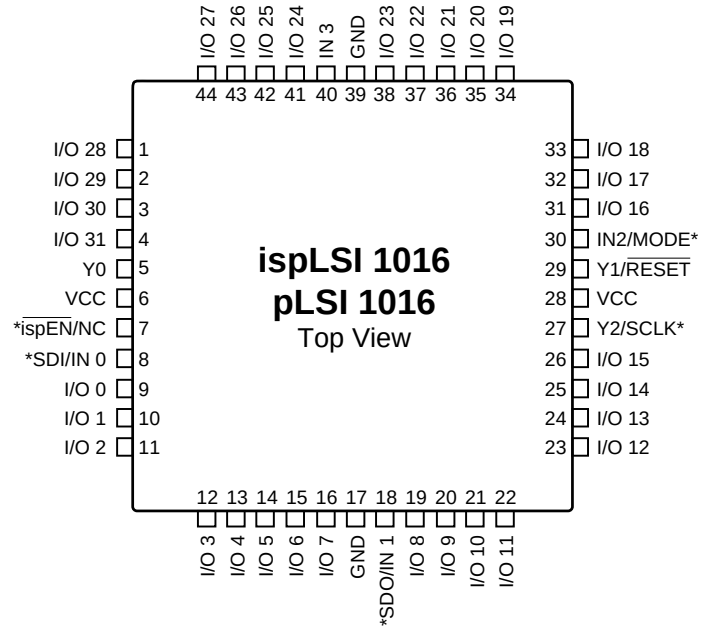
ispLSI and pLSI 1016 44-Pin PLCC Pinout Diagram



* Pins have dual function capability for ispLSI 1016 only (except pin 13, which is $\overline{\text{ispEN}}$ only).

0123A-isp1016

ispLSI and pLSI 1016 44-Pin TQFP Pinout Diagram

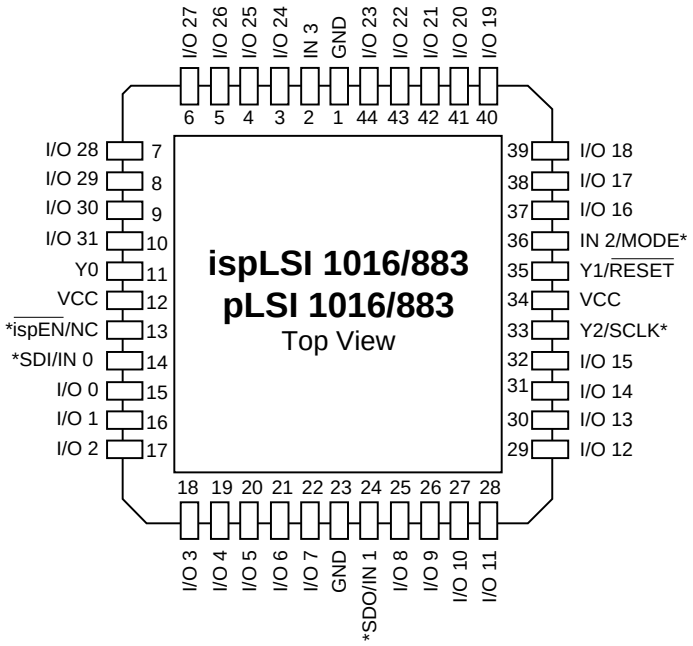


* Pins have dual function capability for ispLSI 1016 only (except pin 7, which is $\overline{\text{ispEN}}$ only).

0851-16/TQFP

Pin Configuration

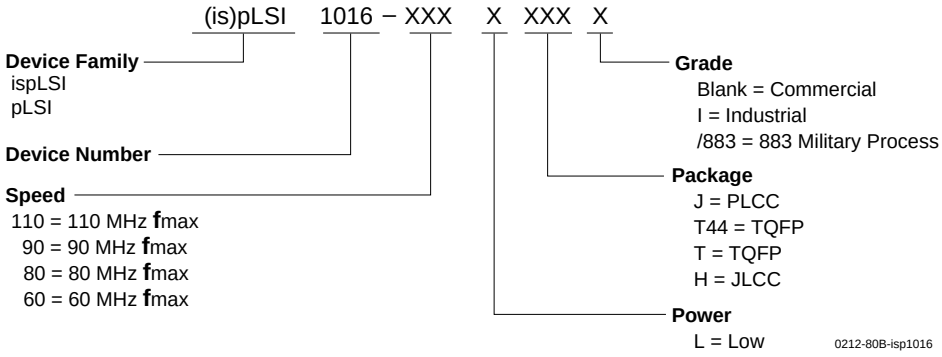
ispLSI and pLSI 1016 44-Pin JLCC Pinout Diagram



* Pins have dual function capability for ispLSI 1016 only (except pin 13, which is $\overline{\text{ispEN}}$ only).

0123-16-isp/JLCC

Part Number Description



ispLSI and pLSI 1016 Ordering Information

COMMERCIAL

Family	fmax (MHz)	tpd (ns)	Ordering Number	Package
ispLSI	110	10	ispLSI 1016-110LJ	44-Pin PLCC
	90	12	ispLSI 1016-90LJ	44-Pin PLCC
	90	12	ispLSI 1016-90LT44	44-Pin TQFP
	90	12	ispLSI 1016-90LT	44-Pin TQFP
	80	15	ispLSI 1016-80LJ	44-Pin PLCC
	80	15	ispLSI 1016-80LT44	44-Pin TQFP
	80	15	ispLSI 1016-80LT	44-Pin TQFP
	60	20	ispLSI 1016-60LJ	44-Pin PLCC
	60	20	ispLSI 1016-60LT44	44-Pin TQFP
	60	20	ispLSI 1016-60LT	44-Pin TQFP
pLSI	110	10	pLSI 1016-110LJ	44-Pin PLCC
	90	12	pLSI 1016-90LJ	44-Pin PLCC
	90	12	pLSI 1016-90LT44	44-Pin TQFP
	90	12	pLSI 1016-90LT	44-Pin TQFP
	80	15	pLSI 1016-80LJ	44-Pin PLCC
	80	15	pLSI 1016-80LT44	44-Pin TQFP
	80	15	pLSI 1016-80LT	44-Pin TQFP
	60	20	pLSI 1016-60LJ	44-Pin PLCC
	60	20	pLSI 1016-60LT44	44-Pin TQFP
	60	20	pLSI 1016-60LT	44-Pin TQFP

INDUSTRIAL

Family	fmax (MHz)	tpd (ns)	Ordering Number	Package
ispLSI	60	20	ispLSI 1016-60LJI	44-Pin PLCC
	60	20	ispLSI 1016-60LT44I	44-Pin TQFP
pLSI	60	20	pLSI 1016-60LJI	44-Pin PLCC

MILITARY/883

Family	fmax (MHz)	tpd (ns)	Ordering Number	SMD #	Package
ispLSI	60	20	ispLSI 1016-60LH/883	5962-9476201MXC	44-Pin JLCC
pLSI	60	20	pLSI 1016-60LH/883	5962-9476301MXC	44-Pin JLCC

Note: Lattice Semiconductor recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number is recommended.

Table 2-0041-16-isp1016

ispLSI® and pLSI® 1024

High-Density Programmable Logic

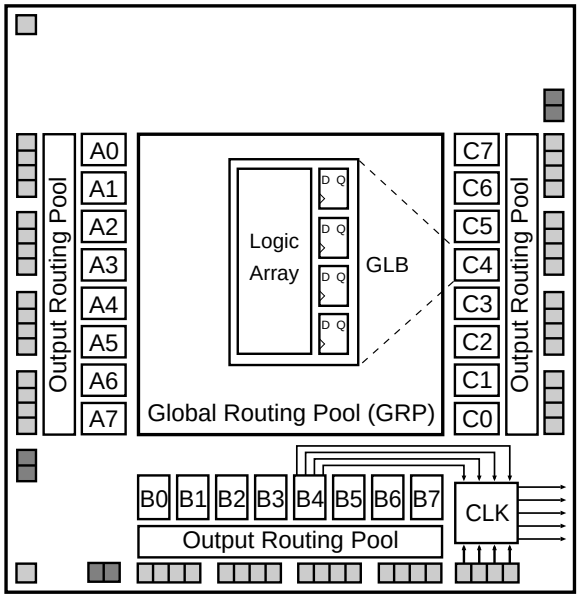
Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— High-Speed Global Interconnect**
  - **— 4000 PLD Gates**
  - **— 48 I/O Pins, Six Dedicated Inputs**
  - **— 144 Registers**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Fast Random Logic**
  - **— Security Cell Prevents Unauthorized Copying**
- **HIGH PERFORMANCE E^2CMOS® TECHNOLOGY**
  - **— f_{max} = 90 MHz Maximum Operating Frequency**
  - **— f_{max} = 60 MHz for Industrial and Military/883 Devices**
  - **— t_{pd} = 12 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile E^2CMOS Technology**
  - **— 100% Tested**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Four Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI AND pLSI DEVELOPMENT TOOLS**

  pDS® Software
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning**
  - **— Automatic Place and Route**
  - **— Static Timing Table**

  pDS+™ Software
  - **— Industry Standard, Third Party Design Environments**
  - **— Schematic Capture, State Machine, HDL**
  - **— Automatic Partitioning and Place and Route**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

Functional Block Diagram



0139-A-isp

Description

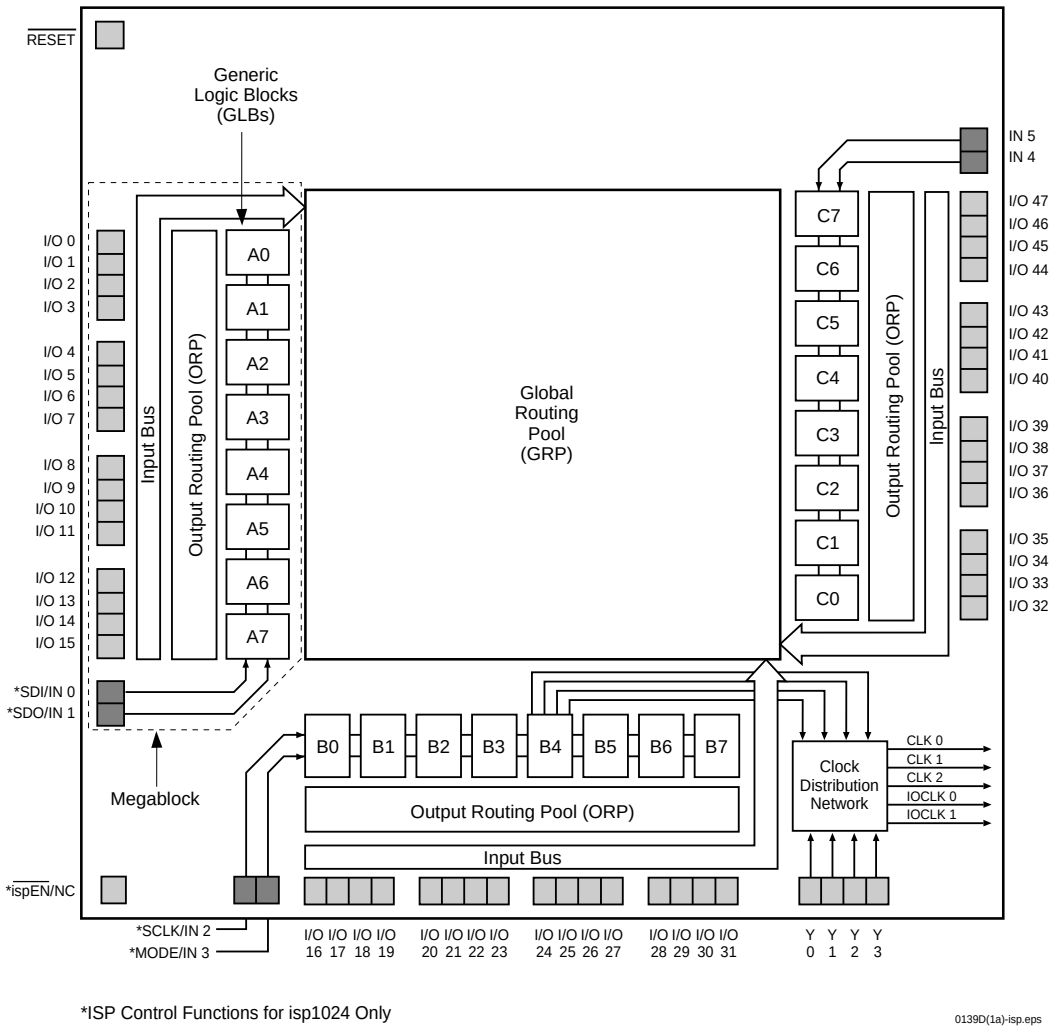
The ispLSI and pLSI 1024 are High-Density Programmable Logic Devices containing 144 Registers, 48 Universal I/O pins, six Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1024 features 5-Volt in-system programmability and in-system diagnostic capabilities. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1024 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the ispLSI and pLSI 1024 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. C7 (see figure 1). There are a total of 24 GLBs in the ispLSI and pLSI 1024 devices. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Functional Block Diagram

Figure 1.ispLSI and pLSI 1024 Functional Block Diagram



*ISP Control Functions for isp1024 Only

0139D(1a)-isp.eps

The devices also have 48 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The I/O cells within the Megablock also share a common Output Enable (OE) signal. The ispLSI and pLSI 1024 devices contain three of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 1024 devices are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (B4 on the ispLSI and pLSI 1024 devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to +70°C	4.75	5.25	V
		Industrial	T_A = -40°C to +85°C	4.5	5.5	
		Military/883	T_C = -55°C to +125°C	4.5	5.5	
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V

Table 2- 0005Aisp w/mil.eps

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER		MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	Commercial/Industrial	8	pf	V_{CC}=5.0V, V_{IN}=2.0V
		Military	10	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance		10	pf	V_{CC}=5.0V, $V_{I/O}$, V_Y=2.0V

1. Guaranteed but not 100% tested.

Table 2- 0006

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2- 0008B

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

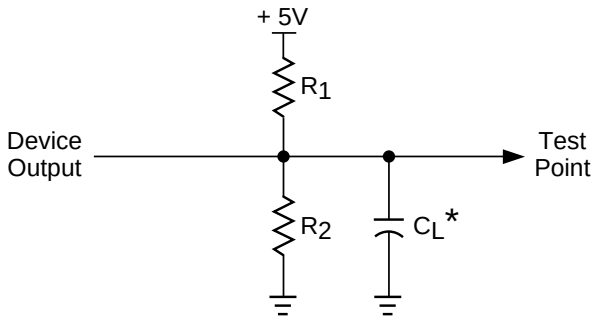
Table 2- 0003

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

Table 2- 0004A

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
I_{IL-isp}	isp Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V	Commercial	–	130	190	mA
		f_{TOGGLE} = 1 MHz	Industrial/Military	–	135	215	mA

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using six 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[5]	#[2]	DESCRIPTION[1]	-90		-80		-60		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	12	–	15	–	20	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	17	–	20	–	25	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	90.9	–	80	–	60	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	58.8	–	50	–	38	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	125	–	100	–	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	6	–	7	–	9	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	–	8	–	10	–	13	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	9	–	10	–	13	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	10	–	12	–	16	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	15	–	17	–	22.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10	–	10	–	13	–	ns
t_{en}	B	14	Input to Output Enable	–	15	–	18	–	24	ns
t_{dis}	C	15	Input to Output Disable	–	15	–	18	–	24	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	4	–	5	–	6	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	4	–	5	–	6	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	–	2	–	2.5	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	–	6.5	–	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit loadable counter using GRP feedback.
4. **f**max (Toggle) may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t_{iobp}	20	I/O Register Bypass	–	1.6	–	2.0	–	2.7	ns
t_{iolat}	21	I/O Latch Delay	–	2.4	–	3.0	–	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	4.8	–	5.5	–	7.3	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	2.1	–	1.0	–	1.3	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	2.4	–	3.0	–	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	2.8	–	2.5	–	3.3	ns
t_{din}	26	Dedicated Input Delay	–	3.2	–	4.0	–	5.3	ns
GRP									
t_{grp1}	27	GRP Delay, 1 GLB Load	–	1.2	–	1.5	–	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	1.6	–	2.0	–	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	2.4	–	3.0	–	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	3.0	–	3.8	–	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	3.6	–	4.5	–	6.0	ns
t_{grp24}	32	GRP Delay, 24 GLB Loads	–	5.0	–	6.3	–	8.3	ns
GLB									
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	5.2	–	6.5	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	5.7	–	7.0	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	7.0	–	8.0	–	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	8.2	–	9.5	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	0.8	–	1.0	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.2	–	1.0	–	1.3	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	3.6	–	4.5	–	6.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	1.6	–	2.0	–	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	2.0	–	2.5	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	8.0	–	10.0	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	7.8	–	9.0	–	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	2.8	6.0	3.5	7.5	4.6	9.9	ns
ORP									
t_{orp}	45	ORP Delay	–	2.4	–	2.5	–	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.4	–	0.5	–	0.7	ns

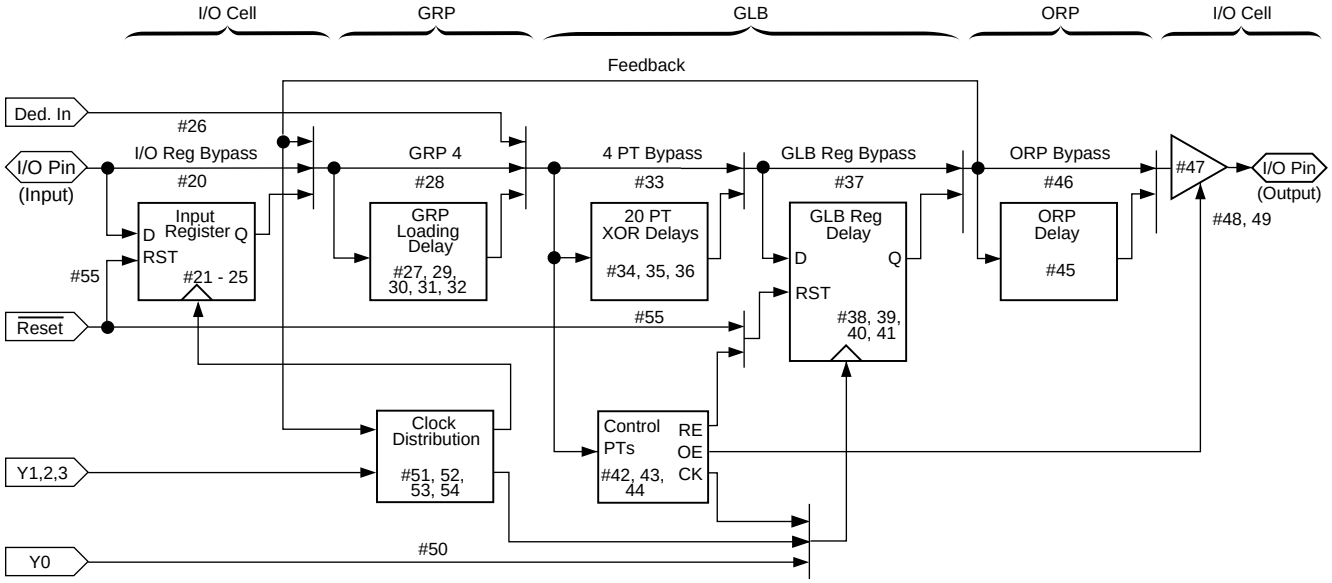
1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Hard Macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
t_{ob}	47	Output Buffer Delay	–	2.4	–	3.0	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	4.0	–	5.0	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	4.0	–	5.0	–	6.7	ns
Clocks									
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	3.6	3.6	4.5	4.5	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.8	4.4	3.5	5.5	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	4.0	1.0	5.0	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	2.8	4.4	3.5	5.5	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	4.0	1.0	5.0	1.3	6.6	ns
Global Reset									
t_{gr}	55	Global Reset to GLB and I/O Registers	–	8.2	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI and pLSI 1024 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (tiobp + tgrp4 + t20ptxor) + (tgsu) - (tiobp + tgrp4 + tptck(min))
= (#20 + #28 + #35) + (#38) - (#20 + #28 + #44)
5.5 ns = (2.0 + 2.0 + 8.0) + (1.0) - (2.0 + 2.0 + 3.5)

th = Clock (max) + Reg h - Logic
= (tiobp + tgrp4 + tptck(max)) + (tgh) - (tiobp + tgrp4 + t20ptxor)
= (#20 + #28 + #44) + (#39) - (#20 + #28 + #35)
4.0 ns = (2.0 + 2.0 + 7.5) + (4.5) - (2.0 + 2.0 + 8.0)

tco = Clock (max) + Reg co + Output
= (tiobp + tgrp4 + tptck(max)) + (tgco) + (torp + tob)
= (#20 + #28 + #44) + (#40) + (#45 + #47)
19.0 ns = (2.0+ 2.0 +7.5) + (2.0) + (2.5 + 3.0)

Derivations of tsu, th and tco from the Clock GLB[1]

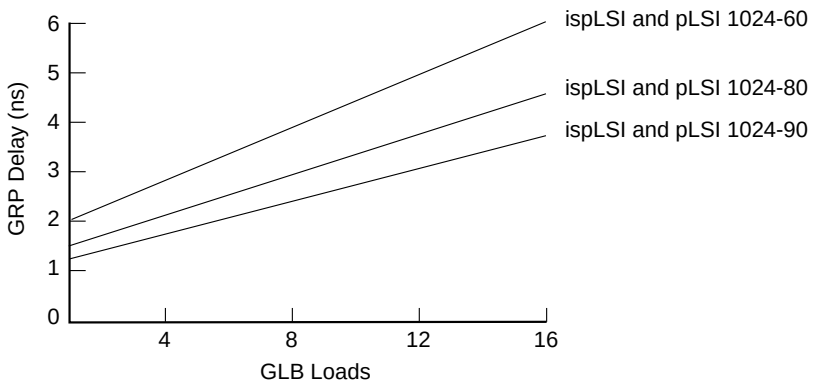
tsu = Logic + Reg su - Clock (min)
= (tiobp + tgrp4 + t20ptxor) + (tgsu) - (tgy0(min) + tgco + tgcp(min))
= (#20 + #28 + #35) + (#38) - (#50 + #40 + #52)
5.5 ns = (2.0 + 2.0 + 8.0) + (1.0) - (4.5 + 2.0 + 1.0)

th = Clock (max) + Reg h - Logic
= (tgy0(max) + tgco + tgcp(max)) + (tgh) - (tiobp + tgrp4 + t20ptxor)
= (#50 + #40 + #52) + (#39) - (#20 + #28 + #35)
4.0 ns = (4.5 + 2.0 + 5.0) + (4.5) - (2.0 + 2.0 + 8.0)

tco = Clock (max) + Reg co + Output
= (tgy0(max) + tgco + tgcp(max)) + (tgco) + (torp + tob)
= (#50 + #40 + #52) + (#40) + (#45 + #47)
19.0 ns = (4.5 + 2.0 + 5.0) + (2.0) + (2.5 + 3.0)

1. Calculations are based upon timing specifications for the ispLSI and pLSI 1024-80.

Maximum GRP Delay vs GLB Loads



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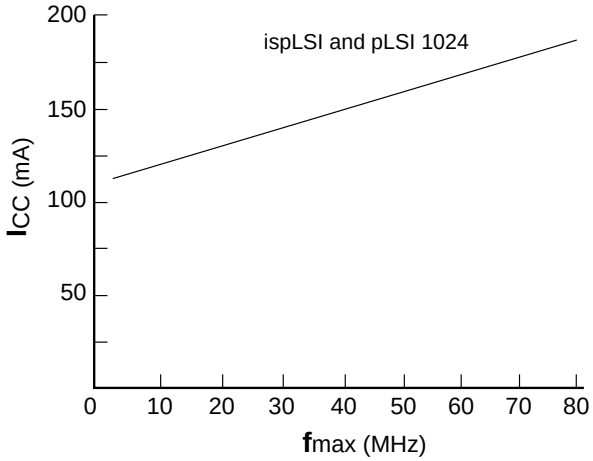
Power Consumption

Power consumption in the ispLSI and pLSI 1024 device depends on two primary factors: the speed at which the device is operating, and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of Six 16-bit Counters
Typical Current at 5V, 25˚C

I_{CC} can be estimated for the ispLSI and pLSI 1024 using the following equation:

I_{CC} = 42 + (# of PTs * 0.45) + (# of nets * Max. freq * 0.008) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A-24-80-isp

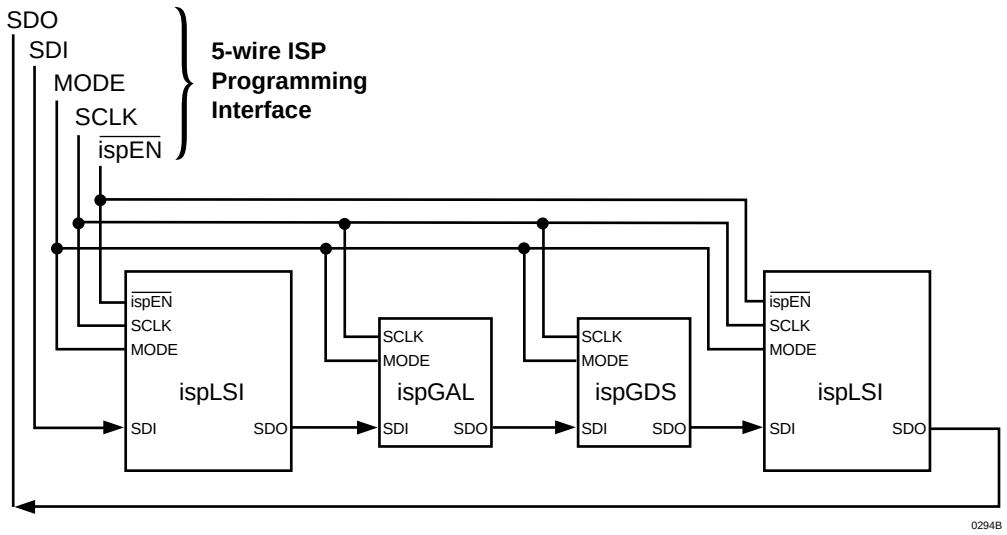
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

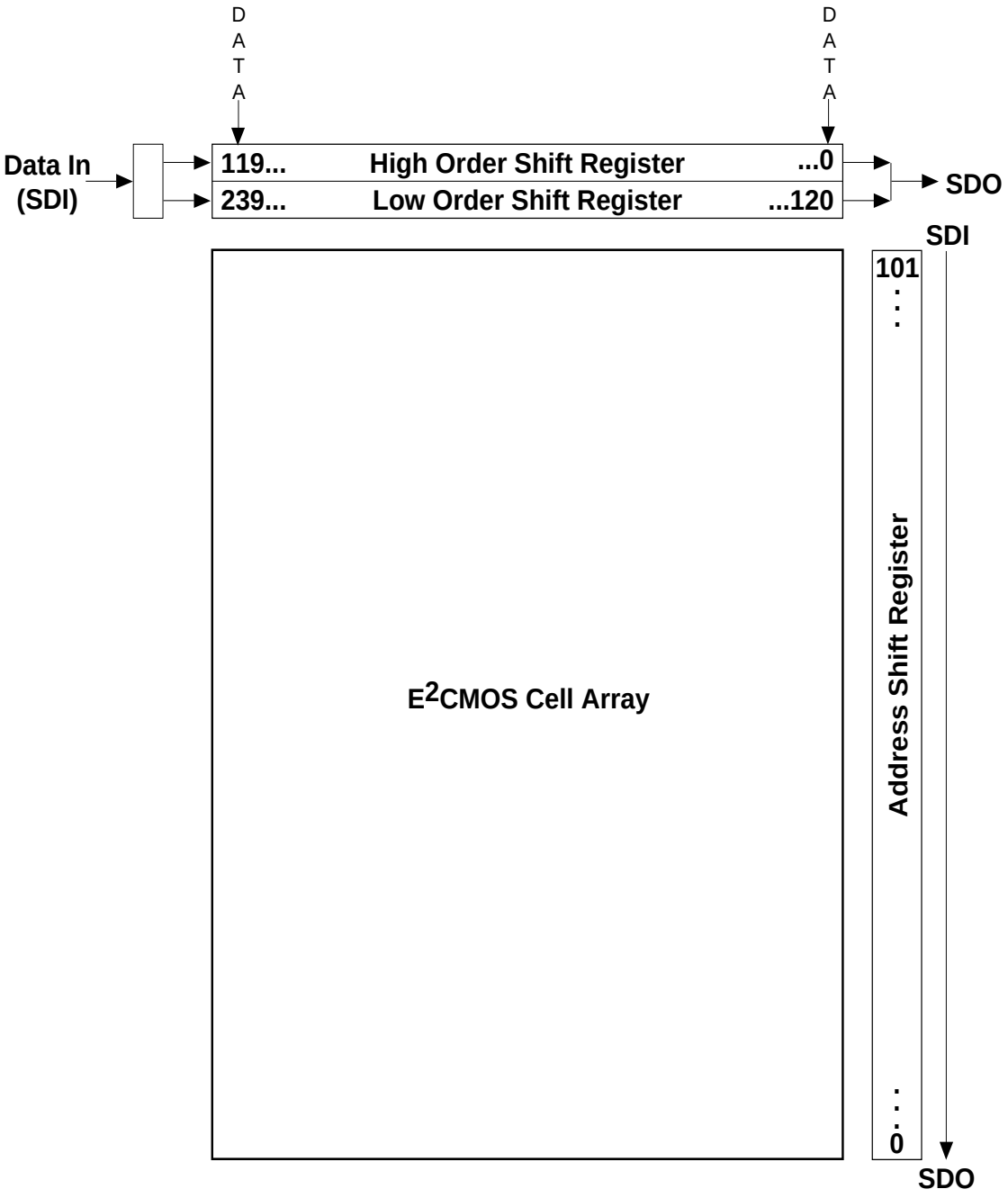
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section in this Data Book.

The device identifier for the ispLSI 1024 is 0000 0010 (02 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 1024 Shift Register Layout



Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

Pin Description

NAME	PLCC and JLCC PIN NUMBERS	TQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47	22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14	19, 20, 21, 22, 23, 28, 29, 30, 31, 32, 33, 34, 42, 43, 44, 45, 46, 47, 48, 53, 54, 55, 56, 57, 69, 70, 71, 72, 73, 78, 79, 80, 81, 82, 83, 84, 92, 93, 94, 95, 96, 97, 98, 3, 4, 5, 6, 7	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 5	2, 15	91, 8	Input - These pins are dedicated input pins to the device.
$\overline{\text{ispEN}}$*/NC	19	16	Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	21	18	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 is also used as one of the two control pins for the isp state machine. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high.
MODE*/IN 3	55	68	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high.
SDO*/IN 1	34	35	Output/Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high.
SCLK*/IN 2	49	58	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high.
$\overline{\text{RESET}}$	20	17	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	16	9	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	54	67	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	51	60	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	50	59	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	1, 18, 35, 52	14, 15, 36, 37, 61, 62, 89, 90	Ground (GND)
VCC	17, 36, 53, 68	10, 11, 40, 41, 65, 66, 85, 86	V_{CC}

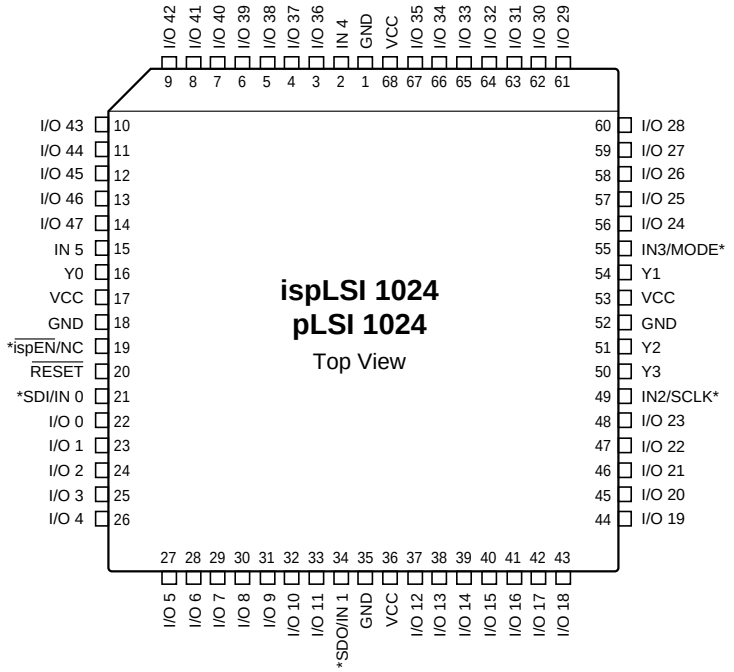
Table 2 - 0002C-24

* ispLSI 1024E only

CC

Pin Configuration

ispLSI and pLSI 1024 68-Pin PLCC Pinout Diagram



* Pins have dual function capability for ispLSI 1024 only (except pin 19, which is $\overline{\text{ispEN}}$ only).

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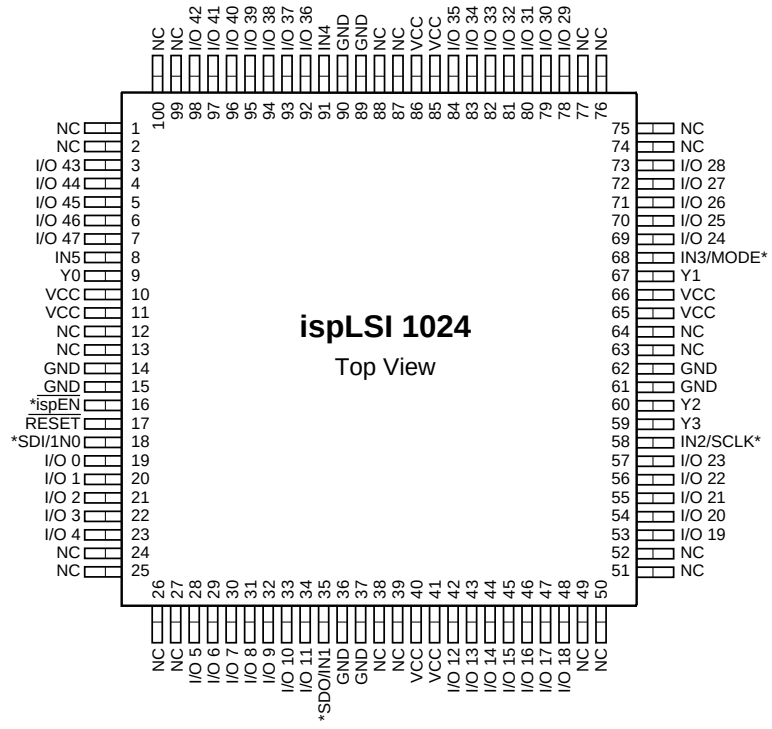
ispLSI 1024 100-Pin TQFP Pinout Diagram



*Pins have dual function

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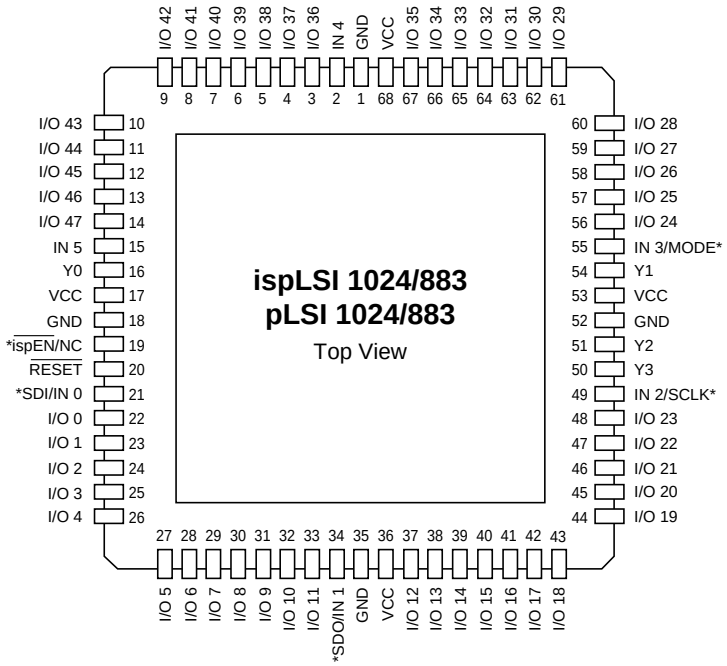
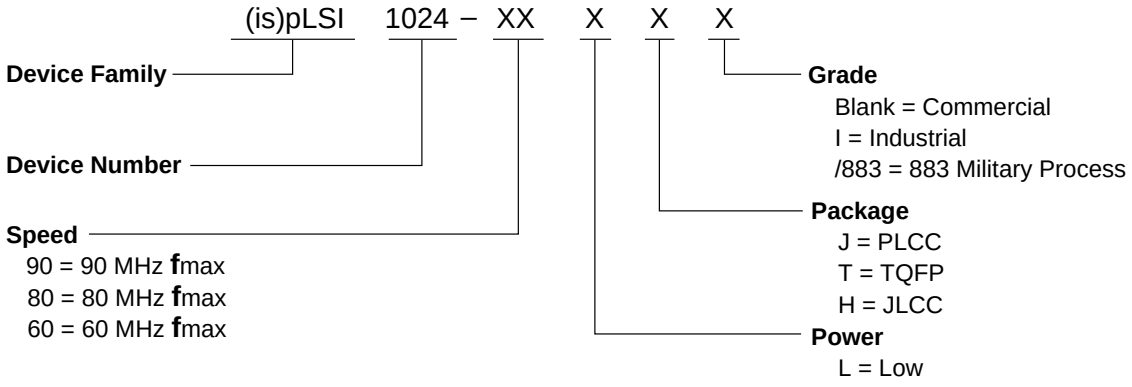
ispLSI and pLSI 1024 68-Pin JLCC Pinout Diagram



* Pins have dual function capability for ispLSI 1024 only (except pin 19, which is $\overline{\text{ispEN}}$ only).

0123-24-isp/JLCC

Part Number Description



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ispLSI and pLSI 1024 Ordering Information

COMMERCIAL

Family	fmax (MHz)	tpd (ns)	Ordering Number	Package
ispLSI	90	12	ispLSI 1024-90LJ	68-Pin PLCC
	90	12	ispLSI 1024-90LT	100-Pin TQFP
	80	15	ispLSI 1024-80LJ	68-Pin PLCC
	80	15	ispLSI 1024-80LT	100-Pin TQFP
	60	20	ispLSI 1024-60LJ	68-Pin PLCC
	60	20	ispLSI 1024-60LT	100-Pin TQFP
pLSI	90	12	pLSI 1024-90LJ	68-Pin PLCC
	80	15	pLSI 1024-80LJ	68-Pin PLCC
	60	20	pLSI 1024-60LJ	68-Pin PLCC

INDUSTRIAL

Family	fmax (MHz)	tpd (ns)	Ordering Number	Package
ispLSI	60	20	ispLSI 1024-60LJI	68-Pin PLCC
	60	20	ispLSI 1024-60LTI	100-Pin TQFP
pLSI	60	20	pLSI 1024-60LJI	68-Pin PLCC

MILITARY/883

Family	fmax (MHz)	tpd (ns)	Ordering Number	SMD #	Package
ispLSI	60	20	ispLSI 1024-60LH/883	5962-9476101MXC	68-Pin JLCC
pLSI	60	20	pLSI 1024-60LH/883	5962-9476001MXC	68-Pin JLCC

Note: Lattice Semiconductor recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number is recommended.

Table 2-0041A-24-isp

ispLSI® and pLSI® 1032E

High-Density Programmable Logic

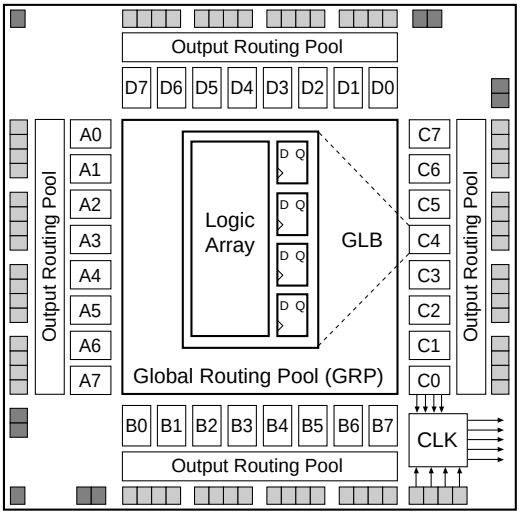
Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **— 6000 PLD Gates**
  - **— 64 I/O Pins, Eight Dedicated Inputs**
  - **— 192 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E^2CMOS® TECHNOLOGY**
  - **— f_{max} = 125 MHz Maximum Operating Frequency**
  - **— t_{pd} = 7.5 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Enhanced Pin Locking Capability**
  - **— Four Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI/pLSI DEVELOPMENT TOOLS**

  pDS® Software
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning**
  - **— Automatic Place and Route**
  - **— Static Timing Table**

  pDS+™ Software
  - **— Industry Standard, Third Party Design Environments**
  - **— Schematic Capture, State Machine, HDL**
  - **— Automatic Partitioning and Place and Route**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

Functional Block Diagram



Description

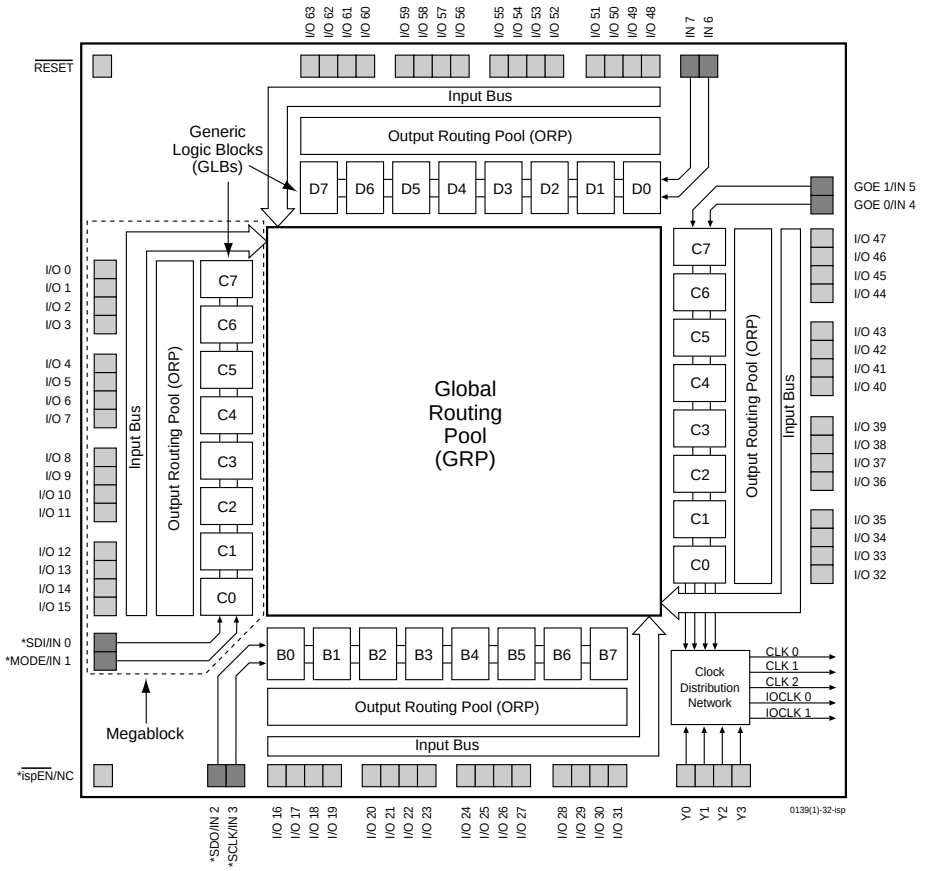
The ispLSI and pLSI 1032E are High Density Programmable Logic Devices containing 192 Registers, 64 Universal I/O pins, eight Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1032E features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 1032E device offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnects to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1032E device, but multiplexes four input pins to control in-system programming. A functional superset of the ispLSI and pLSI 1032 architecture, the ispLSI and pLSI 1032E devices add two new global output enable pins.

The basic unit of logic on the ispLSI and pLSI 1032E devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1…D7 (see figure 1). There are a total of 32 GLBs in the ispLSI and pLSI 1032E devices. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.lattice.com

Functional Block Diagram

Figure 1. ispLSI and pLSI 1032E Functional Block Diagram



*ISP Control Functions for ispLSI 1032E Only

The devices also have 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each ispLSI and pLSI 1032E device contains four Megablocks.

The GRP has, as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 1032E devices are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (C0 on the ispLSI and pLSI 1032E devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2-0005/2000

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input, I/O, Y1, Y2, Y3, Clock Capacitance	8	pf	V_{CC} = 5.0V, V_{PIN} = 2.0V
C_2	Y0 Clock Capacitance	15	pf	V_{CC} = 5.0V, V_{PIN} = 2.0V

1. Guaranteed, but not 100% tested.

Table 2 - 0006a

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2-0008A-isp

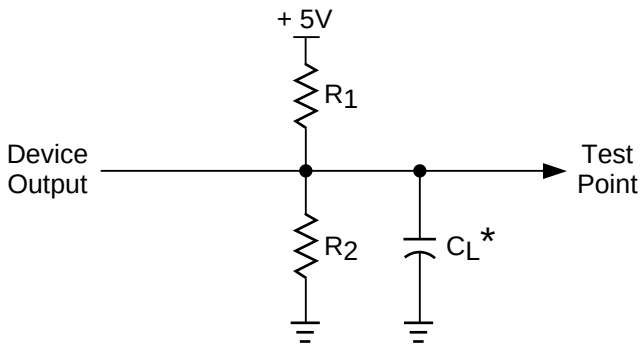
Switching Test Conditions

Input Pulse Levels	GND to 3.0V	
Input Rise and Fall Time 10% to 90%	-125	≤ 2 ns
	Others	≤ 3 ns
Input Timing Reference Levels	1.5V	
Ouput Timing Reference Levels	1.5V	
Output Load	See figure 2	

Table 2a-0003

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213a

Output Load Conditions (see figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2-0004a

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
$I_{IL\text{-}isp}$	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V, f_{CLOCK} = 1 MHz	–	190	–	mA

Table 2-0007b-32-isp

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using eight 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the 1996 Lattice Semiconductor Data Book to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAM.	TEST[4] COND.	#[2]	DESCRIPTION[1]	-125		-90		-80		-70		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd1	A	1	Data Propogation Delay, 4PT Bypass, ORP Bypass	–	7.5	–	10	–	12	–	15	ns
tpd2	A	2	Data Propagation Delay	–	10	–	12.5	–	15	–	17.5	ns
fmax (Int.)	A	3	Clock Frequency with Internal Feedback[3]	125	–	90	–	80	–	70	–	MHz
fmax (Ext.)	—	4	Clock Frequency with External Feedback, 1/(tsu2 + tco1)	91	–	69	–	61	–	56	–	MHz
fmax (Tog.)	—	5	Clock Frequency, Max Toggle[4]	167	–	125	–	111	–	100	–	MHz
tsu1	—	6	GLB Register Setup Time before Clock, 4PT Bypass	5	–	7.5	–	8.5	–	9	–	ns
tco1	A	7	GLB Register Clock to Output Delay, ORP Bypass	–	5	–	6	–	6.5	–	7	ns
th1	—	8	GLB Register Hold Time after Clock, 4PT Bypass	0	–	0	–	0	–	0	–	ns
tsu2	—	9	GLB Register Setup Time before Clock	6	–	8.5	–	10	–	11	–	ns
tco2	—	10	GLB Register Clock to Output Delay	–	6	–	7	–	7.5	–	8	ns
th2	—	11	GLB Register Hold Time after Clock	0	–	0	–	0	–	0	–	ns
tr1	A	12	External Reset Pin to Output Delay	–	10	–	13.5	–	14	–	15	ns
trw1	—	13	External Reset Pulse Duration	5	–	6.5	–	8	–	10	–	ns
tptoeen	B	14	Product Term OE, Enable	–	12	–	15	–	16.5	–	18	ns
tptoedis	C	15	Product Term OE, Disable	–	12	–	15	–	16.5	–	18	ns
tgoeen	B	16	Global OE, Enable	–	7	–	9	–	10	–	12	ns
tgoedis	C	17	Global OE, Disable	–	7	–	9	–	10	–	12	ns
twh	—	18	External Sync. Clock Pulse Duration, High	3	–	4	–	4.5	–	5	–	ns
twl	—	19	External Sync. Clock Pulse Duration, Low	3	–	4	–	4.5	–	5	–	ns
tsu3	—	20	I/O Register Setup Time before External Synchronous Clock (Y2, Y3)	3	–	3.5	–	3.5	–	4	–	ns
th3	—	21	I/O Register Hold Time after External Synchronous Clock (Y3, Y4)	0	–	0	–	0	–	0	–	ns

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 Clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Timing Ext.2/1032E.eps

Internal Timing Parameters[1]

PARAM.	# [2]	DESCRIPTION	-125		-90		-80		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs											
t_{iobp}	22	I/O Register Bypass	–	0.3	–	0.3	–	0.3	–	0.3	ns
t_{iolat}	23	I/O Latch Delay	–	1.9	–	2.3	–	2.7	–	3.3	ns
t_{iosu}	24	I/O Register Setup Time before Clock	3.0	–	3.5	–	3.5	–	4.0	–	ns
t_{ioh}	25	I/O Register Hold Time after Clock	0.0	–	0.0	–	0.0	–	0.0	–	ns
t_{ioco}	26	I/O Register Clock to Out Delay	–	4.6	–	5.0	–	5.4	–	6.1	ns
t_{ior}	27	I/O Register Reset to Out Delay	–	4.6	–	5.0	–	5.4	–	6.0	ns
t_{din}	28	Dedicated Input Delay	–	2.3	–	2.6	–	2.8	–	2.8	ns
GRP											
t_{grp1}	29	GRP Delay, 1 GLB Load	–	1.8	–	2.1	–	2.2	–	2.5	ns
t_{grp4}	30	GRP Delay, 4 GLB Loads	–	2.0	–	2.3	–	2.5	–	2.5	ns
t_{grp8}	31	GRP Delay, 8 GLB Loads	–	2.3	–	2.6	–	2.8	–	3.2	ns
t_{grp16}	32	GRP Delay, 16 GLB Loads	–	2.8	–	3.2	–	3.5	–	4.0	ns
t_{grp32}	33	GRP Delay, 32 GLB Loads	–	3.8	–	4.4	–	4.8	–	5.6	ns
GLB											
t_{4ptbpc}	34	4 Prod.Term Bypass Path Delay (Combinatorial)	–	3.9	–	5.7	–	7.1	–	8.8	ns
t_{4ptbpr}	35	4 Prod. Term Bypass Path Delay (Registered)	–	4.0	–	6.1	–	6.7	–	7.2	ns
t_{1ptxor}	36	1 Prod.Term/XOR Path Delay	–	3.6	–	5.6	–	6.6	–	8.3	ns
$t_{20ptxor}$	37	20 Prod. Term/XOR Path Delay	–	5.0	–	6.8	–	7.8	–	8.7	ns
t_{xoradj}	38	XOR Adjacent Path Delay [3]	–	5.0	–	7.1	–	8.2	–	9.2	ns
t_{gbp}	39	GLB Register Bypass Delay	–	0.4	–	0.4	–	1.3	–	1.6	ns
t_{gsu}	40	GLB Register Setup Time before Clock	0.1	–	0.2	–	0.5	–	0.5	–	ns
t_{gh}	41	GLB Register Hold Time after Clock	4.5	–	6.8	–	7.9	–	8.8	–	ns
t_{gco}	42	GLB Register Clock to Output Delay	–	2.3	–	2.9	–	2.9	–	2.9	ns
t_{gro}	43	GLB Register Reset to Output Delay	–	4.9	–	6.3	–	6.4	–	6.8	ns
t_{ptre}	44	GLB Prod.Term Reset to Register Delay	–	3.9	–	5.1	–	5.5	–	5.8	ns
t_{ptoe}	45	GLB Prod. Term Output Enable to I/O Cell Delay	–	5.4	–	7.1	–	8.0	–	9.0	ns
t_{ptck}	46	GLB Prod. Term Clock Delay	2.9	4.0	4.1	5.3	4.5	5.8	4.8	6.2	ns
ORP											
t_{orp}	47	ORP Delay	–	1.0	–	1.0	–	1.0	–	1.0	ns
t_{orpbp}	48	ORP Bypass Delay	–	0.0	–	0.0	–	0.0	–	0.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Table 2-0036-32A/100

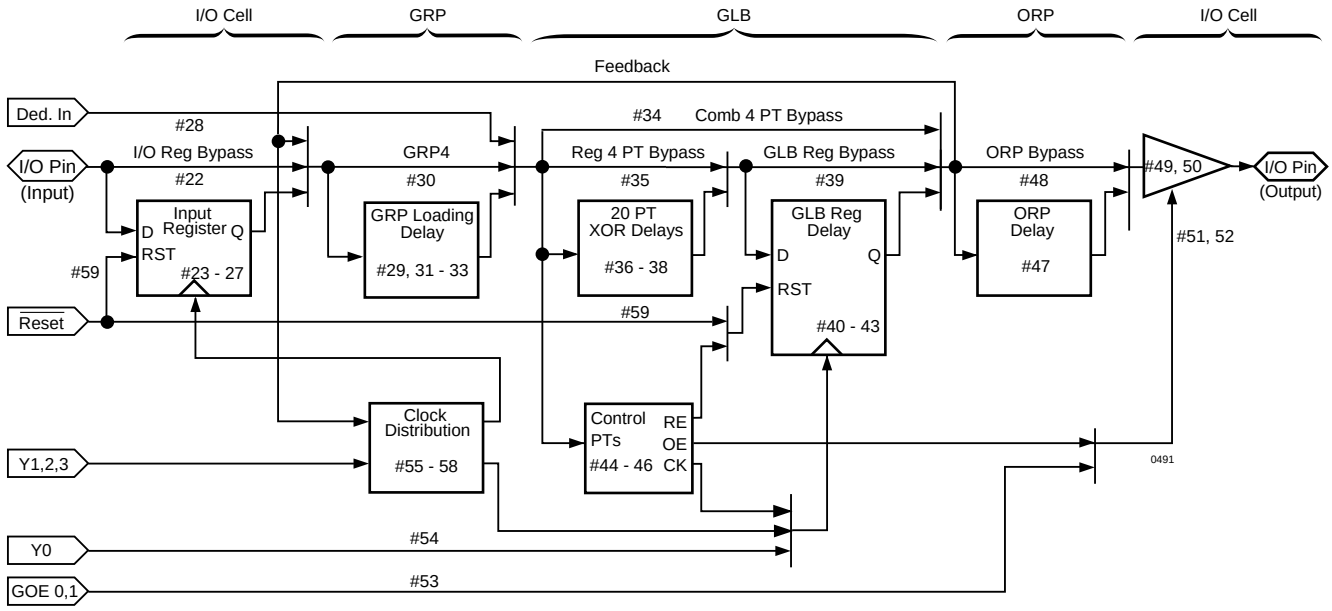
Internal Timing Parameters[1]

PARAM.	#	DESCRIPTION	-125		-90		-80		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs											
t_{ob}	49	Output Buffer Delay	–	1.3	–	1.7	–	2.1	–	2.6	ns
t_{sl}	50	Output Buffer Delay, Slew Limited Adder	–	9.9	–	10.0	–	10.0	–	10.0	ns
t_{oen}	51	I/O Cell OE to Output Enabled	–	4.3	–	5.3	–	5.7	–	6.2	ns
t_{odis}	52	I/O Cell OE to Output Disabled	–	4.3	–	5.3	–	5.7	–	6.2	ns
t_{goe}	53	Global OE	–	2.7	–	3.7	–	4.3	–	5.8	ns
Clocks											
t_{gy0}	54	Clk Delay, Y0 to Global GLB Clk Line (Ref. clk)	1.4	1.4	1.4	1.4	1.5	1.5	1.5	1.5	ns
$t_{gy1/2}$	55	Clk Delay, Y1 or Y2 to Global GLB Clk Line	2.2	2.7	2.4	2.9	2.6	3.1	3.0	3.5	ns
t_{gcp}	56	Clk Delay, Clock GLB to Global GLB Clk Line	0.8	1.8	0.8	1.8	0.8	1.8	0.8	1.8	ns
$t_{ioy2/3}$	57	Clk Delay, Y2 or Y3 to I/O Cell Global Clk Line	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	ns
t_{iocp}	58	Clk Delay, Clk GLB to I/O Cell Global Clk Line	0.8	1.8	0.8	1.8	0.8	1.8	0.8	1.8	ns
Global Reset											
t_{gr}	59	Global Reset to GLB and I/O Registers	–	2.8	–	4.5	–	4.5	–	4.6	ns

1. Internal Timing Parameters are not tested and are for reference only.

Table 2-0037A-32/100

ispLSI and pLSI 1032E Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (**t**iobp + **t**grp4 + **t**20ptxor) + (**t**gsu) – (**t**iobp + **t**grp4 + **t**ptck(min))
= (#22 + #30 + #37) + (#40) – (#22 + #30 + #46)
2.2 ns = (0.3 + 2.0 + 5.0) + (0.1) – (0.3 + 2.0 + 2.9)

th = Clock (max) + Reg h - Logic
= (**t**iobp + **t**grp4 + **t**ptck(max)) + (**t**gh) – (**t**iobp + **t**grp4 + **t**20ptxor)
= (#22 + #30 + #46) + (#41) - (#22 + #30 + #37)
3.5 ns = (0.3 + 2.0 + 4.0) + (4.5) – (0.3 + 2.0 + 5.0)

tco = Clock (max) + Reg co + Output
= (**t**iobp + **t**grp4 + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#22 + #30 + #46) + (#42) + (#47 + #49)
6.3 ns = (0.3 + 2.0 + 4.0) + (2.3) + (1.0 + 1.3)

Derivations of tsu, th and tco from the Clock GLB [1]

tsu = Logic + Reg su - Clock (min)
= (**t**iobp + **t**grp4 + **t**20ptxor) + (**t**gsu) – (**t**gy0(min) + **t**gco + **t**gcp(min))
= (#22 + #30 + #37) + (#40) – (#54 + #42 + #56)
2.9 ns = (0.3 + 2.0 + 5.0) + (0.1) – (1.4 + 2.3 + 0.8)

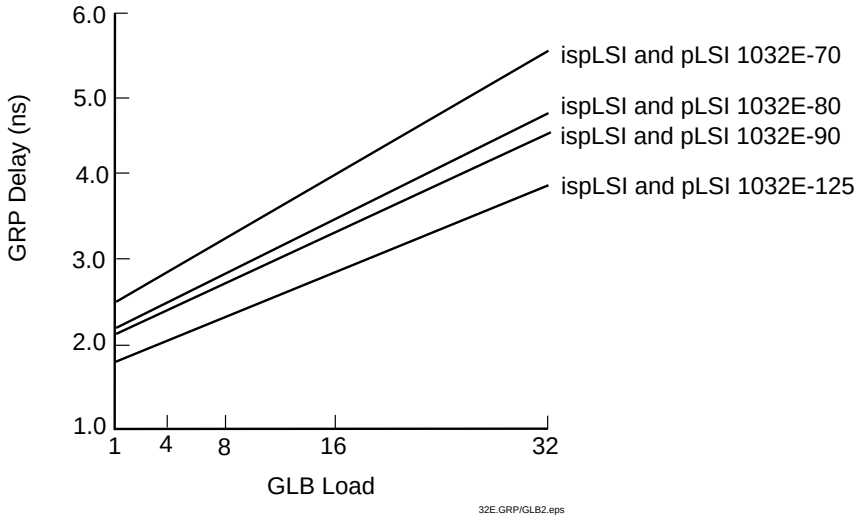
th = Clock (max) + Reg h - Logic
= (**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gh) – (**t**iobp + **t**grp4 + **t**20ptxor)
= (#54 + #42 + #56) + (#41) – (#22 + #30 + #37)
2.7 ns = (1.4 + 2.3 + 1.8) + (4.5) – (0.3 + 2.0 + 5.0)

tco = Clock (max) + Reg co + Output
= (**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#54 + #42 + #56) + (#42) + (#47 + #49)
5.5 ns = (1.4 + 2.3 + 1.8) + (2.3) + (1.0 + 1.3)

Table 2-0042b-32

1. Calculations are based upon timing specifications for the ispLSI and pLSI 1032E-125.

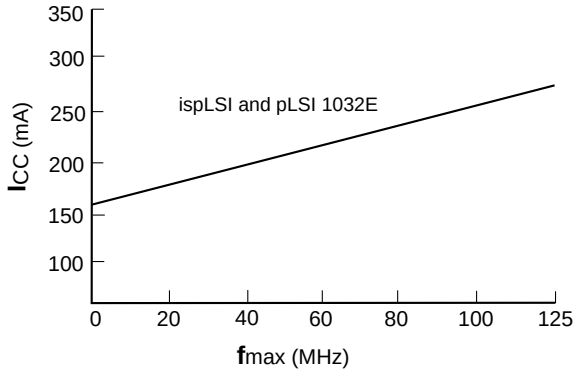
Maximum GRP Delay vs GLB Loads



Power Consumption

Power consumption in the ispLSI and pLSI 1032E device depends on two primary factors: the speed at which the device is operating, and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of eight 16-bit counters
Typical current at 5V, 25°C

I_{CC} can be estimated for the ispLSI and pLSI 1032E using the following equation:

I_{CC}(mA) = 15 + (# of PTs * 0.59) + (# of nets * Max freq * 0.0078)

Where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max freq = Highest Clock Frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 4 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127B-16-80-isp2/1032E

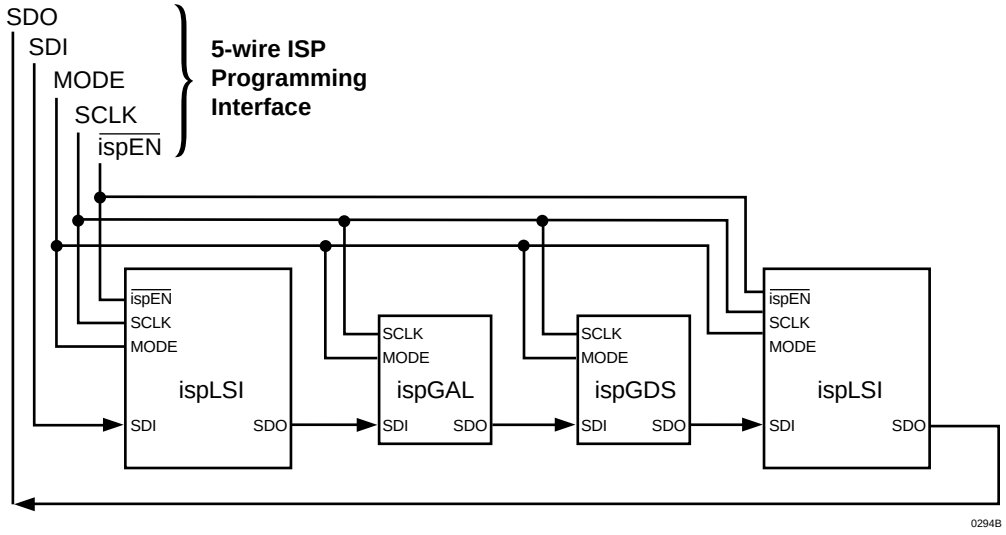
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

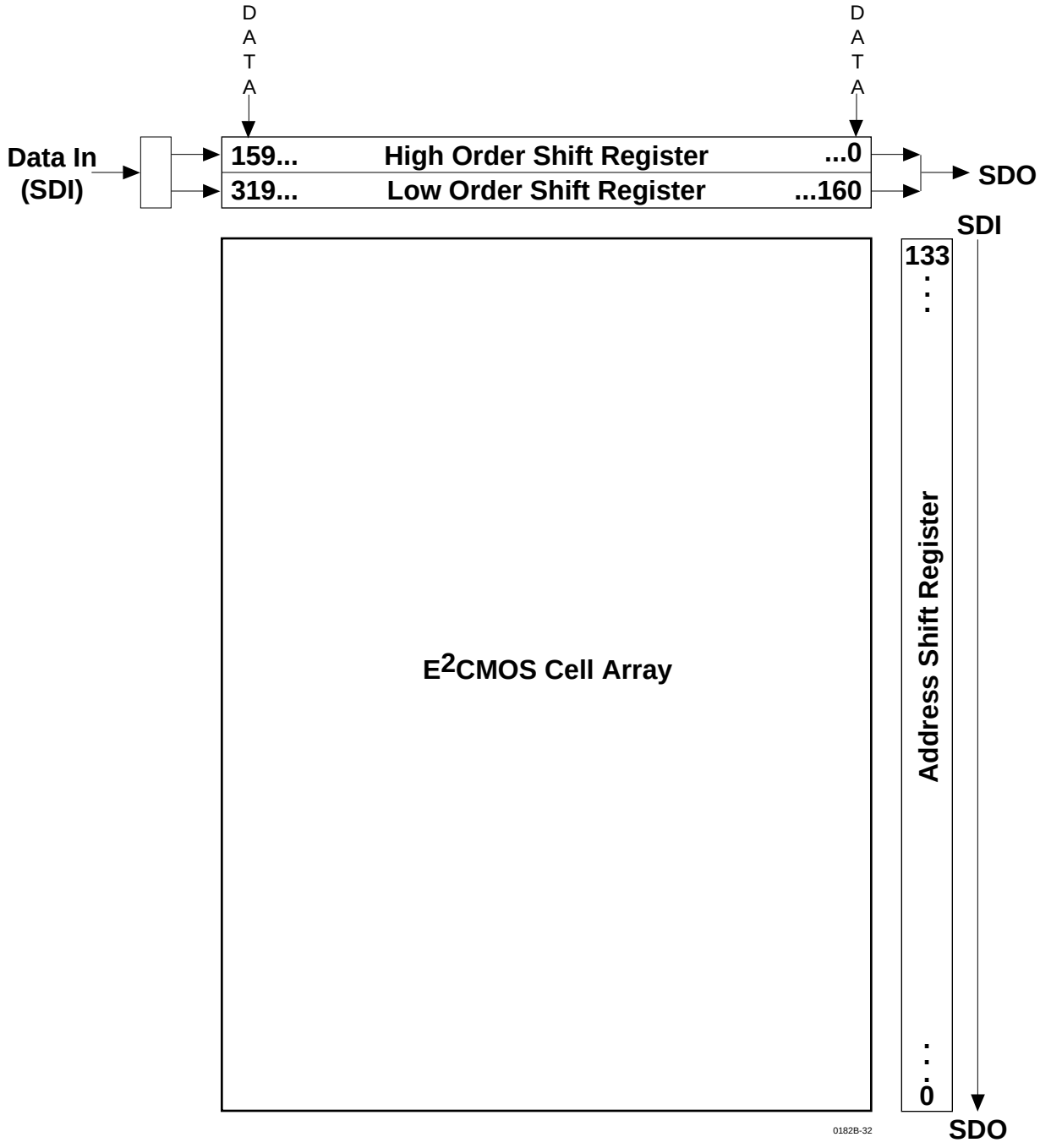
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section of the 1996 Lattice Semiconductor Data Book.

The Device ID for the ispLSI 1032E is 0000 1101 (0D hex). This code is the unique device identifier which is generated when a read ID instruction is performed.

Figure 4. ISP Programming Interface



ispLSI 1032E Shift Register Layout



Note: A logic “1” in the Address Shift Register bit position enables the row for programming or verification. A logic “0” disables it.

Pin Description

NAME	PLCC PIN NUMBERS	TQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18	17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31, 32, 33, 34, 35, 36, 40, 41, 42, 43, 44, 45, 46, 47, 48, 53, 54, 55, 56, 57, 58, 59, 67, 68, 69, 70, 71, 72, 73, 78, 79, 80, 81, 82, 83, 84, 85, 86, 90, 91, 92, 93, 94, 95, 96, 97, 98, 3, 4, 5, 6, 7, 8, 9	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0/IN 4	67	66	This is a dual function pin. It can be used either as Global Output Enable for all I/O cells or it can be used as a dedicated input pin.
GOE 1/IN 5	84	87	This is a dual function pin. It can be used either as Global Output Enable for all I/O cells or it can be used as a dedicated input pin.
IN 6, IN 7	2, 19	89, 10	Dedicated input pins to the device.
$\overline{\text{ispEN}}$**/NC	23	14	Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	25	16	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 is also used as one of the two control pins for the isp state machine. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high.
MODE*/IN 1	42	37	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high.
SDO*/IN 2	44	39	Output/Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high.
SCLK*/IN 3	61	60	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high.
$\overline{\text{RESET}}$	24	15	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	20	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	66	65	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	63	62	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	62	61	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	1, 22, 43, 64	13, 38, 63, 88	Ground (GND)
VCC	21, 65	12, 64	Vcc
NC		1, 2, 24, 25, 26, 27, 49, 50, 51, 52, 74, 75, 76, 77, 99, 100	No connect.

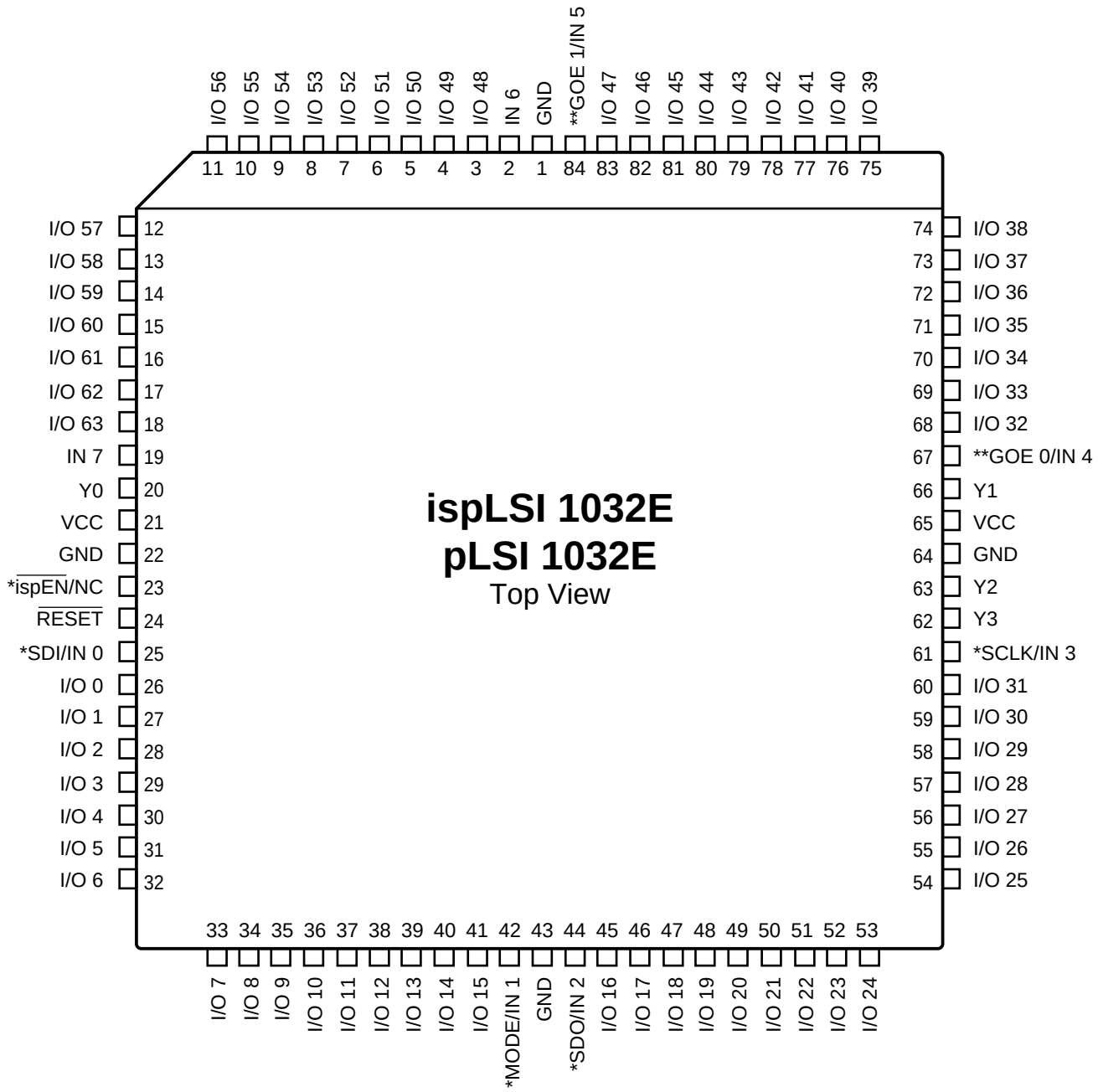
Table 2-0002A-32E

* ispLSI 1032E only

** $\overline{\text{ispEN}}$ for ispLSI 1032E; NC for pLSI 1032E, must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

Pin Configurations

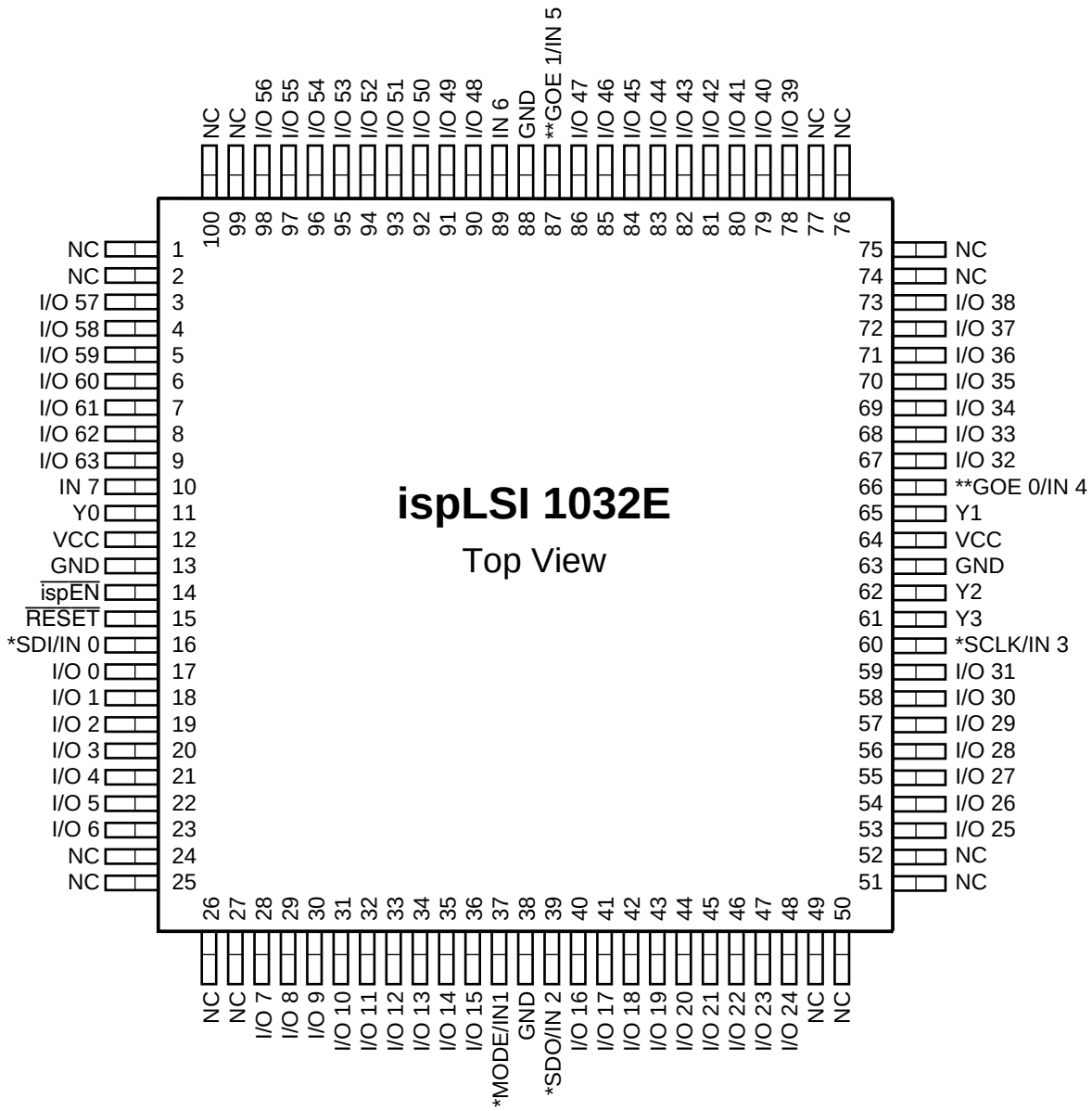
ispLSI and pLSI 1032E 84-Pin PLCC Pinout Diagram



* Pins have dual function capability for ispLSI 1032E only (except pin 23, which is $\overline{\text{ispEN}}$ only).
** Pins have dual function capability which is software selectable.

0123-32-isp

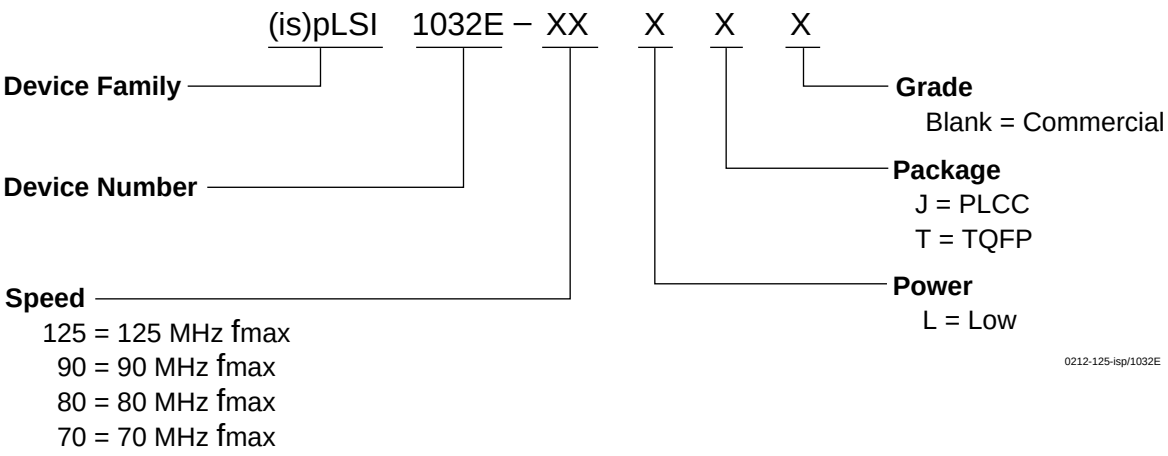
ispLSI 1032E 100-Pin TQFP Pinout Diagram



*Pins have dual function capability.
** Pins have dual function capability which is software selectable.

0766A-32E-isp

Part Number Description



ispLSI and pLSI 1032E Ordering Information

FAMILY	Fmax (MHz)	Tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	125	7.5	ispLSI 1032E-125LJ	84-Pin PLCC
	125	7.5	ispLSI 1032E-125LT	100-Pin TQFP
	90	10	ispLSI 1032E-90LJ	84-Pin PLCC
	90	10	ispLSI 1032E-90LT	100-Pin TQFP
	80	12	ispLSI 1032E-80LJ	84-Pin PLCC
	80	12	ispLSI 1032E-80LT	100-Pin TQFP
	70	15	ispLSI 1032E-70LJ	84-Pin PLCC
	70	15	ispLSI 1032E-70LT	100-Pin TQFP
pLSI	125	7.5	pLSI 1032E-125LJ	84-Pin PLCC
	90	10	pLSI 1032E-90LJ	84-Pin PLCC
	80	12	pLSI 1032E-80LJ	84-Pin PLCC
	70	15	pLSI 1032E-70LJ	84-Pin PLCC

Table 2-0041B-32/isp.eps

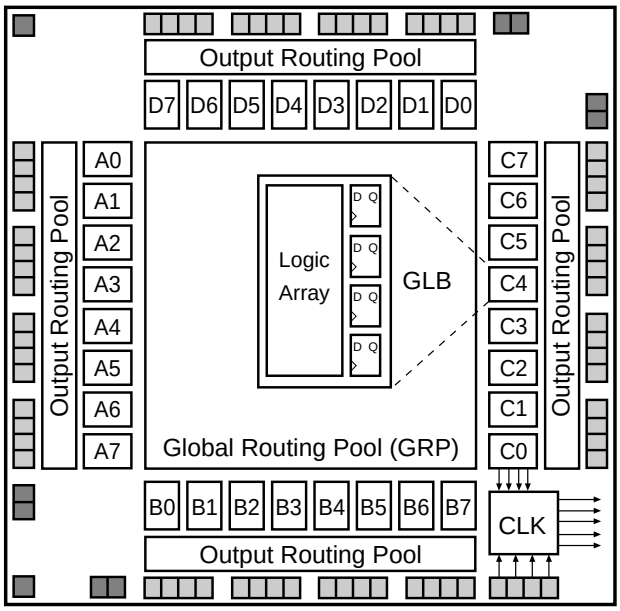
ispLSI® and pLSI® 1032

High-Density Programmable Logic

Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— High Speed Global Interconnect**
  - **— 6000 PLD Gates**
  - **— 64 I/O Pins, Eight Dedicated Inputs**
  - **— 192 Registers**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Fast Random Logic**
  - **— Security Cell Prevents Unauthorized Copying**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 90 MHz Maximum Operating Frequency**
  - **— f_{max} = 60 MHz for Industrial and Military/883 Devices**
  - **— t_{pd} = 12 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile E²CMOS Technology**
  - **— 100% Tested**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Prototyping**
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Four Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI AND pLSI DEVELOPMENT TOOLS**
  - **pDS® Software**
    - **— Easy to Use PC Windows™ Interface**
    - **— Boolean Logic Compiler**
    - **— Manual Partitioning**
    - **— Automatic Place and Route**
    - **— Static Timing Table**
  - **pDS+™ Software**
    - **— Industry Standard, Third Party Design Environments**
    - **— Schematic Capture, State Machine, HDL**
    - **— Automatic Partitioning and Place and Route**
    - **— Comprehensive Logic and Timing Simulation**
    - **— PC and Workstation Platforms**

Functional Block Diagram



Description

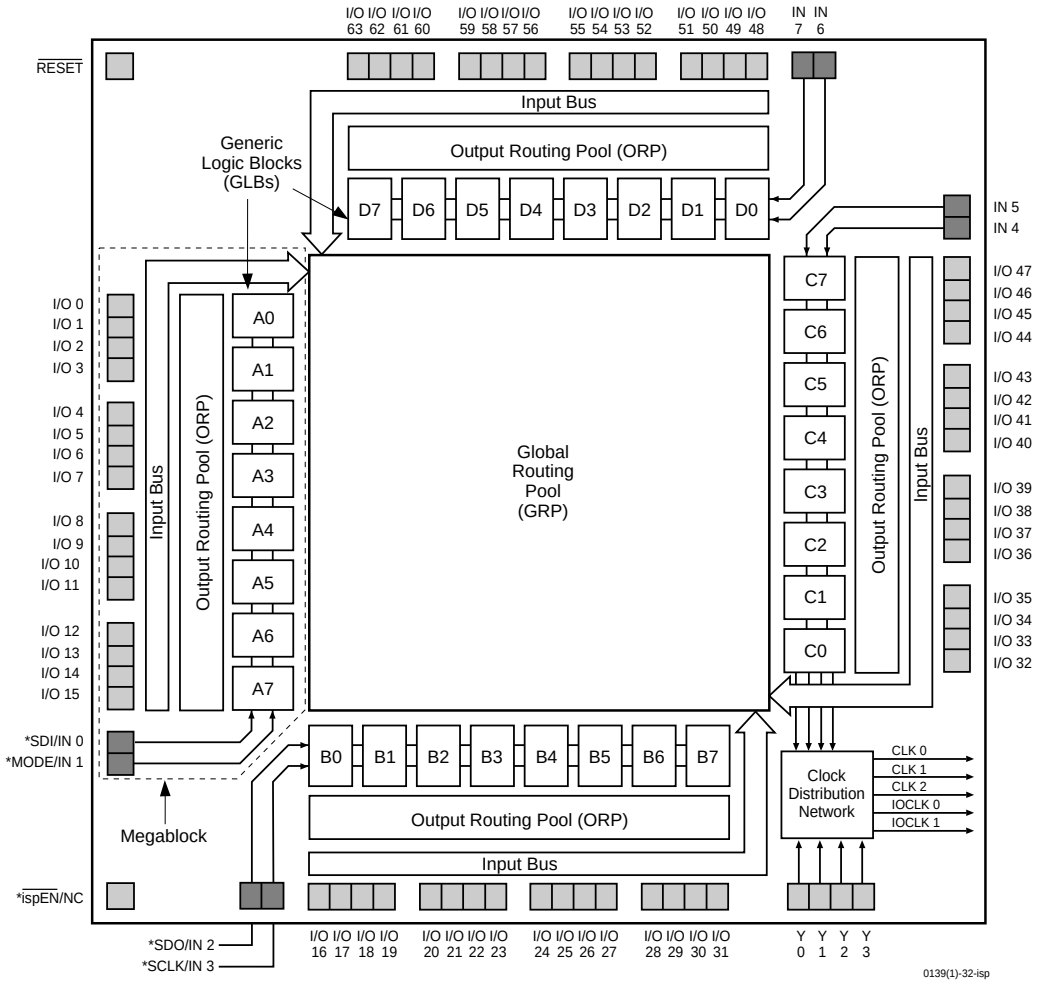
The ispLSI and pLSI 1032 are High-Density Programmable Logic Devices containing 192 Registers, 64 Universal I/O pins, eight Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1032 features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1032 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the ispLSI and pLSI 1032 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7 (see figure 1). There are a total of 32 GLBs in the ispLSI and pLSI 1032 devices. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Functional Block Diagram

Figure 1. ispLSI and pLSI 1032 Functional Block Diagram



*ISP Control Functions for ispLSI 1032 Only

The devices also have 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The I/O cells within the Megablock also share a common Output Enable (OE) signal. The ispLSI and pLSI 1032 devices contain four of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 1032 devices are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (C0 on the ispLSI and pLSI 1032 devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to +70°C	4.75	5.25	V
		Industrial	T_A = -40°C to +85°C	4.5	5.5	
		Military/883	T_C = -55°C to +125°C	4.5	5.5	
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V

Table 2- 0005Aisp w/mil.eps

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER		MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	Commercial/Industrial	8	pf	V_{CC}=5.0V, V_{IN}=2.0V
		Military	10	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance		10	pf	V_{CC}=5.0V, $V_{I/O}$, V_Y=2.0V

1. Guaranteed but not 100% tested.

Table 2- 0006

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2- 0008B

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

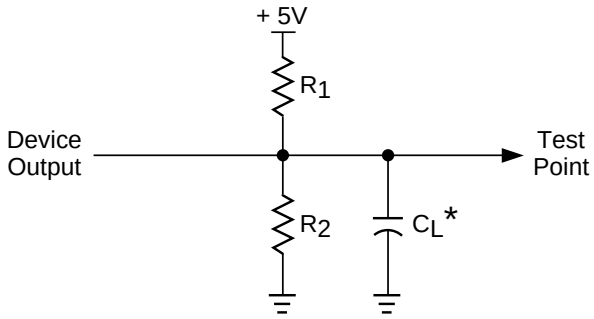
3-state levels are measured 0.5V from steady-state active level.

Table 2- 0003

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
I_{IL-isp}	isp Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V	Commercial	–	130	190	mA
		f_{TOGGLE} = 1 MHz	Industrial/Military	–	135	220	mA

1. One output at a time for a maximum duration of one second.
2. Measured using eight 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[5]	#[2]	DESCRIPTION[1]	-90		-80		-60		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd1	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	12	–	15	–	20	ns
tpd2	A	2	Data Propagation Delay, Worst Case Path	–	17	–	20	–	25	ns
fmax (Int.)	A	3	Clock Frequency with Internal Feedback[3]	90.9	–	80	–	60	–	MHz
fmax (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	58.8	–	50	–	38	–	MHz
fmax (Tog.)	–	5	Clock Frequency, Max Toggle[4]	125	–	100	–	83	–	MHz
tsu1	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	6	–	7	–	9	–	ns
tco1	A	7	GLB Reg. Clock to Output Delay, ORP bypass	–	8	–	10	–	13	ns
th1	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	0	–	ns
tsu2	–	9	GLB Reg. Setup Time before Clock	9	–	10	–	13	–	ns
tco2	–	10	GLB Reg. Clock to Output Delay	–	10	–	12	–	16	ns
th2	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	0	–	ns
tr1	A	12	Ext. Reset Pin to Output Delay	–	15	–	17	–	22.5	ns
trw1	–	13	Ext. Reset Pulse Duration	10	–	10	–	13	–	ns
ten	B	14	Input to Output Enable	–	15	–	18	–	24	ns
tdis	C	15	Input to Output Disable	–	15	–	18	–	24	ns
twh	–	16	Ext. Sync. Clock Pulse Duration, High	4	–	5	–	6	–	ns
twl	–	17	Ext. Sync. Clock Pulse Duration, Low	4	–	5	–	6	–	ns
tsu5	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	–	2	–	2.5	–	ns
th5	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	–	6.5	–	8.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t_{iobp}	20	I/O Register Bypass	–	1.6	–	2.0	–	2.7	ns
t_{iolat}	21	I/O Latch Delay	–	2.4	–	3.0	–	4.0	ns
t_{iosu}	22	I/O Register Setup Time before Clock	4.8	–	5.5	–	7.3	–	ns
t_{ioh}	23	I/O Register Hold Time after Clock	2.1	–	1.0	–	1.3	–	ns
t_{ioco}	24	I/O Register Clock to Out Delay	–	2.4	–	3.0	–	4.0	ns
t_{ior}	25	I/O Register Reset to Out Delay	–	2.8	–	2.5	–	3.3	ns
t_{din}	26	Dedicated Input Delay	–	3.2	–	4.0	–	5.3	ns
GRP									
t_{grp1}	27	GRP Delay, 1 GLB Load	–	1.2	–	1.5	–	2.0	ns
t_{grp4}	28	GRP Delay, 4 GLB Loads	–	1.6	–	2.0	–	2.7	ns
t_{grp8}	29	GRP Delay, 8 GLB Loads	–	2.4	–	3.0	–	4.0	ns
t_{grp12}	30	GRP Delay, 12 GLB Loads	–	3.0	–	3.8	–	5.0	ns
t_{grp16}	31	GRP Delay, 16 GLB Loads	–	3.6	–	4.5	–	6.0	ns
t_{grp32}	32	GRP Delay, 32 GLB Loads	–	6.4	–	8.0	–	10.6	ns
GLB									
t_{4ptbp}	33	4 Product Term Bypass Path Delay	–	5.2	–	6.5	–	8.6	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	5.7	–	7.0	–	9.3	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	7.0	–	8.0	–	10.6	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	8.2	–	9.5	–	12.7	ns
t_{gbp}	37	GLB Register Bypass Delay	–	0.8	–	1.0	–	1.3	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.2	–	1.0	–	1.3	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	3.6	–	4.5	–	6.0	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	1.6	–	2.0	–	2.7	ns
t_{gr}	41	GLB Register Reset to Output Delay	–	2.0	–	2.5	–	3.3	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	8.0	–	10.0	–	13.3	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	7.8	–	9.0	–	12.0	ns
t_{ptck}	44	GLB Product Term Clock Delay	2.8	6.0	3.5	7.5	4.6	9.9	ns
ORP									
t_{orp}	45	ORP Delay	–	2.4	–	2.5	–	3.3	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.4	–	0.5	–	0.7	ns

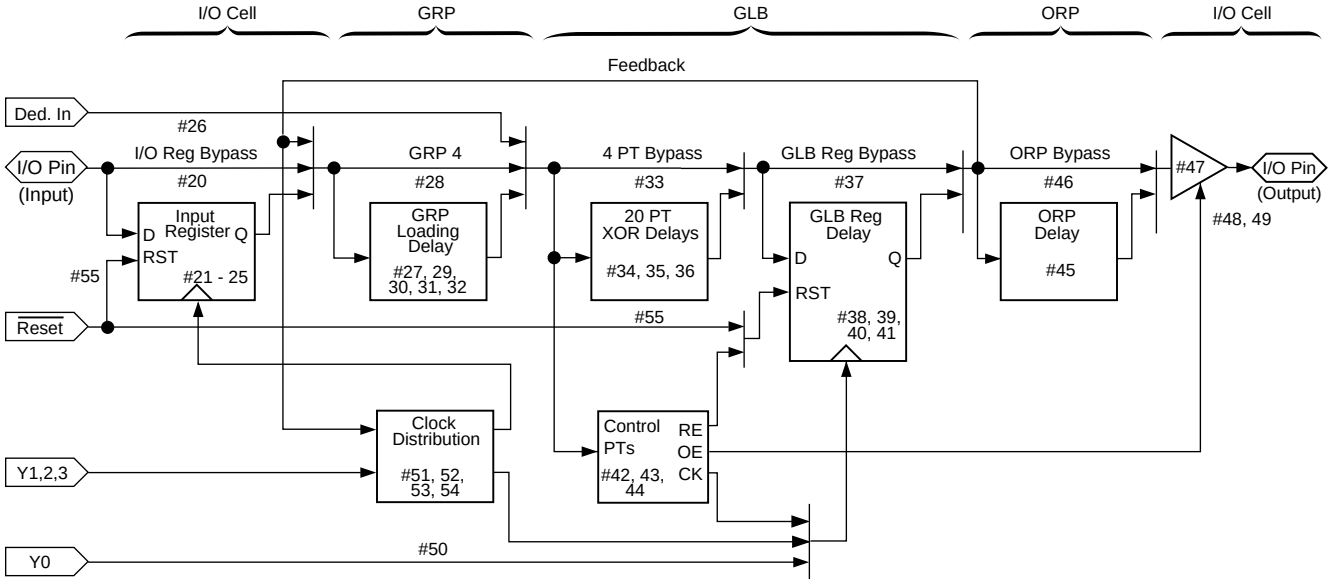
1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-90		-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
t_{ob}	47	Output Buffer Delay	–	2.4	–	3.0	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	4.0	–	5.0	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	4.0	–	5.0	–	6.7	ns
Clocks									
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	3.6	3.6	4.5	4.5	6.0	6.0	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.8	4.4	3.5	5.5	4.6	7.3	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	4.0	1.0	5.0	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	2.8	4.4	3.5	5.5	4.6	7.3	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	4.0	1.0	5.0	1.3	6.6	ns
Global Reset									
t_{gr}	55	Global Reset to GLB and I/O Registers	–	8.2	–	9.0	–	12.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI and pLSI 1032 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

t_{su} = Logic + Reg su - Clock (min)
= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)})$
= (#20 + #28 + #35) + (#38) - (#20 + #28 + #44)
5.5 ns = (2.0 + 2.0 + 8.0) + (1.0) - (2.0 + 2.0 + 3.5)

t_{h} = Clock (max) + Reg h - Logic
= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
= (#20 + #28 + #44) + (#39) - (#20 + #28 + #35)
4.0 ns = (2.0 + 2.0 + 7.5) + (4.5) - (2.0 + 2.0 + 8.0)

t_{co} = Clock (max) + Reg co + Output
= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$
= (#20 + #28 + #44) + (#40) + (#45 + #47)
19.0 ns = (2.0+ 2.0 +7.5) + (2.0) + (2.5 + 3.0)

Derivations of tsu, th and tco from the Clock GLB[1]

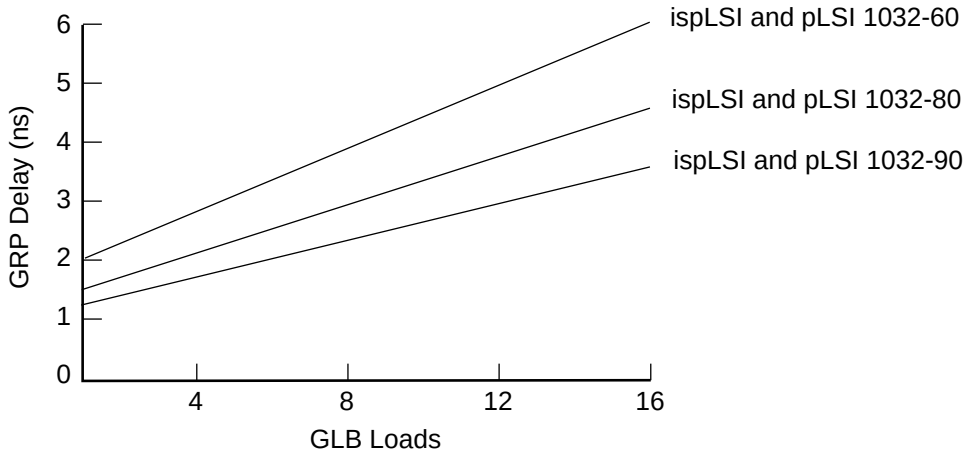
t_{su} = Logic + Reg su - Clock (min)
= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)})$
= (#20 + #28 + #35) + (#38) - (#50 + #40 + #52)
5.5 ns = (2.0 + 2.0 + 8.0) + (1.0) - (4.5 + 2.0 + 1.0)

t_{h} = Clock (max) + Reg h - Logic
= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
= (#50 + #40 + #52) + (#39) - (#20 + #28 + #35)
4.0 ns = (4.5 + 2.0 + 5.0) + (4.5) - (2.0 + 2.0 + 8.0)

t_{co} = Clock (max) + Reg co + Output
= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$
= (#50 + #40 + #52) + (#40) + (#45 + #47)
19.0 ns = (4.5 + 2.0 + 5.0) + (2.0) + (2.5 + 3.0)

1. Calculations are based upon timing specifications for the ispLSI and pLSI 1032-80.

Maximum GRP Delay vs GLB Loads



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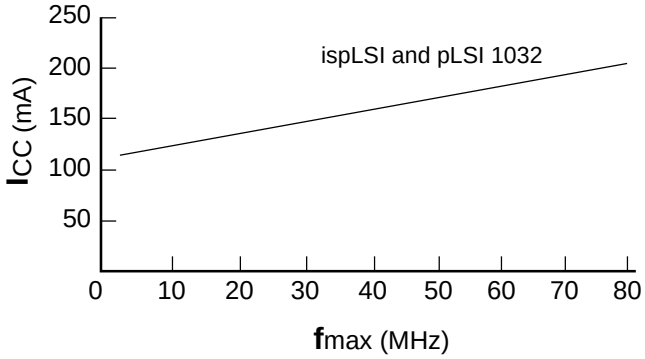
Power Consumption

Power consumption in the ispLSI and pLSI 1032 device depends on two primary factors: the speed at which the device is operating, and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of eight 16-bit Counters
Typical Current at 5V, 25°C

I_{CC} can be estimated for the ispLSI and pLSI 1032 using the following equation:

I_{CC} = 52 + (# of PTs * 0.30) + (# of nets * Max. freq * 0.009) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A-32-80-isp

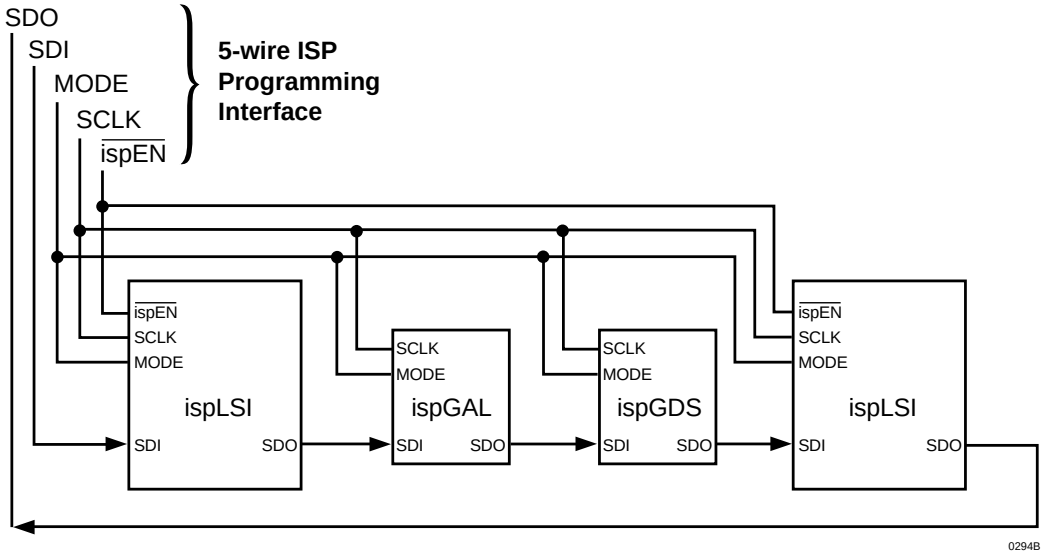
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

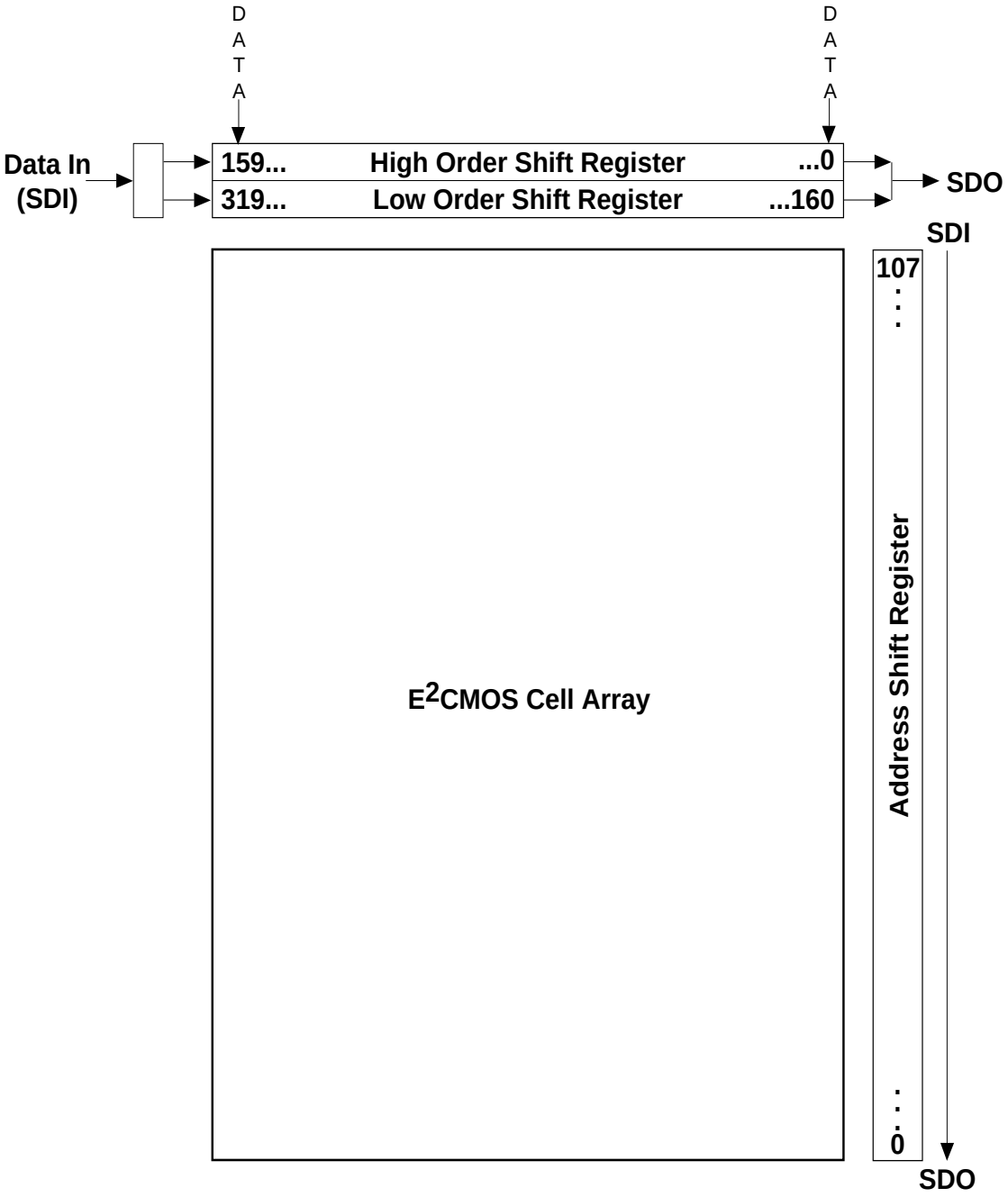
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section in this Data Book.

The device identifier for the ispLSI 1032 is 0000 0011 (03 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 1032 Shift Register Layout



Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

Pin Description

Name	PLCC Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 7	67, 84, 2, 19	Dedicated input pins to the device.
$\overline{\text{ispEN}}$*/NC	23	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	25	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE*/IN 1	42	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO*/IN 2	44	Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK*/IN 3	61	Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	24	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	20	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	66	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	63	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	62	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND VCC	1, 22, 43, 64 21, 65	Ground (GND) V_{CC}

* For ispLSI 1032 Only

Table 2-0002A-32-isp

Pin Description

Name	TQFP Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31, 32, 33, 34, 35, 36, 40, 41, 42, 43, 44, 45, 46, 47, 48, 53, 54, 55, 56, 57, 58, 59, 67, 68, 69, 70, 71, 72, 73, 78, 79, 80, 81, 82, 83, 84, 85, 86, 90, 91, 92, 93, 94, 95, 96, 97, 98, 3, 4, 5, 6, 7, 8, 9	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 7	66, 87, 89, 10	Dedicated input pins to the device.
$\overline{\text{ispEN}}$*/NC	14	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	16	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE*/IN 1	37	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO*/IN 2	39	Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK*/IN 3	60	Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
NC	1, 2, 24, 25, 26, 27, 49, 50, 51, 52, 74, 75 76, 77, 99, 100	These pins are not used.
$\overline{\text{RESET}}$	15	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	65	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	62	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	61	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	13, 38, 63, 88	Ground (GND)
VCC	12, 64	V_{CC}

* For ispLSI 1032 Only

Table 2- 0002B-32-isp

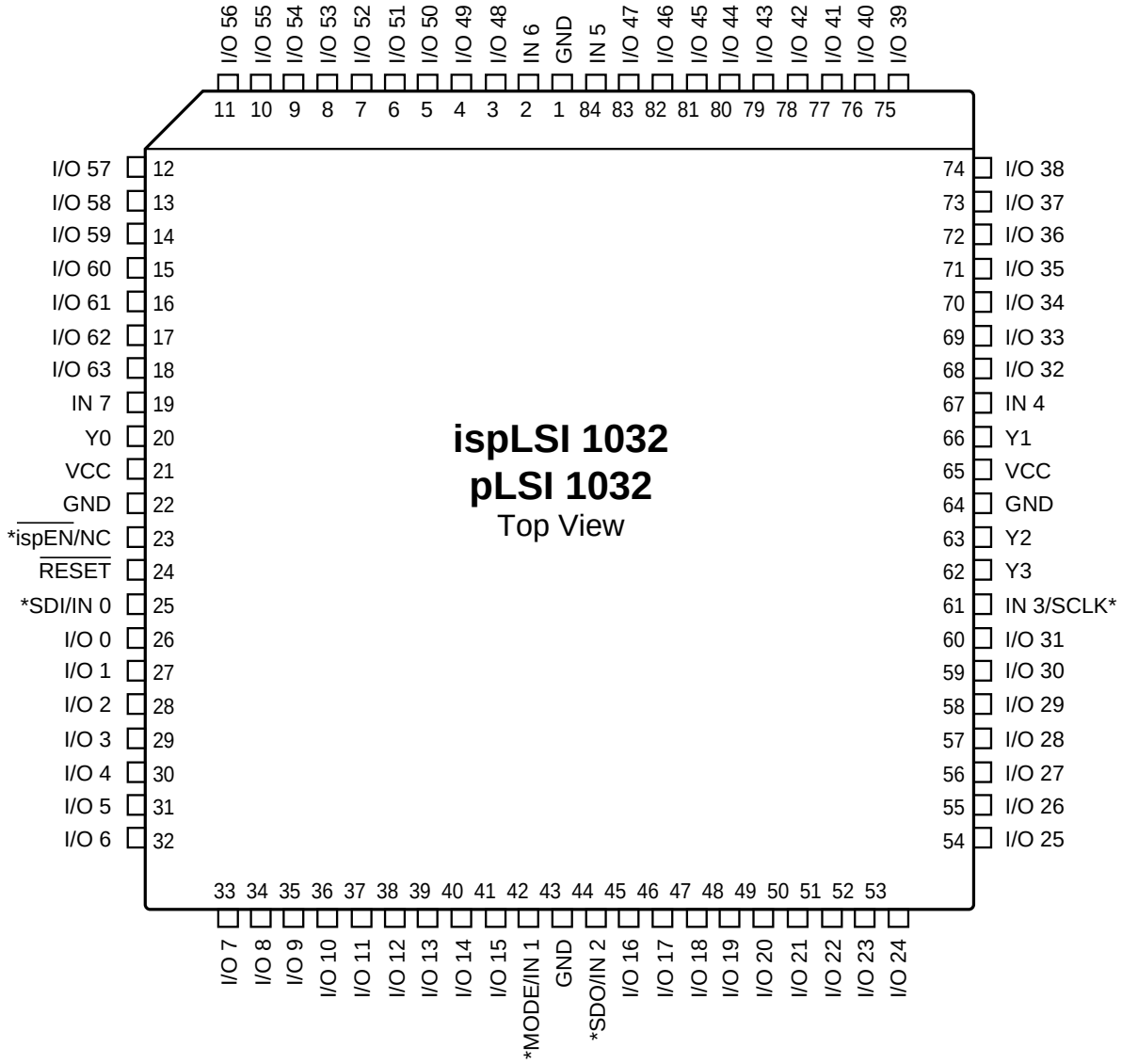
Pin Description

Name	CPGA Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	F1, H1, H2, J1, K1, J2, L1, K2, K3, L2, L3, K4, L4, J5, K5, L5, L7, K7, L6, L8, K8, L9, L10, K9, L11, K10, J10, K11, J11, H10, H11, F10, E9, D11, D10, C11, B11, C10, A11, B10, B9, A10, A9, B8, A8, B6, B7, A7, A5, B5, C5, A4, B4, A3, A2, B3, A1, B2, C2, B1, C1, D2, D1, E3	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 7	E10, C7, A6, E2	Dedicated input pins to the device.
$\overline{\text{ispEN}}$*/NC	G3	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	G2	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE*/IN 1	K6	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO*/IN 2	J7	Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK*/IN 3	G10	Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	G1	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	E1	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	E11	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	G9	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	G11	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
NC	G3	This pin should be left floating or tied to $V_{CC.}$ This pin should never be tied to GND.
GND VCC	C6, F3, F9, J6 F2, F11	Ground (GND) V_{CC}

Table 2-0002-32/883

Pin Configuration

ispLSI and pLSI 1032 84-Pin PLCC Pinout Diagram

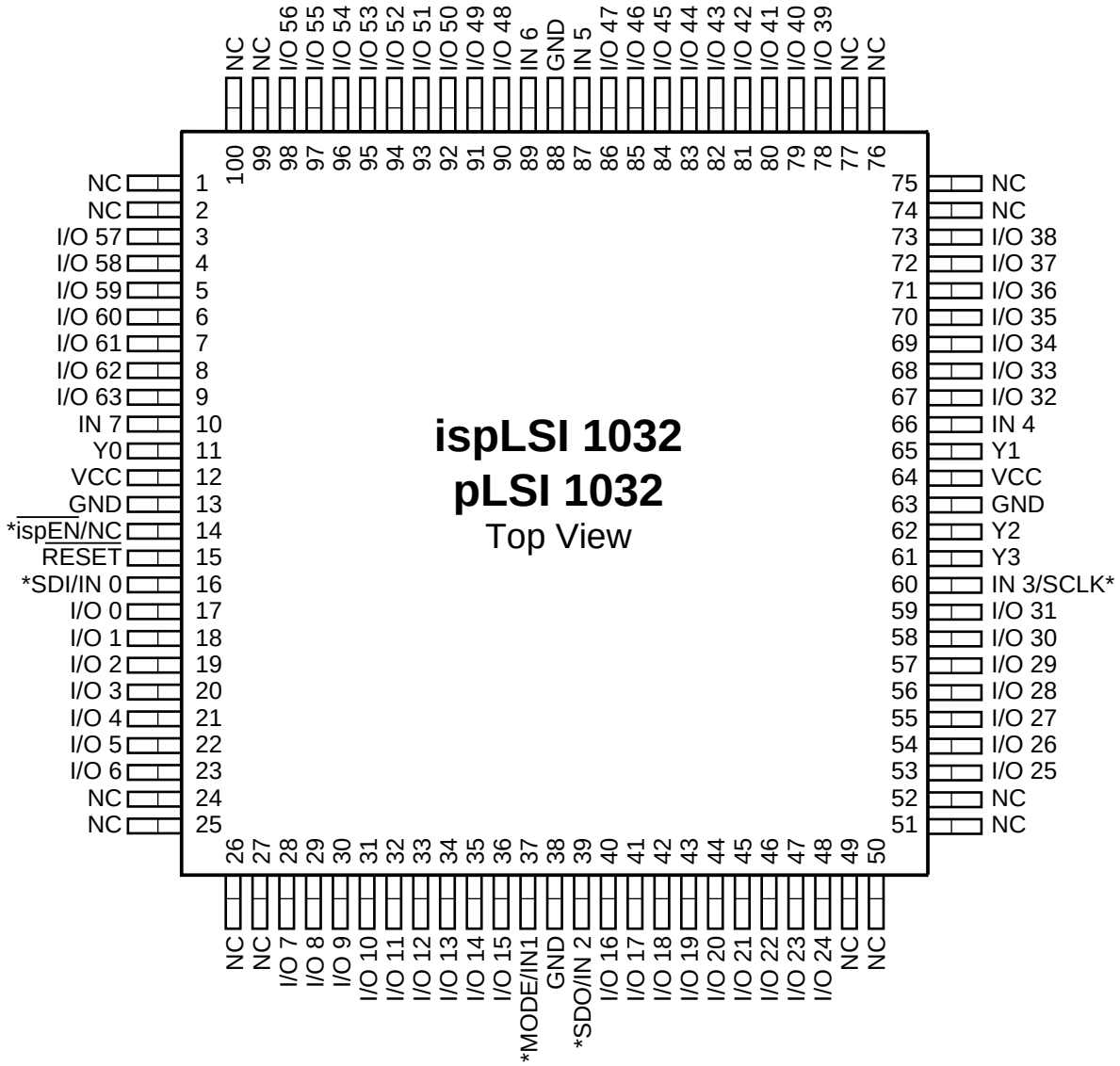


*Pins have dual function capability for ispLSI 1032 only (except pin 23, which is $\overline{\text{ispEN}}$ only).

0123-32-isp

Pin Configuration

ispLSI and pLSI 1032 100-pin TQFP Pinout Diagram

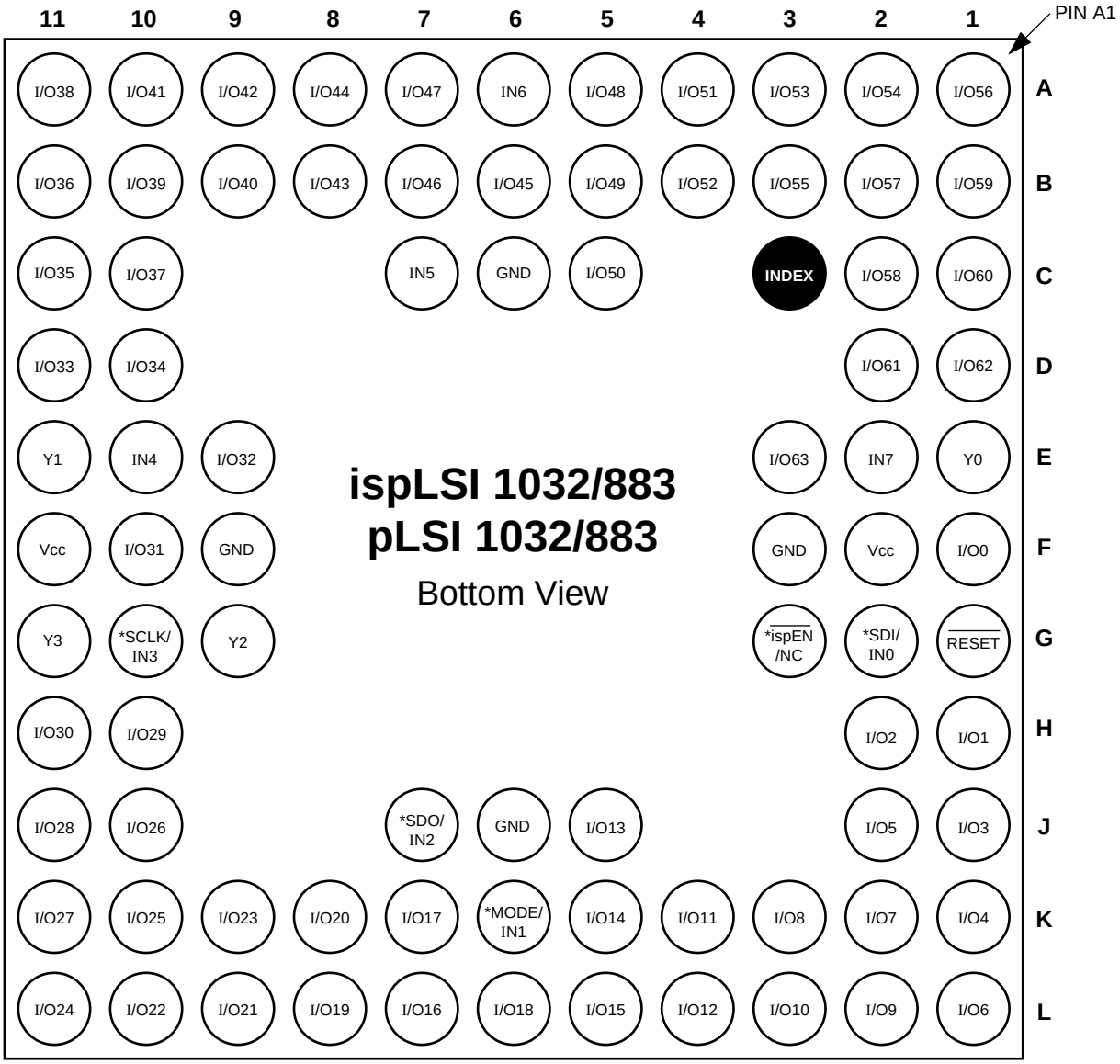


*Pins have dual function capability for ispLSI 1032 only (except pin 14, which is $\overline{\text{ispEN}}$ only).

0766A-32-isp

Pin Configuration

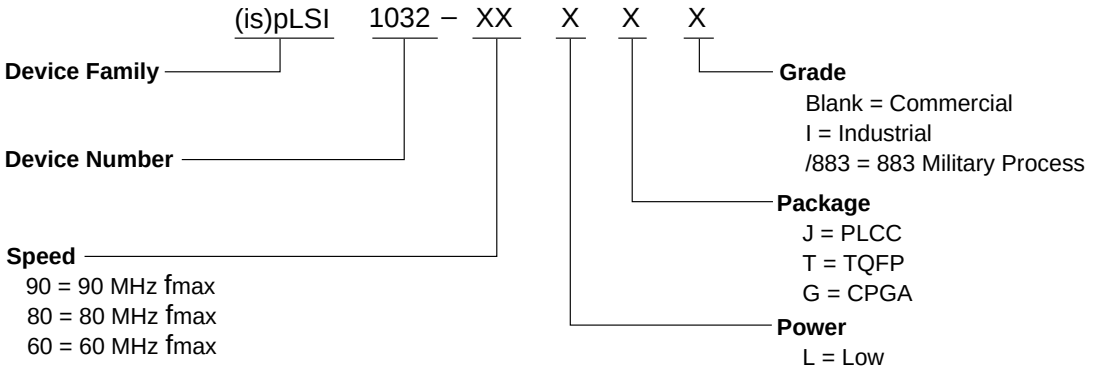
ispLSI and pLSI 1032/883 84-Pin CPGA Pinout Diagram



*Pins have dual function capability for ispLSI 1032/883 only (except pin G3, which is $\overline{\text{ispEN}}$ only).

0488A-32-isp/883

Part Number Description



ispLSI and pLSI 1032 Ordering Information

COMMERCIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
ispLSI	90	12	ispLSI 1032-90LJ	84-Pin PLCC
	90	12	ispLSI 1032-90LT	100-Pin TQFP
	80	15	ispLSI 1032-80LJ	84-Pin PLCC
	80	15	ispLSI 1032-80LT	100-Pin TQFP
	60	20	ispLSI 1032-60LJ	84-Pin PLCC
	60	20	ispLSI 1032-60LT	100-Pin TQFP
pLSI	90	12	pLSI 1032-90LJ	84-Pin PLCC
	90	12	pLSI 1032-90LT	100-Pin TQFP
	80	15	pLSI 1032-80LJ	84-Pin PLCC
	80	15	pLSI 1032-80LT	100-Pin TQFP
	60	20	pLSI 1032-60LJ	84-Pin PLCC
	60	20	pLSI 1032-60LT	100-Pin TQFP

INDUSTRIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
ispLSI	60	20	ispLSI 1032-60LJI	84-Pin PLCC
	60	20	ispLSI 1032-60LTI	100-Pin TQFP
pLSI	60	20	pLSI 1032-60LJI	84-Pin PLCC

MILITARY/883

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	SMD Number	Package
ispLSI	60	20	ispLSI 1032-60LG/883	5962-9308501MXC	84-Pin CPGA
pLSI	60	20	pLSI 1032-60LG/883	5962-9466801MXC	84-Pin CPGA

Note: Lattice Semiconductor recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number is recommended.

Table 2- 0041A-32-isp

ispLSI® and pLSI® 1048E

High-Density Programmable Logic

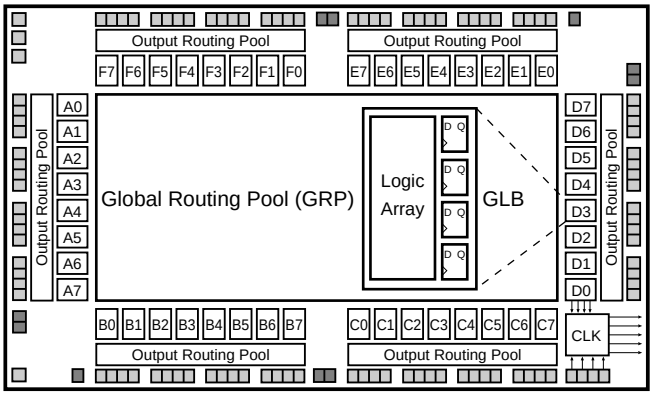
Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **— 8,000 PLD Gates**
  - **— 96 I/O Pins, Twelve Dedicated Inputs**
  - **— 288 Registers**
  - **— High-Speed Global Interconnects**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 90 MHz Maximum Operating Frequency**
  - **— t_{pd} = 10 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Eraseable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Enhanced Pin Locking Capability**
  - **— Four Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI and pLSI DEVELOPMENT TOOLS**

  pDS® Software
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning**
  - **— Automatic Place and Route**
  - **— Static Timing Table**

  pDS+™ Software
  - **— Industry Standard, Third Party Design Environments**
  - **— Schematic Capture, State Machine, HDL**
  - **— Automatic Partitioning and Place and Route**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

Functional Block Diagram



0139G1A-isp

Description

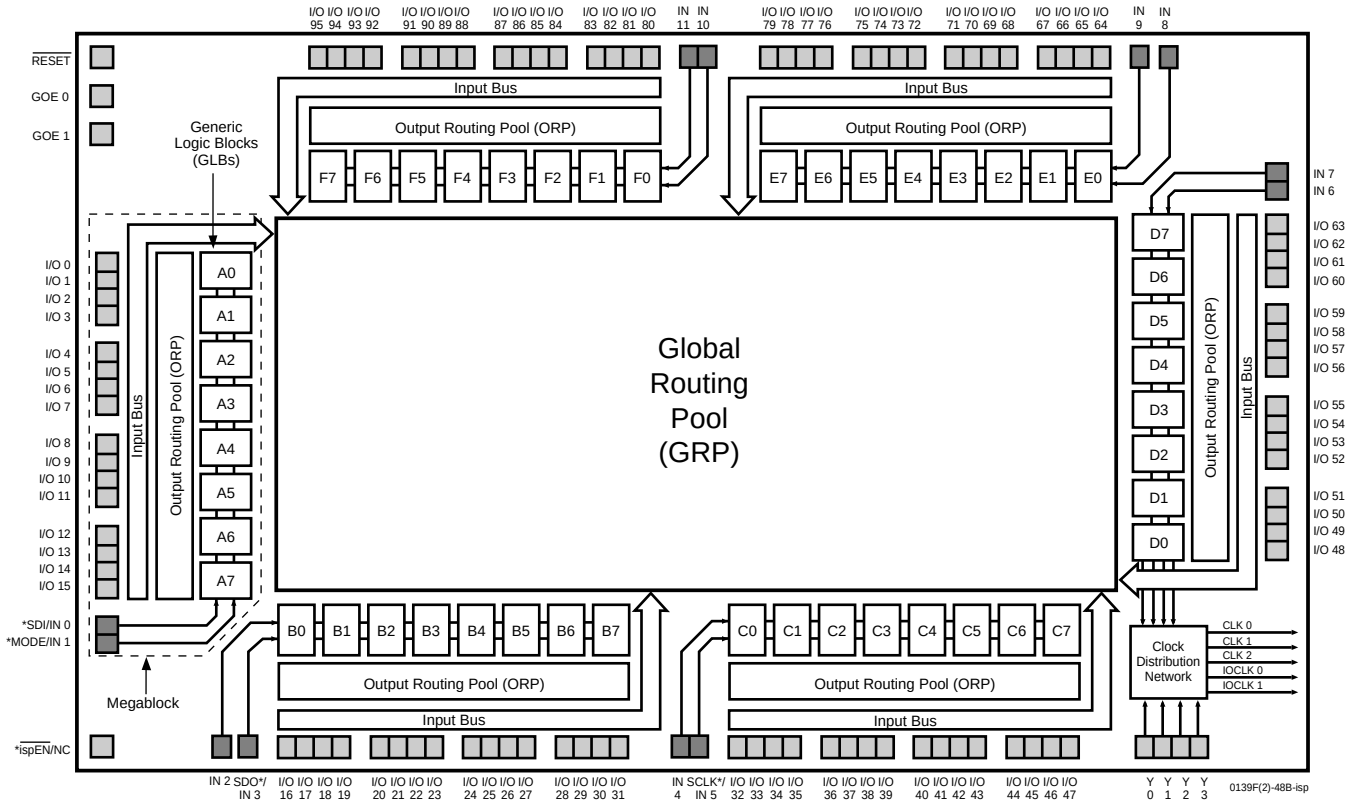
The ispLSI and pLSI 1048E are High-Density Programmable Logic Devices containing 288 Registers, 96 Universal I/O pins, 12 Dedicated Input pins, four Dedicated Clock Input pins, two dedicated Global OE input pins, and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1048E features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 1048E offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1048E device, but multiplexes four of the dedicated input pins to control in-system programming. A functional superset of the ispLSI and pLSI 1048 architecture, the ispLSI and pLSI 1048E devices add two new global output enable pins and two additional dedicated inputs.

The basic unit of logic on the ispLSI and pLSI 1048E devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1…F7 (see figure 1). There are a total of 48 GLBs in the ispLSI and pLSI 1048E devices. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Functional Block Diagram

Figure 1. ispLSI and pLSI 1048E Functional Block Diagram



*ispLSI 1048E Only

The devices also have 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each ispLSI and pLSI 1048E device contains six Megablocks.

The GRP has, as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 1048E devices are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (D0 on the ispLSI and pLSI 1048E devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2 - 0005/2000

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input, I/O, Y1, Y2, Y3, Clock Capacitance	8	pf	V_{CC} = 5.0V, V_{PIN} = 2.0V
C_2	Y0 Clock Capacitance	15	pf	V_{CC} = 5.0V, V_{PIN} = 2.0V

1. Guaranteed, but not 100% tested.

Table 2-0006a/1048C

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2-0008A-isp

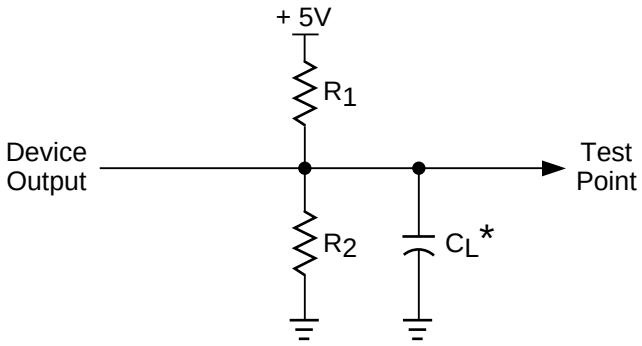
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3 ns 10% to 90%
Input Timing Reference Levels	1.5V
Ouput Timing Reference Levels	1.5V
Output Load	See figure 2

Table 2-0003

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213a

Output Load Conditions (see Figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2-0004a

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH}= -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
I_{IL-isp}	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= 5V, V_{OUT}= 0.5V	–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL}= 0.0V, V_{IH}= 3.0V f_{CLOCK} = 1 MHz	–	175	–	mA

Table 2-0007a-48-isp

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using twelve 16-bit counters.
3. Typical values are at V_{CC}= 5V and T_A= 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to Power Consumption section of this data sheet and Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-90		-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propogation Delay, 4PT Bypass, ORP Bypass	–	10.0	–	15.0	–	20.0	ns
t_{pd2}	A	2	Data Propogation Delay, Worst Case Path	–	12.5	–	18.5	–	24.5	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	90.9	–	70.0	–	50.0	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	71.0	–	56.0	–	42.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle $\left(\frac{1}{twh + twl}\right)$	125.0	–	100.0	–	77.0	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock,4 PT Bypass	6.5	–	9.0	–	12.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	6.5	–	7.0	–	9.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	7.5	–	11.0	–	14.5	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	7.5	–	9.0	–	12.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	13.5	–	15.0	–	20.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	6.5	–	10.0	–	13.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	15.0	–	18.0	–	24.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	15.0	–	18.0	–	24.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	9.0	–	12.0	–	16.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	9.0	–	12.0	–	16.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	4.0	–	5.0	–	6.5	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	4.0	–	5.0	–	6.5	–	ns
t_{su3}	–	20	I/O Reg. Setup Time before Ext. Sync Clock (Y2, Y3)	4.0	–	4.0	–	6.5	–	ns
t_{h3}	–	21	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	0.0	–	0.0	–	0.0	–	ns

Table 2-0030-48E/90,70,50

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-90		-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
tiobp	22	I/O Register Bypass	–	0.5	–	0.6	–	0.7	ns
tiolat	23	I/O Latch Delay	–	2.5	–	3.6	–	4.7	ns
tiosu	24	I/O Register Setup Time before Clock	4.0	–	4.1	–	6.5	–	ns
tioh	25	I/O Register Hold Time after Clock	-0.5	–	-0.6	–	-0.7	–	ns
tioco	26	I/O Register Clock to Out Delay	–	5.0	–	6.0	–	7.0	ns
tior	27	I/O Register Reset to Out Delay	–	5.0	–	6.0	–	7.0	ns
tdin	28	Dedicated Input Delay	–	2.9	–	4.3	–	6.1	ns
GRP									
tgrp1	29	GRP Delay, 1 GLB Load	–	2.2	–	3.5	–	5.1	ns
tgrp4	30	GRP Delay, 4 GLB Loads	–	2.4	–	3.7	–	5.4	ns
tgrp8	31	GRP Delay, 8 GLB Loads	–	2.7	–	4.1	–	5.8	ns
tgrp16	32	GRP Delay, 16 GLB Loads	–	3.3	–	4.8	–	6.6	ns
tgrp48	33	GRP Delay, 48 GLB Loads	–	5.7	–	7.5	–	9.8	ns
GLB									
t4ptbpc	34	4 Product Term Bypass Path Delay (Combinatorial)	–	5.4	–	8.5	–	10.7	ns
t4ptbpr	35	4 Product Term Bypass Path Delay (Registered)	–	6.3	–	7.4	–	9.2	ns
t1ptxor	36	1 Product Term/XOR Path Delay	–	6.5	–	8.4	–	10.5	ns
t20ptxor	37	20 Product Term/XOR Path Delay	–	6.5	–	8.4	–	10.5	ns
txoradj	38	XOR Adjacent Path Delay[3]	–	7.3	–	9.4	–	11.7	ns
tgbp	39	GLB Register Bypass Delay	–	0.4	–	1.6	–	2.2	ns
tgsu	40	GLB Register Setup Time before Clock	0.1	–	0.1	–	0.0	–	ns
tgh	41	GLB Register Hold Time after Clock	6.4	–	8.5	–	11.5	–	ns
tgco	42	GLB Register Clock to Output Delay	–	2.0	–	2.0	–	3.0	ns
tgro	43	GLB Register Reset to Output Delay	–	6.3	–	6.3	–	7.3	ns
tptre	44	GLB Product Term Reset to Register Delay	–	5.0	–	6.1	–	7.9	ns
tptoe	45	GLB Product Term Output Enable to I/O Cell Delay	–	5.7	–	6.8	–	10.0	ns
tptck	46	GLB Product Term Clock Delay	4.0	5.2	5.1	6.4	6.9	8.3	ns
ORP									
torp	47	ORP Delay	–	1.0	–	2.0	–	2.5	ns
torpbp	48	ORP Bypass Delay	–	0.0	–	0.0	–	0.0	ns

Table 2-0036-48E/90,70,50

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

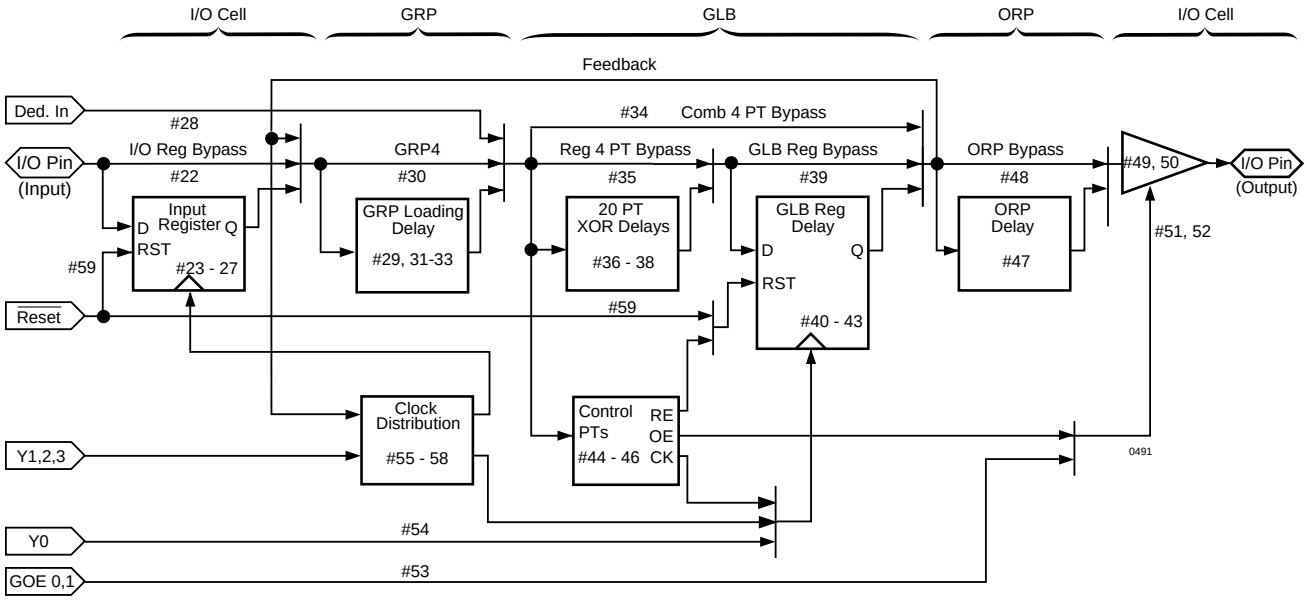
Internal Timing Parameters[1]

PARAMETER	#	DESCRIPTION	-90		-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
t_{ob}	49	Output Buffer Delay	–	1.7	–	2.2	–	3.2	ns
t_{sl}	50	Output Slew Limited Delay Adder	–	12.0	–	12.0	–	12.0	ns
t_{oen}	51	I/O Cell OE to Output Enabled	–	6.4	–	6.9	–	7.9	ns
t_{odis}	52	I/O Cell OE to Output Disabled	–	6.4	–	6.9	–	7.9	ns
t_{goe}	53	Global OE	–	2.6	–	5.1	–	8.1	ns
Clocks									
t_{gy0}	54	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.8	2.8	2.8	2.8	3.3	3.3	ns
$t_{gy1/2}$	55	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.8	2.8	2.8	2.8	3.3	3.3	ns
t_{gcp}	56	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	1.8	0.8	1.8	0.8	1.8	ns
$t_{ioy2/3}$	57	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	0.0	0.5	0.1	0.6	0.0	0.7	ns
t_{iocp}	58	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	1.8	0.8	1.8	0.8	1.8	ns
Global Reset									
t_{gr}	59	Global Reset to GLB and I/O Registers	–	4.5	–	4.5	–	7.5	ns

Table 2-0037-48E/90,70,50

1. Internal timing parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI and pLSI 1048E Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (**t**iobp + **t**grp4 + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp4 + **t**ptck(min))
= (#22 + #30 + #37) + (#40) - (#22 + #30 + #46)
2.6 ns = (0.5 + 2.4 + 6.5) + (0.1) - (0.5 + 2.4 + 4.0)

th = Clock (max) + Reg h - Logic
= (**t**iobp + **t**grp4 + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp4 + **t**20ptxor)
= (#22 + #30 + #46) + (#41) - (#22 + #30 + #37)
5.1 ns = (0.5 + 2.4 + 5.2) + (6.4) - (0.5 + 2.4 + 6.5)

tco = Clock (max) + Reg co + Output
= (**t**iobp + **t**grp4 + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#22 + #30 + #46) + (#42) + (#47 + #49)
12.8 ns = (0.5 + 2.4 + 5.2) + (2.0) + (1.0 + 1.7)

Derivations of tsu, th and tco from the Clock GLB[1]

tsu = Logic + Reg su - Clock (min)
= (**t**iobp + **t**grp4 + **t**20ptxor) + (**t**gsu) - (**t**gy0(min) + **t**gco + **t**gcp(min))
= (#22 + #30 + #37) + (#40) - (#54 + #42 + #56)
3.9 ns = (0.5 + 2.4 + 6.5) + (0.1) - (2.8 + 2.0 + 0.8)

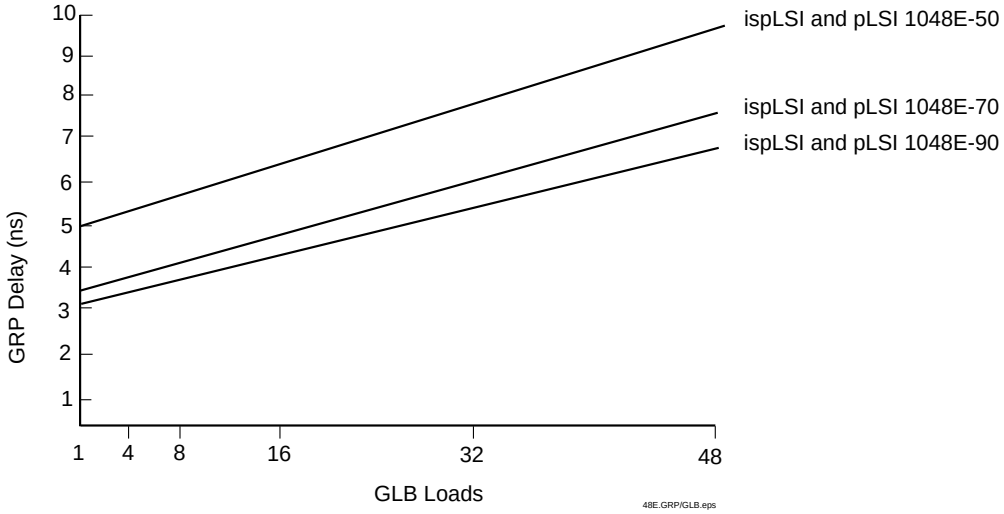
th = Clock (max) + Reg h - Logic
= (**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gh) - (**t**iobp + **t**grp4 + **t**20ptxor)
= (#54 + #42 + #56) + (#41) - (#22 + #30 + #37)
3.6 ns = (2.8 + 2.0 + 1.8) + (6.4) - (0.5 + 2.4 + 6.5)

tco = Clock (max) + Reg co + Output
= (**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#54 + #42 + #56) + (#42) + (#47 + #49)
11.3 ns = (2.8 + 2.0 + 1.8) + (2.0) + (1.0 + 1.7)

1. Calcuations are based upon timing specifications for the ispLSI and pLSI 1048E-90

Table 2-0042-1048E

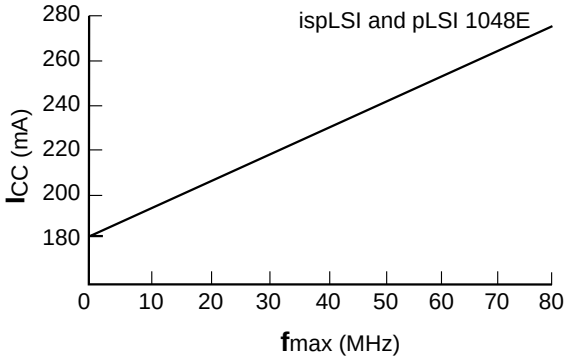
Maximum GRP Delay vs. GLB Loads



Power Consumption

Power Consumption in the ispLSI and pLSI 1048E device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of twelve 16-bit counters
Typical current at 5V, 25°C

I_{CC} can be estimated for the ispLSI and pLSI 1048E using the following equation:

I_{CC} = 20 + (# of PTs * 0.42) + (# of nets * Max. freq * 0.100)

Where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 4 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A-48E-80-isp

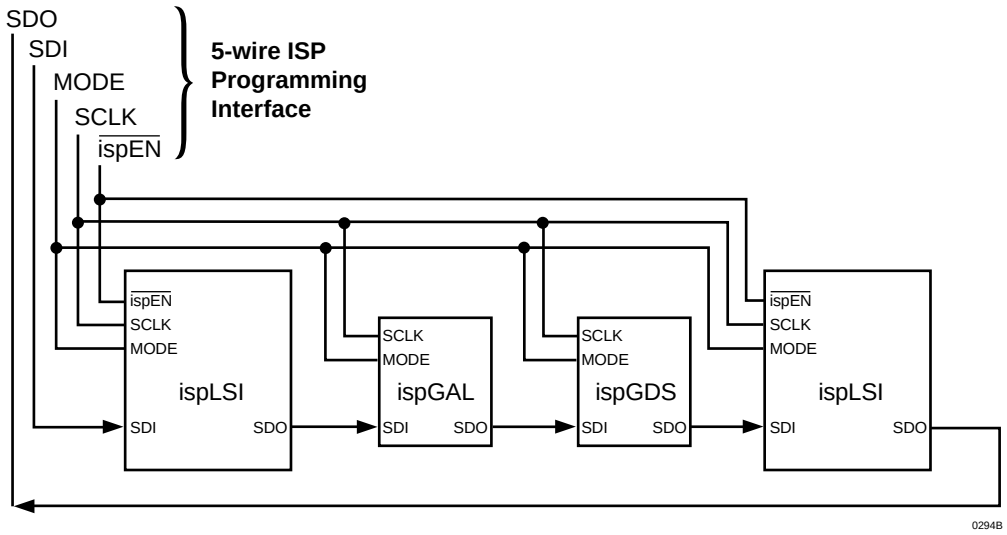
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

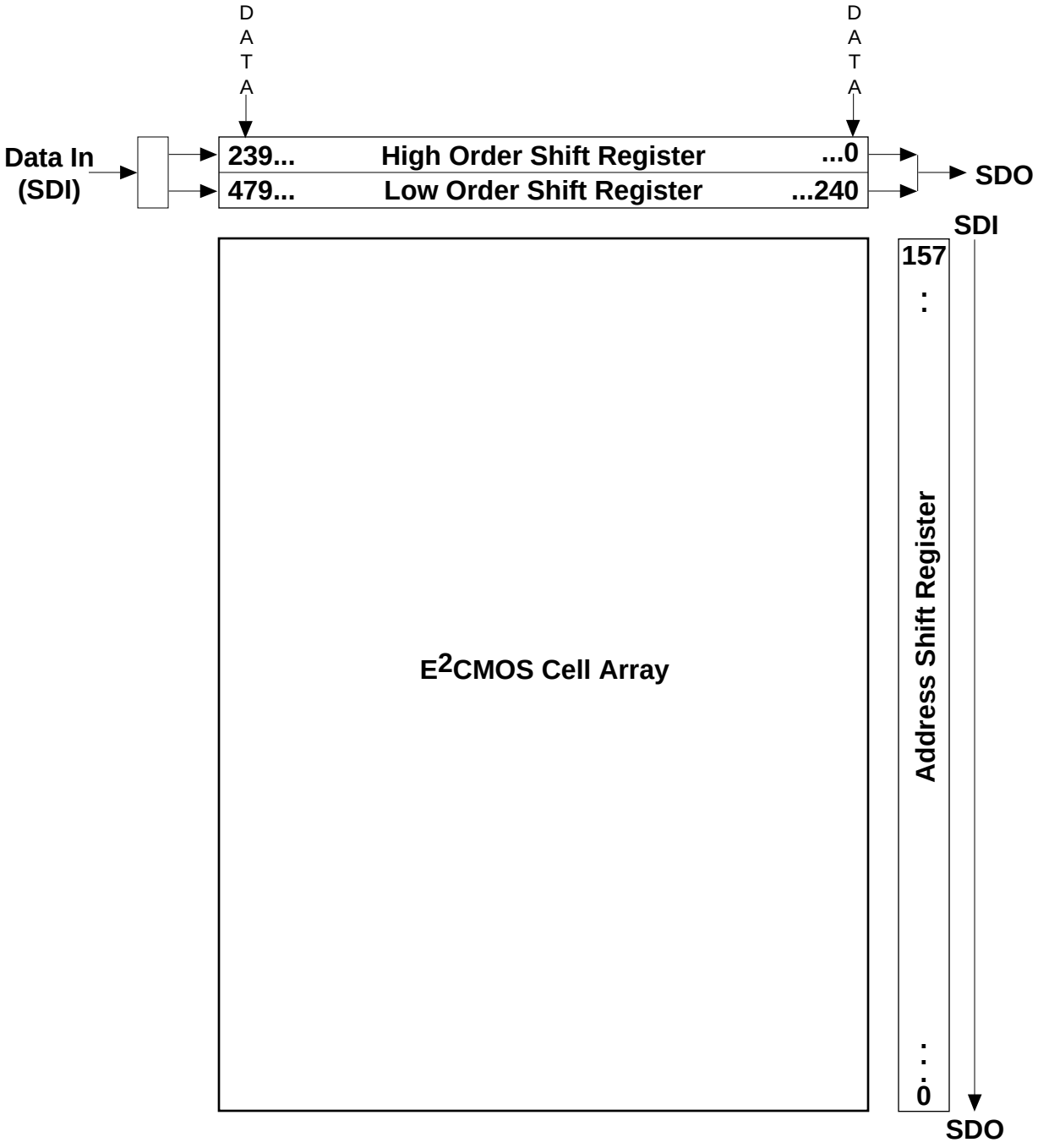
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals for the interface include isp Enable (ispEN), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section of this Data Book.

The device identifier for the ispLSI 1048E is 0000 1110 (0E hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 1048E Shift Register Layout



Note: A logic “1” in the Address Shift Register bit position enables the row for programming or verification. A logic “0” disables it.

Pin Description

NAME	PQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0, GOE1	64, 114	Global Output Enable input pins.
IN 2, IN 4 IN 6 - IN 11	47, 51 84, 110, 111, 115, 116, 14	Dedicated input pins to the device.
$\overline{\text{ispEN}}$**/NC	18	Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. When low, the MODE, SDI, SDO and SCLK controls become active.
SDI*/IN 0	20	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the ISP state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
MODE*/IN 1	46	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SDO*/IN 3	50	Output/Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SCLK*/IN 5	78	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
$\overline{\text{RESET}}$	19	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	15	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	83	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	80	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	79	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	1, 17, 33, 49, 65, 81, 97, 112	Ground (GND)
VCC	16, 48, 82, 113	V_{CC}

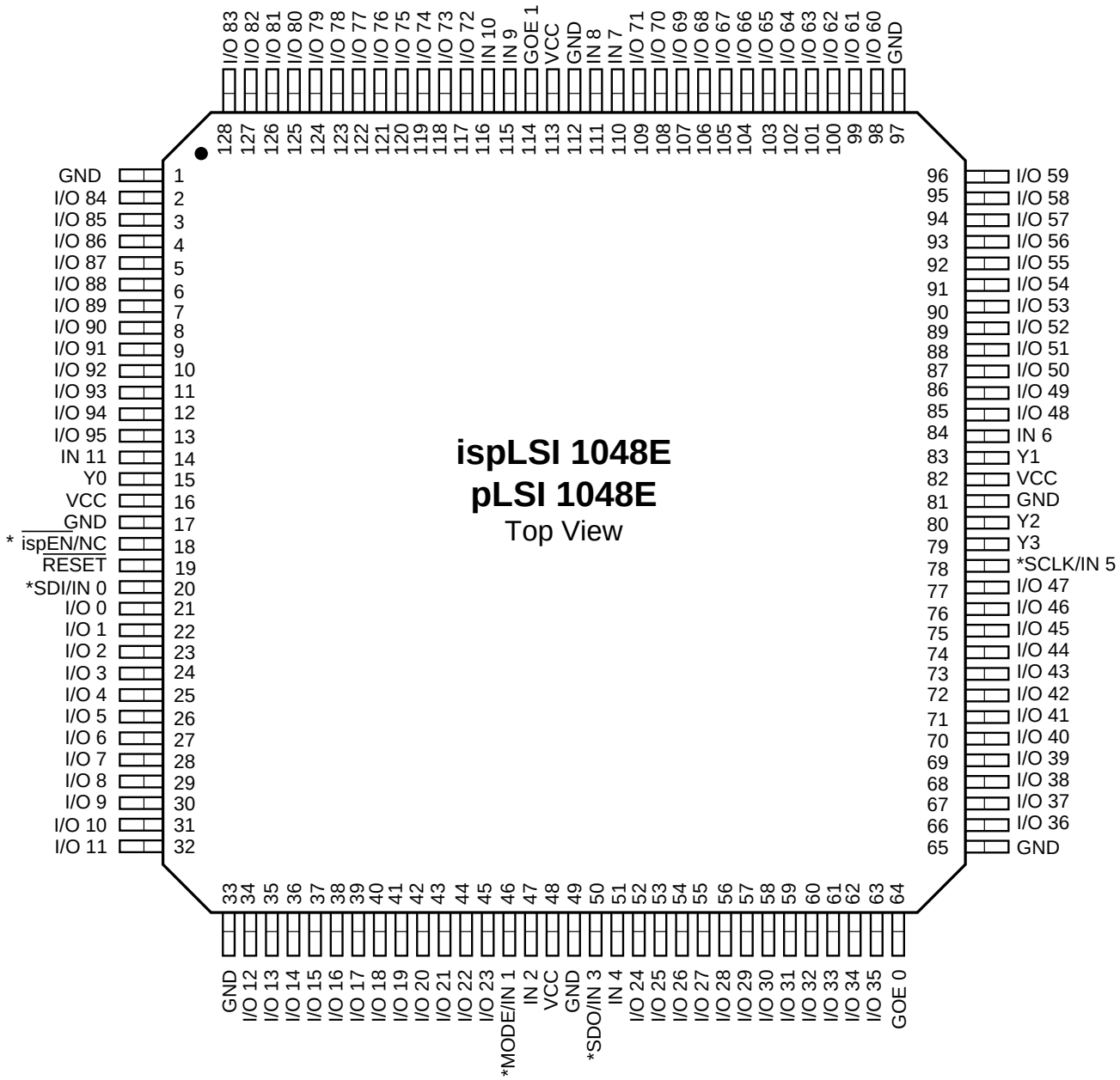
Table 2 - 0002C-48E

* ispLSI 1048E only

** $\overline{\text{ispEN}}$ for ispLSI 1048E, NC for pLSI 1048E, must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

Pin Configuration

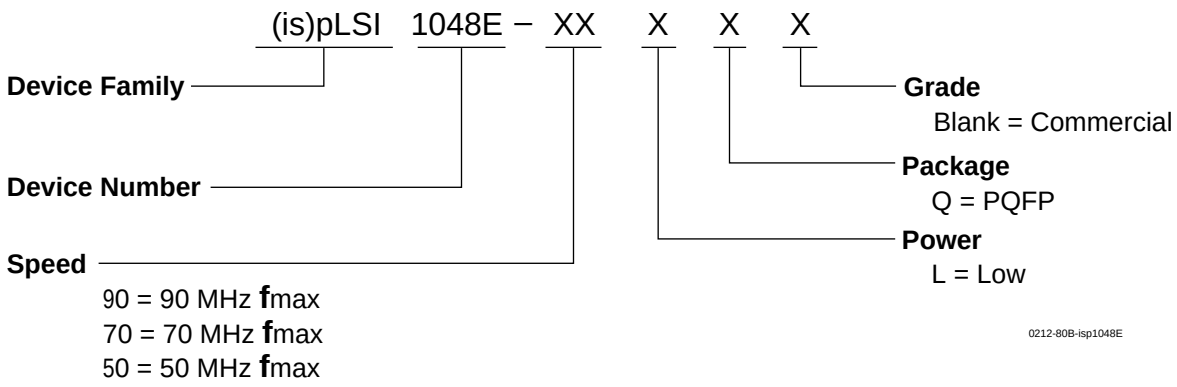
ispLSI and pLSI 1048E 128-Pin PQFP Pinout Diagram



*Pins have dual function capability for ispLSI 1048E only (except pin 18, which is $\overline{\text{ispEN}}$ only).

0124-48C

Part Number Description



ispLSI and pLSI 1048E Ordering Information

FAMILY	Fmax (MHz)	Tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	90	10	ispLSI 1048E-90LQ	128-Pin PQFP
	70	15	ispLSI 1048E-70LQ	128-Pin PQFP
	50	20	ispLSI 1048E-50LQ	128-Pin PQFP
pLSI	90	10	pLSI 1048E-90LQ	128-Pin PQFP
	70	15	pLSI 1048E-70LQ	128-Pin PQFP
	50	20	pLSI 1048E-50LQ	128-Pin PQFP

Table 2-0041-48-isp

ispLSI® and pLSI® 1048C

High-Density Programmable Logic

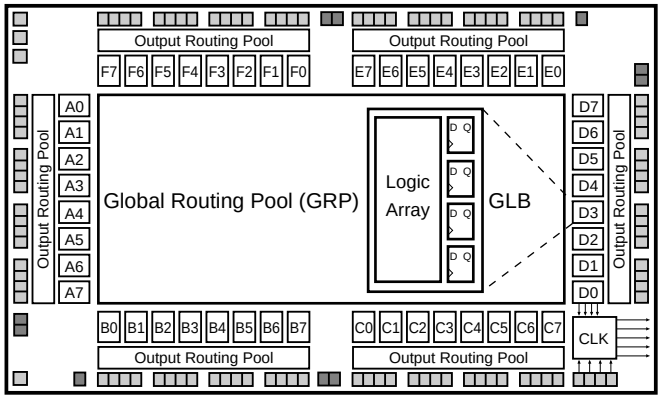
Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— 8000 PLD Gates**
  - **— 96 I/O Pins, 12 Dedicated Inputs, 2 Global Output Enables**
  - **— 288 Registers**
  - **— High-Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
  - **— Security Cell Prevents Unauthorized Copying**
- **HIGH PERFORMANCE E^2CMOS® TECHNOLOGY**
  - **— f_{max} = 70 MHz Maximum Operating Frequency**
  - **— f_{max} = 50 MHz for Industrial and Military/883 Devices**
  - **— t_{pd} = 16 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile E^2CMOS Technology**
  - **— 100% Tested at Time of Manufacture**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Four Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI AND pLSI DEVELOPMENT TOOLS**

  pDS® Software
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning**
  - **— Automatic Place and Route**
  - **— Static Timing Table**

  pDS+™ Software
  - **— Industry Standard, Third-Party Design Environments**
  - **— Schematic Capture, State Machine, VHDL, Verilog**
  - **— Automatic Partitioning and Place and Route**
  - **— Multi-Level Logic Synthesis**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

Functional Block Diagram



0139G1A-isp

Description

The ispLSI and pLSI 1048C are High-Density Programmable Logic Devices containing 288 Registers, 96 Universal I/O pins, 12 Dedicated Input pins, two Global Output Enables (GOE), four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1048C features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, and the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1048C device, but multiplexes four of the dedicated input pins to control in-system programming. Compared to the ispLSI and pLSI 1048, the ispLSI and pLSI 1048C offer two additional dedicated inputs and two new Global Output Enable pins.

The basic unit of logic on the ispLSI and pLSI 1048C devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. F7 in figure 1. There are a total of 48 GLBs in the ispLSI and pLSI 1048C devices. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

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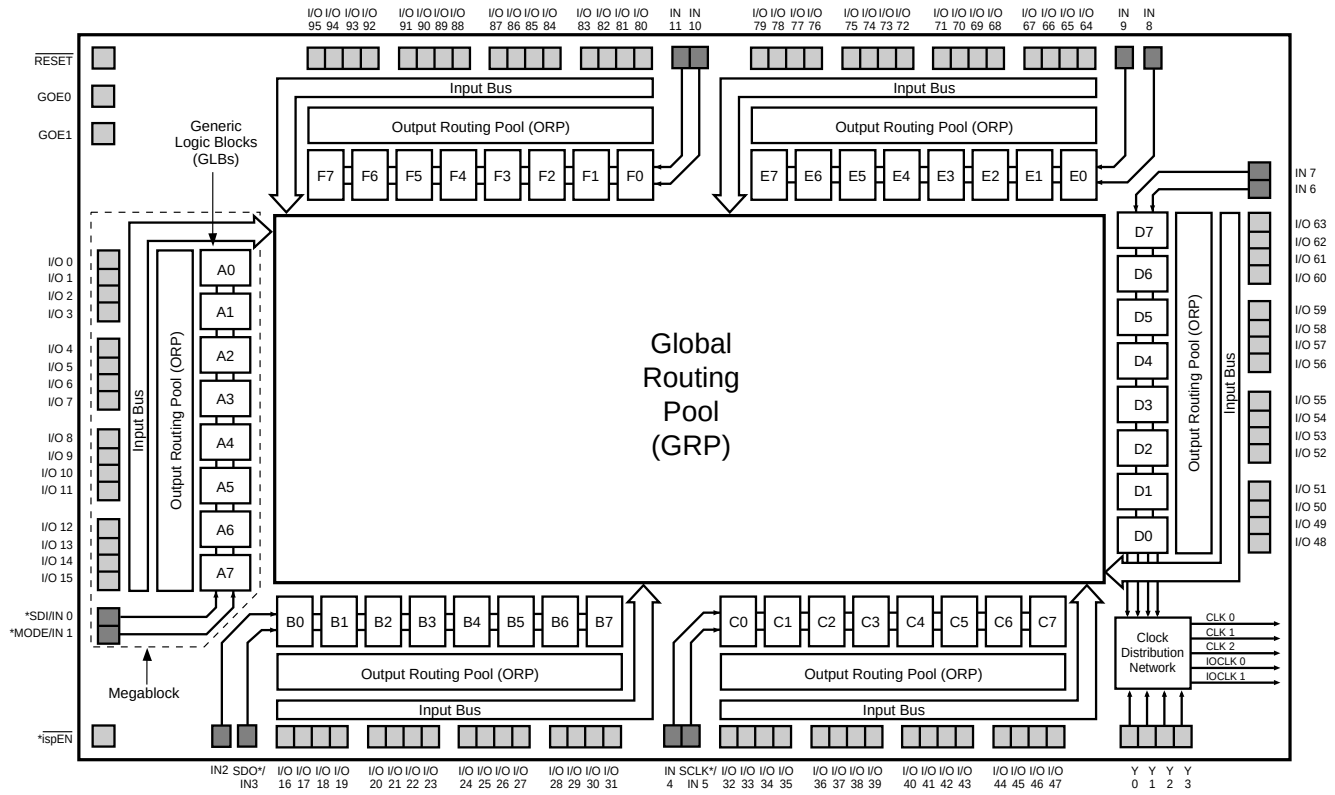
Functional Block Diagram

Figure 1. ispLSI and pLSI 1048C Functional Block Diagram



*ISP Control Functions for ispLSI 1048C Only

The devices also have 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs have selectable polarity, active high or active low. The signal voltage levels are TTL-compatible, and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock as shown in figure 1. The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The ispLSI and pLSI 1048C devices contain six of these Megablocks.

The GRP has, as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 1048C devices are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (D0 on the ispLSI and pLSI 1048C devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0˚C to +70˚C	4.75	5.25	V
		Industrial	T_A = -40˚C to +85˚C	4.5	5.5	
		Military/883	T_C = -55°C to +125°C	4.5	5.5	
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V

Table 2- 0005Aisp w/mil.eps

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER		MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	Commercial/Industrial	8	pf	V_{CC}=5.0V, V_{IN}=2.0V
		Military	10	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance		10	pf	V_{CC}=5.0V, $V_{I/O}$, V_Y=2.0V

1. Guaranteed but not 100% tested.

Table 2- 0006

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2- 0008B

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

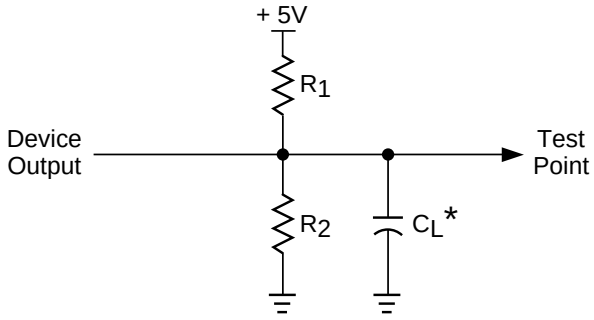
Table 2- 0003

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

Table 2- 0004A

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
I_{IL-isp}	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V	Commercial	–	165	235	mA
		f_{TOGGLE} = 1 MHz	Industrial/Military	–	165	260	mA

1. One output at a time for a maximum duration of one second. V_{out} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using twelve 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	16.0	–	22.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	19.0	–	26.0	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	70.4	–	50.3	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $(\frac{1}{tsu2 + tco1})$	47.6	–	34.5	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle $(\frac{1}{twh + twl})$	83.3	–	58.8	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	9.5	–	13.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	–	10.0	–	14.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	11.0	–	15.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	11.5	–	16.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	15.0	–	20.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10.0	–	13.5	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	20.0	–	27.5	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	20.0	–	27.5	ns
t_{goeen}	B	16	Global OE Output Enable	–	15.0	–	20.5	ns
t_{goedis}	C	17	Global OE Output Disable	–	15.0	–	20.5	ns
t_{wh}	–	20	Ext. Sync. Clock Pulse Duration, High	6.0	–	8.5	–	ns
t_{wl}	–	21	Ext. Sync. Clock Pulse Duration, Low	6.0	–	8.5	–	ns
t_{su3}	–	22	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2.0	–	3.0	–	ns
t_{h3}	–	23	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	–	9.0	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{iobp}	24	I/O Register Bypass	–	3.1	–	4.3	ns
t_{iolat}	25	I/O Latch Delay	–	4.0	–	5.5	ns
t_{iosu}	26	I/O Register Setup Time before Clock	6.5	–	9.1	–	ns
t_{ioh}	27	I/O Register Hold Time after Clock	0.1	–	0.3	–	ns
t_{ioco}	28	I/O Register Clock to Out Delay	–	3.4	–	4.6	ns
t_{ior}	29	I/O Register Reset to Out Delay	–	3.7	–	5.1	ns
t_{din}	30	Dedicated Input Delay	–	5.4	–	7.4	ns
GRP							
t_{grp1}	31	GRP Delay, 1 GLB Load	–	4.5	–	6.2	ns
t_{grp4}	32	GRP Delay, 4 GLB Loads	–	4.9	–	6.7	ns
t_{grp8}	33	GRP Delay, 8 GLB Loads	–	5.8	–	8.0	ns
t_{grp16}	34	GRP Delay, 16 GLB Loads	–	7.6	–	10.5	ns
t_{grp48}	35	GRP Delay, 48 GLB Loads	–	16.5	–	22.7	ns
GLB							
t_{4ptbp}	36	4 Product Term Bypass Path Delay	–	4.0	–	5.5	ns
t_{1ptxor}	37	1 Product Term/XOR Path Delay	–	4.9	–	6.7	ns
$t_{20ptxor}$	38	20 Product Term/XOR Path Delay	–	5.5	–	7.5	ns
t_{xoradj}	39	XOR Adjacent Path Delay[3]	–	6.5	–	8.9	ns
t_{gbp}	40	GLB Register Bypass Delay	–	0.9	–	1.2	ns
t_{gsu}	41	GLB Register Setup Time before Clock	2.9	–	3.9	–	ns
t_{gh}	42	GLB Register Hold Time after Clock	5.3	–	7.3	–	ns
t_{gco}	43	GLB Register Clock to Output Delay	–	1.5	–	2.3	ns
t_{gro}	44	GLB Register Reset to Output Delay	–	2.1	–	2.8	ns
t_{ptre}	45	GLB Product Term Reset to Register Delay	–	8.1	–	11.1	ns
t_{ptoe}	46	GLB Product Term Output Enable to I/O Cell Delay	–	7.0	–	9.6	ns
t_{ptck}	47	GLB Product Term Clock Delay	2.5	6.0	3.4	8.2	ns
ORP							
t_{orp}	48	ORP Delay	–	2.5	–	3.4	ns
t_{orpbp}	49	ORP Bypass Delay	–	1.0	–	1.4	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

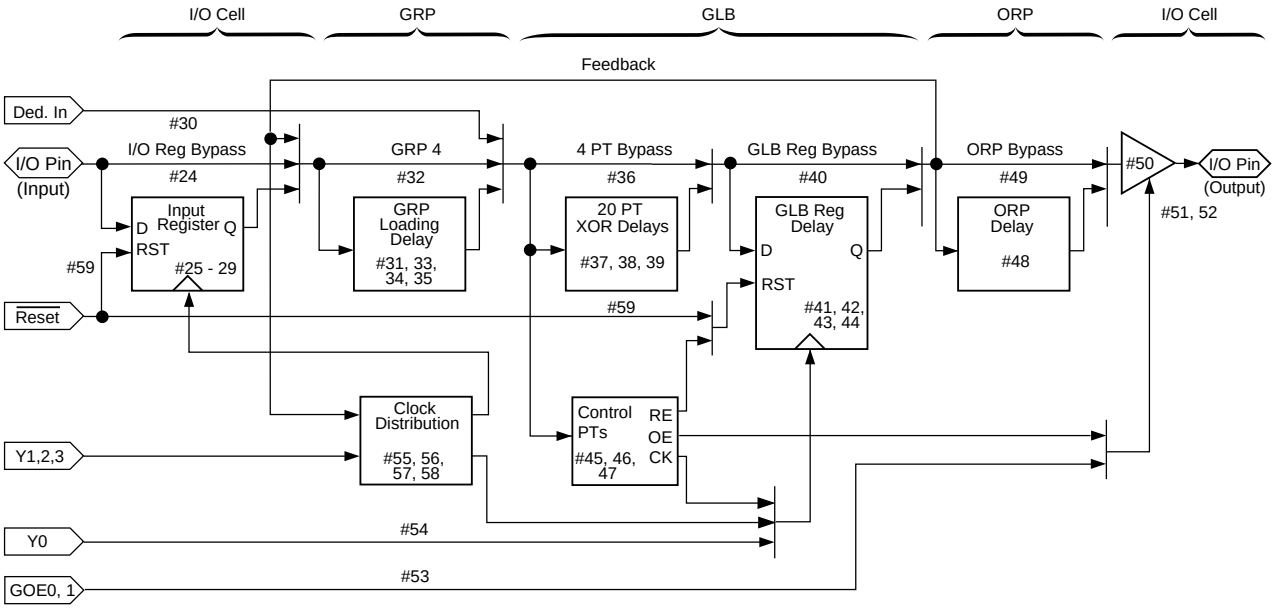
Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	50	Output Buffer Delay	–	2.1	–	2.9	ns
t_{oen}	51	I/O Cell OE to Output Enabled	–	5.0	–	6.9	ns
t_{odis}	52	I/O Cell OE to Output Disabled	–	5.0	–	6.9	ns
t_{goe}	53	Global OE	–	10.0	–	13.6	ns
Clocks							
t_{gy0}	54	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	5.4	5.4	7.4	7.4	ns
$t_{gy1/2}$	55	Clock Delay, Y1 or Y2 to Global GLB Clock Line	4.5	6.4	6.1	8.7	ns
t_{gcp}	56	Clock Delay, Clock GLB to Global GLB Clock Line	1.9	5.5	2.6	7.6	ns
$t_{ioy2/3}$	57	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	4.5	6.4	6.1	8.7	ns
t_{iocp}	58	Clock Delay, Clock GLB to I/O Cell Global Clock Line	1.9	5.5	2.6	7.6	ns
Global Reset							
t_{gr}	59	Global Reset to GLB and I/O Registers	–	8.3	–	11.4	ns

1. Internal Timing Parameters are not tested and are for reference only.

Table 2- 0037-48C/70, 50

ispLSI and pLSI 1048C Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (tiobp + tgrp4 + t20ptxor) + (tgsu) - (tiobp + tgrp4 + tptck(min))
= (#24 + #32 + #38) + (#41) - (#24 + #32 + #47)
5.9 ns = (3.1 + 4.9 + 5.5) + (2.9) - (3.1 + 4.9 + 2.5)

th = Clock (max) + Reg h - Logic
= (tiobp + tgrp4 + tptck(max)) + (tgh) - (tiobp + tgrp4 + t20ptxor)
= (#24 + #32 + #47) + (#42) - (#24 + #32 + #38)
5.8 ns = (3.1 + 4.9 + 6.0) + (5.3) - (3.1 + 4.9 + 5.5)

tco = Clock (max) + Reg co + Output
= (tiobp + tgrp4 + tptck(max)) + (tgco) + (torp + tob)
= (#24 + #32 + #47) + (#43) + (#48 + #50)
20.1 ns = (3.1 + 4.9 +6.0) + (1.5) + (2.5 + 2.1)

Derivations of tsu, th and tco from the Clock GLB[1]

tsu = Logic + Reg su - Clock (min)
= (tiobp + tgrp4 + t20ptxor) + (tgsu) - (tgy0(min) + tgco + tgcp(min))
= (#24 + #32 + #38) + (#41) - (#54 + #43 + #56)
7.6 ns = (3.1 + 4.9 + 5.5) + (2.9) - (5.4 + 1.5 + 1.9)

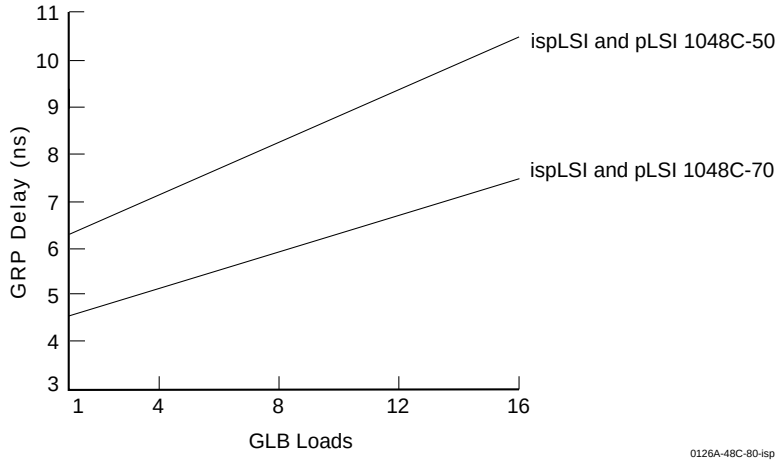
th = Clock (max) + Reg h - Logic
= (tgy0(max) + tgco + tgcp(max)) + (tgh) - (tiobp + tgrp4 + t20ptxor)
= (#54 + #43 + #56) + (#42) - (#24 + #32 + #38)
4.2 ns = (5.4 + 1.5 + 5.5) + (5.3) - (3.1 + 4.9 + 5.5)

tco = Clock (max) + Reg co + Output
= (tgy0(max) + tgco + tgcp(max)) + (tgco) + (torp + tob)
= (#54 + #43 + #56) + (#43) + (#48 + #50)
18.5 ns = (5.4 + 1.5 + 5.5) + (1.5) + (2.5 + 2.1)

1. Calculations are based upon timing specifications for the ispLSI and pLSI 1048C-70

Table 2- 0042-48C

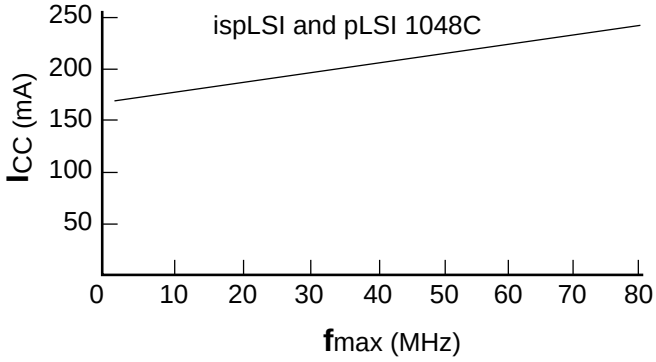
Maximum GRP Delay vs GLB Loads



Power Consumption

Power consumption in the ispLSI and pLSI 1048C device depends on two primary factors: the speed at which the device is operating, and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of Twelve 16-bit Counters
Typical Current at 5V, 25˚C

I_{CC} can be estimated for the ispLSI and pLSI 1048C using the following equation:

I_{CC} = 73 + (# of PTs * 0.23) + (# of nets * Max. freq * 0.010) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A-48C-80-isp

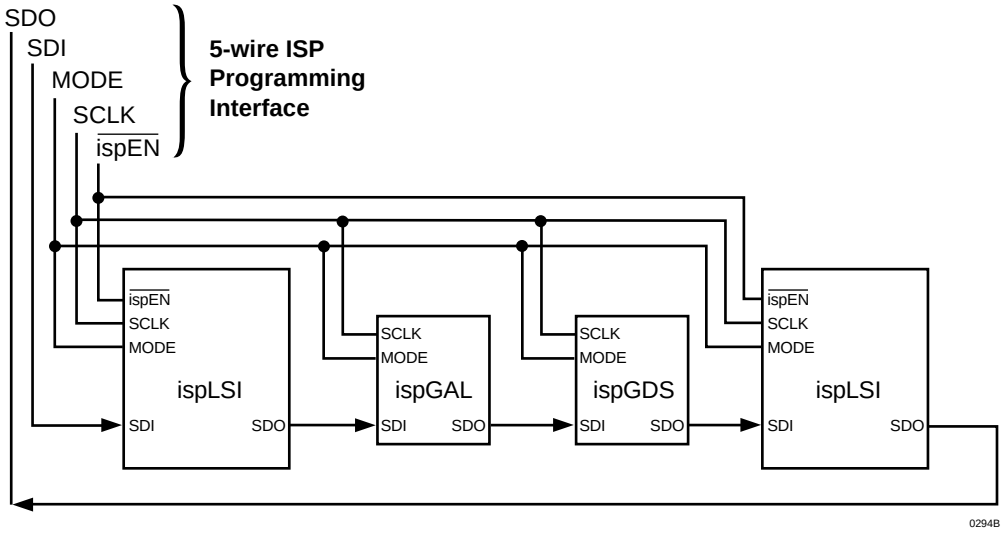
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

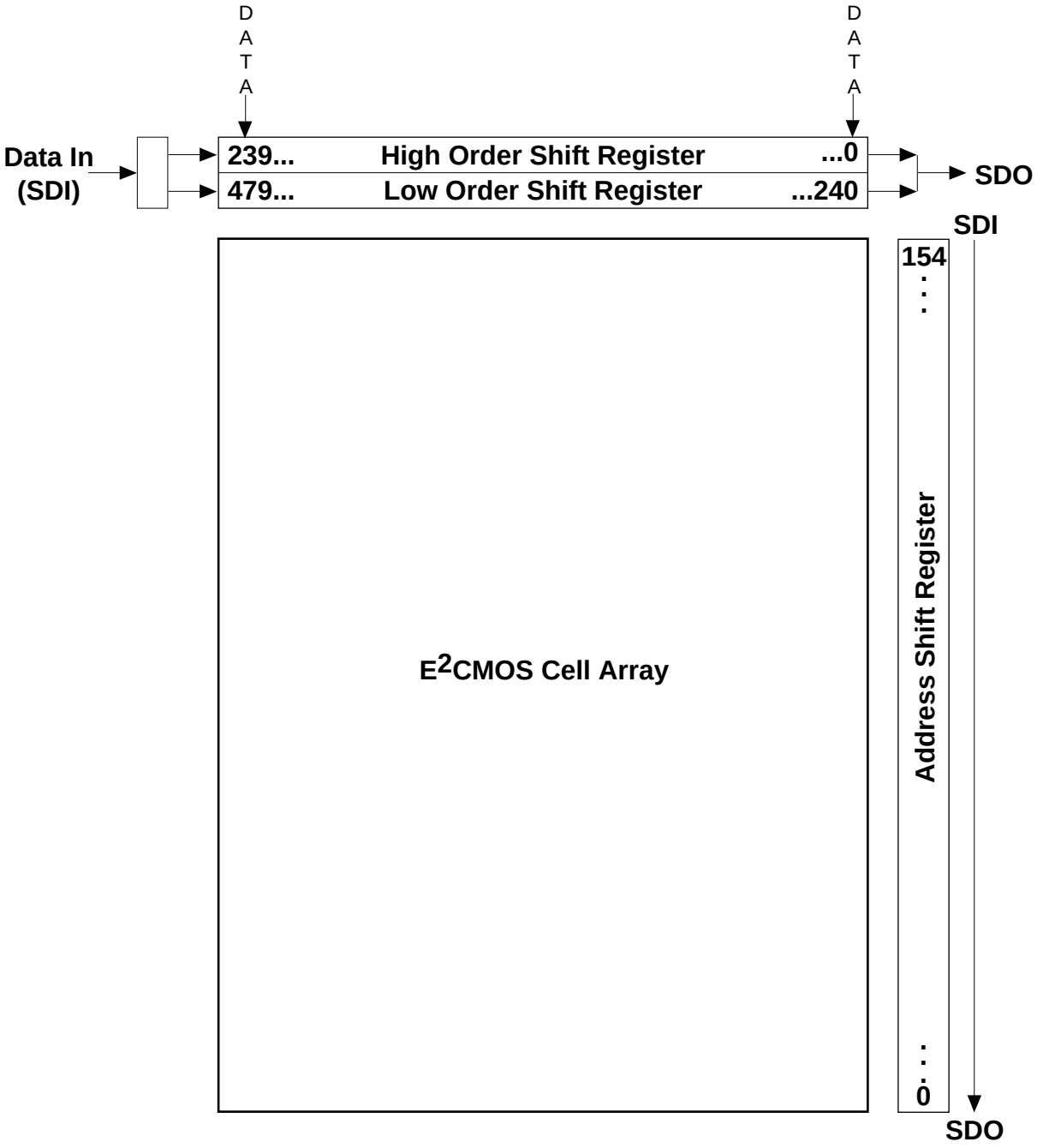
All necessary programming is done via five TTL-level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates one possible ispLSI device programming scheme. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section in this Data Book.

The device identifier for the ispLSI 1048C is 0000 0101 (05 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 1048C Shift Register Layout



Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

Pin Description

NAME	PQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	21, 22, 23, 24, 25, 26 27, 28, 29, 30, 31, 32 34, 35, 36, 37, 38, 39 40, 41, 42, 43, 44, 45 52, 53, 54, 55, 56, 57 58, 59, 60, 61, 62, 63 66, 67, 68, 69, 70, 71 72, 73, 74, 75, 76, 77 85, 86, 87, 88, 89, 90 91, 92, 93, 94, 95, 96 98, 99,100,101,102, 103 104,105,106,107,108, 109 117,118,119,120,121, 122 123,124,125,126,127, 128 2, 3, 4, 5, 6, 7 8, 9, 10, 11, 12, 13	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0, GOE1	64, 114	Global output enables for all I/Os.
IN 2, IN 4 IN 6 - IN 11	47, 51 84,110,111, 115,116, 14	Dedicated input pins to the device.
$\overline{\text{ispEN}}$*/NC	18	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	20	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE*/IN 1	46	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO*/IN 3	50	Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK*/IN 5	78	Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When ispEN is logic low, it functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	19	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	15	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	83	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	80	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	79	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	1, 17, 33, 49, 65, 81 97, 112	Ground (GND)
VCC	16, 48, 82, 113	V_{CC}

*For ispLSI 1048C Only

Table 2- 0002C-48C

Pin Description

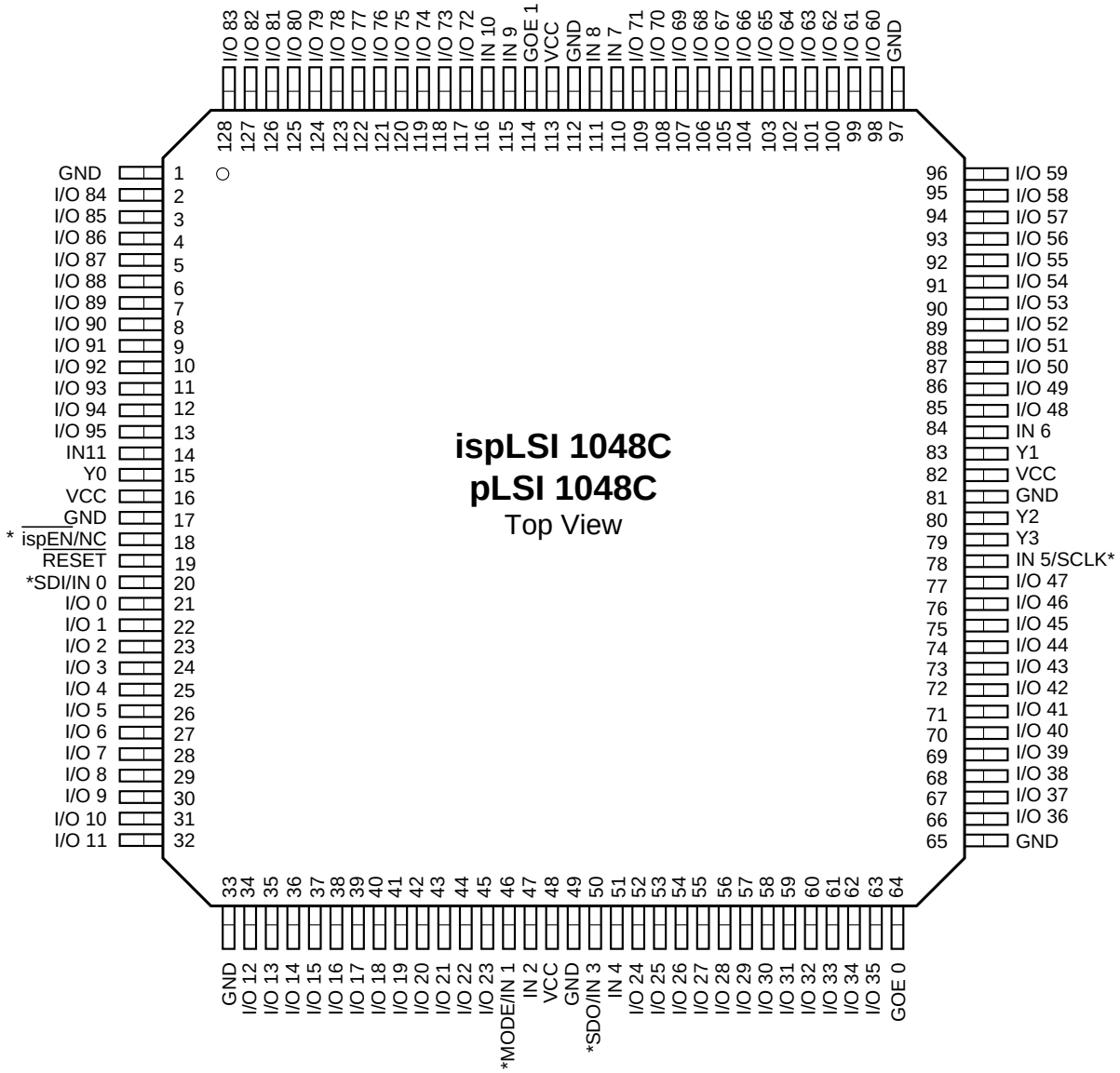
NAME	CPGA PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	J2, J3, K1, L1, K2, M1, L2, K3, N1, M2, L3, P1, M3, P2, N3, M4, P3, N4, P4, M5, N5, P5, M6, N6, N9, M9, P10, P11, N10, P12, N11, M10, P13, N12, M11, P14, M12, N14, M13, L12, M14, L13, L14, K12, K13, K14, J12, J13, F13, F12, E14, D14, E13, C14, D13, E12, B14, C13, D12, A14, C12, A13, B12, C11, A12, B11, A11, C10, B10, A10, C9, B9, B6, C6, A5, A4, B5, A3, B4, C5, A2, B3, C4, A1, C3, B1, C2, D3, C1, D2, D1, E3, E2, E1, F3, F2	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0, GOE1	N13, B7,	Global output enables for all I/Os.
IN 2, IN 4 IN 6 - IN 11	P7, P9 F14, A9, A8, A7, A6, F1	Dedicated input pins to the device.
$\overline{\text{ispEN}}$*/NC	H2	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	J1	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE*/IN 1	P6	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO*/IN 3	P8	Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK*/IN 5	J14	Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	H1	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	G1	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	G14	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	H13	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	H14	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	B2, B8, B13, C8, H3, H12, M8, N2, N8	Ground (GND)
VCC	C7, G2, G3, G12, G13, M7, N7	V_{CC}

Table 2- 0002C-48C/CPGA

*For ispLSI 1048C Only

Pin Configuration

ispLSI and pLSI 1048C 128-Pin PQFP Pinout Diagram

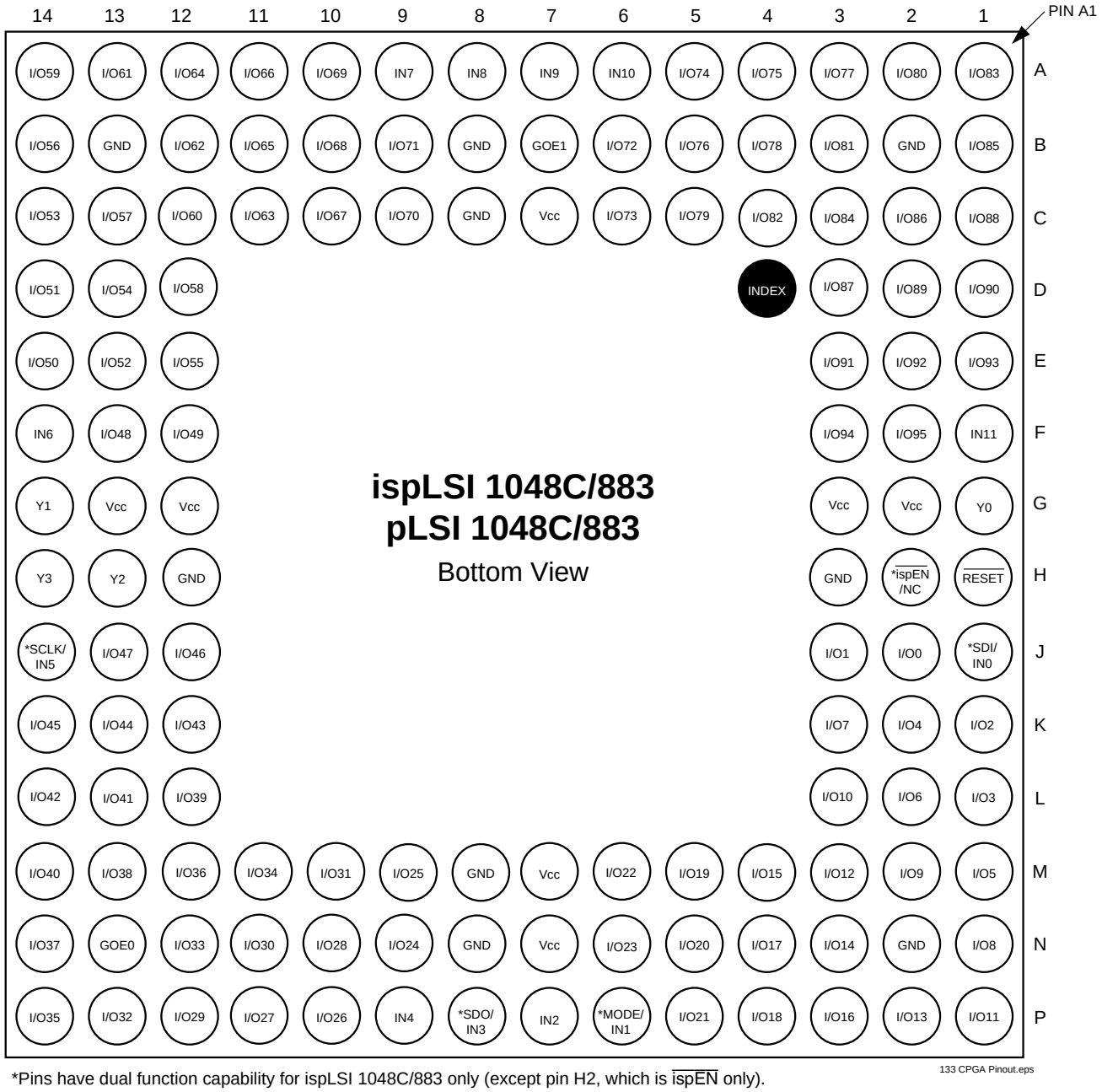


*Pins have dual function capability for ispLSI 1048C only (except pin 18, which is $\overline{\text{ispEN}}$ only).

0124-48C

Pin Configuration

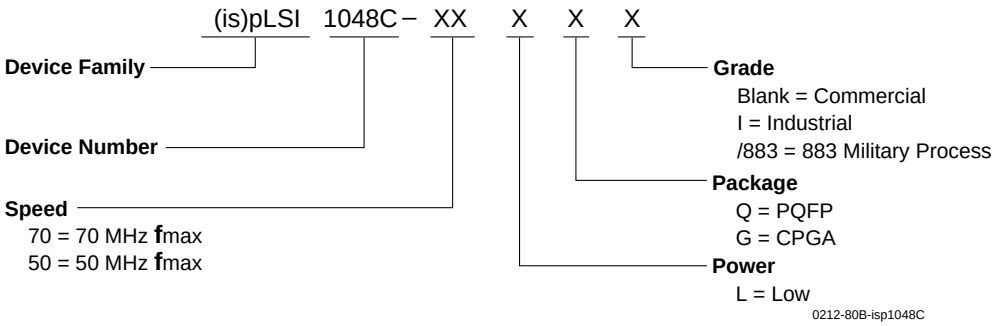
ispLSI and pLSI 1048C 133-Pin CPGA Pinout Diagram



133 CPGA Pinout.eps

*Pins have dual function capability for ispLSI 1048C/883 only (except pin H2, which is $\overline{\text{ispEN}}$ only).

Part Number Description



ispLSI and pLSI 1048C Ordering Information

COMMERCIAL

Family	fmax (MHz)	tpd (ns)	Ordering Number	Package
ispLSI	70	16	ispLSI 1048C-70LQ	128-Pin PQFP
	50	22	ispLSI 1048C-50LQ	128-Pin PQFP
pLSI	70	16	pLSI 1048C-70LQ	128-Pin PQFP
	50	22	pLSI 1048C-50LQ	128-Pin PQFP

INDUSTRIAL

Family	fmax (MHz)	tpd (ns)	Ordering Number	Package
ispLSI	50	22	ispLSI 1048C-50LQI	128-Pin PQFP
pLSI	50	22	pLSI 1048C-50LQI	128-Pin PQFP

MILITARY

Family	fmax (MHz)	tpd (ns)	Ordering Number	SMD Number	Package
ispLSI	50	22	ispLSI 1048C-50LG/883	5962-9558701MXC*	133-Pin CPGA
pLSI	50	22	pLSI 1048C-50LG/883	5962-9558801MXC*	133-Pin CPGA

*Preliminary

Table 2- 0041A-48C-isp

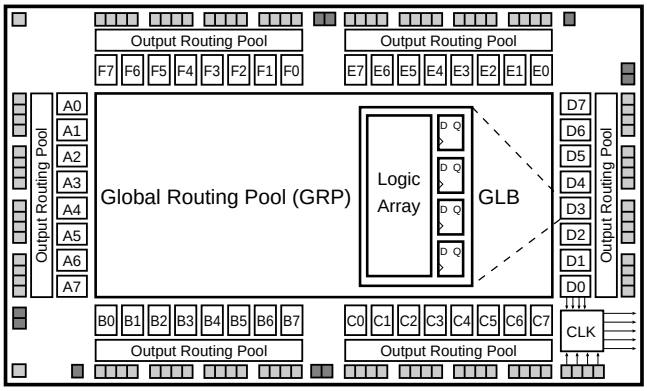
ispLSI® and pLSI® 1048

High-Density Programmable Logic

Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— 8000 PLD Gates**
  - **— 96 I/O Pins, Ten Dedicated Inputs**
  - **— 288 Registers**
  - **— High-Speed Global Interconnects**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
  - **— Security Cell Prevents Unauthorized Copying**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 80 MHz Maximum Operating Frequency**
  - **— f_{max} = 50 MHz for Industrial Devices**
  - **— t_{pd} = 15 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile E²CMOS Technology**
  - **— 100% Tested**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Four Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI AND pLSI DEVELOPMENT TOOLS**
  - **pDS® Software**
    - **— Easy to Use PC Windows™ Interface**
    - **— Boolean Logic Compiler**
    - **— Manual Partitioning**
    - **— Automatic Place and Route**
    - **— Static Timing Table**
  - **pDS+™ Software**
    - **— Industry Standard, Third Party Design Environments**
    - **— Schematic Capture, State Machine, HDL**
    - **— Automatic Partitioning and Place and Route**
    - **— Comprehensive Logic and Timing Simulation**
    - **— PC and Workstation Platforms**

Functional Block Diagram



Description

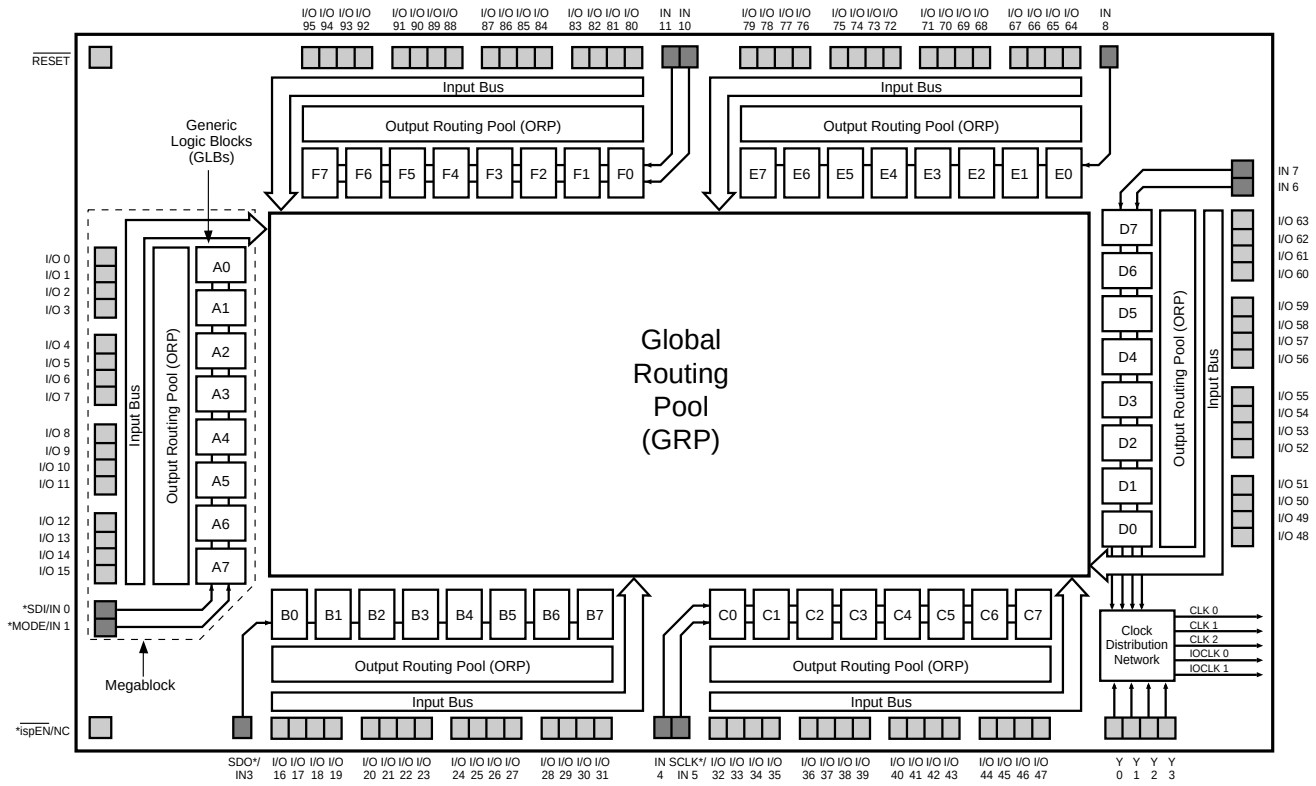
The ispLSI and pLSI 1048 are High-Density Programmable Logic Devices which contain 288 Registers, 96 Universal I/O pins, ten Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1048 features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1048 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the ispLSI and pLSI 1048 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. F7 (see figure 1). There are a total of 48 GLBs in the ispLSI and pLSI 1048 devices. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Functional Block Diagram

Figure 1. ispLSI and pLSI 1048 Functional Block Diagram



*ISP Control Functions for ispLSI 1048 Only

The devices also have 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. Additionally, all outputs are polarity selectable, active high or active low. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Eight GLBs, 16 I/O cells, two dedicated inputs (one dedicated input in Megablock B and E) and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The ispLSI and pLSI 1048 devices contain six of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 1048 devices are selected using the Clock Distribution Network. Four dedicated clockpins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (D0 on the ispLSI and pLSI 1048 devices). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial T_A = 0°C to +70°C	4.75	5.25	V
		Industrial T_A = -40°C to +85°C	4.5	5.5	
V_{IL}	Input Low Voltage		0	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 1	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O and Clock Capacitance	10	pf	V_{CC}=5.0V, $V_{I/O}$, V_Y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2- 0008B

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

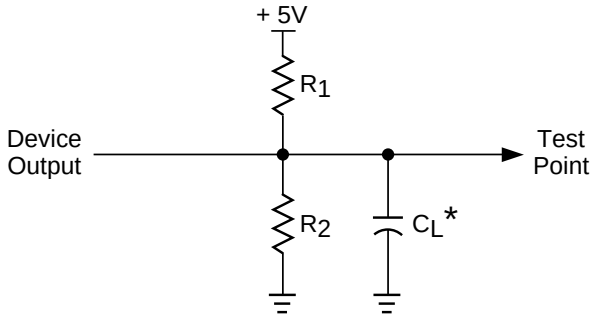
3-state levels are measured 0.5V from steady-state active level.

Table 2- 0003

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
I_{IL-isp}	isp Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V	Commercial	–	165	235	mA
		f_{TOGGLE} = 1 MHz	Industrial	–	165	260	mA

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using twelve 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[5]	#[2]	DESCRIPTION[1]	-80		-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	15	–	18	–	24	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	20	–	23	–	30.7	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	80	–	71.4	–	53.6	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	50	–	41.7	–	31.3	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max Toggle[4]	100	–	83	–	71.4	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4PT bypass	7	–	9	–	12	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP bypass	–	10	–	12	–	16	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass	0	–	0	–	0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	10	–	12	–	16	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	12	–	14	–	18.7	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0	–	0	–	0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	17	–	17	–	22.7	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10	–	10	–	13	–	ns
t_{en}	B	14	Input to Output Enable	–	18	–	20	–	26.7	ns
t_{dis}	C	15	Input to Output Disable	–	18	–	20	–	26.7	ns
t_{wh}	–	16	Ext. Sync. Clock Pulse Duration, High	5	–	6	–	7	–	ns
t_{wl}	–	17	Ext. Sync. Clock Pulse Duration, Low	5	–	6	–	7	–	ns
t_{su5}	–	18	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)	2	–	2	–	2.7	–	ns
t_{h5}	–	19	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	6.5	–	6.5	–	8.7	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit loadable counter using GRP feedback.
4. **f**max (Toggle) may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-80		-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
tiobp	20	I/O Register Bypass	–	2.5	–	3.0	–	4.0	ns
tiolat	21	I/O Latch Delay	–	3.3	–	4.0	–	5.3	ns
tiosu	22	I/O Register Setup Time before Clock	5.3	–	6.0	–	8.1	–	ns
tioh	23	I/O Register Hold Time after Clock	1.5	–	0.5	–	0.9	–	ns
tioco	24	I/O Register Clock to Out Delay	–	2.5	–	3.0	–	3.9	ns
tior	25	I/O Register Reset to Out Delay	–	2.9	–	3.5	–	4.6	ns
tdin	26	Dedicated Input Delay	–	5.0	–	6.0	–	8.0	ns
GRP									
tgrp1	27	GRP Delay, 1 GLB Load	–	2.1	–	2.5	–	3.3	ns
tgrp4	28	GRP Delay, 4 GLB Loads	–	2.5	–	3.0	–	4.0	ns
tgrp8	29	GRP Delay, 8 GLB Loads	–	3.3	–	4.0	–	5.3	ns
tgrp12	30	GRP Delay, 12 GLB Loads	–	4.2	–	5.0	–	6.7	ns
tgrp16	31	GRP Delay, 16 GLB Loads	–	5.0	–	6.0	–	8.0	ns
tgrp48	32	GRP Delay, 48 GLB Loads	–	13.3	–	16.0	–	21.3	ns
GLB									
t4ptbp	33	4 Product Term Bypass Path Delay	–	5.4	–	6.5	–	8.6	ns
t1ptxor	34	1 Product Term/XOR Path Delay	–	6.5	–	7.0	–	9.3	ns
t20ptxor	35	20 Product Term/XOR Path Delay	–	7.6	–	7.5	–	10.0	ns
txoradj	36	XOR Adjacent Path Delay[3]	–	8.4	–	9.5	–	12.7	ns
tgbp	37	GLB Register Bypass Delay	–	0.8	–	1.0	–	1.3	ns
tgsu	38	GLB Register Setup Time before Clock	0.8	–	1.5	–	2.0	–	ns
tgh	39	GLB Register Hold Time after Clock	5.0	–	6.0	–	8.0	–	ns
tgco	40	GLB Register Clock to Output Delay	–	2.1	–	2.5	–	3.3	ns
tgr	41	GLB Register Reset to Output Delay	–	2.1	–	2.5	–	3.3	ns
tptre	42	GLB Product Term Reset to Register Delay	–	8.3	–	10.0	–	13.3	ns
tptoe	43	GLB Product Term Output Enable to I/O Cell Delay	–	8.8	–	9.0	–	11.9	ns
tptck	44	GLB Product Term Clock Delay	2.9	6.3	3.5	7.5	4.6	9.9	ns
ORP									
torp	45	ORP Delay	–	3.2	–	3.5	–	4.7	ns
torpbp	46	ORP Bypass Delay	–	1.3	–	1.5	–	2.0	ns

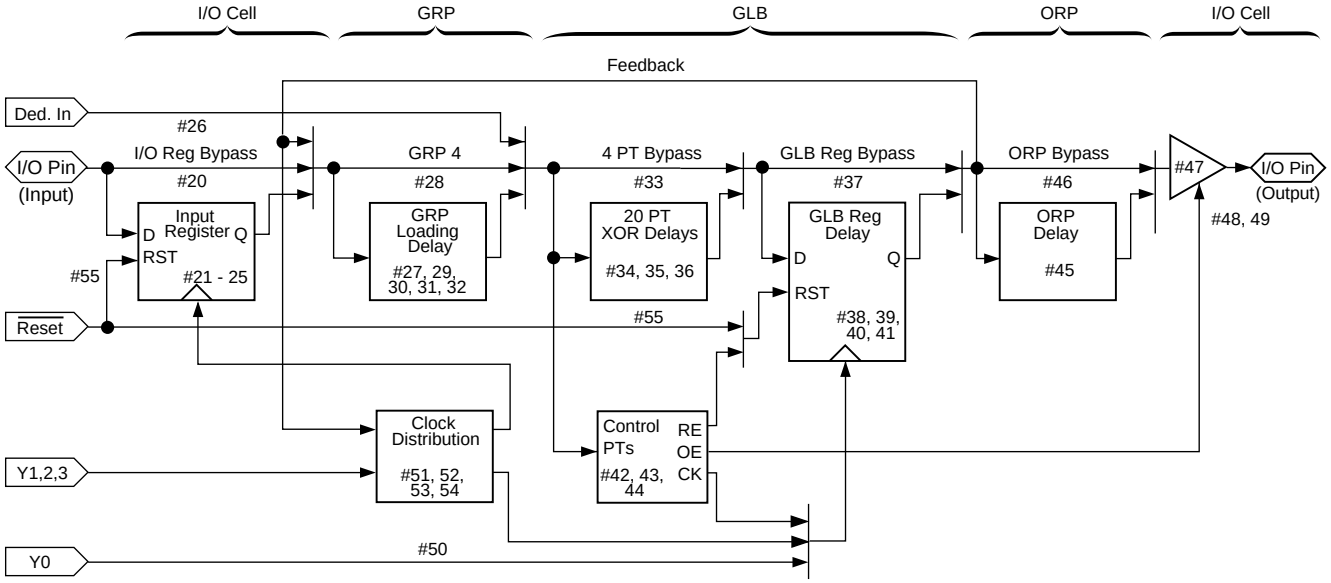
1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters[1]

PARAMETER	#[2]	DESCRIPTION	-80		-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Outputs									
t_{ob}	47	Output Buffer Delay	–	2.5	–	3.0	–	4.0	ns
t_{oen}	48	I/O Cell OE to Output Enabled	–	4.2	–	5.0	–	6.7	ns
t_{odis}	49	I/O Cell OE to Output Disabled	–	4.2	–	5.0	–	6.7	ns
Clocks									
t_{gy0}	50	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	4.2	4.2	5.0	5.0	6.7	6.7	ns
$t_{gy1/2}$	51	Clock Delay, Y1 or Y2 to Global GLB Clock Line	3.3	5.0	4.0	6.0	5.3	8.0	ns
t_{gcp}	52	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	4.2	1.0	5.0	1.3	6.6	ns
$t_{ioy2/3}$	53	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	3.3	5.0	4.0	6.0	5.3	8.0	ns
t_{iocp}	54	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	4.2	1.0	5.0	1.3	6.6	ns
Global Reset									
t_{gr}	55	Global Reset to GLB and I/O Registers	–	9.2	–	8.0	–	10.6	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI and pLSI 1048 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

t_{su} = Logic + Reg su - Clock (min)
= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)})$
= $(\#20 + \#28 + \#35) + (\#38) - (\#20 + \#28 + \#44)$
5.5 ns = (3.0 + 3.0 + 7.5) + (1.5) - (3.0 + 3.0 + 3.5)

t_{h} = Clock (max) + Reg h - Logic
= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
= $(\#20 + \#28 + \#44) + (\#39) - (\#20 + \#28 + \#35)$
6.0 ns = (3.0 + 3.0 + 7.5) + (6.0) - (3.0 + 3.0 + 7.5)

t_{co} = Clock (max) + Reg co + Output
= $(t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$
= $(\#20 + \#28 + \#44) + (\#40) + (\#45 + \#47)$
22.5 ns = (3.0 + 3.0 +7.5) + (2.5) + (3.5 + 3.0)

Derivations of tsu, th and tco from the Clock GLB[1]

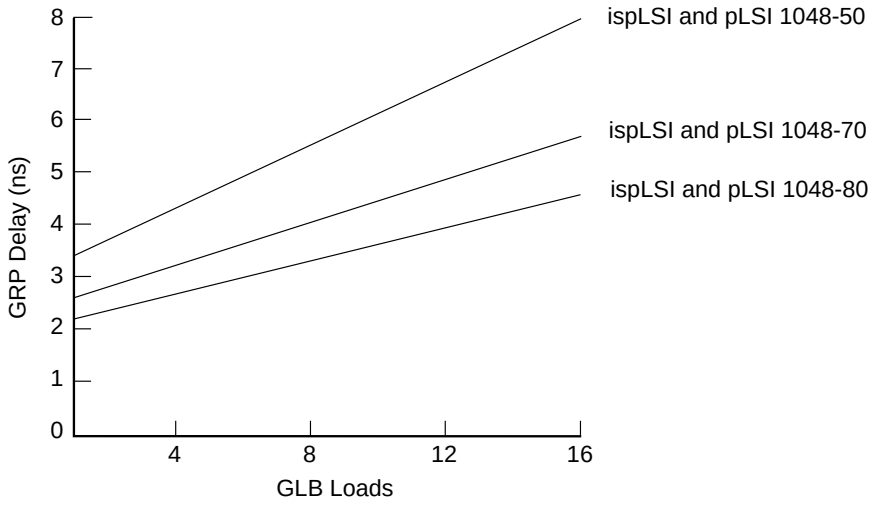
t_{su} = Logic + Reg su - Clock (min)
= $(t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)})$
= $(\#20 + \#28 + \#35) + (\#38) - (\#50 + \#40 + \#52)$
6.5 ns = (3.0 + 3.0 + 7.5) + (1.5) - (5.0 + 2.5 + 1.0)

t_{h} = Clock (max) + Reg h - Logic
= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor})$
= $(\#50 + \#40 + \#52) + (\#39) - (\#20 + \#28 + \#35)$
5.0 ns = (5.0 + 2.5 + 5.0) + (6.0) - (3.0 + 3.0 + 7.5)

t_{co} = Clock (max) + Reg co + Output
= $(t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob})$
= $(\#50 + \#40 + \#52) + (\#40) + (\#45 + \#47)$
21.5 ns = (5.0 + 2.5 + 5.0) + (2.5) + (3.5 + 3.0)

1. Calculations are based upon timing specifications for the ispLSI and pLSI 1048-70.

Maximum GRP Delay vs GLB Loads

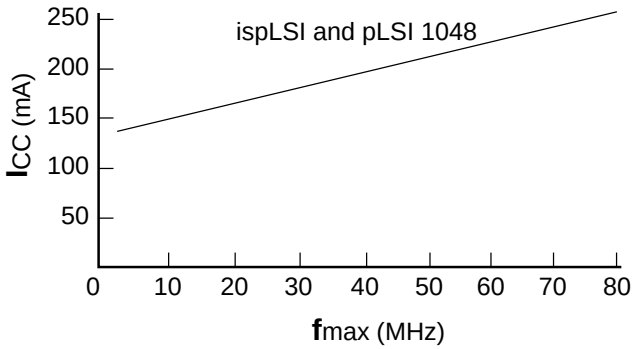


0126A-48-80-isp

Power Consumption

Power consumption in the ispLSI and pLSI 1048 device depends on two primary factors: the speed at which the device is operating, and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of Twelve 16-bit Counters
Typical Current at 5V, 25°C

I_{CC} can be estimated for the ispLSI and pLSI 1048 using the following equation:

I_{CC} = 73 + (# of PTs * 0.23) + (# of nets * Max. freq * 0.010) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A-48-80-isp

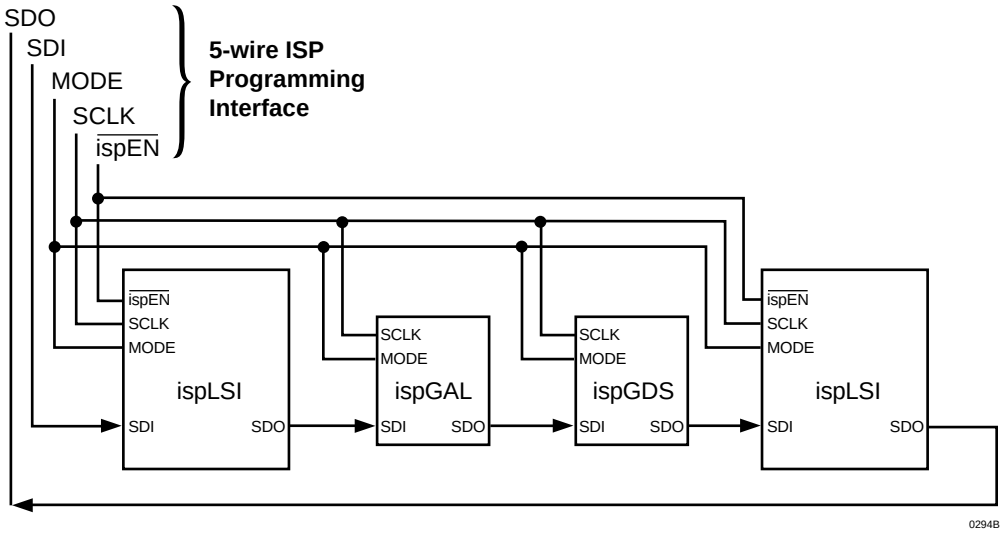
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor High-Density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

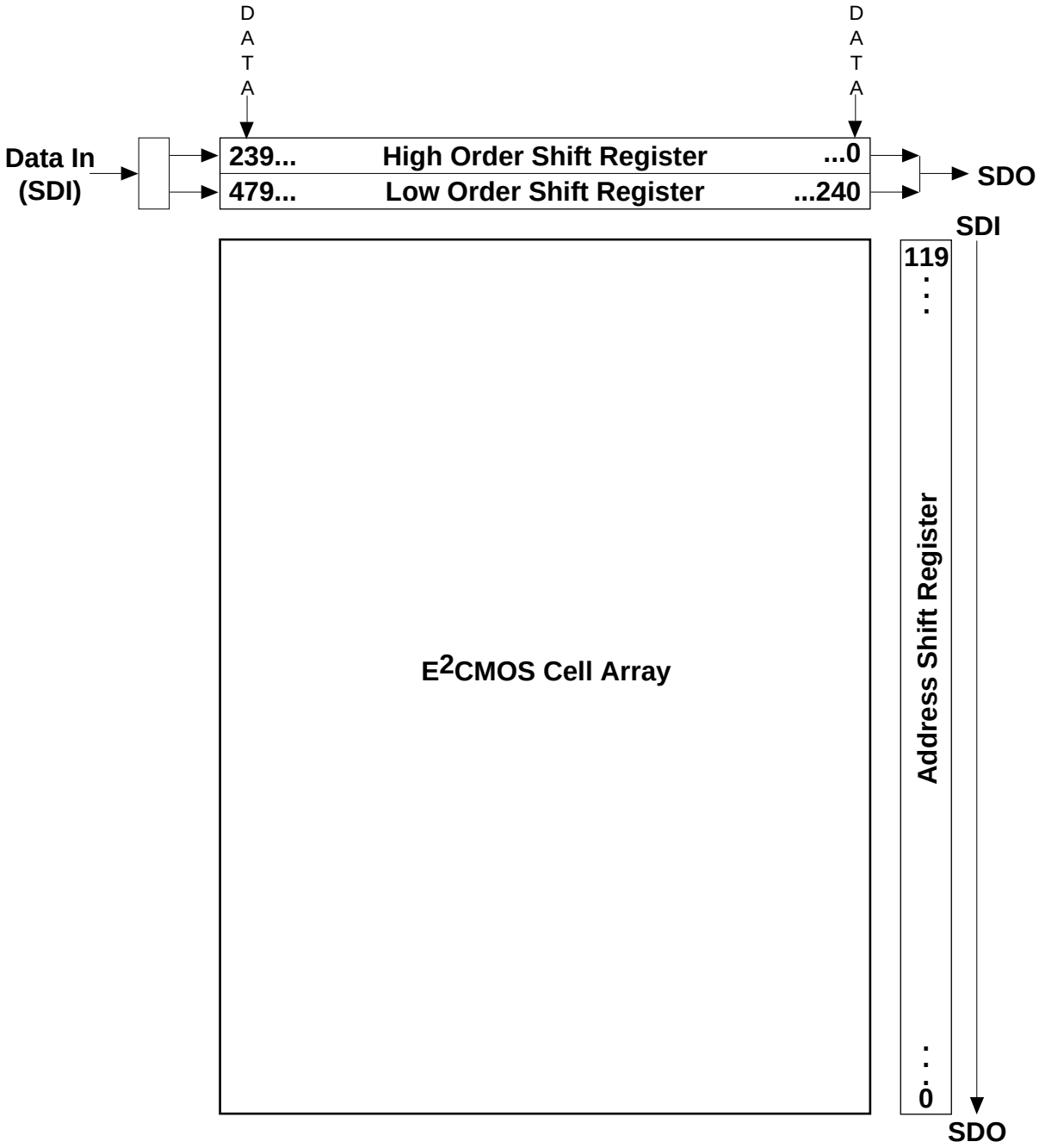
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme for programming the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section in this Data Book.

The device identifier for the ispLSI 1048 is 0000 0100 (04 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 1048 Shift Register Layout



Note: A logic "1" in the Address Shift Register bit position enables the row for programming or verification. A logic "0" disables it.

Pin Description

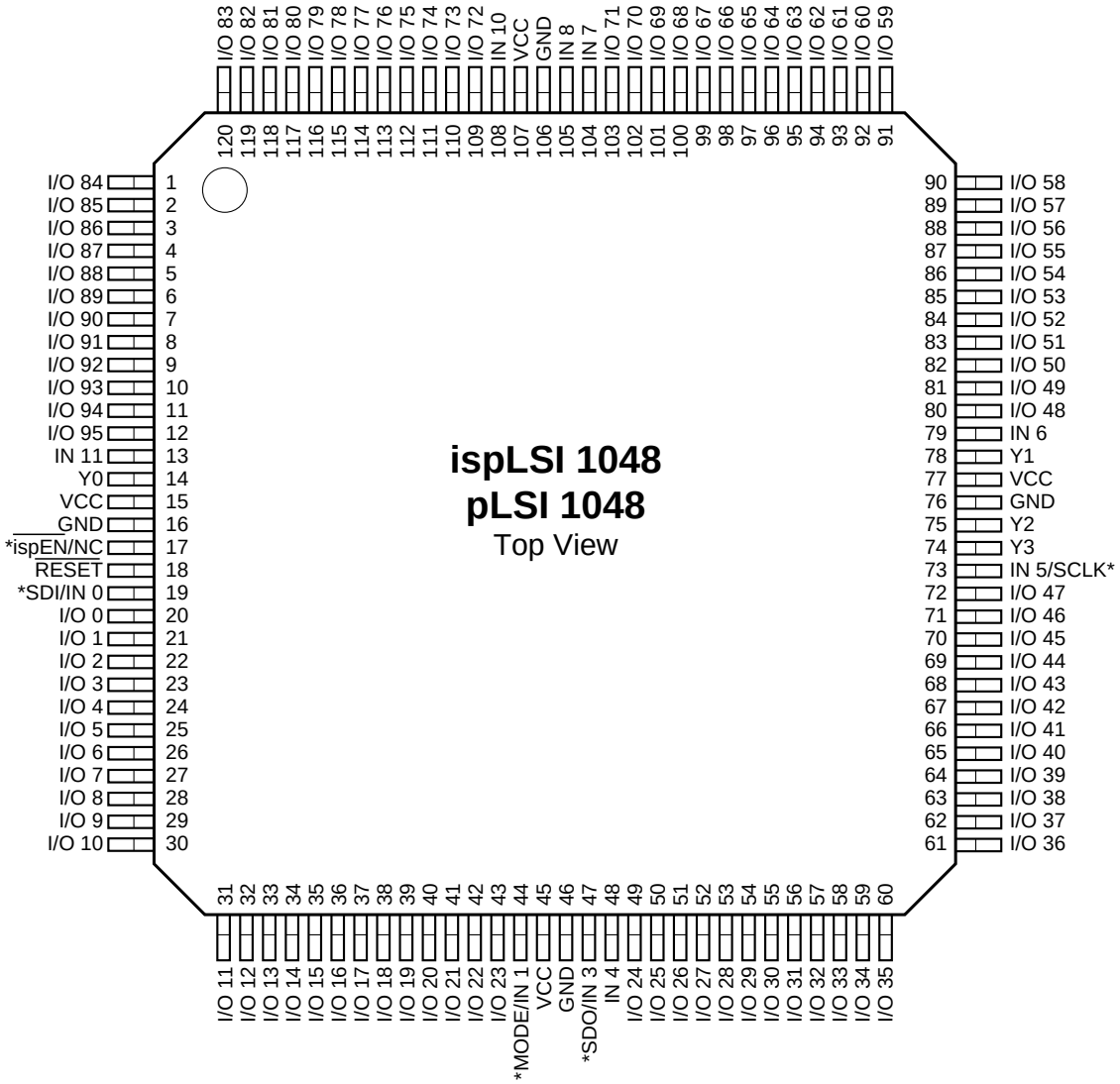
NAME	PQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99,100,101,102,103, 109,110,111,112,113,114, 115,116,117,118,119,120, 1, 2, 3, 4 5, 6, 7, 8, 9, 10, 11, 12	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 IN 6 - IN 11	48, 79,104,105, – 108, 13	Dedicated input pins to the device. (IN 2 and IN 9 not available)
$\overline{\text{ispEN}}$*/NC	17	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	19	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE*/IN 1	44	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO*/IN 3	47	Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK*/IN 5	73	Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	18	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	14	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	78	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	75	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	74	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND VCC	46, 76,106, 16 15, 45, 77, 107	Ground (GND) V_{CC}

*For ispLSI 1048 Only

Table 2- 0002C-48-isp

Pin Configuration

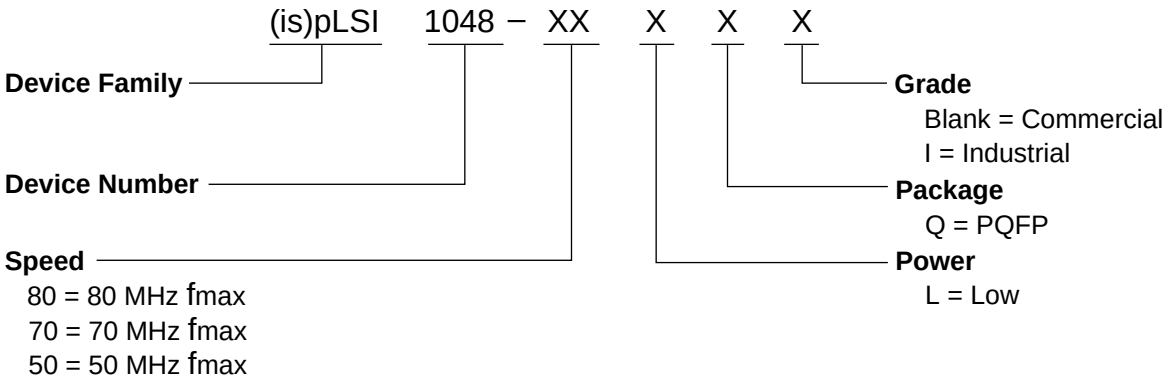
ispLSI and pLSI 1048 120-Pin PQFP Pinout Diagram



* Pins have dual function capability for ispLSI 1048 only (except pin 17, which is $\overline{\text{ispEN}}$ only).

0124 -48-isp

Part Number Description



0212-80B-isp1048

ispLSI and pLSI 1048 Ordering Information

COMMERCIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
ispLSI	80	15	ispLSI 1048-80LQ	120-Pin PQFP
	70	18	ispLSI 1048-70LQ	120-Pin PQFP
	50	24	ispLSI 1048-50LQ	120-Pin PQFP
pLSI	80	15	pLSI 1048-80LQ	120-Pin PQFP
	70	18	pLSI 1048-70LQ	120-Pin PQFP
	50	24	pLSI 1048-50LQ	120-Pin PQFP

INDUSTRIAL

Family	f_{max} (MHz)	t_{pd} (ns)	Ordering Number	Package
ispLSI	50	24	ispLSI 1048-50LQI	120-Pin PQFP
pLSI	50	24	pLSI 1048-50LQI	120-Pin PQFP

Table 2- 0041A-48-isp

Introduction to ispLSI® and pLSI® 2000 Family

Introduction

Lattice Semiconductor Corporation's (LSC) ispLSI and pLSI families are high-density and high-performance E^2CMOS® programmable logic devices. They provide design engineers with a superior system solution for integrating high-speed logic on a single chip.

The ispLSI and pLSI 2000 families are I/O intensive, programmable logic devices that combine the high performance and ease of use of PLDs with the density and flexibility of FPGAs.

The ispLSI and pLSI 2000 families are ideal for designs needing high performance in conjunction with high I/O requirements.

The ispLSI family incorporates Lattice Semiconductor's innovative in-system programmable™ (ISP™) technology. ISP technology allows for real-time programming, less expensive manufacturing and end-user feature reconfiguration.

E^2CMOS technology features reprogrammability, the ability to program the device again and again to easily incorporate any design modifications. This same capability allows full parametric testability during manufacturing, which guarantees 100 percent programming and functional yield.

All necessary development tools are available from LSC and third-party vendors. Development tools offered range from LSC's low cost pDS® software, featuring Boolean entry in a graphical Windows™ based environment, to the pDS+™ family of fitters that interfaces with third party development software packages. Design systems interfacing with pDS+ Fitters feature schematic capture, state machine and HDL design entry. Designs can now be completed in hours as opposed to days or weeks.

ispLSI and pLSI 2000 Family

- ❑ 154 MHz System Performance
- ❑ 5.5 ns Pin-to-Pin Delay
- ❑ Deterministic Performance
- ❑ High Density (1,000-6,000 PLD Gates)
- ❑ 44-Pin to 176-Pin Package Options
- ❑ Flexible Architecture
- ❑ Easy-to-Use
- ❑ In-System Programmable (ispLSI)
- ❑ Ideal for I/O Intensive Designs

ispLSI and pLSI Technology

- ❑ UltraMOS E^2CMOS — the PLD Technology of Choice
- ❑ Electrically Erasable/Programmable/ Reprogrammable
- ❑ 100% Tested During Manufacture
- ❑ 100% Programming Yield
- ❑ Fast Programming

ispLSI and pLSI Development Tools

- ❑ Low Cost, Fully Integrated pDS Design System for the PC
- ❑ Boolean Equations and Macro Input
- ❑ HDL, VHDL, Boolean Equation, State Machine and Schematic Capture Entry
- ❑ pDS+ Support for Industry-Standard Third-Party Design Environments and Platforms
- ❑ Timing and Functional Simulation
- ❑ PC and Workstation Platforms

2000 Family Overview

The ispLSI and pLSI 2000 families of high-density devices address high-performance system logic needs, implementing logic functions ranging from registers, to counters, to multiplexers, to complex state machines.

With PLD density ranging from 1,000 to 6,000 gates, the ispLSI and pLSI 2000 family provides a wide range of programmable logic solutions which meet tomorrow's design requirements today.

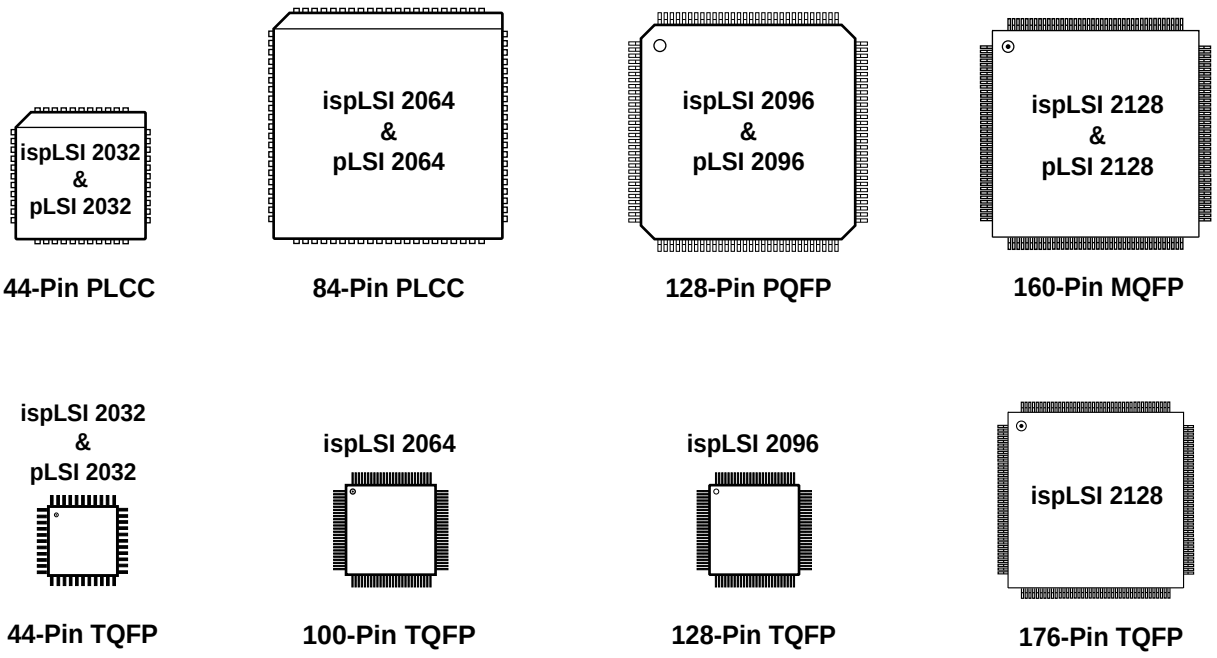
Each device contains multiple Generic Logic Blocks (GLBs), which are designed to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provides the optimum combination of internal logic and external connections. A global interconnect scheme ties everything together, enabling utilization of up to 80% of available logic. Table 1 describes the family attributes.

Table 1. ispLSI and pLSI 2000 Family Attributes

	2032	2064	2096	2128
Density (PLD Gates)	1,000	2,000	4,000	6,000
Speed: **f**max (MHz)	154	125	125	100
Speed: **t**pd (ns)	5.5	7.5	7.5	10
Macrocells	32	64	96	128
Registers	32	64	96	128
Inputs + I/O	34	68	102	136
Pin/Package	44-pin PLCC 44-pin TQFP	84-pin PLCC 100-pin TQFP	128-pin PQFP 128-pin TQFP	160-pin MQFP 176-pin TQFP

Table 1-0003A/2K

Figure 1. 2000 Family Packages



0288-2000

ispLSI® and pLSI® 2032

High Density Programmable Logic

Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **— 1000 PLD Gates**
  - **— 32 I/O Pins, Two Dedicated Inputs**
  - **— 32 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 154 MHz Maximum Operating Frequency**
  - **— t_{pd} = 5.5 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Enhanced Pin Locking Capability**
  - **— Three Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI/pLSI DEVELOPMENT TOOLS**

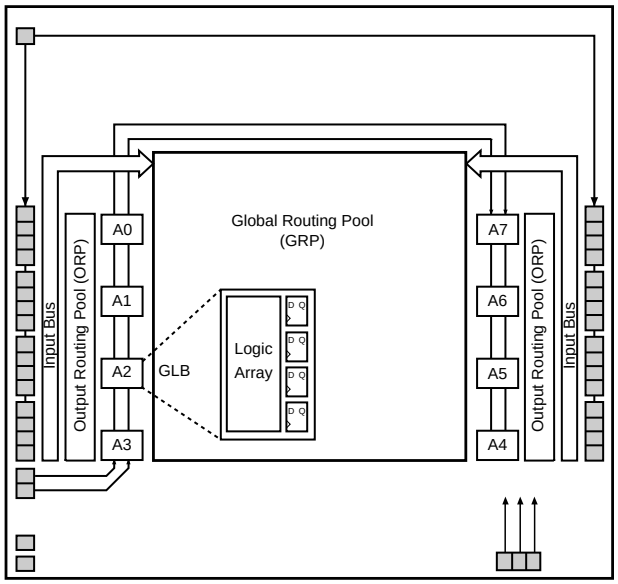
pDS® Software

- **— Easy to Use PC Windows™ Interface**
- **— Boolean Logic Compiler**
- **— Manual Partitioning**
- **— Automatic Place and Route**
- **— Static Timing Table**

pDS+™ Software

- **— Industry Standard, Third Party Design Environments**
- **— Schematic Capture, State Machine, HDL**
- **— Automatic Partitioning and Place and Route**
- **— Comprehensive Logic and Timing Simulation**
- **— PC and Workstation Platforms**

Functional Block Diagram



0139Bisp/2000

Description

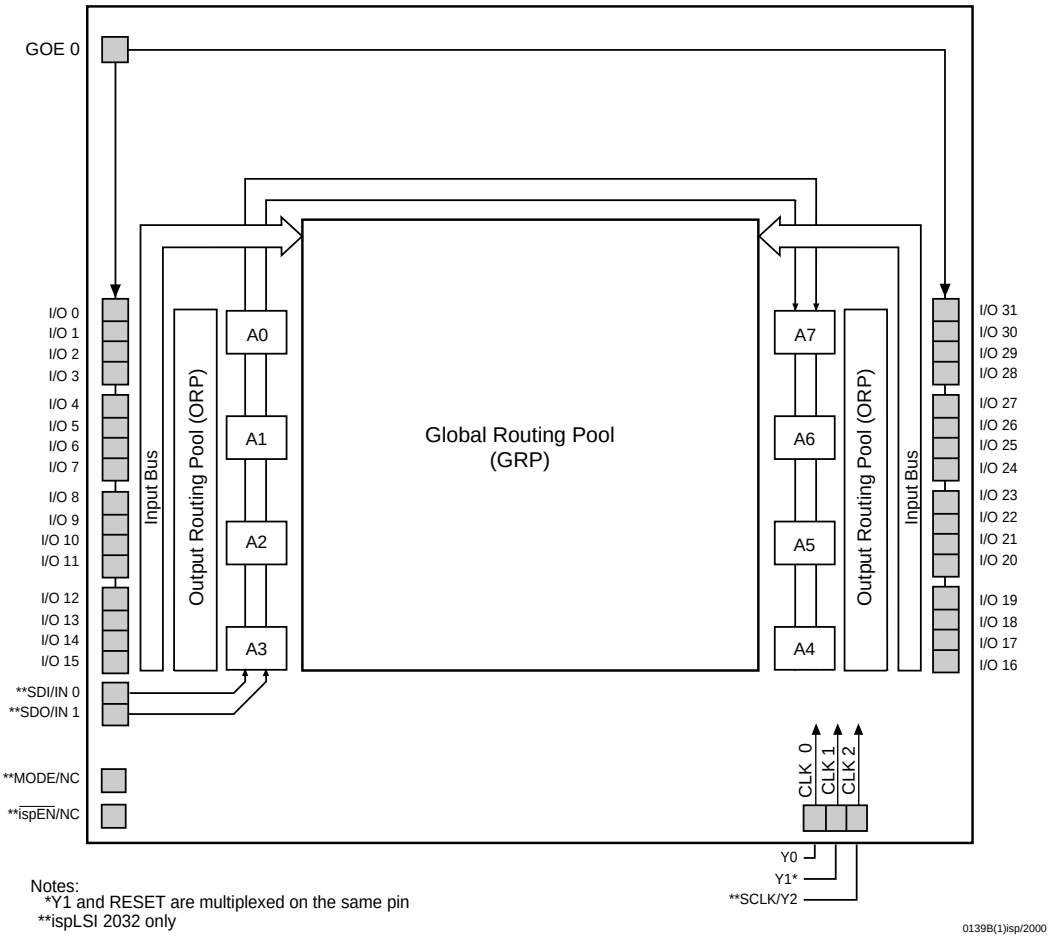
The ispLSI and pLSI 2032 are High Density Programmable Logic Devices. The devices contain 32 Registers, 32 Universal I/O pins, two Dedicated Input Pins, three Dedicated Clock Input Pins, one dedicated Global OE input pin and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2032 features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 2032 offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 2032 device, but multiplexes four input pins to control in-system programming.

The basic unit of logic on the ispLSI and pLSI 2032 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. A7 (see figure 1). There are a total of eight GLBs in the ispLSI and pLSI 2032 devices. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Functional Block Diagram

Figure 1. ispLSI and pLSI 2032 Functional Block Diagram



The devices also have 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the ORP. Each ispLSI and pLSI 2032 device contains one Megablock.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 2032 devices are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	4.75	5.25	V
		Industrial	T_A = -40°C to + 85°C	4.5	5.5	V
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V

Table 2 - 0005/2032

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	6	pf	V_{CC} = 5.0V, V_{IN} = 2.0V
C_2	I/O Capacitance	7	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_3	Clock Capacitance	10	pf	V_{CC} = 5.0V, V_Y = 2.0V

1. Guaranteed, but not 100% tested.

Table 2 - 0006

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2-0008A-isp

Switching Test Conditions

Input Pulse Levels	GND to 3.0V	
Input Rise and Fall Time 10% to 90%	-135, -150	≤ 1.5 ns
	Others	≤ 3 ns
Input Timing Reference Levels	1.5V	
Ouput Timing Reference Levels	1.5V	
Output Load	See figure 2	

Table 2 - 0003/2032

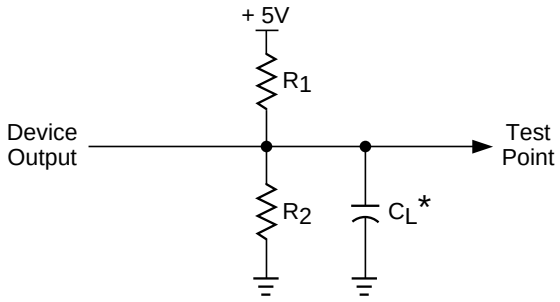
3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION			MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA			–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA			2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)			–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}			–	–	10	µA
I_{IL-isp}	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}			–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}			–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V			–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V f_{TOGGLE} = 1 MHz	Commercial	-150	–	60	150	mA
				Others	–	40	120	mA
			Industrial		–	40	–	mA

Table 2 - 0007Aisp/2032

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using two 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-150		-135		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	5.5	–	7.5	ns
t_{pd2}	A	2	Data Propagation Delay	–	8.0	–	10.0	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	154	–	137	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	111	–	100	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	167	–	167	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	3.0	–	4.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	4.5	–	4.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	4.5	–	5.5	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	5.0	–	5.5	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	8.0	–	10.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	4.5	–	5.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	11.0	–	12.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	11.0	–	12.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	5.0	–	6.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	5.0	–	6.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	3.0	–	3.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	3.0	–	3.0	–	ns

Table 2 - 0030B/2032-150

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-110		-80		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	13.0	–	18.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	111	–	84	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	77	–	57	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	125	–	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	5.5	–	7.5	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	5.5	–	8.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	7.5	–	9.5	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	6.5	–	9.5	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	13.5	–	19.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	6.5	–	10.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	14.5	–	24.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	14.5	–	24.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	7.0	–	12.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	7.0	–	12.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	4.0	–	6.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	4.0	–	6.0	–	ns

Table 2 - 0030B/2128-110

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-150		-135		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	20	Input Buffer Delay	–	0.6	–	1.1	ns
t_{din}	21	Dedicated Input Delay	–	1.3	–	2.4	ns
GRP							
t_{grp}	22	GRP Delay	–	0.7	–	1.3	ns
GLB							
t_{4ptbpc}	23	4 Product Term Bypass Path Delay (Combinatorial)	–	2.6	–	3.6	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay (Registered)	–	3.1	–	3.6	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	4.3	–	5.0	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	4.6	–	5.1	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	5.0	–	5.6	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.0	–	0.0	ns
t_{gsu}	29	GLB Register Setup Time befor Clock	0.7	–	0.3	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	1.8	–	3.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.8	–	0.7	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.2	–	1.1	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	2.9	–	4.4	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	6.9	–	6.4	ns
t_{ptck}	35	GLB Product Term Clock Delay	2.5	4.1	2.9	5.2	ns
ORP							
t_{orp}	36	ORP Delay	–	0.8	–	1.3	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.3	–	0.3	ns
Outputs							
t_{ob}	38	Output Buffer Delay	–	1.3	–	1.2	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	10.0	–	10.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	2.8	–	3.2	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	2.8	–	3.2	ns
t_{goe}	42	Global Output Enable	–	2.2	–	2.8	ns
Clocks							
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.1	2.1	2.3	2.3	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.1	2.1	2.3	2.3	ns
Global Reset							
t_{gr}	45	Global Reset to GLB	–	4.7	–	6.4	ns

Table 2- 0036C/2032-150

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters[1]

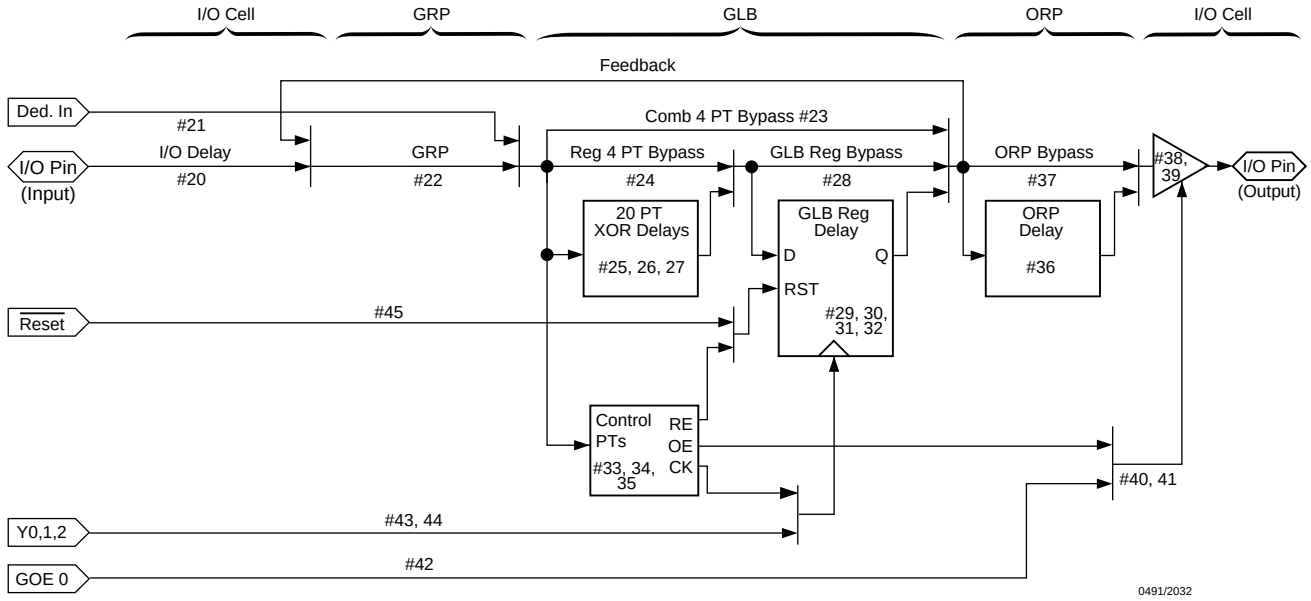
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-110		-80		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	20	Input Buffer Delay	–	1.7	–	2.2	ns
t_{din}	21	Dedicated Input Delay	–	3.4	–	4.8	ns
GRP							
t_{grp}	22	GRP Delay	–	1.7	–	2.6	ns
GLB							
t_{4ptbpc}	23	4 Product Term Bypass Path Delay (Combinatorial)	–	4.9	–	7.2	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay (Registered)	–	4.8	–	7.2	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	6.2	–	8.8	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	6.8	–	9.2	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	7.5	–	10.2	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.1	–	0.0	ns
t_{gsu}	29	GLB Register Setup Time befor Clock	0.5	–	0.1	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	4.0	–	6.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.6	–	0.4	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.8	–	2.2	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	5.9	–	8.8	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	7.1	–	12.8	ns
t_{ptck}	35	GLB Product Term Clock Delay	4.0	7.0	5.5	9.5	ns
ORP							
t_{orp}	36	ORP Delay	–	1.5	–	2.1	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.5	–	0.6	ns
Outputs							
t_{ob}	38	Output Buffer Delay	–	1.2	–	2.4	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	10.0	–	10.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	4.0	–	6.4	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	4.0	–	6.4	ns
t_{goe}	42	Global Output Enable	–	3.0	–	5.6	ns
Clocks							
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	3.2	3.2	4.6	4.6	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	3.2	3.2	4.6	4.6	ns
Global Reset							
t_{gr}	45	Global Reset to GLB	–	9.0	–	12.8	ns

Table 2- 0036C/2032-110

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

ispLSI and pLSI 2032 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (**t**io + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**io + **t**grp + **t**ptck(min))
= (#20+ #22+ #26) + (#29) - (#20+ #22+ #35)
1.9 ns = (1.1 + 1.3 + 5.1) + (0.3) - (1.1 + 1.3 + 2.9)

th = Clock (max) + Reg h - Logic
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**io + **t**grp + **t**20ptxor)
= (#20+ #22+ #35) + (#30) - (#20+ #22+ #26)
1.4 ns = (1.1 + 1.3 + 5.2) + (3.0) - (1.1 + 1.3 + 5.1)

tco = Clock (max) + Reg co + Output
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#20+ #22+ #35) + (#31) + (#36 + #38)
9.1 ns = (1.1 + 1.3 + 5.2) + (0.7) + (1.3 + 1.2)

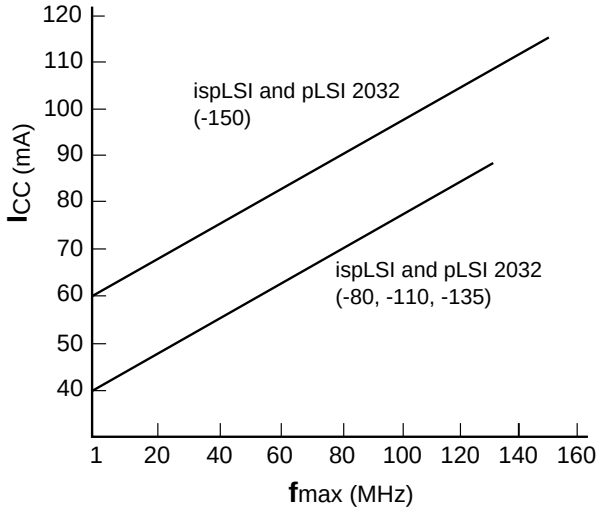
Table 2- 0042-16/2032

Note: Calculations are based upon timing specifications for the ispLSI and pLSI 2032-135L.

Power Consumption

Power Consumption in the ispLSI and pLSI 2032 device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of Two 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI and pLSI 2032 using the following equation:

For 2032 -150: I_{CC}(mA) = 30 + (# of PTs * 0.46) + (# of nets * Max freq * 0.012)
For 2032 -135, -110, -80: I_{CC}(mA) = 21 + (# of PTs * 0.30) + (# of nets * Max freq * 0.012)

Where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max freq = Highest Clock Frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A-16-80-isp/2000

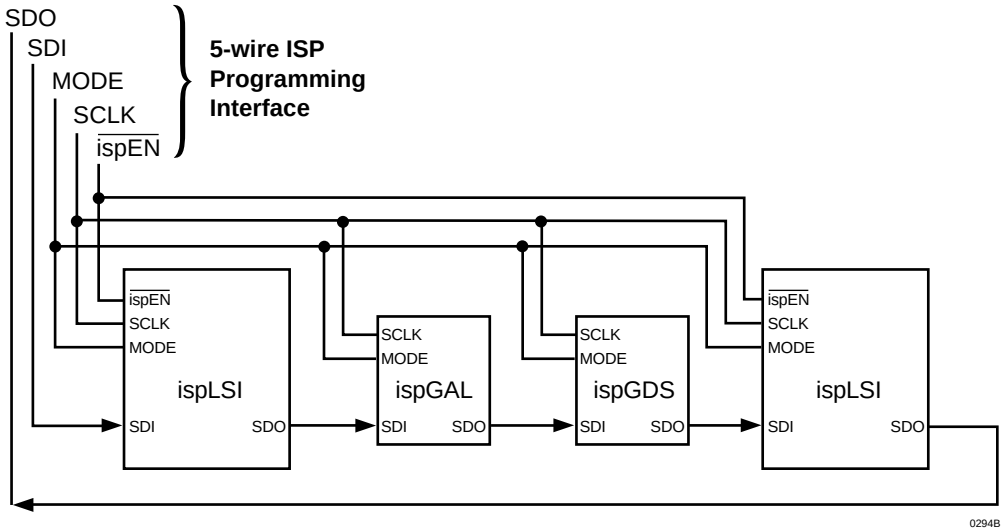
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

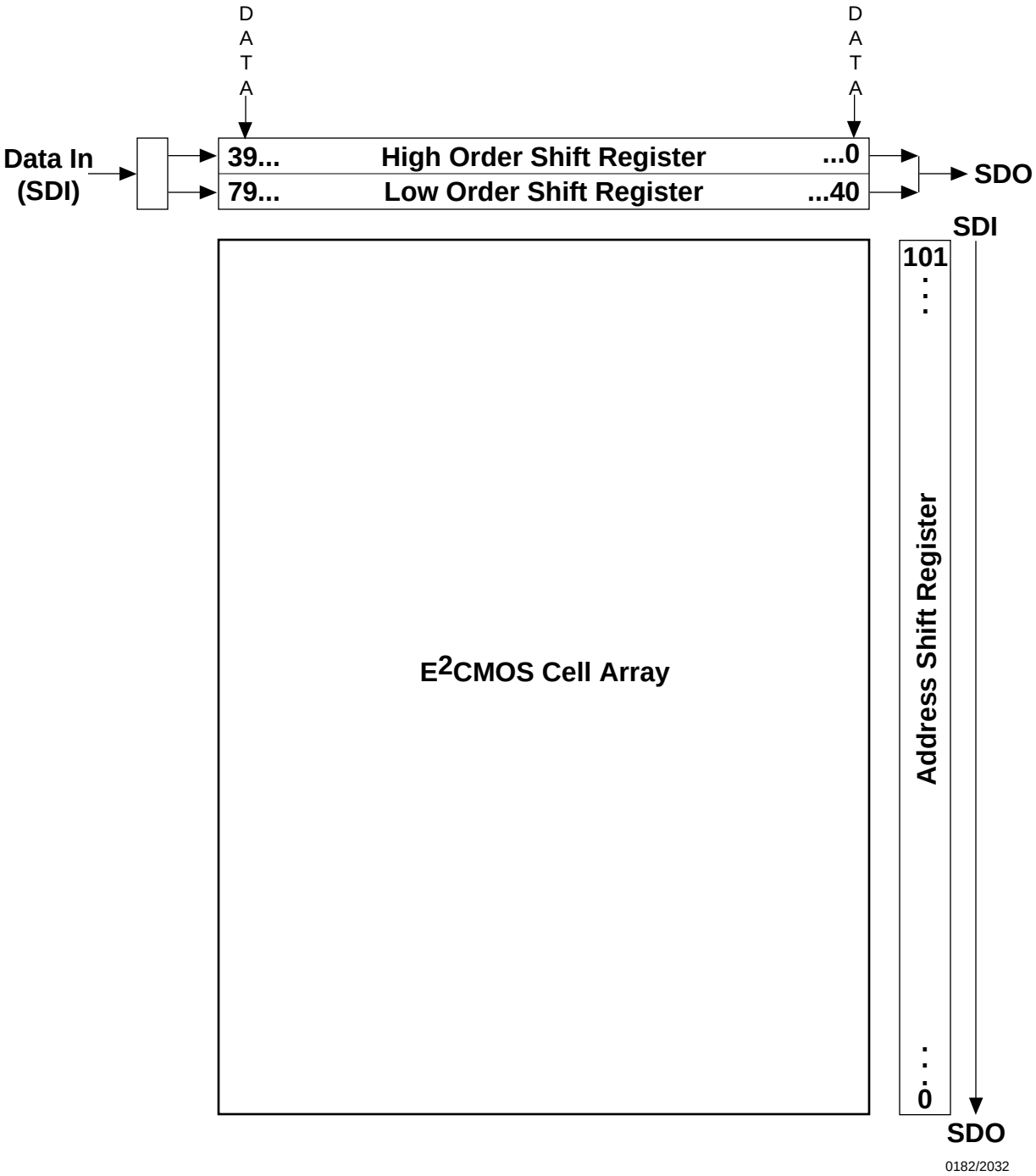
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for the interface include isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section of this Data Book.

The device identifier for the ispLSI 2032 is 0001 0101 (15 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 2032 Shift Register Layout



Note: A logic "1" in the address shift register enables the row for programming or verification. A logic "0" disables it.

Pin Description

NAME	PLCC PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0	2	Global Output Enable input pin.
Y0	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs on the device.
$\overline{\text{RESET}}$/Y1	35	This pin performs two functions: - Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. - Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
$\overline{\text{ispEN}}$**/NC	13	Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK controls become active.
SDI*/IN 0	14	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN0 also is used as one of the two control pins for the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
MODE*/NC	36	Input - When in ISP Mode, controls operation of ISP state-machine.
SDO*/IN 1	24	Output/Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SCLK*/Y2	33	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated clock input.This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device.
GND	1, 23	Ground (GND)
VCC	12, 34	V_{CC}

Table 2 - 0002A-08isp/2000

* ispLSI 2032 only

** $\overline{\text{ispEN}}$ for ispLSI 2032 only; NC for pLSI 2032 must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

Pin Description

NAME	44-PIN TQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	9, 10, 11, 12, 13, 14, 15, 16, 19, 20, 21, 22, 23, 24, 25, 26, 31, 32, 33, 34, 35, 36, 37, 38, 41, 42, 43, 44, 1, 2, 3, 4	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0	40	Global Output Enable input pin.
Y0	5	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs on the device.
$\overline{\text{RESET}}$/Y1	29	This pin performs two functions: - Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. - Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
$\overline{\text{ispEN}}$**/NC	7	Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK controls become active.
SDI*/IN 0	8	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN0 also is used as one of the two control pins for the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
MODE*/NC	30	Input - When in ISP Mode, controls operation of ISP state-machine.
SDO*/IN 1	18	Output/Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SCLK*/Y2	27	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.It is a dedicated clock input when $\overline{\text{ispEN}}$ is logic high. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device.
GND	17, 39	Ground (GND)
VCC	6, 28	V_{CC}

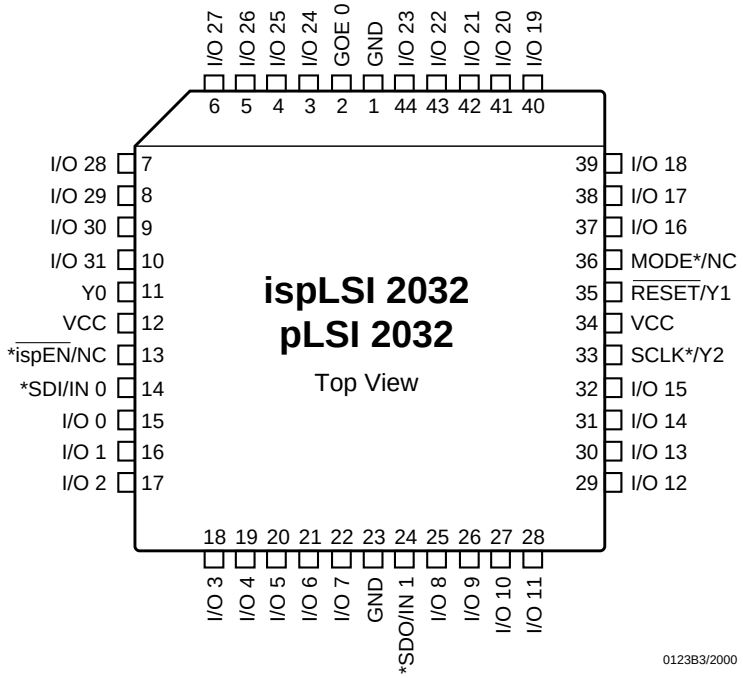
* ispLSI 2032 only

Table 2 - 0002B-2032

** $\overline{\text{ispEN}}$ for ispLSI 2032 only; NC for pLSI 2032 must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

Pin Configuration

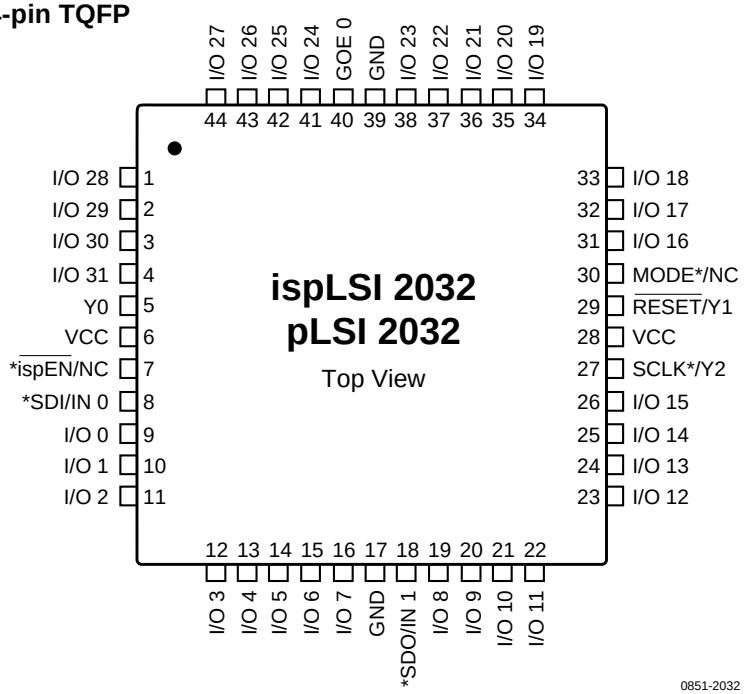
ispLSI and pLSI 2032 44-pin PLCC



*Pins have dual function capability for ispLSI 2032 only (except pin 13, which is ispEN only).

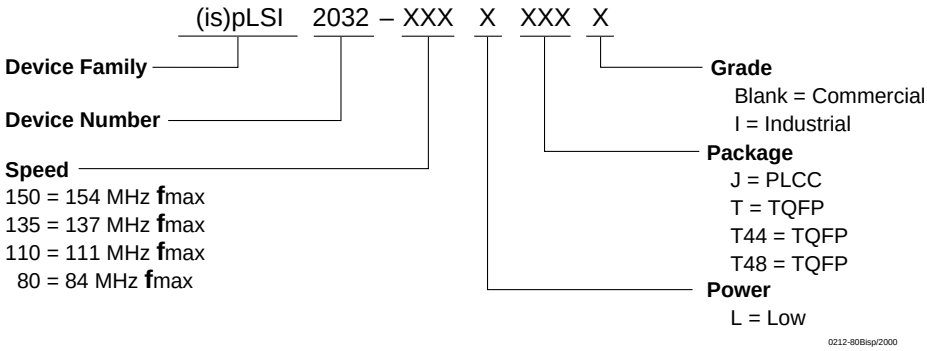
Pin Configuration

ispLSI and pLSI 2032 44-pin TQFP



*Pins have dual function capability for ispLSI 2032 only (except pin 13, which is ispEN only).

Part Number Description



ispLSI and pLSI 2032 Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	154	5.5	ispLSI 2032-150LJ	44-Pin PLCC
	154	5.5	ispLSI 2032-150LT	44-Pin TQFP
	154	5.5	ispLSI 2032-150LT44	44-Pin TQFP
	154	5.5	ispLSI 2032-150LT48	48-Pin TQFP
	137	7.5	ispLSI 2032-135LJ	44-Pin PLCC
	137	7.5	ispLSI 2032-135LT	44-Pin TQFP
	137	7.5	ispLSI 2032-135LT44	44-Pin TQFP
	137	7.5	ispLSI 2032-135LT48	48-Pin TQFP
	111	10	ispLSI 2032-110LJ	44-Pin PLCC
	111	10	ispLSI 2032-110LT	44-Pin TQFP
	111	10	ispLSI 2032-110LT44	44-Pin TQFP
	111	10	ispLSI 2032-110LT48	48-Pin TQFP
	84	15	ispLSI 2032-80LJ	44-Pin PLCC
	84	15	ispLSI 2032-80LT	44-Pin TQFP
	84	15	ispLSI 2032-80LT44	44-Pin TQFP
pLSI	154	5.5	pLSI 2032-150LJ	44-Pin PLCC
	154	5.5	pLSI 2032-150LT	44-Pin TQFP
	154	5.5	pLSI 2032-150LT44	44-Pin TQFP
	137	7.5	pLSI 2032-135LJ	44-Pin PLCC
	137	7.5	pLSI 2032-135LT	44-Pin TQFP
	137	7.5	pLSI 2032-135LT44	44-Pin TQFP
	111	10	pLSI 2032-110LJ	44-Pin PLCC
	111	10	pLSI 2032-110LT	44-Pin TQFP
	111	10	pLSI 2032-110LT44	44-Pin TQFP
	84	15	pLSI 2032-80LJ	44-Pin PLCC
	84	15	pLSI 2032-80LT	44-Pin TQFP
	84	15	pLSI 2032-80LT44	44-Pin TQFP

Table 2-0041A-08isp/2000

INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	84	15	ispLSI 2032-80LJI	44-Pin PLCC
	84	15	ispLSI 2032-80LT44I	44-Pin TQFP
	84	15	ispLSI 2032-80LT48I	48-Pin TQFP

Table 2-0041B-08isp/2000

ispLSI® and pLSI® 2064

High Density Programmable Logic

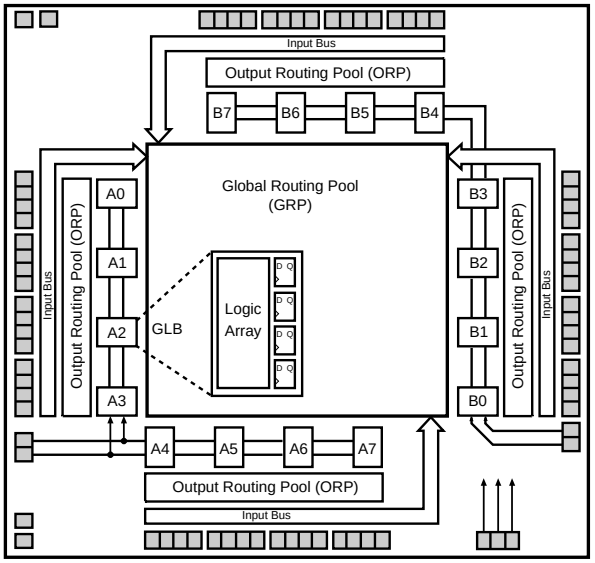
Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **— 2000 PLD Gates**
  - **— 64 I/O Pins, Four Dedicated Inputs**
  - **— 64 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 125 MHz Maximum Operating Frequency**
  - **— t_{pd} = 7.5 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Marketand Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Enhanced Pin Locking Capability**
  - **— Three Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI/pLSI DEVELOPMENT TOOLS**

pDS® Software
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning**
  - **— Automatic Place and Route**
  - **— Static Timing Table**

pDS+™ Software
  - **— Industry Standard, Third Party Design Environments**
  - **— Schematic Capture, State Machine, HDL**
  - **— Automatic Partitioning and Place and Route**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

Functional Block Diagram



0139Bisp/2064

Description

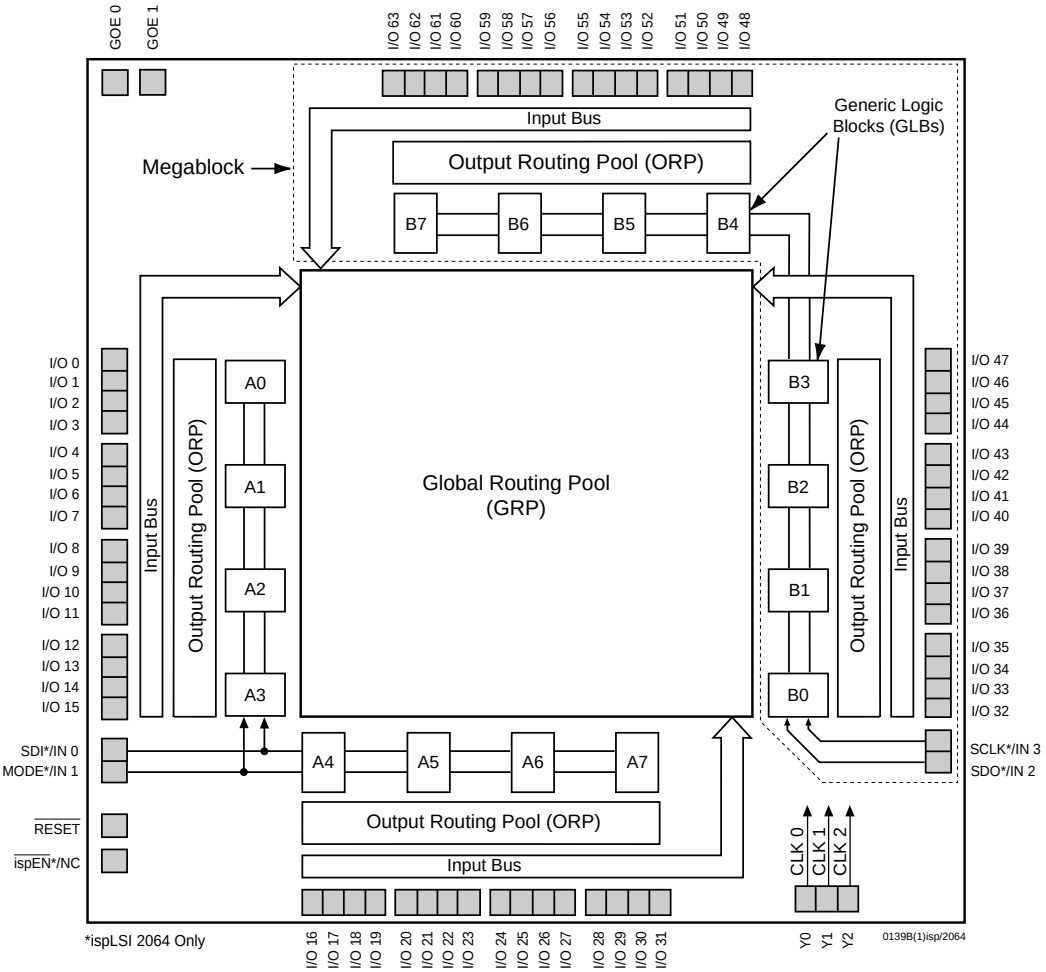
The ispLSI and pLSI 2064 are High-Density Programmable Logic Devices. The devices contain 64 Registers, 64 Universal I/O pins, four Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2064 features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 2064 offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect, to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 2064 device, but multiplexes four input pins to control in-system programming.

The basic unit of logic on the ispLSI and pLSI 2064 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1…B7 (see figure 1). There are a total of 16 GLBs in the ispLSI and pLSI 2064 devices. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Functional Block Diagram

Figure 1. ispLSI and pLSI 2064 Functional Block Diagram



The devices also have 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by two ORPs. Each ispLSI and pLSI 2064 device contains two Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 2064 devices are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ..... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	4.75	5.25	V
		Industrial	T_A = -40°C to + 85°C	4.5	5.5	V
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{cc}+1	V

Table 2 - 0005/2064

Capacitance (TA=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	V_{CC} = 5.0V, V_{IN} = 2.0V
C_2	I/O Capacitance	9	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_3	Clock Capacitance	15	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2 - 0006B

1. Guaranteed. but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2-0008A-isp

Switching Test Conditions

Input Pulse Levels	GND to 3.0V	
Input Rise and Fall Time 10% to 90%	-125	≤ 2 ns
	Others	≤ 3 ns
Input Timing Reference Levels	1.5V	
Ouput Timing Reference Levels	1.5V	
Output Load	See figure 2	

Table 2 - 0003/2064

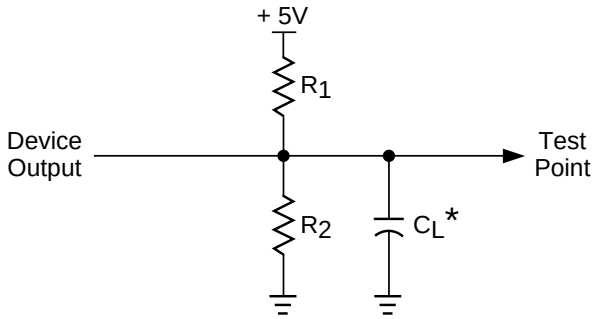
3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
I_{IL-isp}	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V	Commercial	–	95	175	mA
		f_{CLOCK} = 1 MHz	Industrial	–	95	–	mA

Table 2 - 0007Aisp/2064

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using four 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-125		-100		-80		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	7.5	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	10.0	–	13.0	–	18.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	125	–	100	–	81	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	100	–	77	–	57	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	125	–	111	–	100	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	5.0	–	6.5	–	9.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	4.0	–	5.0	–	6.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	6.0	–	8.0	–	11.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	4.5	–	6.0	–	8.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	10.0	–	13.5	–	17.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	5.0	–	6.5	–	10.0	–	ns
t_{ptoeen}	B	14	Product Term OE, Enable	–	12.0	–	15.0	–	18.0	ns
$t_{ptoedis}$	C	15	Product Term OE, Disable	–	12.0	–	15.0	–	18.0	ns
t_{goeen}	B	16	Global OE, Enable	–	7.0	–	9.0	–	12.0	ns
t_{goedis}	C	17	Global OE, Disable	–	7.0	–	9.0	–	12.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	4.0	–	4.5	–	5.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	4.0	–	4.5	–	5.0	–	ns

Table 2 - 0030B/2064-130

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

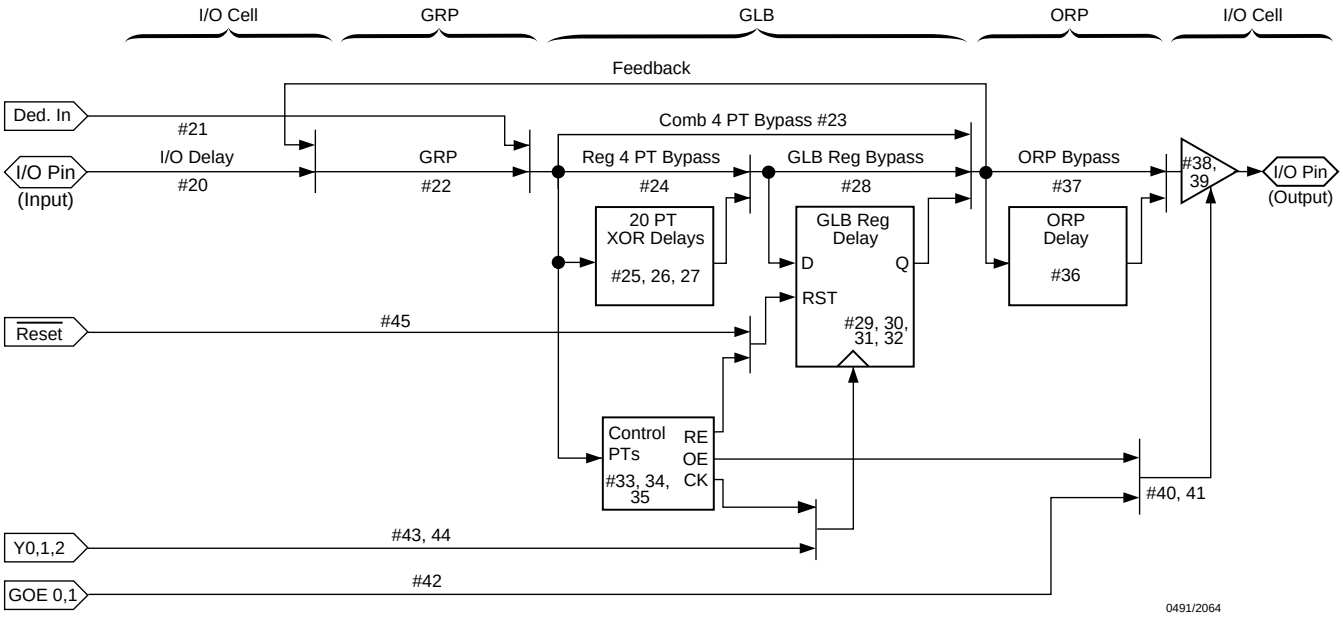
Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-125		-100		-80		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t_{io}	20	Input Buffer Delay	–	0.2	–	0.5	–	1.8	ns
t_{din}	21	Dedicated Input Delay	–	1.5	–	2.2	–	4.4	ns
GRP									
t_{grp}	22	GRP Delay	–	1.3	–	1.7	–	2.6	ns
GLB									
t_{4ptbp}	23	4 Product Term Bypass Comb. Path Delay	–	4.5	–	5.8	–	8.1	ns
t_{4ptbp}	24	4 Product Term Bypass Reg. Path Delay	–	5.0	–	5.8	–	6.8	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	5.7	–	6.8	–	8.0	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	6.0	–	7.3	–	8.8	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	6.5	–	8.0	–	9.8	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.5	–	0.5	–	1.3	ns
t_{gsu}	29	GLB Register Setup Time before Clock	0.8	–	1.2	–	1.4	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	3.0	–	4.0	–	6.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.2	–	0.3	–	0.4	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.1	–	1.3	–	1.6	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	4.8	–	6.1	–	8.6	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	7.3	–	8.6	–	9.0	ns
t_{ptck}	35	GLB Product Term Clock Delay	3.3	5.6	4.1	7.1	5.6	10.2	ns
ORP									
t_{orp}	36	ORP Delay	–	0.8	–	1.4	–	2.0	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.3	–	0.4	–	0.5	ns
Outputs									
t_{ob}	38	Output Buffer Delay	–	1.2	–	1.6	–	2.0	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	10.0	–	10.0	–	10.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	3.2	–	4.2	–	4.6	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	3.2	–	4.2	–	4.6	ns
t_{goe}	42	Global Output Enable	–	3.8	–	4.8	–	7.4	ns
Clocks									
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.3	2.3	2.7	2.7	3.6	3.6	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.3	2.3	2.7	2.7	3.6	3.6	ns
Global Reset									
t_{gr}	45	Global Reset to GLB	–	6.9	–	9.2	–	11.4	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

ispLSI and pLSI 2064 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu
= Logic + Reg su - Clock (min)
= (**t**io + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**io + **t**grp + **t**ptck(min))
= (#20 + #22 + #26) + (#29) - (#20 + #22 + #35)
3.5 ns = (0.2 + 1.3 + 6.0) + (0.8) - (0.2 + 1.3 + 3.3)

th
= Clock (max) + Reg h - Logic
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**io + **t**grp + **t**20ptxor)
= (#20 + #22 + #35) + (#30) - (#20 + #22 + #26)
2.6 ns = (0.2 + 1.3 + 5.6) + (3.0) - (0.2 + 1.3 + 6.0)

tco
= Clock (max) + Reg co + Output
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#20 + #22 + #35) + (#31) + (#36 + #38)
9.4 ns = (0.2 + 1.3 + 5.6) + (0.2) + (0.8 + 1.2)

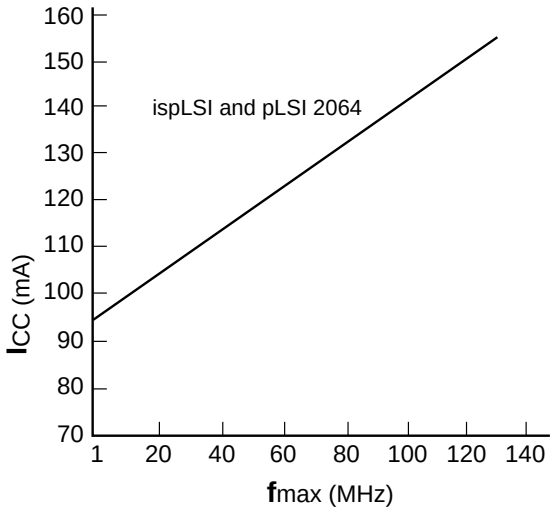
Table 2- 0042A-2064

Note: Calculations are based upon timing specifications for the ispLSI and pLSI 2064-125L.

Power Consumption

Power Consumption in the ispLSI and pLSI 2064 device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of Four 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI and pLSI 2064 using the following equation:

I_{CC}(mA) = 38 + (# of PTs * 0.33) + (# of nets * Max freq * 0.007)

Where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max freq = Highest Clock Frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A-64-80isp/2000

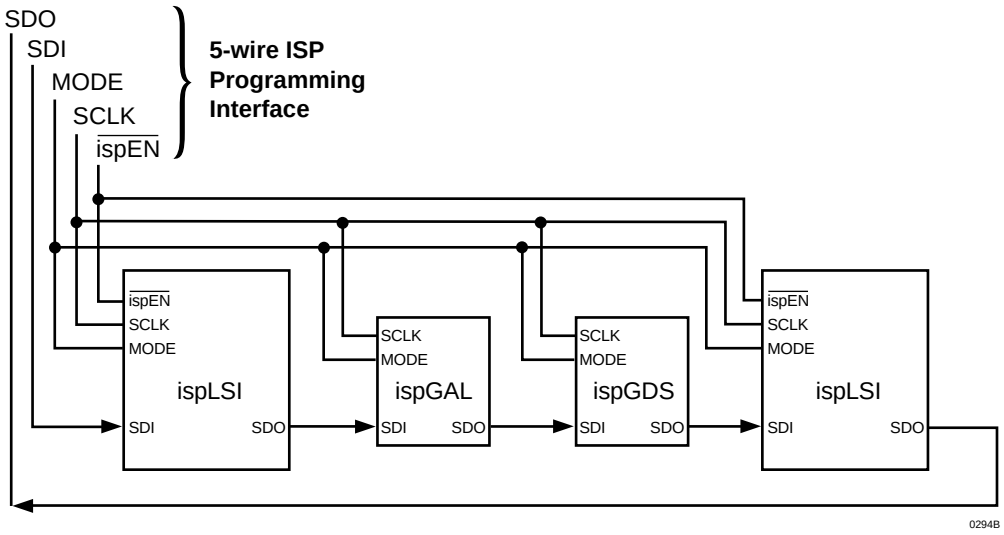
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

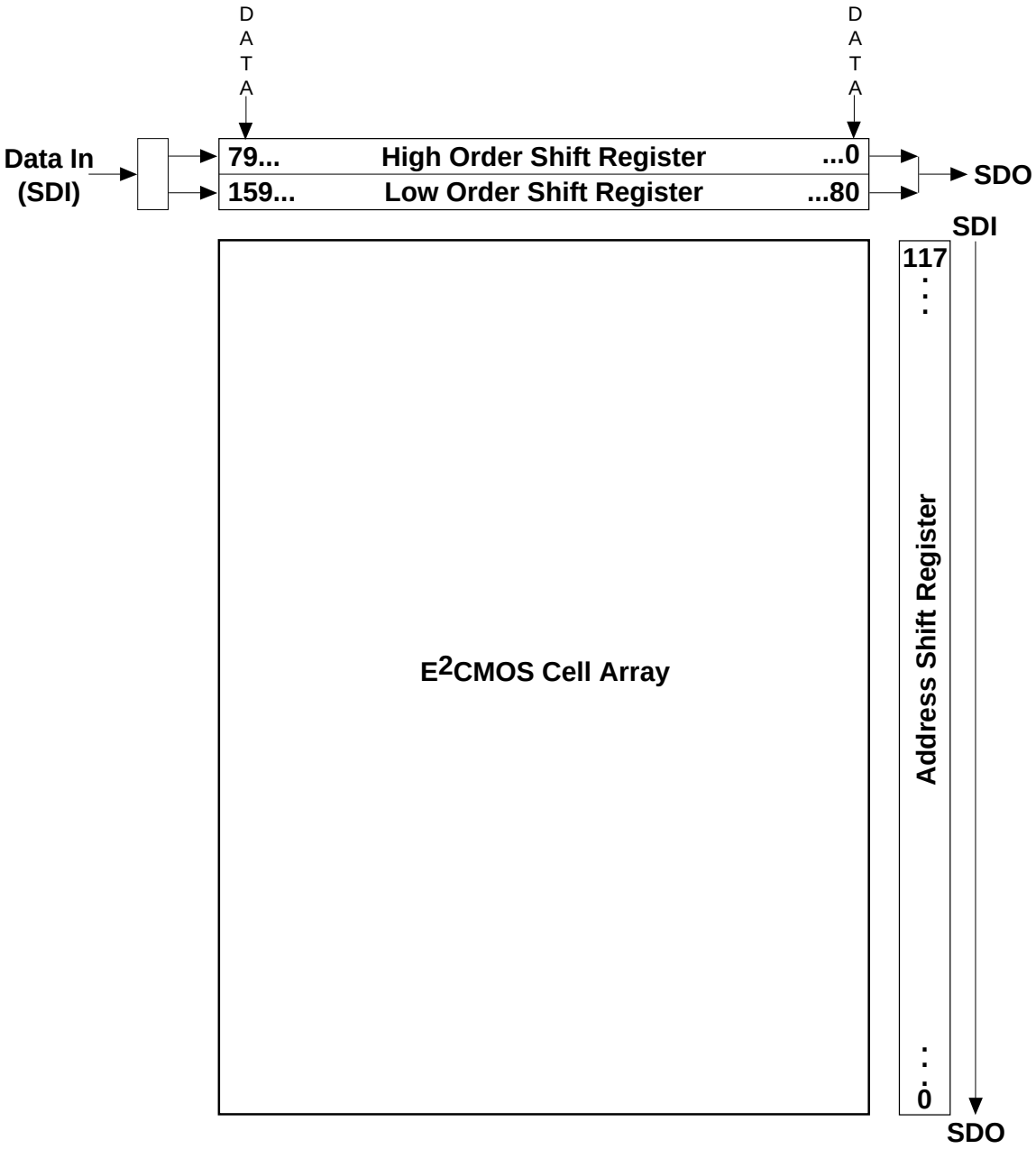
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for the interface include isp Enable (ispEN), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device, please refer to the ISP Architecture and Programming section of this Data Book.

The device identifier for the ispLSI 2064 is 0001 0010 (12 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 2064 Shift Register Layout



Note: A logic "1" in the address shift register enables the row for programming or verification. A logic "0" disables it.

Pin Description

Name	PLCC Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0, GOE 1	67, 84	Global Output Enable input pins.
Y0, Y1, Y2	20, 66, 63	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs in the device.
$\overline{\text{RESET}}$	24	Active Low (0) Reset pin which resets all the registers in the device.
$\overline{\text{ispEN}}$**/NC	23	Input — Dedicated in-system programming enable pin. This pin is brought low to enable the programming mode. When low, the MODE, SDI, SDO and SCLK controls become active.
SDI*/IN 0	25	Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the ISP state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
MODE*/IN 1	42	Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the ISP state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SDO*/IN 2	44	Output/Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SCLK*/IN 3	61	Input — This pin performs two functions. When $\overline{\text{ispEN}}$ is a logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
NC	2, 19, 62	These pins are not used.
GND	1, 22, 43, 64	Ground (GND)
VCC	21, 65	V_{CC}

* ispLSI 2064 Only

** $\overline{\text{ispEN}}$ for ispLSI 2064 only; NC for pLSI 2064, must be left floating or tied to Vcc, must not be grounded or tied to any other signal.

Table 2- 0002A-08isp/2064

Pin Description

Name	TQFP Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31, 32, 33, 34, 35, 36, 40, 41, 42, 43, 44, 45, 46, 47, 48, 53, 54, 55, 56, 57, 58, 59, 67, 68, 69, 70, 71, 72, 73, 78, 79, 80, 81, 82, 83, 84, 85, 86, 90, 91, 92, 93, 94, 95, 96, 97, 98, 3, 4, 5, 6, 7, 8, 9	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0, GOE 1	66, 87	Global Output Enable input pins.
Y0, Y1, Y2	11, 65, 62	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
$\overline{\text{RESET}}$	15	Active Low (0) Reset pin which resets all of the registers in the device.
$\overline{\text{ispEN}}$**/NC	14	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK controls become active.
SDI*/IN 0	16	Input – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the ISP state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
MODE*/IN 1	37	Input – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the ISP state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SDO*/IN 2	39	Output/Input – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SCLK*/IN 3	60	Input – This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
NC	1, 2, 10, 24, 25, 26, 27, 49, 50, 51, 52, 61, 74, 75, 76, 77, 89, 99, 100	These pins are not used.
GND	13, 38, 63, 88	Ground (GND)
VCC	12, 64	V_{CC}

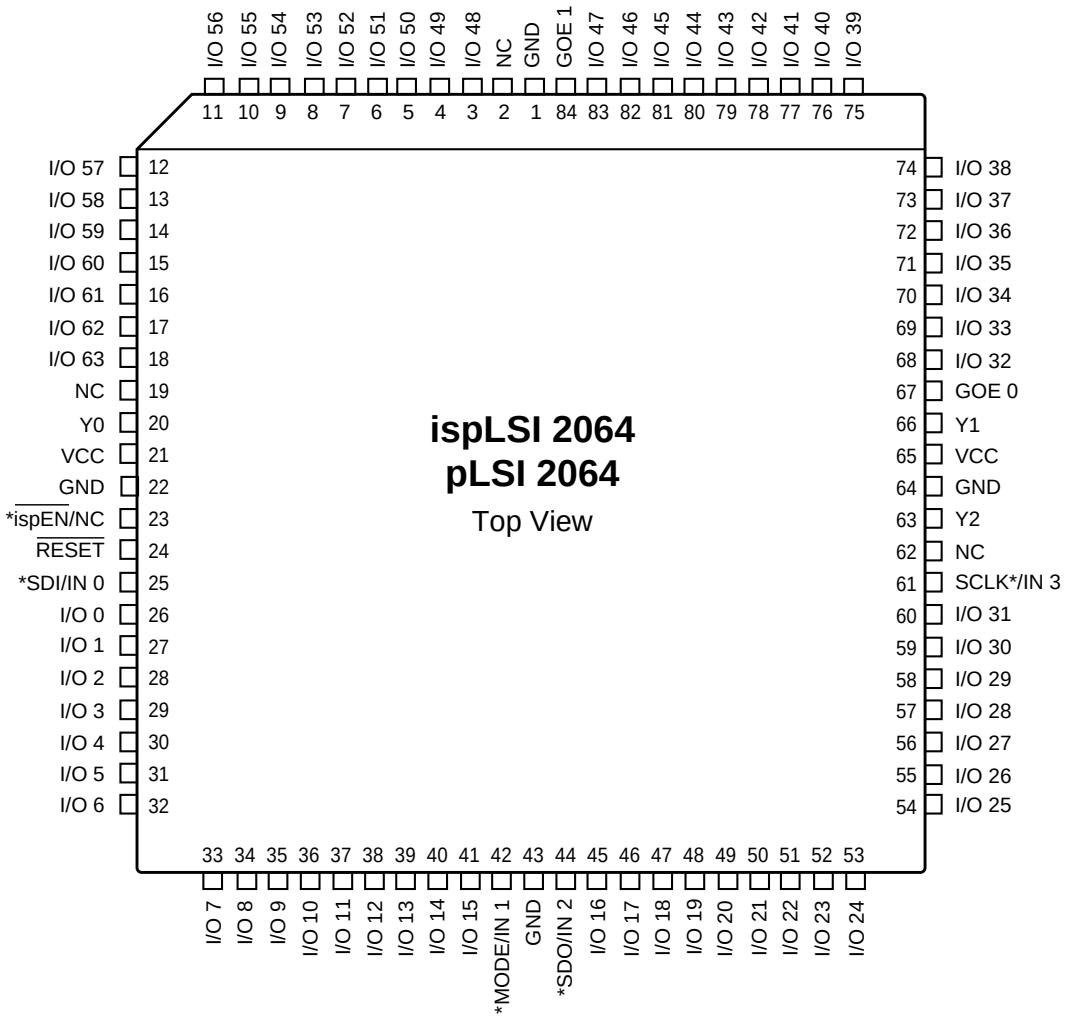
* ispLSI 2064 Only

** $\overline{\text{ispEN}}$ for ispLSI 2064 only; NC for pLSI 2064, must be left floating or tied to Vcc, must not be grounded or tied to any other signal.

Table 2- 0002-2064.eps

Pin Configuration

ispLSI and pLSI 2064 84-pin PLCC

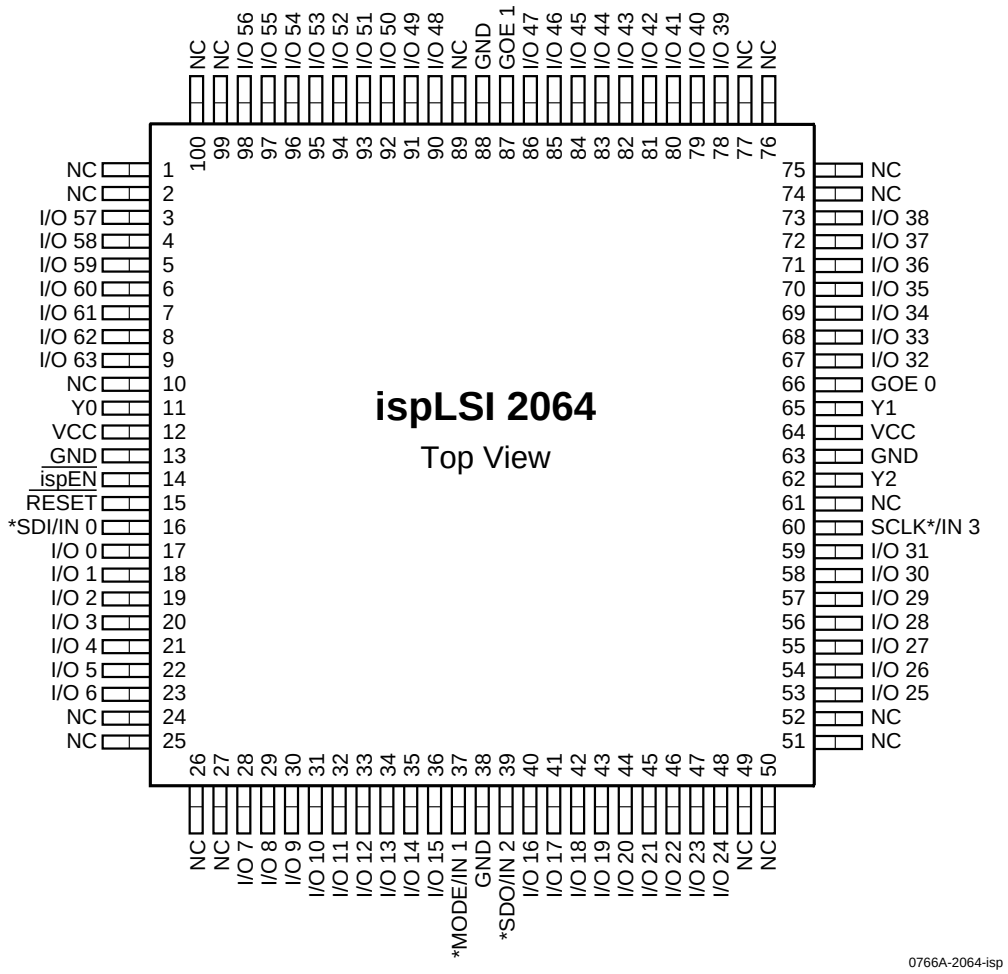


*Pins have dual function capability for ispLSI 2064 only (except pin 23, which is $\overline{\text{ispEN}}$ only).

0123A/2064

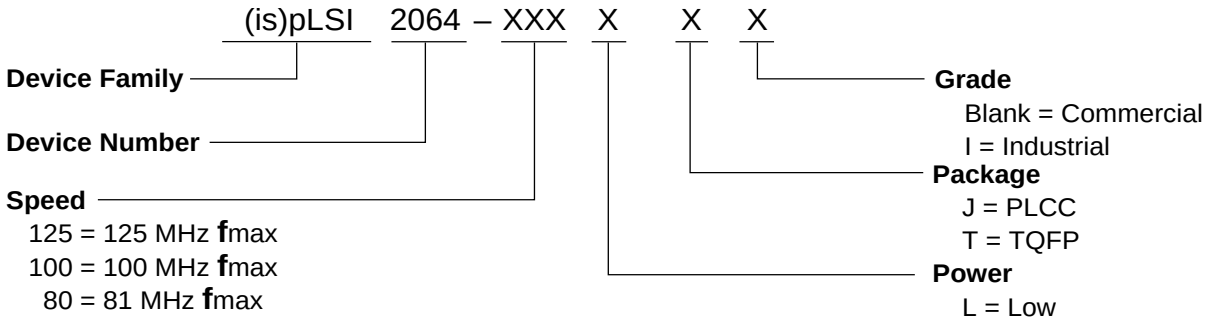
Pin Configuration

ispLSI 2064 100-pin TQFP



*Pins have dual function capability.

Part Number Description



212-80Bisp/2000

ispLSI and pLSI 2064 Ordering Information

COMMERCIAL

Device Family	fmax (MHz)	tpd (ns)	Ordering Number	Package
ispLSI	125	7.5	ispLSI 2064-125LJ	84-Pin PLCC
	125	7.5	ispLSI 2064-125LT	100-Pin TQFP
	100	10	ispLSI 2064-100LJ	84-Pin PLCC
	100	10	ispLSI 2064-100LT	100-Pin TQFP
	81	15	ispLSI 2064-80LJ	84-Pin PLCC
	81	15	ispLSI 2064-80LT	100-Pin TQFP
pLSI	125	7.5	pLSI 2064-125LJ	84-Pin PLCC
	100	10	pLSI 2064-100LJ	84-Pin PLCC
	81	15	pLSI 2064-80LJ	84-Pin PLCC

Table 2- 0041A-08isp/2000

INDUSTRIAL

Device Family	fmax (MHz)	tpd (ns)	Ordering Number	Package
ispLSI	81	15	ispLSI 2064-80LJI	84-Pin PLCC
	81	15	ispLSI 2064-80LTI	100-Pin TQFP

Table 2- 0041B-08isp/2000

ispLSI® and pLSI® 2096

High Density Programmable Logic

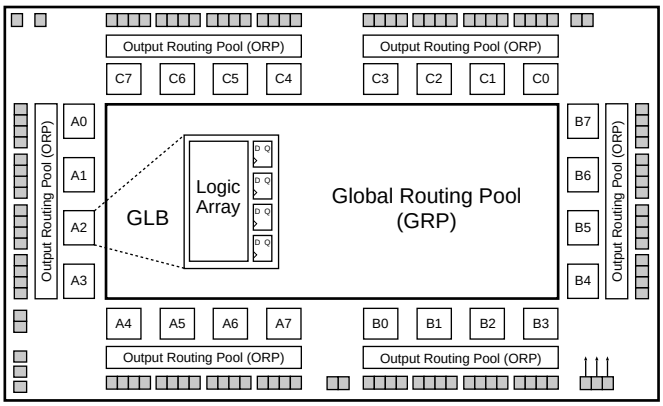
Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **— 4000 PLD Gates**
  - **— 96 I/O Pins, Six Dedicated Inputs**
  - **— 96 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 125 MHz Maximum Operating Frequency**
  - **— t_{pd} = 7.5 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Enhanced Pin Locking Capability**
  - **— Three Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI/pLSI DEVELOPMENT TOOLS**

  pDS® Software
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning**
  - **— Automatic Place and Route**
  - **— Static Timing Table**

  pDS+™ Software
  - **— Industry Standard, Third Party Design Environments**
  - **— Schematic Capture, State Machine, HDL**
  - **— Automatic Partitioning and Place and Route**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

Functional Block Diagram



0919/2096

Description

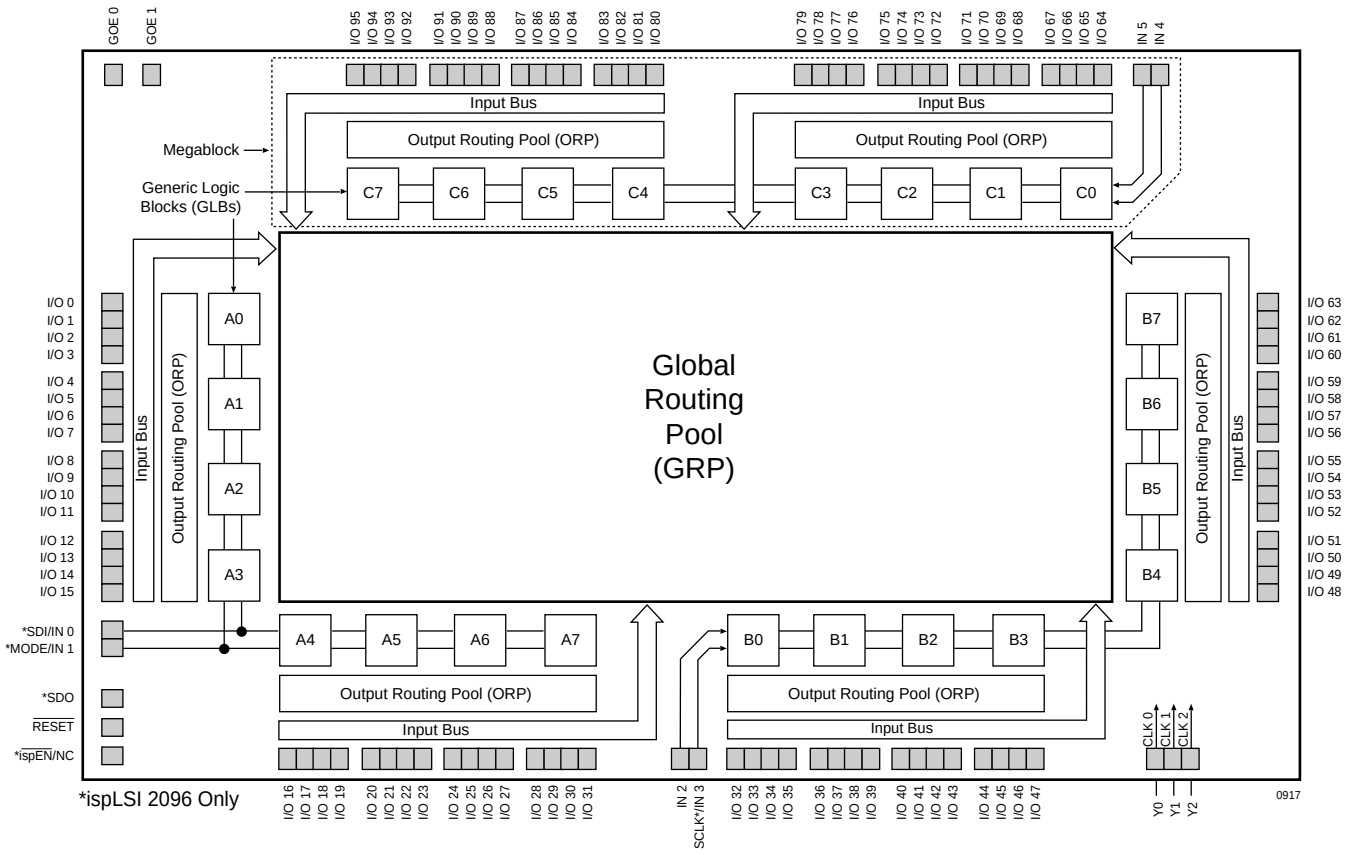
The ispLSI and pLSI 2096 are High Density Programmable Logic Devices. The devices contain 96 Registers, 96 Universal I/O pins, six Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2096 features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 2096 offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 2096 device, but multiplexes three input pins to control in-system programming.

The basic unit of logic on the ispLSI and pLSI 2096 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1…C7 (see figure 1). There are a total of 24 GLBs in the ispLSI and pLSI 2096 devices. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Functional Block Diagram

Figure 1. ispLSI and pLSI 2096 Functional Block Diagram



The devices also have 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the two ORPs. Each ispLSI and pLSI 2096 device contains three Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 2096 devices are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (TJ) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{cc}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	4.75	5.25	V
		Industrial	T_A = -40°C to + 85°C	4.5	5.5	V
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{cc}+1	V

Table 2 - 0005/2096

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL[1]	UNITS	TEST CONDITIONS
C_1	I/O and Dedicated Input Capacitance	8	pf	V_{CC} = 5.0V, $V_{I/O, IN}$ = 2.0V
C_2	Clock Capacitance	15	pf	V_{CC} = 5.0V, V_Y = 2.0V

1. Guaranteed, but not 100% tested.

Table 2-0006a

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2-0008A-isp

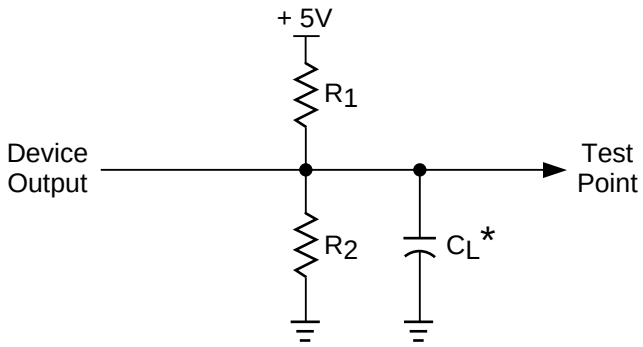
Switching Test Conditions

Input Pulse Levels	GND to 3.0V	
Input Rise and Fall Time 10% to 90%	-125	≤ 2 ns
	Others	≤ 3 ns
Input Timing Reference Levels	1.5V	
Output Timing Reference Levels	1.5V	
Output Load	See figure 2	

Table 2-0003/2096

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213a

Output Load Conditions (see figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2-0004a

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
I_{IL-isp}	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V	Commercial	–	150	295	mA
		f^{CLOCK} = 1 MHz	Industrial	–	150	–	mA

Table 2-0007a-isp/2096

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using eight 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and the Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-125		-100		-80		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	7.5	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	10.0	–	13.0	–	18.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	125	–	100	–	81	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	100	–	77	–	57	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	125	–	100	–	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	5.0	–	6.5	–	9.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	4.0	–	5.0	–	6.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	6.0	–	8.0	–	11.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	4.5	–	6.0	–	8.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	10.0	–	13.5	–	17.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	5.0	–	6.5	–	10.0	–	ns
t_{ptoeen}	B	14	Product Term OE, Enable	–	12.0	–	15.0	–	18.0	ns
$t_{ptoedis}$	C	15	Product Term OE, Disable	–	12.0	–	15.0	–	18.0	ns
t_{goeen}	B	16	Global OE, Enable	–	7.0	–	9.0	–	12.0	ns
t_{goedis}	C	17	Global OE, Disable	–	7.0	–	9.0	–	12.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	4.0	–	5.0	–	6.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	4.0	–	5.0	–	6.0	–	ns

Table 2 - 0030B/2096-125

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

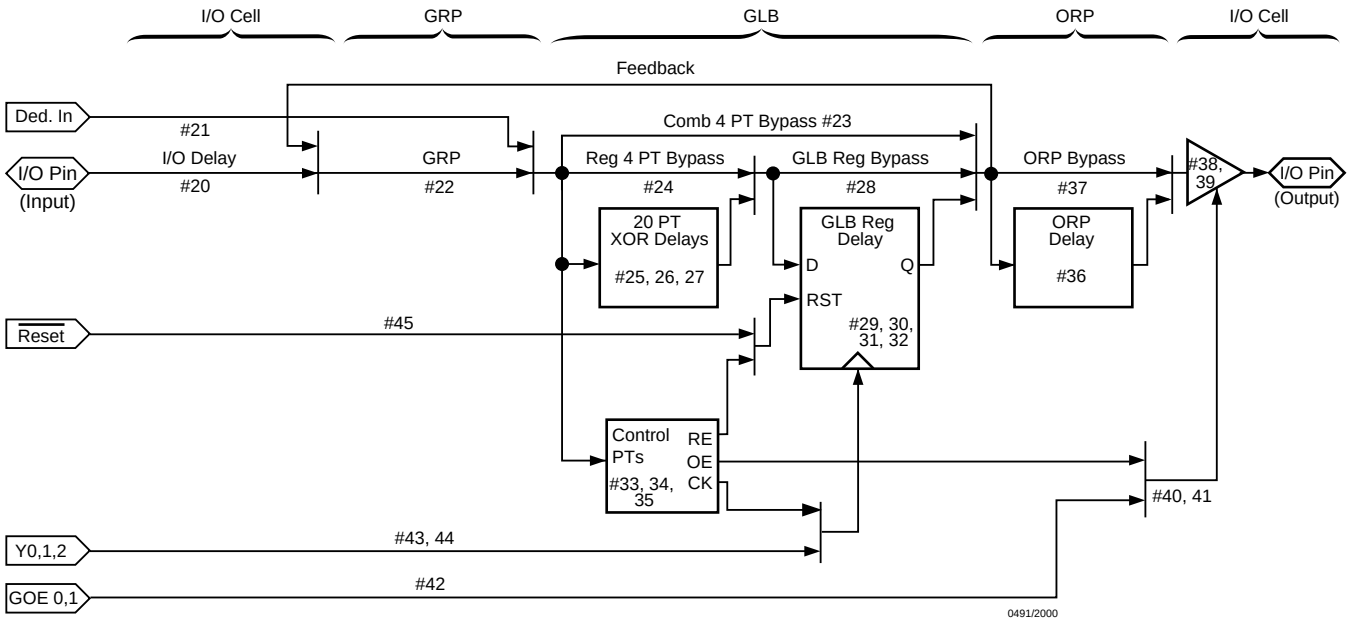
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-125		-100		-80		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t_{io}	20	Input Buffer Delay	–	0.2	–	0.5	–	1.8	ns
t_{din}	21	Dedicated Input Delay	–	1.5	–	2.2	–	4.4	ns
GRP									
t_{grp}	22	GRP Delay	–	1.3	–	1.7	–	2.6	ns
GLB									
t_{4ptbpc}	23	4 Product Term Bypass Comb. Path Delay	–	4.5	–	5.8	–	8.1	ns
t_{4ptbpr}	24	4 Product Term Bypass Reg. Path Delay	–	5.0	–	5.8	–	6.8	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	5.7	–	6.8	–	8.0	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	6.0	–	7.3	–	8.8	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	6.5	–	8.0	–	9.8	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.5	–	0.5	–	1.3	ns
t_{gsu}	29	GLB Register Setup Time before Clock	0.8	–	1.2	–	1.4	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	3.0	–	4.0	–	6.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.2	–	0.3	–	0.4	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.1	–	1.3	–	1.6	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	4.8	–	6.1	–	8.6	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	7.3	–	8.6	–	9.0	ns
t_{ptck}	35	GLB Product Term Clock Delay	3.3	5.6	4.1	7.1	5.6	10.2	ns
ORP									
t_{orp}	36	ORP Delay	–	0.8	–	1.4	–	2.0	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.3	–	0.4	–	0.5	ns
Outputs									
t_{ob}	38	Output Buffer Delay	–	1.2	–	1.6	–	2.0	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	10.0	–	10.0	–	10.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	3.2	–	4.2	–	4.6	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	3.2	–	4.2	–	4.6	ns
t_{goe}	42	Global Output Enable	–	3.8	–	4.8	–	7.4	ns
Clocks									
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. Clock)	2.3	2.3	2.7	2.7	3.6	3.6	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.3	2.3	2.7	2.7	3.6	3.6	ns
Global Reset									
t_{gr}	45	Global Reset to GLB	–	6.9	–	9.2	–	11.4	ns

Table 2-0036C/2096-125

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

ispLSI and pLSI 2096 Timing Model



Derivations of tsu, th and tco from the Product Term Clock

tsu = Logic + Reg su - Clock (min)
= (**t**io + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**io + **t**grp + **t**ptck(min))
= (#20+ #22+ #26) + (#29) - (#20+ #22+ #35)
3.5 ns = (0.2 + 1.3 + 6.0) + (0.8) - (0.2 + 1.3 + 3.3)

th = Clock (max) + Reg h - Logic
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**io + **t**grp + **t**20ptxor)
= (#20+ #22+ #35) + (#30) - (#20+ #22+ #26)
2.6 ns = (0.2 + 1.3 + 5.6) + (3.0) - (0.2 + 1.3 + 6.0)

tco = Clock (max) + Reg co + Output
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#20+ #22+ #35) + (#31) + (#36 + #38)
9.3 ns = (0.2 + 1.3 + 5.6) + (0.2) + (0.8 + 1.2)

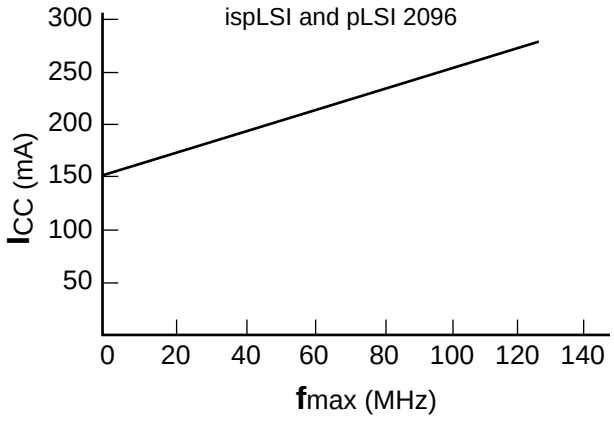
Table 2- 0042A-2096

Note: Calculations are based upon timing specifications for the ispLSI and pLSI 2096-125L.

Power Consumption

Power Consumption in the ispLSI and pLSI 2096 device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of six 16-bit counters
Typical current at 5V, 25°C

I_{CC} can be estimated for the ispLSI and pLSI 2096 using the following equation:

I_{CC}(mA) = 20 + (# of PTs * 0.67) + (# of nets * Max freq * 0.011)

Where:

# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max freq = Highest Clock Frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A-96-80-isp/2000

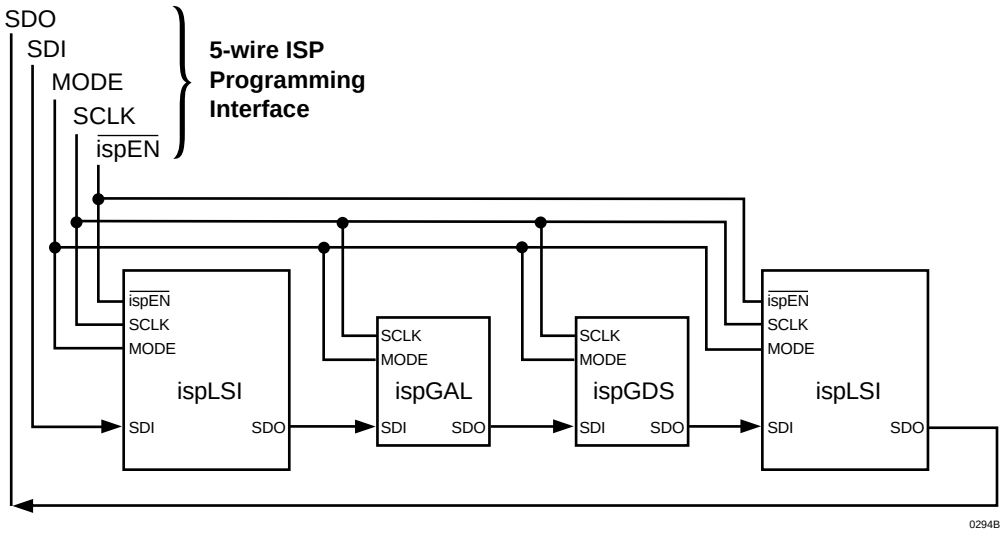
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high-density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

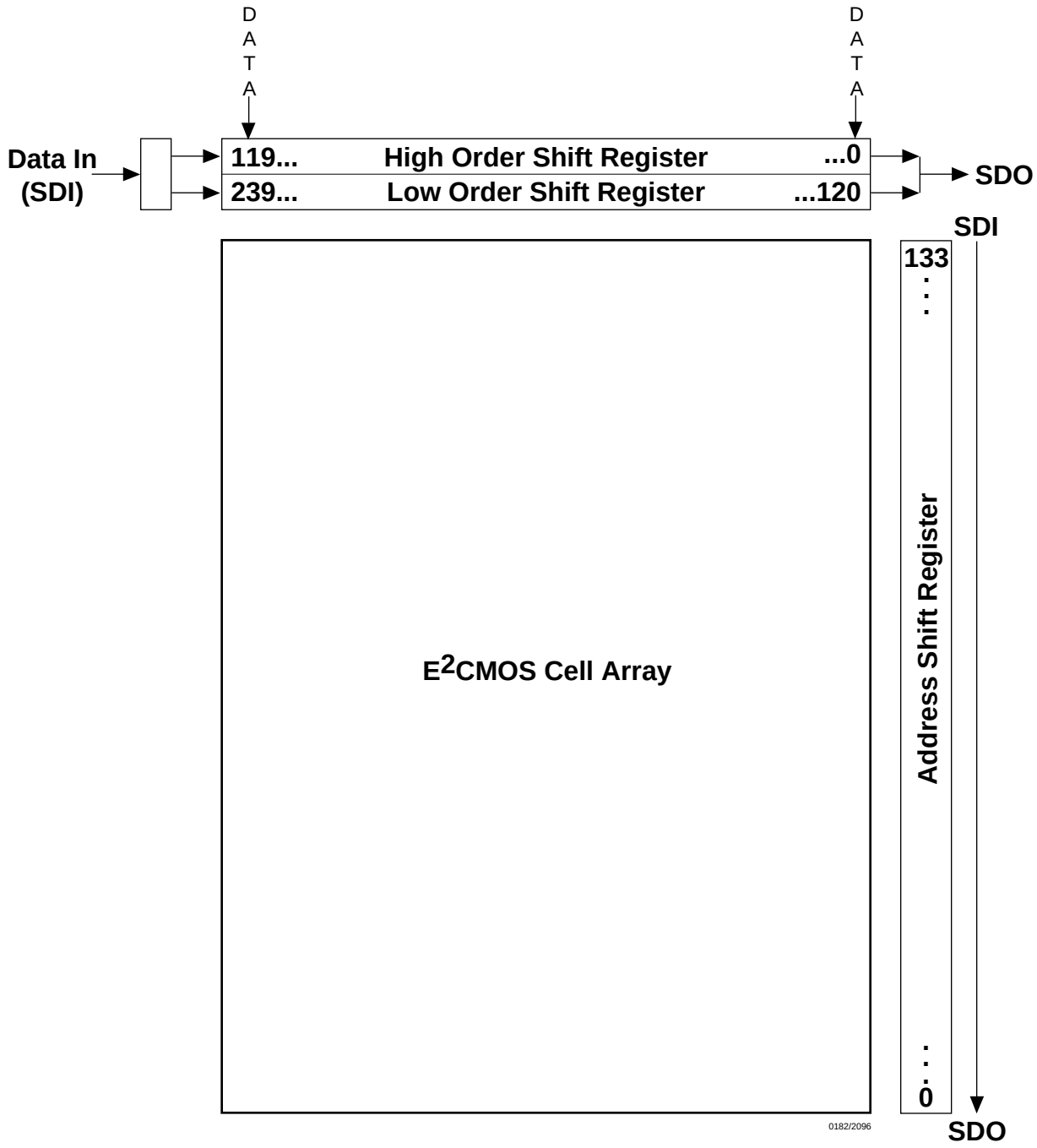
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for interface include isp Enable (ispEN), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section of this Data Book.

The device identifier for the ispLSI 2096 is 0001 0011 (13 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 2096 Shift Register Layout



Note: A logic “1” in the address shift register enables the row for programming or verification. A logic “0” disables it.

Pin Description

NAME	PQFP & TQFP* PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	21, 22, 23, 24, 25, 26 27, 28, 29, 30, 31, 32 34, 35, 36, 37, 38, 39 40, 41, 42, 43, 44, 45 52, 53, 54, 55, 56, 57 58, 59, 60, 61, 62, 63 66, 67, 68, 69, 70, 71 72, 73, 74, 75, 76, 77 85, 86, 87, 88, 89, 90 91, 92, 93, 94, 95, 96 98, 99, 100, 101, 102, 103 104, 105, 106, 107, 108, 109 117, 118, 119, 120, 121, 122 123, 124, 125, 126, 127, 128 2, 3, 4, 5, 6, 7 8, 9, 10, 11, 12, 13	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0, GOE 1	64, 114	Global Output Enables input pins.
IN 2, IN 4, IN 5	51, 84, 110	Dedicated input pins to the device.
$\overline{\text{ispEN}}$**/NC	18	Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI*/IN 0	20	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN0 also is used as one of the two control pins for the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
MODE*/IN 1	46	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
SDO**/NC	50	Output - When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK*/IN 3	78	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When ispEN is high, it functions as a dedicated input pin.
$\overline{\text{RESET}}$	19	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0, Y1, Y2	15 83, 80	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs on the device.
NC	14, 47, 79, 111, 115, 116	These pins are not used.
GND	1, 17, 33, 49, 65, 81, 97, 112	Ground (GND)
VCC	16, 48, 82, 113	V_{CC}

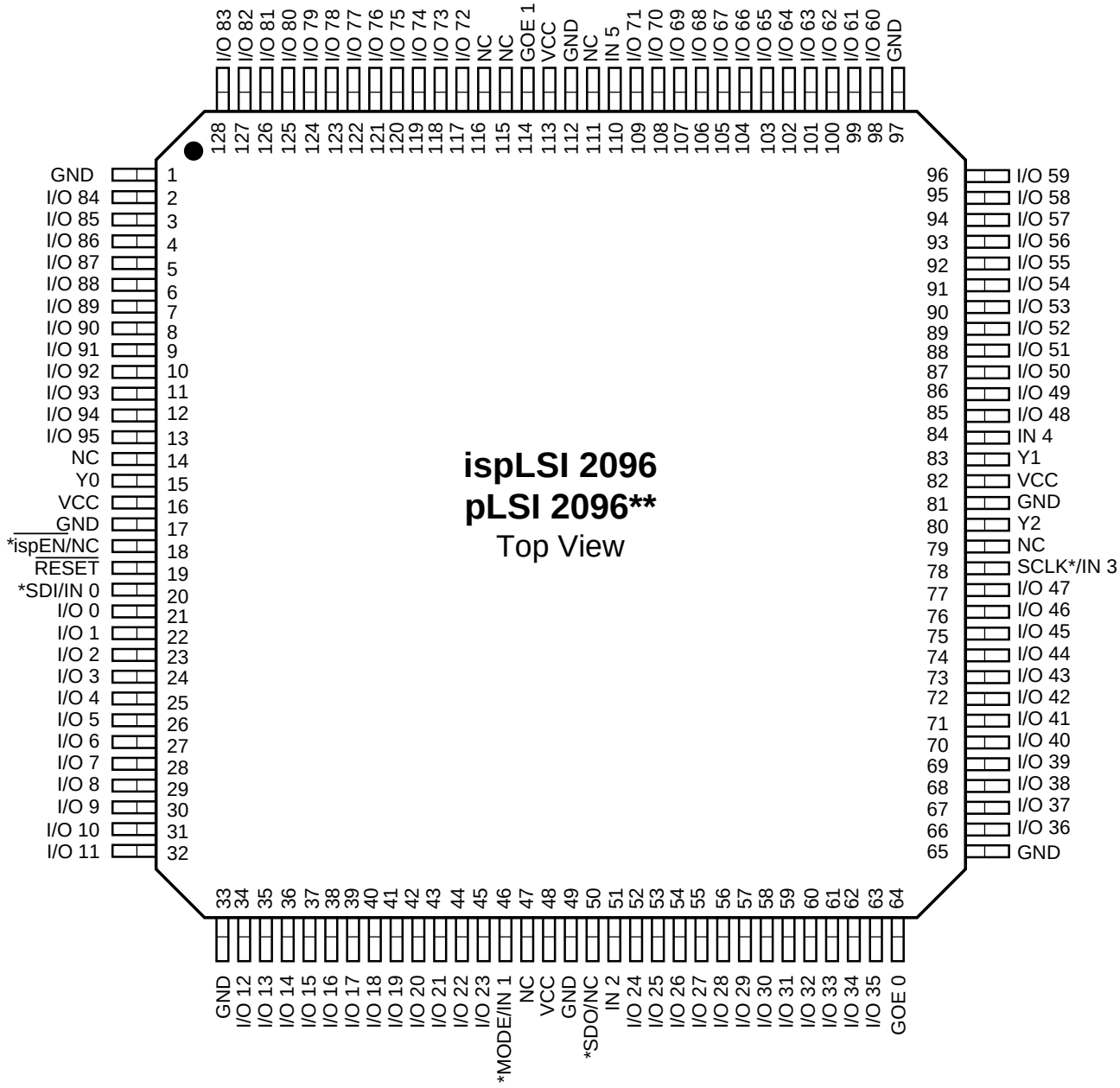
Table 2-0002-2096

* ispLSI 2096 only

** $\overline{\text{ispEN}}$ and SDO for ispLSI 2096 only; NC for pLSI 2096 must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

Pin Configuration

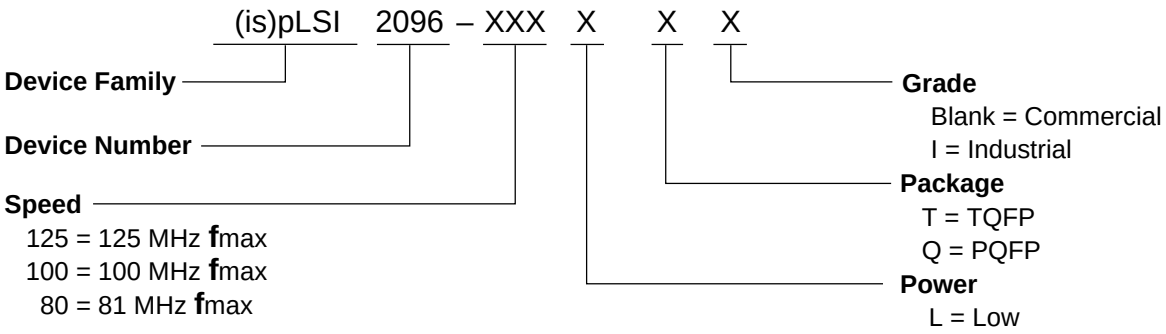
ispLSI and pLSI 2096 128-pin PQFP and TQFP



*Pins have dual function capability for ispLSI 2096 only (except pin 18 and 50, which are $\overline{\text{ispEN}}$ and SDO only, respectively).
**pLSI 2096 available in PQFP package only.

0124-2096

Part Number Description



ispLSI and pLSI 2096 Ordering Information

COMMERCIAL

DEVICE FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	125	7.5	ispLSI 2096-125LQ	128-Pin PQFP
	125	7.5	ispLSI 2096-125LT	128-Pin TQFP
	100	10	ispLSI 2096-100LQ	128-Pin PQFP
	100	10	ispLSI 2096-100LT	128-Pin TQFP
	81	15	ispLSI 2096-80LQ	128-Pin PQFP
	81	15	ispLSI 2096-80LT	128-Pin TQFP
pLSI	125	7.5	pLSI 2096-125LQ	128-Pin PQFP
	100	10	pLSI 2096-100LQ	128-Pin PQFP
	81	15	pLSI 2096-80LQ	128-Pin PQFP

Table 2- 0041A-08isp/2096

INDUSTRIAL

DEVICE FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	81	15	ispLSI 2096-80LQI	128-Pin PQFP
	81	15	ispLSI 2096-80LTI	128-Pin TQFP

Table 2- 0041B-08isp/2096

ispLSI® and pLSI® 2128

High-Density Programmable Logic

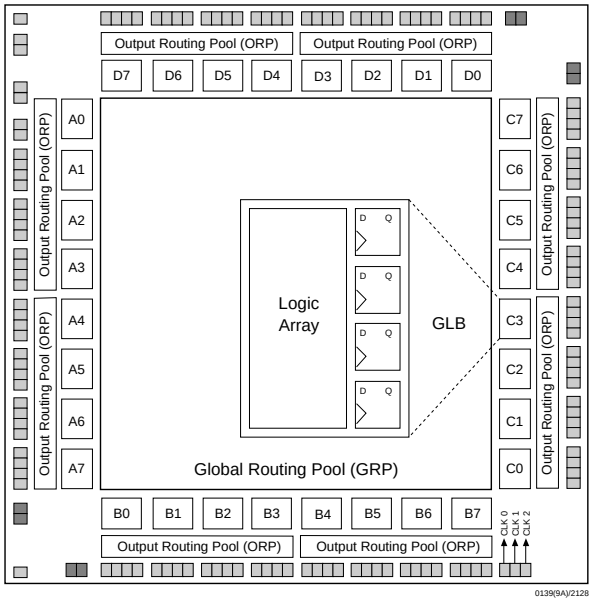
Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **— 6000 PLD Gates**
  - **— 128 I/O Pins, Eight Dedicated Inputs**
  - **— 128 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 100 MHz Maximum Operating Frequency**
  - **— t_{pd} = 10 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Enhanced Pin Locking Capability**
  - **— Three Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI/pLSI DEVELOPMENT TOOLS**

  pDS® Software
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning**
  - **— Automatic Place and Route**
  - **— Static Timing Table**

  pDS+™ Software
  - **— Industry Standard, Third Party Design Environments**
  - **— Schematic Capture, State Machine, HDL**
  - **— Automatic Partitioning and Place and Route**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

Functional Block Diagram



Description

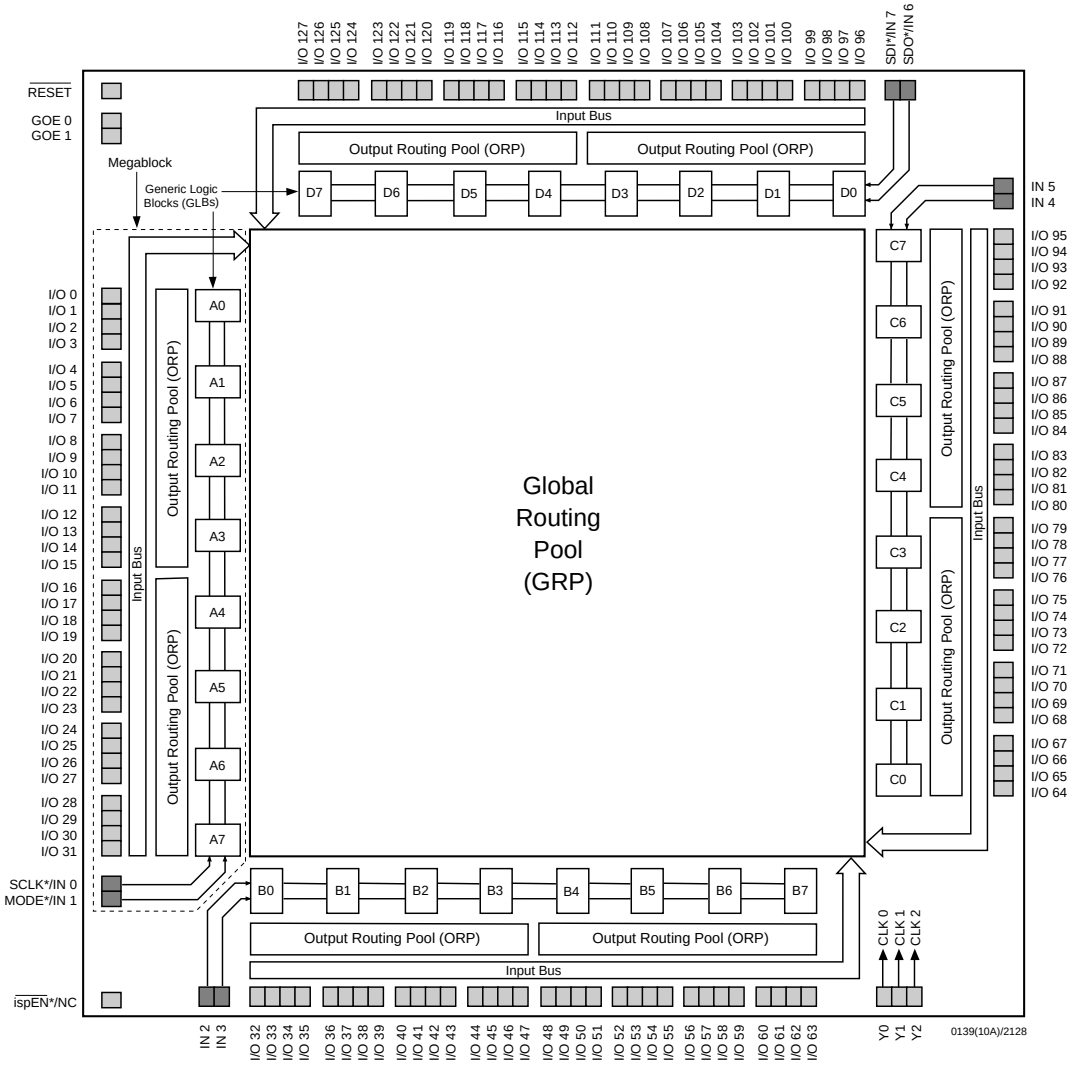
The ispLSI and pLSI 2128 are High Density Programmable Logic Devices. The devices contain 128 Registers, 128 Universal I/O pins, eight Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2128 features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 2128 offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 2128 device, but multiplexes four input pins to control in-system programming.

The basic unit of logic on the ispLSI and pLSI 2128 devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7 (see figure 1). There are a total of 32 GLBs in the ispLSI and pLSI 2128 devices. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Functional Block Diagram

Figure 1. ispLSI and pLSI 2128 Functional Block Diagram



* ispLSI 2128 Only

The devices also have 128 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the two ORPs. Each ispLSI and pLSI 2128 device contains four Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 2128 devices are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	4.75	5.25	V
		Industrial	T_A = -40°C to + 85°C	4.5	5.5	V
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{cc}+1	V

Table 2 - 0005/2128

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL[1]	UNITS	TEST CONDITIONS
C_1	I/O and Dedicated Input Capacitance	8	pf	V_{CC} = 5.0V, $V_{I/O, IN}$ = 2.0V
C_2	Clock Capacitance	15	pf	V_{CC} = 5.0V, V_Y = 2.0V

1. Guaranteed, but not 100% tested.

Table 2- 0006/2000

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2-0008A-isp

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

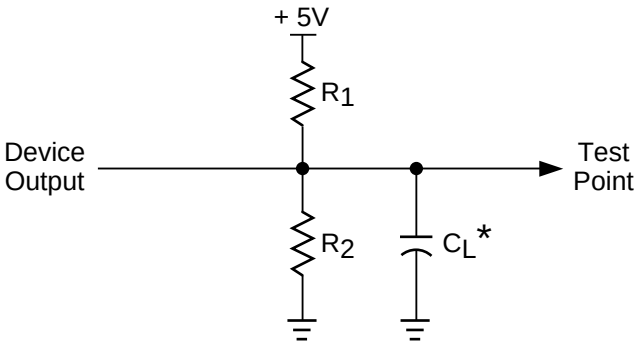
Table 2 - 0003/2000

Output Load Conditions (see figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2 - 0004A/2000

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
I_{IL-isp}	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V f_{CLOCK} = 1 MHz	Commercial	–	165	325	mA
			Industrial	–	165	–	mA

Table 2 - 0007isp/2128

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using eight 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and the Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-100		-80		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	13.0	–	18.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	100	–	81	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	77	–	57	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	100	–	83	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	6.5	–	9.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	5.0	–	6.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	8.0	–	11.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	6.0	–	8.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	13.5	–	17.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	6.5	–	10.0	–	ns
t_{ptoeen}	B	14	Product Term OE, Enable	–	15.0	–	18.0	ns
$t_{ptoedis}$	C	15	Product Term OE, Disable	–	15.0	–	18.0	ns
t_{goeen}	B	16	Global OE, Enable	–	9.0	–	12.0	ns
t_{goedis}	C	17	Global OE, Disable	–	9.0	–	12.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	5.0	–	6.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	5.0	–	6.0	–	ns

Table 2 - 0030B/2128-100

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

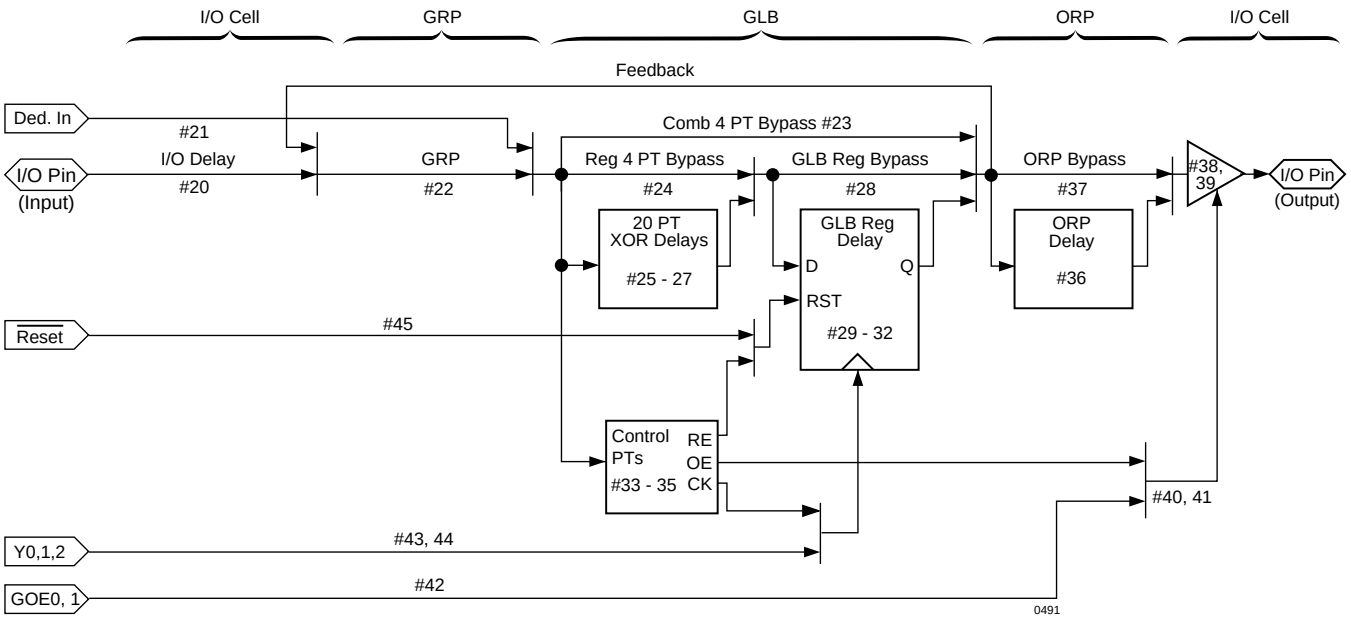
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-100		-80		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	20	Input Buffer Delay	–	0.5	–	1.8	ns
t_{din}	21	Dedicated Input Delay	–	2.2	–	4.4	ns
GRP							
t_{grp}	22	GRP Delay	–	1.7	–	2.6	ns
GLB							
t_{4ptbpc}	23	4 Product Term Bypass Path Delay	–	5.8	–	8.1	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay	–	5.8	–	6.8	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	6.8	–	8.0	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	7.3	–	8.8	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	8.0	–	9.8	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.5	–	1.3	ns
t_{gsu}	29	GLB Register Setup Time befor Clock	1.2	–	1.4	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	4.0	–	6.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.3	–	0.4	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.3	–	1.6	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	6.1	–	8.6	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	8.6	–	9.0	ns
t_{ptck}	35	GLB Product Term Clock Delay	4.1	7.1	5.6	10.2	ns
ORP							
t_{orp}	36	ORP Delay	–	1.4	–	2.0	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.4	–	0.5	ns
Outputs							
t_{ob}	38	Output Buffer Delay	–	1.6	–	2.0	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	10.0	–	10.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	4.2	–	4.6	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	4.2	–	4.6	ns
t_{goe}	42	Global Output Enable	–	4.8	–	7.4	ns
Clocks							
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.7	2.7	3.6	3.6	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.7	2.7	3.6	3.6	ns
Global Reset							
t_{gr}	45	Global Reset to GLB	–	9.2	–	11.4	ns

Table 2- 0036C/2128-100

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

ispLSI and pLSI 2128 Timing Model



Derivations of tsu, th and tco from the Product Term Clock

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**io + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**io + **t**grp + **t**ptck(min))
	=	(#20+ #22+ #26) + (#29) - (#20+ #22+ #35)
4.4 ns	=	(0.5 + 1.7 + 7.3) + (1.2) + (0.5 + 1.7 + 4.1)
th	=	Clock (max) + Reg h - Logic
	=	(**t**io + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**io + **t**grp + **t**20ptxor)
	=	(#20+ #22+ #35) + (#30) - (#20+ #22+ #26)
3.8 ns	=	(0.5 + 1.7 + 7.1) + (4.0) + (0.5 + 1.7 + 7.3)
tco	=	Clock (max) + Reg co + Output
	=	(**t**io + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#20+ #22+ #35) + (#31) + (#36 + #38)
12.6 ns	=	(0.5 + 1.7 + 7.1) + (0.3) + (1.4 + 1.6)

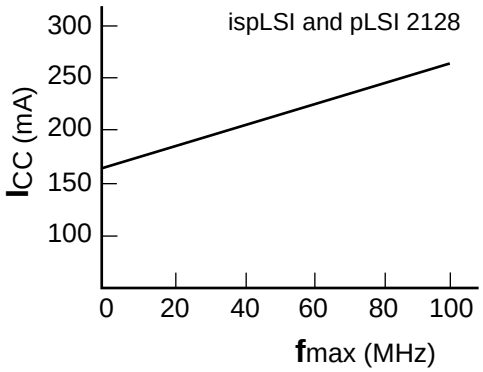
Table 2- 0042-16/2128

Note: Calculations are based upon timing specifications for the ispLSI and pLSI 2128-100L.

Power Consumption

Power Consumption in the ispLSI and pLSI 2128 device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of eight 16-bit counters
Typical current at 5V, 25° C

I_{CC} can be estimated for the ispLSI and pLSI 2128 using the following equation:

I_{CC} (mA) = 20 + (# of PTs * 0.48) + (# of nets * Max freq * 0.009)

Where:

# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max freq = Highest Clock Frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127B-16-80-isp/2128

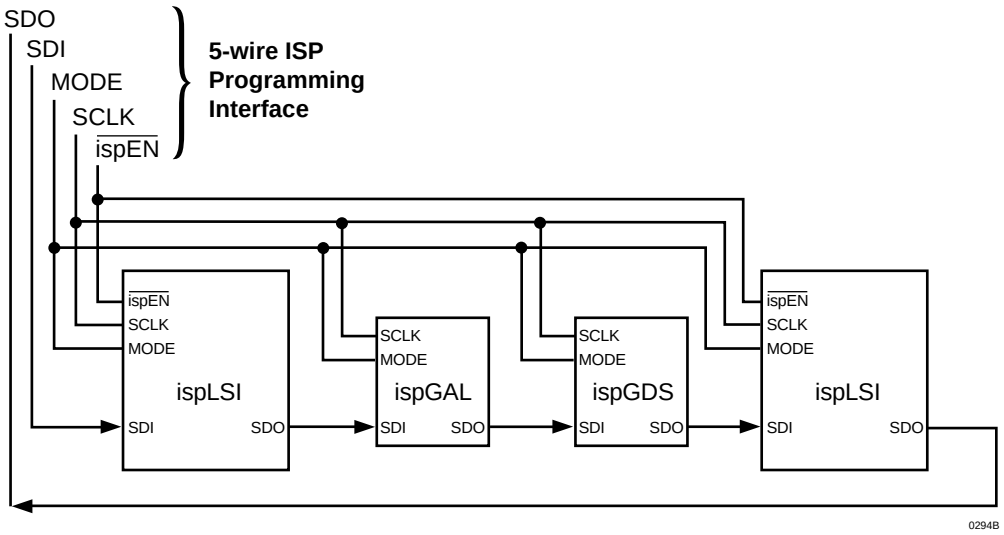
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

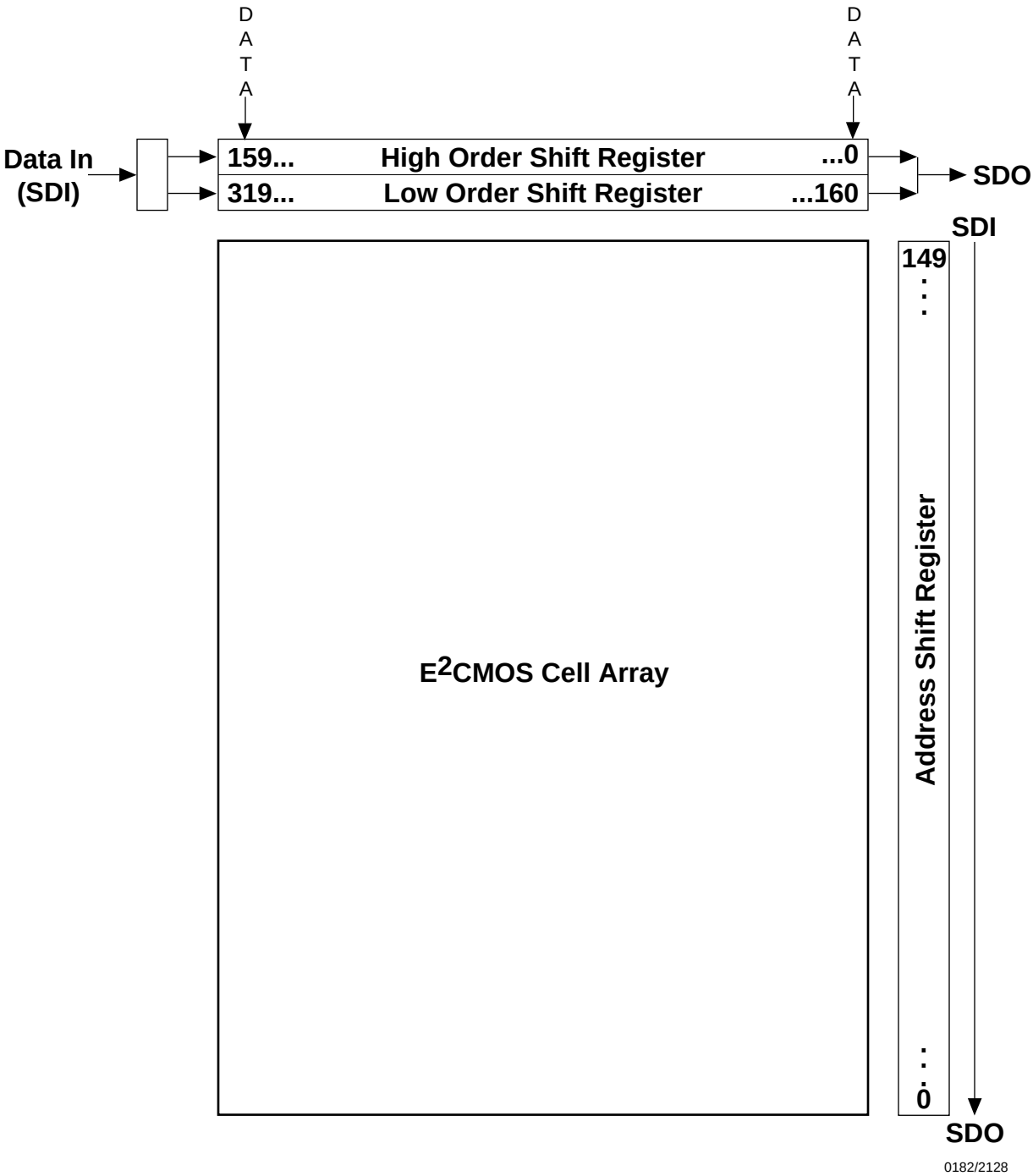
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for interface include isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section of this Data Book.

The device identifier for the ispLSI 2128 is 0001 0100 (14 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 2128 Shift Register Layout



Note: A logic "1" in the address shift register enables the row for programming or verification. A logic "0" disables it.

Pin Description

NAME	MQFP PIN NUMBERS	TQFP PIN NUMBERS*	DESCRIPTION
I/O 0 - I/O 4 I/O 5 - I/O 9 I/O 10 - I/O 14 I/O 15 - I/O 19 I/O 20 - I/O 24 I/O 25 - I/O 29 I/O 30 - I/O 34 I/O 35 - I/O 39 I/O 40 - I/O 44 I/O 45 - I/O 49 I/O 50 - I/O 54 I/O 55 - I/O 59 I/O 60 - I/O 64 I/O 65 - I/O 69 I/O 70 - I/O 74 I/O 75 - I/O 79 I/O 80 - I/O 84 I/O 85 - I/O 89 I/O 90 - I/O 94 I/O 95 - I/O 99 I/O 100 - I/O 104 I/O 105 - I/O 109 I/O 110 - I/O 114 I/O 115 - I/O 119 I/O 120 - I/O 124 I/O 125 - I/O 127	25, 26, 28, 29, 30, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 46, 47, 48, 49, 50, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 64, 65, 66, 67, 68, 69, 70, 72, 73, 74, 75, 76, 77, 78, 79, 80, 82, 83, 84, 85, 86, 87, 88, 89, 90, 92, 93, 94, 95, 96, 105, 106, 108, 109, 110, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 126, 127, 128, 129, 130, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 144, 145, 146, 147, 148, 149, 150, 152, 153, 154, 155, 156, 157, 158, 159, 160, 2, 3, 4, 5, 6, 7, 8, 9, 11, 13, 14, 15, 16, 17	27, 28, 31, 32, 33, 35, 36, 37, 38, 39, 41, 42, 43, 44, 45, 46, 47, 48, 50, 51, 52, 53, 55, 57, 58, 59, 60, 61, 62, 63, 65, 66, 67, 68, 70, 71, 72, 73, 75, 76, 77, 79, 80, 81, 82, 83, 85, 86, 87, 88, 90, 91, 92, 93, 94, 95, 96, 97, 99, 101, 102, 103, 104, 105, 115, 116, 119, 120, 121, 123, 124, 125, 126, 127, 129, 130, 131, 132, 133, 134, 135, 136, 138, 139, 140, 141, 143, 145, 146, 147, 148, 149, 150, 151, 153, 154, 155, 156, 158, 159, 160, 161, 163, 164, 165, 167, 168, 169, 170, 171, 173, 174, 175, 176, 2, 3, 4, 5, 6, 7, 8, 9, 12, 14, 15, 16, 17, 18	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 2 - IN 5	97, 98, 102, 103	106, 107, 112, 113	Dedicated input pins to the device.
GOE 0, GOE 1	100, 99,	110, 109,	Global Output Enable input pins.
$\overline{\text{RESET}}$	20	22	Active Low (0) Reset pin which resets all of the GLB registers in the device.
Y0, Y1, Y2	18, 19, 101	19, 21, 111	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device.
**$\overline{\text{ispEN}}$/NC	21	23	Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
*SDI/IN 7	22	24	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
*SCLK/IN 0	23	25	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
*MODE/IN 1	24	26	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
*SDO/IN 6	104	114	Output/Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the isp data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
GND	1, 10, 27, 45, 63, 81, 107, 125, 143	1, 11, 29, 49, 69, 89, 117, 137, 157	Ground (GND)
VCC	12, 31, 51, 71, 91, 111, 131, 151	13, 34, 56, 78, 100, 122, 144, 166	V_{CC} (+5V)

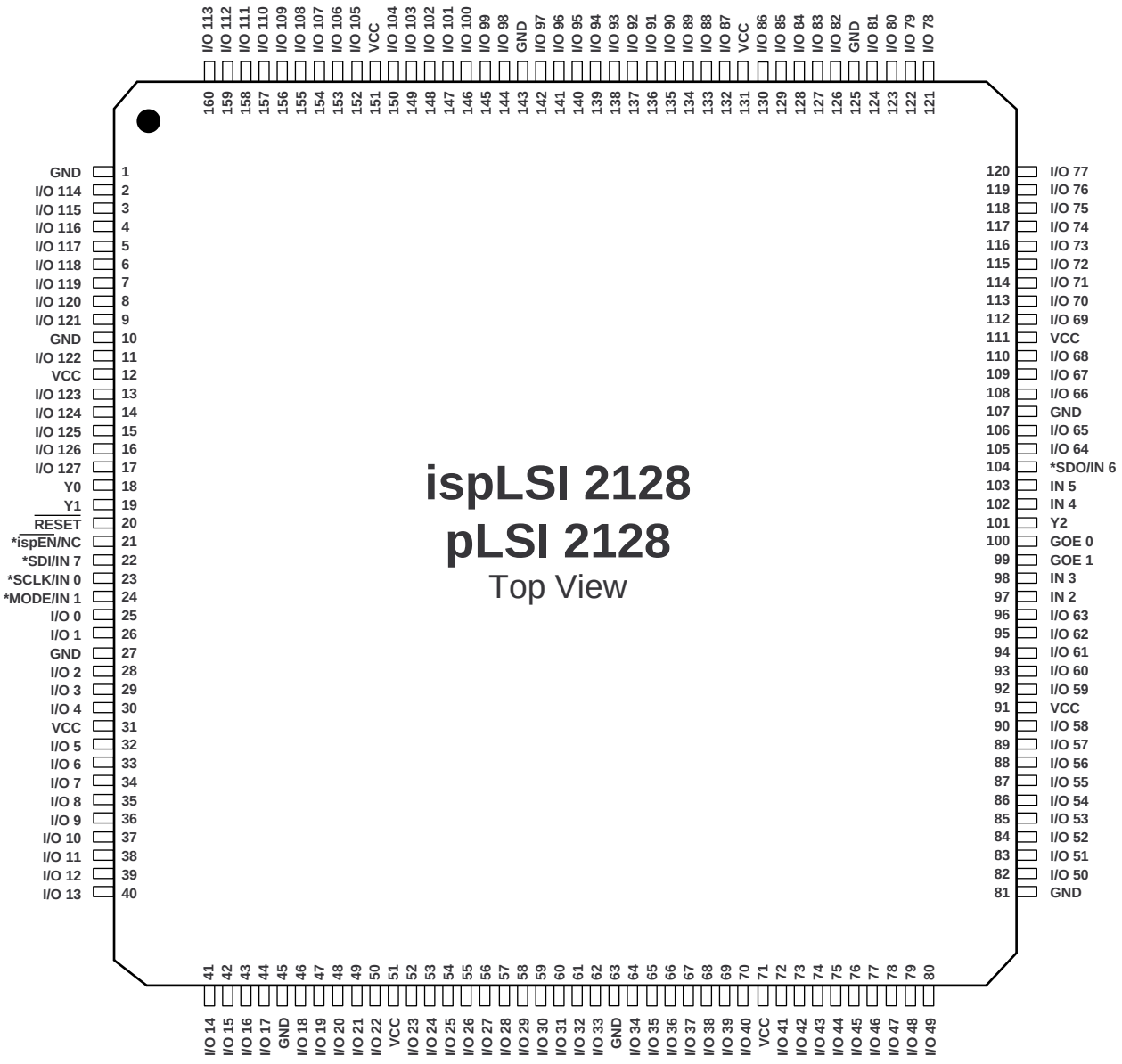
Table 2 - 0002Cisp/2128

* ispLSI 2128 only

** $\overline{\text{ispEN}}$ for ispLSI 2128 only; NC for pLSI 2128 must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

Pin Configuration

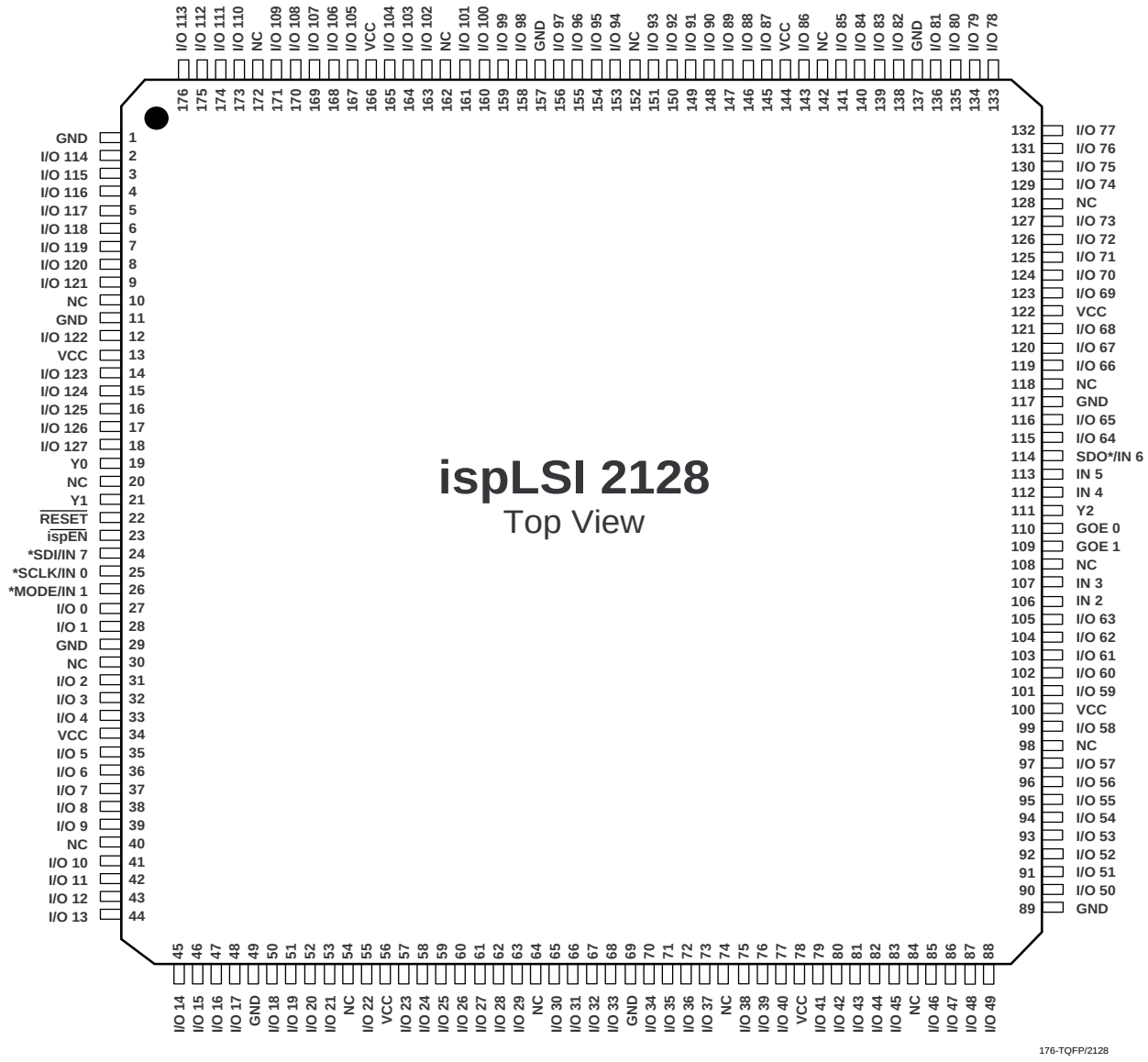
ispLSI and pLSI 2128 160-pin MQFP



* Pins have dual function capability for ispLSI 2128 only (except pin 21, which is $\overline{\text{ispEN}}$ only).

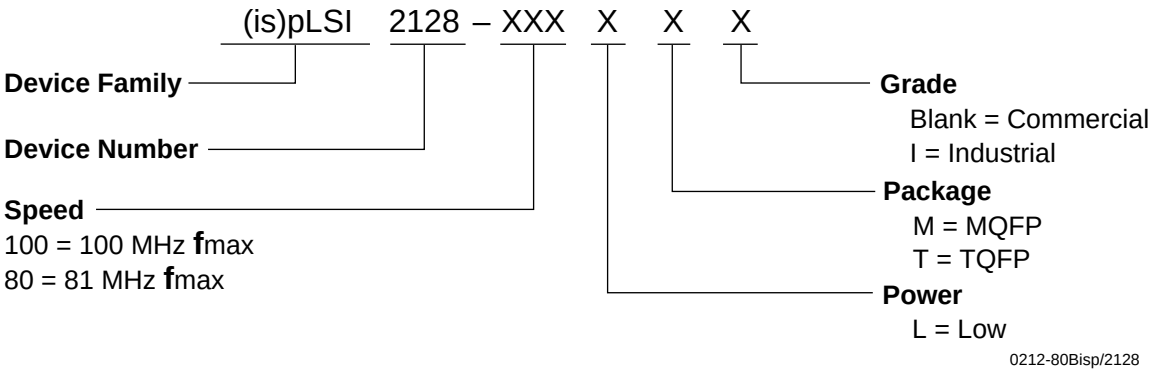
Pin Configuration

ispLSI 2128 176-pin TQFP



* Pins have dual function capability.

Part Number Description



0212-80Bisp/2128

ispLSI and pLSI 2128 Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	100	10	ispLSI 2128-100LM	160-Pin MQFP
	100	10	ispLSI 2128-100LT	176-Pin TQFP
	81	15	ispLSI 2128-80LM	160-Pin MQFP
	81	15	ispLSI 2128-80LT	176-Pin TQFP
pLSI	100	10	pLSI 2128-100LM	160-Pin MQFP
	81	15	pLSI 2128-80LM	160-Pin MQFP

Table 2 - 0041A-08isp/2128

INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	81	15	ispLSI 2128-80LTI	176-Pin TQFP

Table 2 - 0041B-08isp/2128

ispLSI® and pLSI® 2032LV

3.3V High Density Programmable Logic

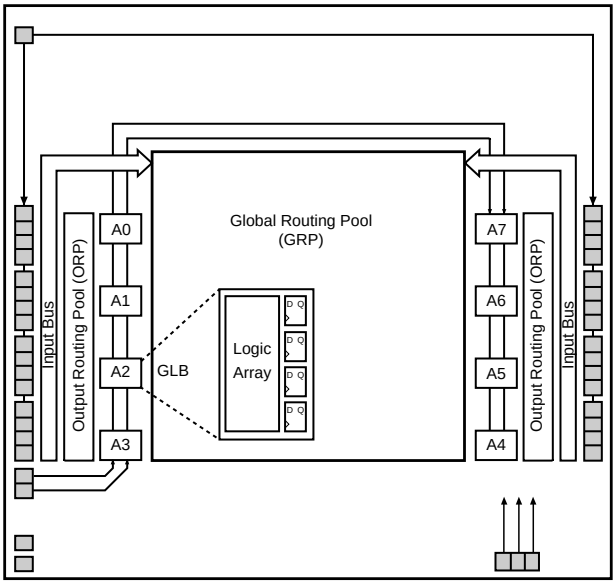
Features

- **3.3V LOW VOLTAGE 2032 ARCHITECTURE**
  - **— Interfaces With Standard 5V TTL Devices**
  - **— 60 mA Typical Active Current**
  - **— Fuse Map Compatible with 5V ispLSI/pLSI 2032**
- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **— 1000 PLD Gates**
  - **— 32 I/O Pins, Two Dedicated Inputs**
  - **— 32 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 80 MHz Maximum Operating Frequency**
  - **— t_{pd} = 10 ns Propagation Delay**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— 3.3V In-System Programmability™ Using Boundary Scan Test Access Port (TAP)**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Prototyping**
- **THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FPGAs**
  - **— Enhanced Pin Locking Capability**
  - **— Three Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI/pLSI DEVELOPMENT TOOLS**

pDS® Software
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning, Automatic Place and Route**
  - **— Static Timing Table**

pDS+™ Software
  - **— Industry Standard, Third Party Design Environments**
  - **— Schematic Capture, State Machine, HDL**
  - **— Automatic Partitioning and Place and Route**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

Functional Block Diagram



Description

The ispLSI and pLSI 2032LV are High Density Programmable Logic Devices that can be used in both 3.3V and 5V systems. The devices contain 32 Registers, 32 Universal I/O pins, two Dedicated Input Pins, three Dedicated Clock Input Pins, one dedicated Global OE input pin and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2032LV features in-system programmability through the Boundary Scan Test Access Port (TAP). The ispLSI 2032LV offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 2032LV device, but multiplexes four input pins to control in-system programming.

The basic unit of logic on the ispLSI and pLSI 2032LV devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. A7 (see figure 1). There are a total of eight GLBs in the ispLSI and pLSI 2032LV devices. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are

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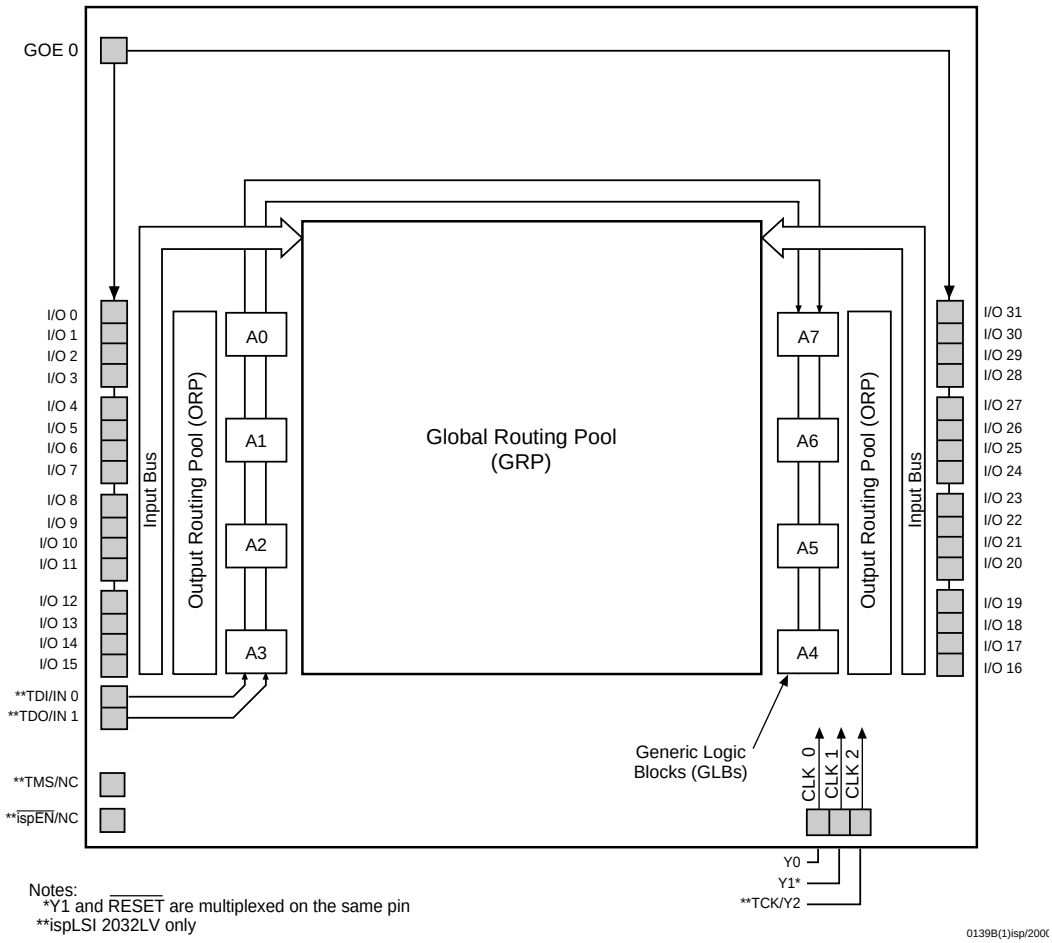
Functional Block Diagram

Figure 1. ispLSI and pLSI 2032LV Functional Block Diagram



brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

The devices also have 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. Device pins can be safely driven to 5 Volt signal levels to support mixed-voltage systems.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the ORP. Each ispLSI and pLSI 2032LV device contains one Megablock.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI and pLSI 2032LV devices are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +5.6V

Input Voltage Applied ..... -0.5 to +5.6V

Off-State Output Voltage Applied ..... -0.5 to +5.6V

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	3.0	3.6	V
		Industrial	T_A = -40°C to + 85°C	3.0	3.6	V
V_{IL}	Input Low Voltage			V_{SS} – 0.5	0.8	V
V_{IH}	Input High Voltage			2.0	5.25	V

Table 2 - 0005/2032LV

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL[1]	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	V_{CC} = 3.3V, V_{IN} = 2.0V
C_2	I/O Capacitance	8	pf	V_{CC} = 3.3V, $V_{I/O}$ = 2.0V
C_3	Clock Capacitance	13	pf	V_{CC} = 3.3V, V_Y = 2.0V

1. Guaranteed, but not 100% tested.

Table 2 - 0006

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2-0008A-isp

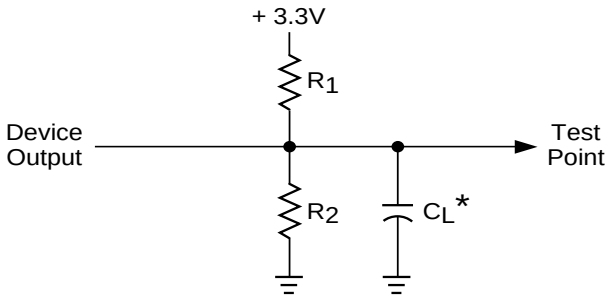
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time 10% to 90%	≤ 1.5 ns
Input Timing Reference Levels	1.5V
Ouput Timing Reference Levels	1.5V
Output Load	See figure 2

Table 2 - 0003/2032

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A

Output Load Conditions (see figure 2)

TEST CONDITION		R1	R2	CL
A		316Ω	348Ω	35pF
B	Active High	∞	348Ω	35pF
	Active Low	316Ω	348Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	348Ω	5pF
	Active Low to Z at V_{OL}+0.5V	316Ω	348Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V ≤ V_{IN}(Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	(V_{CC} - 0.2)V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
		V_{CC} ≤ V_{IN} ≤ 5.25V		–	–	50	mA
I_{IL-isp}	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V, V_{OUT} = 0.5V		–	–	-100	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V f_{TOGGLE} = 1 MHz	Commercial	–	60	–	mA
			Industrial	–	60	–	mA

Table 2 - 0007Aisp/2032.b

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using two 16-bit counters.
3. Typical values are at V_{CC} = 3.3V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to Power Consumption section of this data sheet and Thermal Management section of this Data Book to estimate Maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-80		-60		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	15.0	–	20.0	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	80.0	–	60.0	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	64.5	–	50.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	100	–	71.4	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	6.0	–	7.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	8.0	–	10.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	7.5	–	10.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	9.0	–	12.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	14.0	–	16.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	7.0	–	8.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	15.0	–	18.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	15.0	–	18.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	10.0	–	12.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	10.0	–	12.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	5.0	–	7.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	5.0	–	7.0	–	ns

Table 2 - 0030B/2032LV-150

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

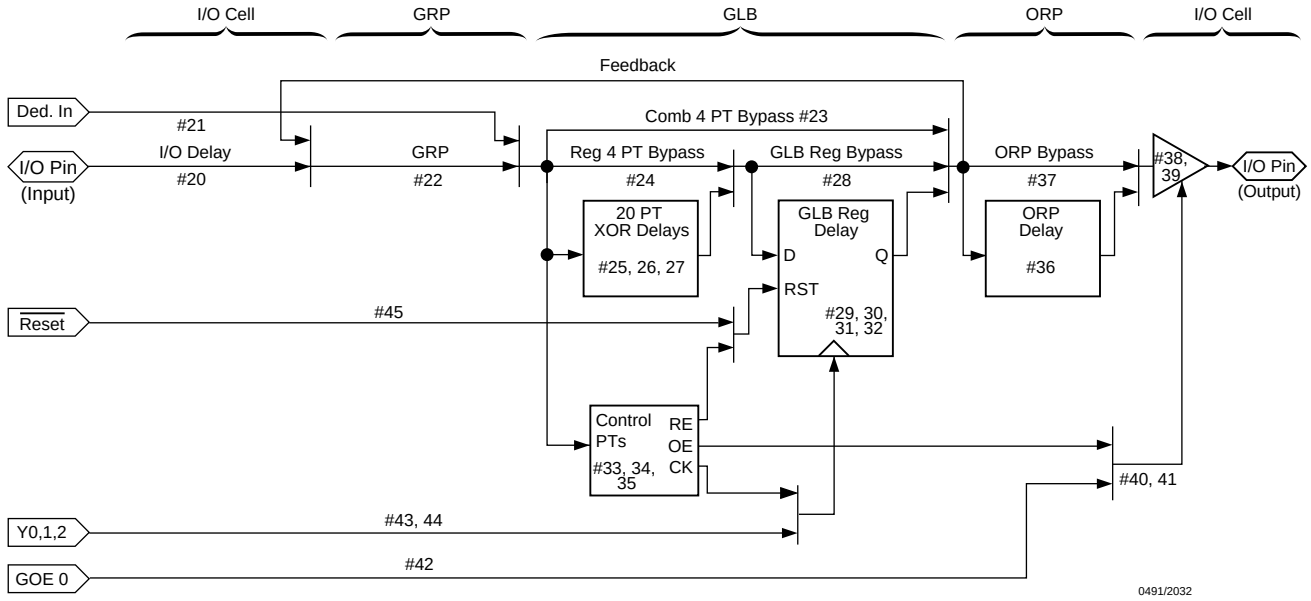
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-80		-60		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	20	Input Buffer Delay	–	0.9	–	1.3	ns
t_{din}	21	Dedicated Input Delay	–	1.9	–	2.8	ns
GRP							
t_{grp}	22	GRP Delay	–	1.3	–	1.9	ns
GLB							
t_{4ptbpc}	23	4 Product Term Bypass Path Delay (Combinatorial)	–	5.0	–	8.3	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay (Registered)	–	7.2	–	7.9	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	9.4	–	12.4	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	8.7	–	10.9	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	9.8	–	12.4	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.3	–	0.4	ns
t_{gsu}	29	GLB Register Setup Time befor Clock	0.4	–	0.8	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	3.7	–	4.3	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	1.4	–	1.6	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	2.7	–	2.9	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	5.6	–	8.5	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	7.4	–	9.1	ns
t_{ptck}	35	GLB Product Term Clock Delay	4.8	6.6	6.2	9.0	ns
ORP							
t_{orp}	36	ORP Delay	–	1.7	–	2.8	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.7	–	0.8	ns
Outputs							
t_{ob}	38	Output Buffer Delay	–	2.1	–	2.7	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	12.1	–	12.7	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	5.4	–	5.7	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	5.4	–	5.7	ns
t_{goe}	42	Global Output Enable	–	4.6	–	6.3	ns
Clocks							
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	3.8	3.8	4.9	4.9	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	3.8	3.8	4.9	4.9	ns
Global Reset							
t_{gr}	45	Global Reset to GLB	–	7.5	–	7.6	ns

Table 2- 0036C/2032-150a

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

ispLSI and pLSI 2032LV Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**io + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**io + **t**grp + **t**ptck(min))
	=	(#20+ #22+ #26) + (#29) - (#20+ #22+ #35)
4.3 ns	=	(0.9 + 1.3 + 8.7) + (0.4) - (0.9 + 1.3 + 4.8)
th	=	Clock (max) + Reg h - Logic
	=	(**t**io + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**io + **t**grp + **t**20ptxor)
	=	(#20+ #22+ #35) + (#30) - (#20+ #22+ #26)
1.6 ns	=	(0.9 + 1.3 + 6.6) + (3.7) - (0.9 + 1.3 + 8.7)
tco	=	Clock (max) + Reg co + Output
	=	(**t**io + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#20+ #22+ #35) + (#31) + (#36 + #38)
14 ns	=	(0.9 + 1.3 + 6.6) + (1.4) + (1.7 + 2.1)

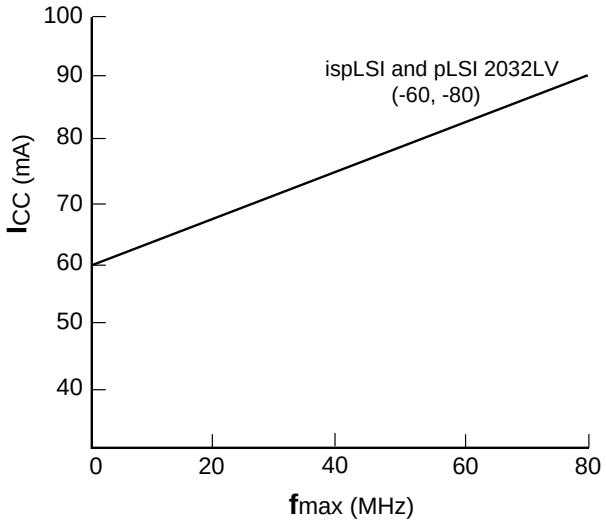
Note: Calculations are based upon timing specifications for the ispLSI and pLSI 2032LV-80.

Table 2- 0042-16/2032

Power Consumption

Power consumption in the ispLSI and pLSI 2032LV device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of two 16-bit counters
Typical current at 5V, 25° C

I_{CC} can be estimated for the ispLSI and pLSI 2032LV using the following equation:

For 2032LV -80, -60: $I_{CC}(mA) = 15 + (\#\ of\ PTs * 0.70) + (\#\ of\ nets * Max\ freq * 0.012)$

Where:
# of PTs = Number of product terms used in design
# of nets = Number of signals used in device
Max freq = Highest clock frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 3.3V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127A-16-80-isp/2000

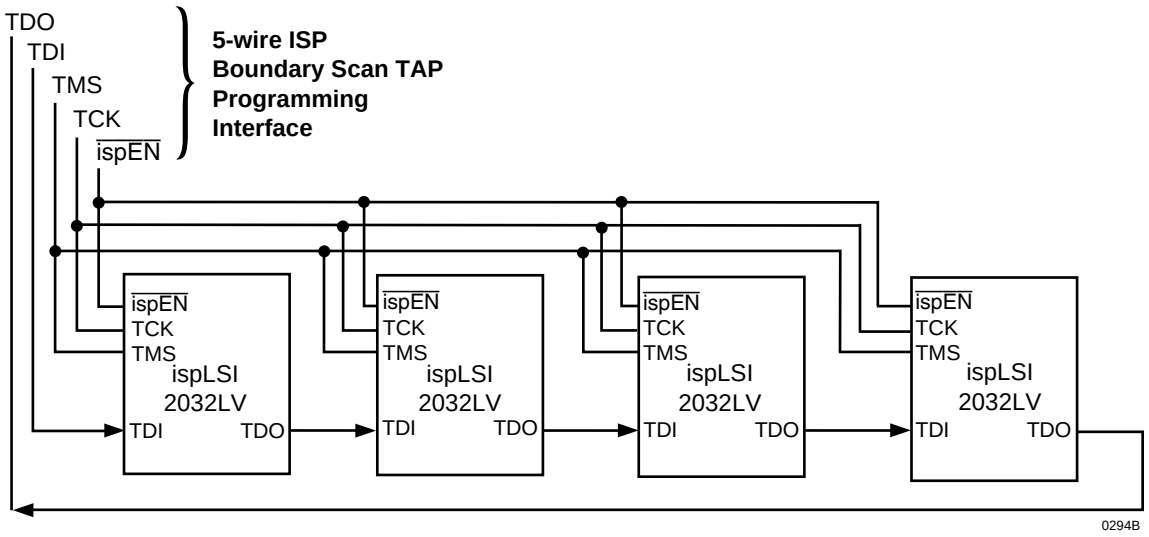
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

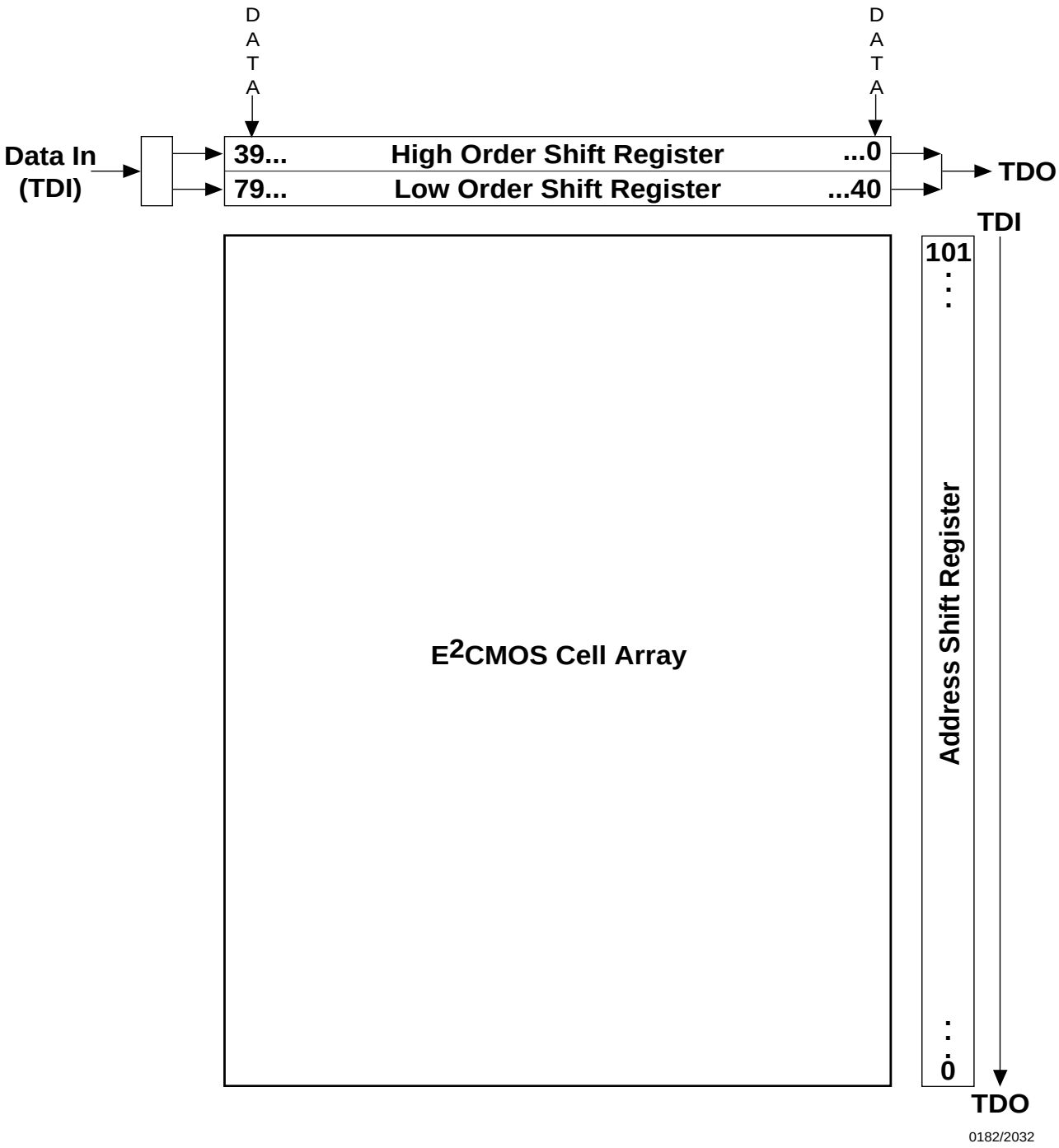
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for the TAP interface include ISP Enable ($\overline{\text{ispEN}}$), Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK) and Test Mode Select (TMS). Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI 2032LV devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section of this Data Book.

The device identifier for the ispLSI 2032LV is 00301043 hex. This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 2032LV Shift Register Layout



Note: A logic "1" in the address shift register enables the row for programming or verification. A logic "0" disables it.

Pin Description

NAME	PLCC PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0	2	Global Output Enable input pin.
Y0	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs on the device.
$\overline{\text{RESET}}$/Y1	35	This pin performs two functions: - Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. - Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
$\overline{\text{ispEN}}$**/NC	13	Input - Dedicated in-system programming Boundary Scan Enable input pin. This pin is brought low to enable the programming mode. The TMS, TDI, TDO and TCK controls become active.
TDI*/IN 0	14	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. TDI/IN0 also is used as one of the two control pins for the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
TMS*/NC	36	Input - When in ISP Mode, controls operation of ISP state-machine.
TDO*/IN 1	24	Output/Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
TCK*/Y2	33	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated clock input.This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device.
GND	1, 23	Ground (GND)
VCC	12, 34	V_{CC}

Table 2 - 0002A-08isp/2000

* ispLSI 2032LV only

** $\overline{\text{ispEN}}$ for ispLSI 2032LV only; NC for pLSI 2032LV must be left floating or tied to V_{CC}, and must not be grounded or tied to any other signal.

Pin Description

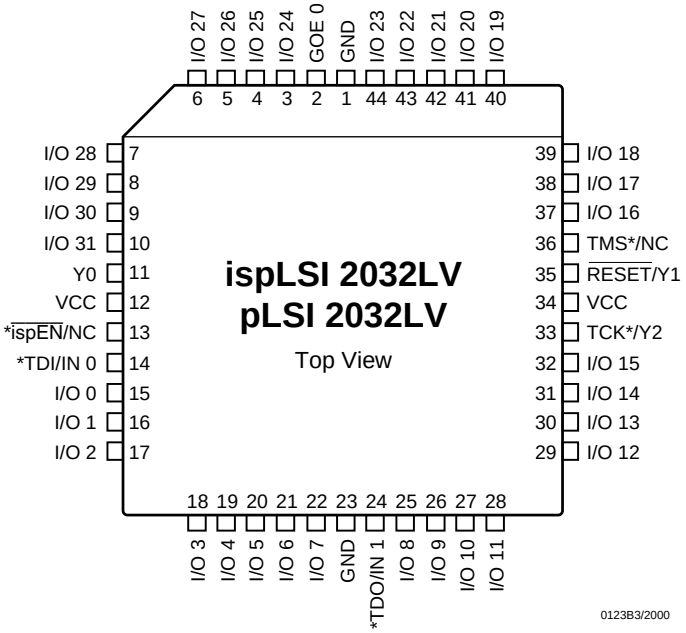
NAME	TQFP PIN NUMBERS*	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	9, 10, 11, 12, 13, 14, 15, 16, 19, 20, 21, 22, 23, 24, 25, 26, 31, 32, 33, 34, 35, 36, 37, 38, 41, 42, 43, 44, 1, 2, 3, 4	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0	40	Global Output Enable input pin.
Y0	5	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs on the device.
$\overline{\text{RESET}}$/Y1	29	This pin performs two functions: - Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device. - Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
$\overline{\text{ispEN}}$	7	Input - Dedicated in-system programming Boundary Scan enable input pin. This pin is brought low to enable the programming mode. The TMS, TDI, TDO and TCK controls become active.
TDI/IN 0	8	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. TDI/IN0 also is used as one of the two control pins for the isp state machine. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
TMS	30	Input - When in ISP Mode, controls operation of ISP state-machine.
TDO/IN 1	18	Output/Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{ispEN}}$ is high, it functions as a dedicated input pin.
TCK/Y2	27	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.It is a dedicated clock input when $\overline{\text{ispEN}}$ is logic high. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O cell on the device.
GND	17, 39	Ground (GND)
VCC	6, 28	V_{CC}

Table 2 - 0002B-2032

* ispLSI 2032LV only

Pin Configuration

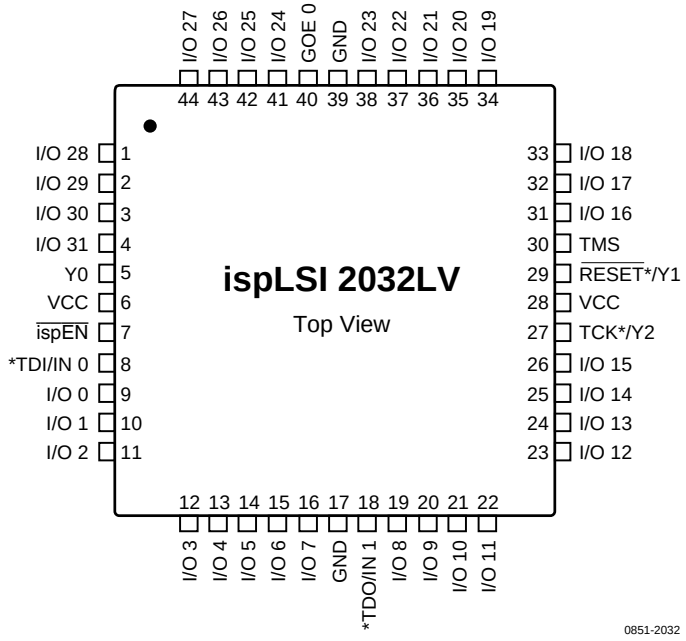
ispLSI and pLSI 2032LV 44-pin PLCC



* Pins have dual function capability for ispLSI 2032LV only (except pin 13, which is ispEN only).

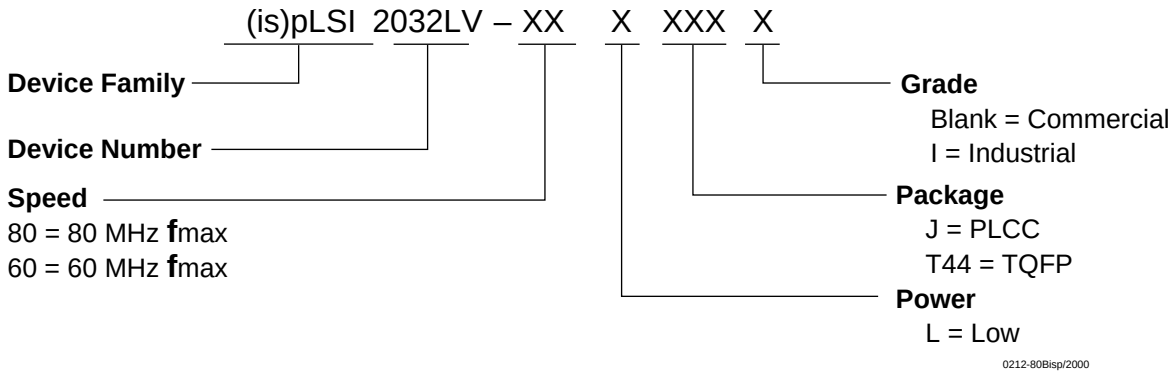
Pin Configuration

ispLSI 2032LV 44-pin TQFP



* Pins have dual function capability.

Part Number Description



ispLSI and pLSI 2032LV Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	80	10	ispLSI 2032LV-80LJ	44-Pin PLCC
	80	10	ispLSI 2032LV-80LT44	44-Pin TQFP
	60	15	ispLSI 2032LV-60LJ	44-Pin PLCC
	60	15	ispLSI 2032LV-60LT44	44-Pin TQFP
pLSI	80	10	pLSI 2032LV-80LJ	44-Pin PLCC
	60	15	pLSI 2032LV-60LJ	44-Pin PLCC

Table 2-0041A-08isp/2000

INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	60	15	ispLSI 2032LV-60LJI	44-Pin PLCC
	60	15	ispLSI 2032LV-60LT44I	44-Pin TQFP

Table 2-0041B-08isp/2000

Introduction to ispLSI® and pLSI® 3000 Family

Introduction

Lattice Semiconductor Corporation's (LSC) ispLSI and pLSI families are high-density and high-performance E^2CMOS® programmable logic devices. They provide design engineers with a superior system solution for integrating high-speed logic on a single chip.

The ispLSI and pLSI 3000 Families are the third generation to combine the performance and ease of use of PLDs with the density and flexibility of FPGAs. This family is ideal for high density designs, where integration of complete logic subsystems into a single device is necessary.

The ispLSI family incorporates Lattice Semiconductor's innovative in-system programmable™ (ISP™) technology. ISP technology allows for real-time programming, less expensive manufacturing and end-user feature reconfiguration.

E^2CMOS technology features reprogrammability, the ability to program the device again and again to easily incorporate any design modifications. This same capability allows full parametric testability during manufacturing, which guarantees 100 percent programming and functional yield.

All necessary development tools are available from LSC and third-party vendors. Development tools offered range from LSC's low cost pDS® software, featuring Boolean entry in a graphical Windows™ based environment, to the pDS+™ family of Fitters that interface with third party development software packages. pDS+ systems support schematic capture, state machine, Boolean, and HDL Design entry. Designs can now be completed in hours as opposed to days or weeks.

ispLSI and pLSI 3000 Family

- ❑ 100 MHz System Performance
- ❑ 10 ns Pin-to-Pin Delay
- ❑ Deterministic Performance
- ❑ High Density (8000 - 14,000 PLD Gates)
- ❑ 160-Pin to 240-Pin Package Options
- ❑ Flexible Easy-to-Use Architecture
- ❑ In-System Programmable (ispLSI)
- ❑ Boundary Scan (IEEE 1149.1)

ispLSI and pLSI Technology

- ❑ UltraMOS E^2CMOS — the PLD Technology of Choice
- ❑ Electrically Erasable/Programmable/ Reprogrammable
- ❑ 100% Tested During Manufacture
- ❑ 100% Programming Yield
- ❑ Fast Programming

ispLSI and pLSI Development Tools

- ❑ Low Cost, Fully Integrated pDS Design System for the PC
- ❑ HDL, VHDL, Boolean Equation, State Machine and Schematic Capture Entry
- ❑ pDS+ Support for Industry-Standard Third-Party Design Environments and Platforms
- ❑ Timing and Functional Simulation
- ❑ PC and Workstation Platforms

Introduction to ispLSI and pLSI 3000 Family

3000 Family Overview

The ispLSI and pLSI 3000 family of high-density devices address high-performance system logic designs implementing logic functions, ranging from registers, to counters, to multiplexers, to complex state machines.

With up to 14,000 PLD gates density, the ispLSI and pLSI 3000 Family provides a wide range of programmable logic solutions which meet tomorrow's design requirements today.

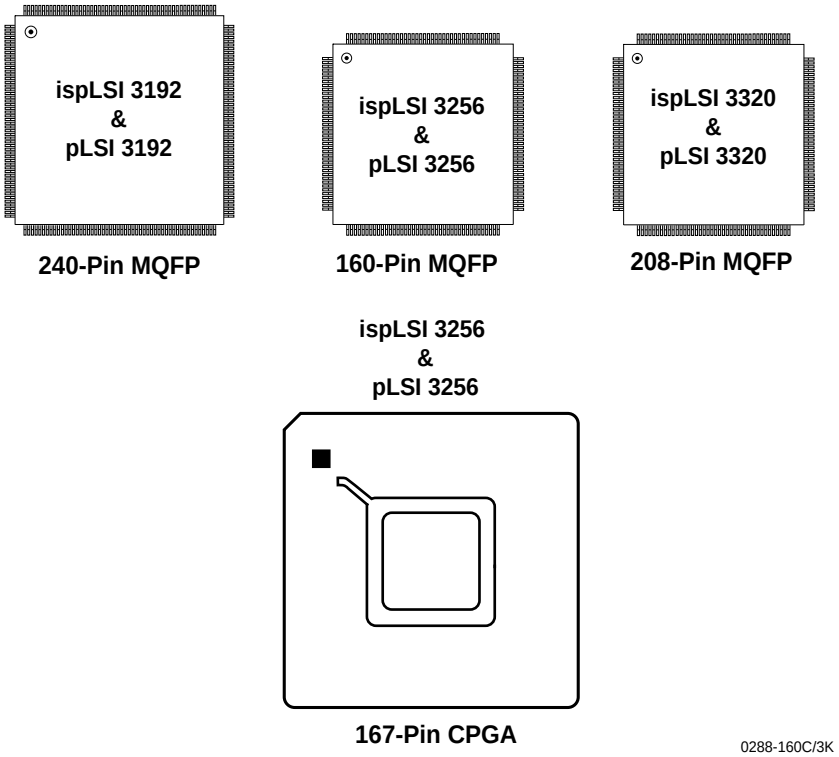
Each device contains multiple Generic Logic Blocks (GLBs), which are designed to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provides the optimum combination of internal logic and external connections. A global interconnect scheme ties everything together, enabling utilization of up to 80% of available logic. Table 1 describes the family attributes.

Table 1. ispLSI and pLSI 3000 Family Attributes

Family Member	3192	3256	3320
Density (PLD Gates)	8,000	11,000	14,000
Speed: f_{max} (MHz)	100	70	70
Speed: t_{pd} (ns)	10	15	15
Macrocells	192	256	320
Registers	384	384	480
Inputs + I/O	192	128	160
Pin/Package	240-pin MQFP	160-pin MQFP 167-pin CPGA	208-pin MQFP

Table 1- 0003B/3K

Figure 1. 3000 Family Packages



0288-160C/3K

ispLSI® and pLSI® 3192

High Density Programmable Logic

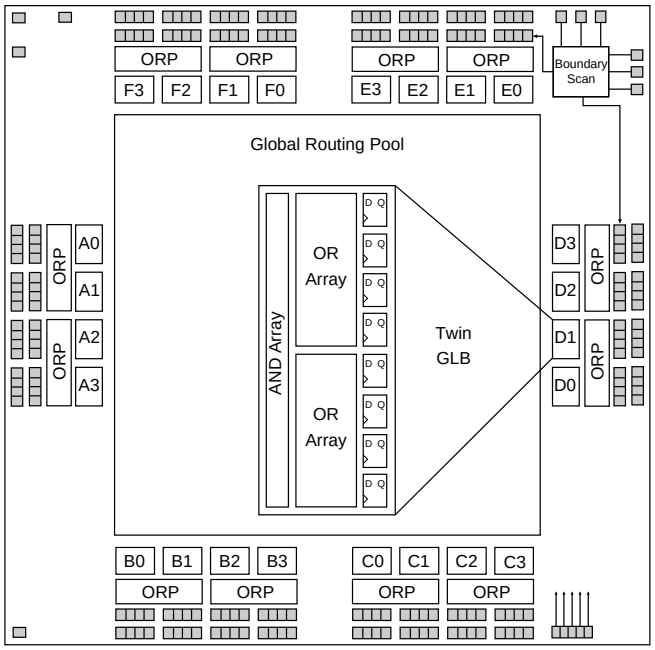
Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— 192 I/O Pins**
  - **— 8000 PLD Gates**
  - **— 384 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 100 MHz Maximum Operating Frequency**
  - **— t_{pd} = 10 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **100% IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Five Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI AND pLSI DEVELOPMENT TOOLS**

  pDS® Software
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning**
  - **— Automatic Place and Route**
  - **— Static Timing Table**

  pDS+™ Software
  - **— Industry Standard, Third Party Design Environments**
  - **— Schematic Capture, State Machine, HDL**
  - **— Automatic Partitioning and Place and Route**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

Functional Block Diagram



0139/3192

Description

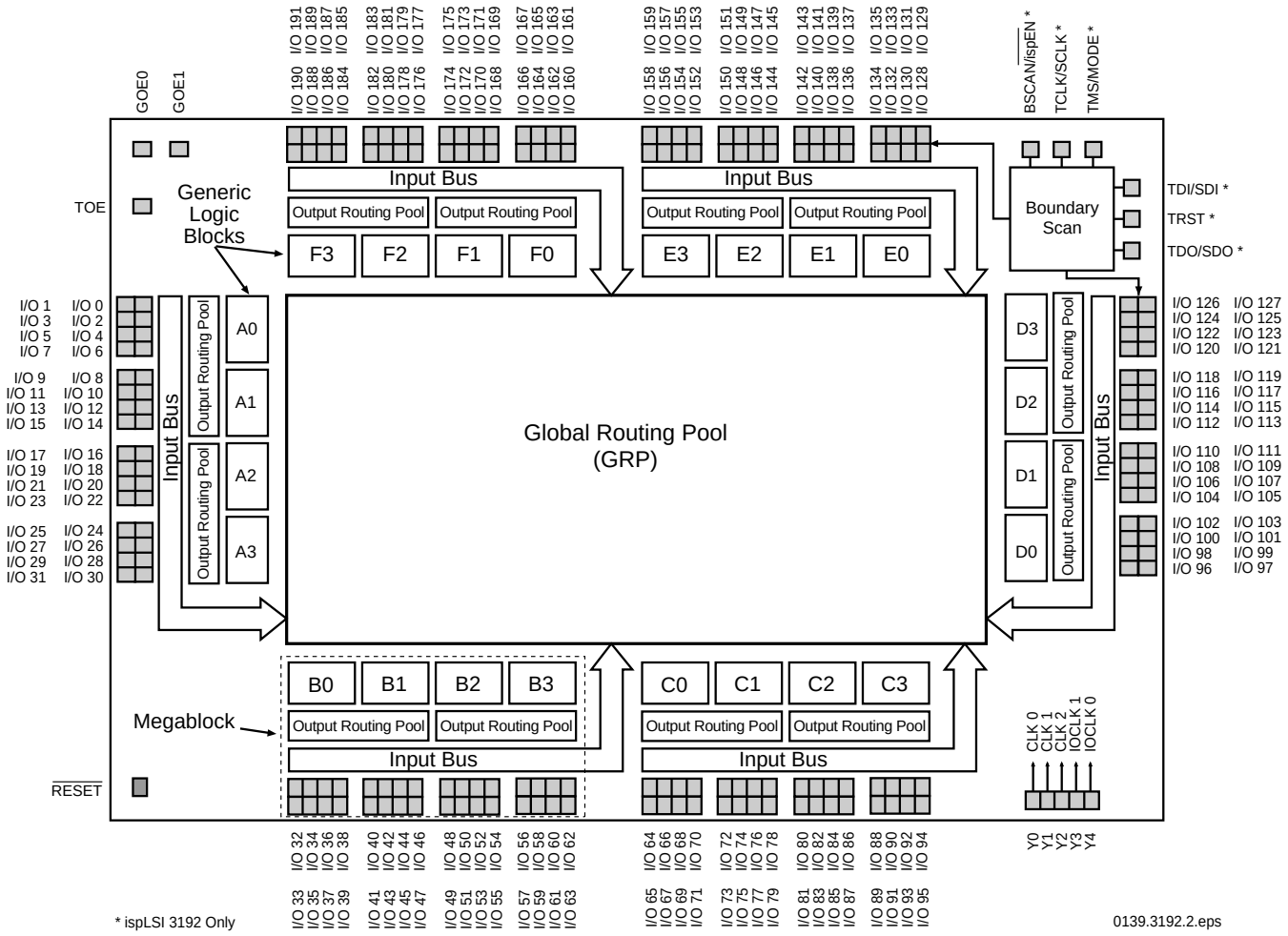
The ispLSI and pLSI 3192 are High Density Programmable Logic Devices which contain 384 Registers, 192 Universal I/O pins, five Dedicated Clock Input Pins, twelve Output Routing Pools (ORP), and a Global Routing Pool (GRP) which allows complete inter-connectivity between all of these elements. The ispLSI 3192 features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 3192 offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 3192 devices.

The basic unit of logic on the ispLSI and pLSI 3192 devices is the Twin Generic Logic Block (Twin GLB) labelled A0, A1...F3. There are a total of 24 of these Twin GLBs in the ispLSI and pLSI 3192 devices. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays, and eight outputs which can be configured to be either combinatorial or registered. All Twin GLB inputs come from the GRP.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Functional Block Diagram

Figure 1. ispLSI and pLSI 3192 Functional Block Diagram



Description (continued)

All local logic block outputs are brought back into the GRP so they can be connected to the inputs of any other logic block on the device. The device also has 192 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a registered input, a latched input, an output or a bidirectional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

The 192 I/O Cells are grouped into six sets of 32 bits. Each of these I/O groups is associated with a logic Megablock through the use of the ORP. Each Megablock is able to provide one Product Term Output Enable (PTOE) signal which is globally distributed to all I/O cells. That PTOE signal can be generated within any GLB in the Megablock. Each I/O cell can select either a Global OE or a PTOE.

Four Twin GLBs, 32 I/O Cells and two ORPs are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of the four Twin GLBs are connected to a set of 32 I/O cells by the two ORPs. The ispLSI and pLSI 3192 device contains six of these Megablocks.

The GRP has as its inputs the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the ispLSI and pLSI 3192 devices are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

The table below lists key attributes of the device along with the number of resources available.

An additional feature of the ispLSI and pLSI 3192 is the Boundary Scan capability, which is composed of cells connected between the on-chip system logic and the device's input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one.

The ispLSI and pLSI 3192 supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

Key Attributes of the ispLSI and pLSI 3192

Attribute	Quantity
Twin GLBs	24
Registers	384
I/O Pins	192
Global Clocks	5
Global OE	2
Test OE	1

Table - 003/3192

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to +70°C	4.75	5.25	V
		Industrial	T_A = -40°C to +85°C	4.5	5.5	V
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} +1	V

Table 2 - 0005/3192

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL [1]	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	15	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2 - 0006/3192

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2- 0008B

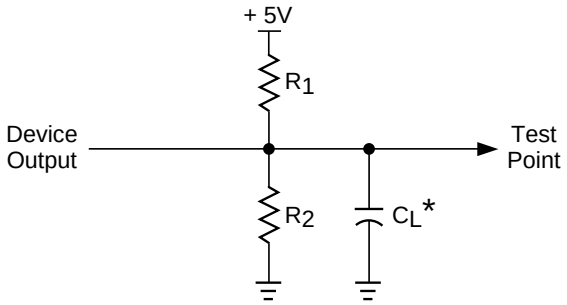
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Ouput Timing Reference Levels	1.5V
Output Load	See figure 2

Table 2 - 0003

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A

Output Load conditions (See figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
I_{IL-isp}	Bscan/$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V, f_{TOGGLE} = 1 MHz	Commercial	–	320	–	mA
			Industrial	–	320	–	mA

Table 2 - 0007isp/3192

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using twelve 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-100		-70		UNITS
				MIN.	MAX.	MIN.	MAX.	
tpd1	A	1	Data Prop. Delay, 4PT Bypass, ORP Bypass	—	10	—	15	ns
tpd2	A	2	Data Propagation Delay	—	13	—	18	ns
fmax	A	3	Clock Frequency with Internal Feedback[3]	100	—	70	—	MHz
fmax (Ext.)	—	4	Clock Freq. with Ext. Feedback,1/(tsu2 + tco1)	80	—	50	—	MHz
fmax (Tog.)	—	5	Clock Frequency, Max Toggle[4]	125	—	83	—	MHz
tsu1	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	5.5	—	9	—	ns
tco1	A	7	GLB Reg. Clock to Output Delay, ORP bypass	—	6	—	9	ns
th1	—	8	GLB Reg. Hold Time after Clock, 4PT bypass	0	—	0	—	ns
tsu2	—	9	GLB Reg. Setup Time before Clock	6.5	—	11	—	ns
tco2	—	10	GLB Reg. Clock to Output Delay	—	6.5	—	10	ns
th2	—	11	GLB Reg. Hold Time after Clock	0	—	0	—	ns
tr1	A	12	Ext. Reset Pin to Output Delay	—	13.5	—	15	ns
trw1	—	13	Ext. Reset Pulse Duration	6.5	—	12	—	ns
tptoeen	B	14	Input to Output Enable	—	15	—	18	ns
tptoedis	C	15	Input to Output Disable	—	15	—	18	ns
tgoeen	B	16	Global OE Output Enable	—	9	—	12	ns
tgoedis	C	17	Global OE Output Disable	—	9	—	12	ns
ttoeen	—	18	Test OE Output Enable	—	12	—	15	ns
ttoedis	—	19	Test OE Output Disable	—	12	—	15	ns
twh	—	20	Ext. Sync. Clock Pulse Duration, High	4	—	6	—	ns
twl	—	21	Ext. Sync. Clock Pulse Duration, Low	4	—	6	—	ns
tsu3	—	22	I/O Reg. Setup Time before Ext. Sync. Clock (Y3, Y4)	3.5	—	5	—	ns
th3	—	23	I/O Reg. Hold Time after Ext. Sync. Clock (Y3, Y4)	0	—	0	—	ns

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Timing Ext.6192.eps

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-100		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
tiobp	24	I/O Register Bypass	—	1.3	—	1.9	ns
tiolat	25	I/O Latch Delay	—	9.2	—	13.2	ns
tiosu	26	I/O Register Setup Time before Clock	6.5	—	9.3	—	ns
tioh	27	I/O Register Hold Time after Clock	-3.0	—	-4.3	—	ns
tioch	28	I/O Register Clock to Out Delay	—	1.5	—	2.3	ns
tior	29	I/O Register Reset to Out Delay	—	3.3	—	3.9	ns
GRP							
tgrp	30	GRP Delay	—	1.4	—	2.1	ns
GLB							
t4ptbp	31	4 Product Term Bypass Path Delay (Comb.)	—	4.3	—	7.8	ns
t4ptbr	32	4 Product Term Bypass Path Delay (Reg.)	—	5.5	—	7.4	ns
t1ptxor	33	1 Product Term/XOR Path Delay	—	6.0	—	8.3	ns
t20ptxor	34	20 Product Term/XOR Path Delay	—	6.5	—	9.4	ns
txoradj	35	XOR Adjacent Path Delay[3]	—	7.1	—	10.3	ns
tgbp	36	GLB Register Bypass Delay	—	0.3	—	0.4	ns
tgsu	37	GLB Register Setup Time before Clock	0.2	—	1.7	—	ns
tgh	38	GLB Register Hold Time after Clock	3.5	—	5.3	—	ns
tgco	39	GLB Register Clock to Output Delay	—	0.1	—	1.7	ns
tgro	40	GLB Register Reset to Output Delay	—	2.4	—	2.8	ns
tptre	41	GLB Product Term Reset to Register Delay	—	5.0	—	7.5	ns
tptoe	42	GLB Product Term Output Enable to I/O Cell Delay	—	7.6	—	9.2	ns
tptck	43	GLB Product Term Clock Delay	4.9	5.9	7.4	8.8	ns
ORP							
torp	44	ORP Delay	—	1.1	—	1.7	ns
torpbp	45	ORP Bypass Delay	—	0.6	—	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters[1]

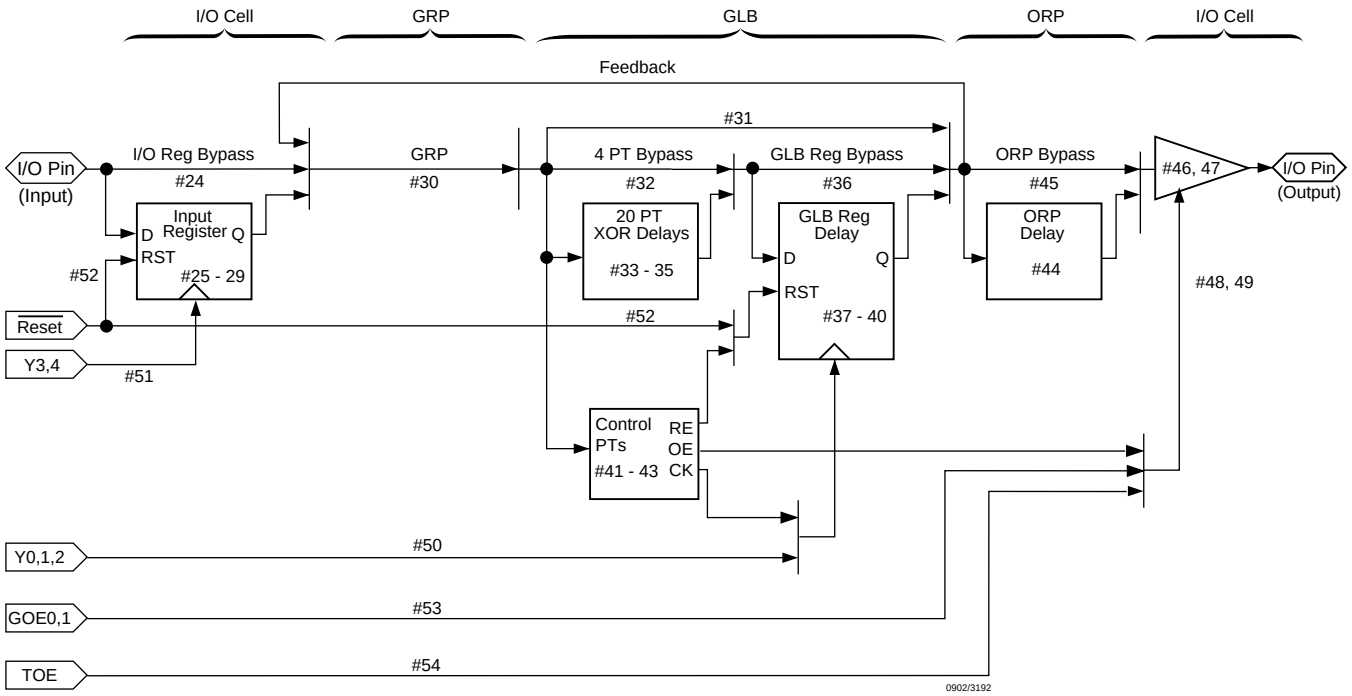
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-100		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
tob	46	Output Buffer Delay	—	2.4	—	2.5	ns
tobs	47	Output Buffer Delay, Slow Slew	—	22.4	—	27.5	ns
toen	48	I/O Cell OE to Output Enabled	—	4.7	—	4.8	ns
todis	49	I/O Cell OE to Output Disabled	—	4.7	—	4.8	ns
Clocks							
tgy0/1/2	50	Clock Delay, Y0 or Y1 or Y2 to Global GLB Clk Line	2.9	2.9	4.1	4.1	ns
tioy3/4	51	Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line	3.0	3.0	4.3	4.3	ns
Global Reset							
tgr	52	Global Reset to GLB and I/O Registers	—	7.6	—	8.0	ns
tgoe	53	Global OE Pad Buffer	—	4.3	—	7.2	ns
ttoe	54	Test OE Pad Buffer	—	7.3	—	10.2	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

Timing Int.2.3192.eps

ispLSI and pLSI 3192 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**iobp + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp + **t**ptck(min))
	=	(#24+ #30+ #34) + (#37) - (#24+ #30+ #43)
1.8 ns	=	(1.3 + 1.4 + 6.5) + (0.2) - (1.3 + 1.4 + 4.9)
th	=	Clock (max) + Reg h - Logic
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp + **t**20ptxor)
	=	(#24+ #30+ #43) + (#38) - (#24+ #30+ #34)
2.9 ns	=	(1.3 + 1.4 + 5.9) + (3.5) - (1.3 + 1.4 + 6.5)
tco	=	Clock (max) + Reg co + Output
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#24 + #30 + #43) + (#39) + (#44 + #46)
12.2 ns	=	(1.3 + 1.4 + 5.9) + (0.1) + (1.1 + 2.4)

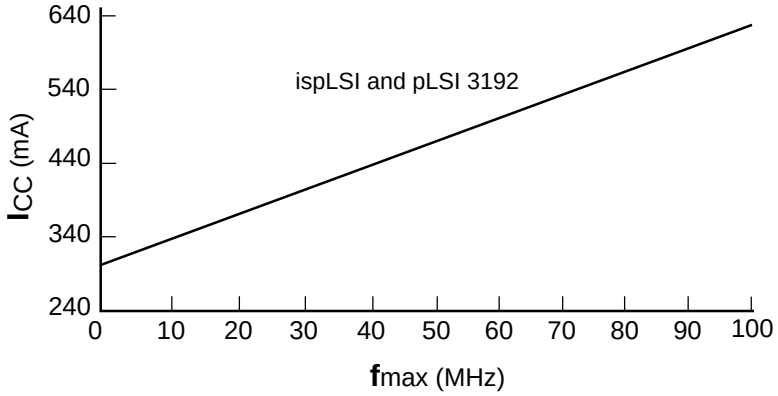
Table 2- 0042-3192

Note: Calculations are based upon timing specifications for the ispLSI and pLSI 3192-100L.

Power Consumption

Power Consumption in the ispLSI and pLSI 3192 device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of 16 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI and pLSI 3192 using the following equation:

I_{CC} = 50 + (# of PTs * 0.65) + (# of nets * Max. freq * 0.015) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

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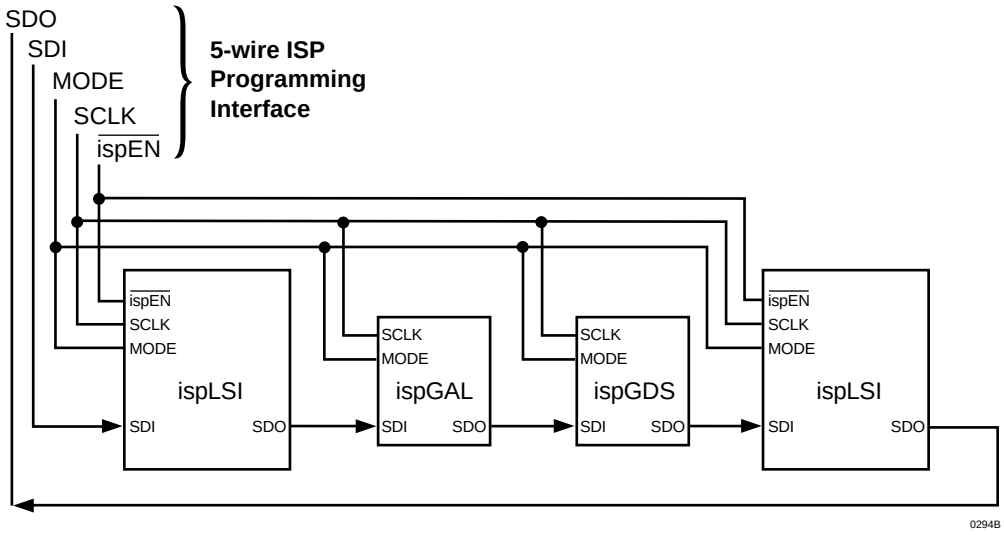
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

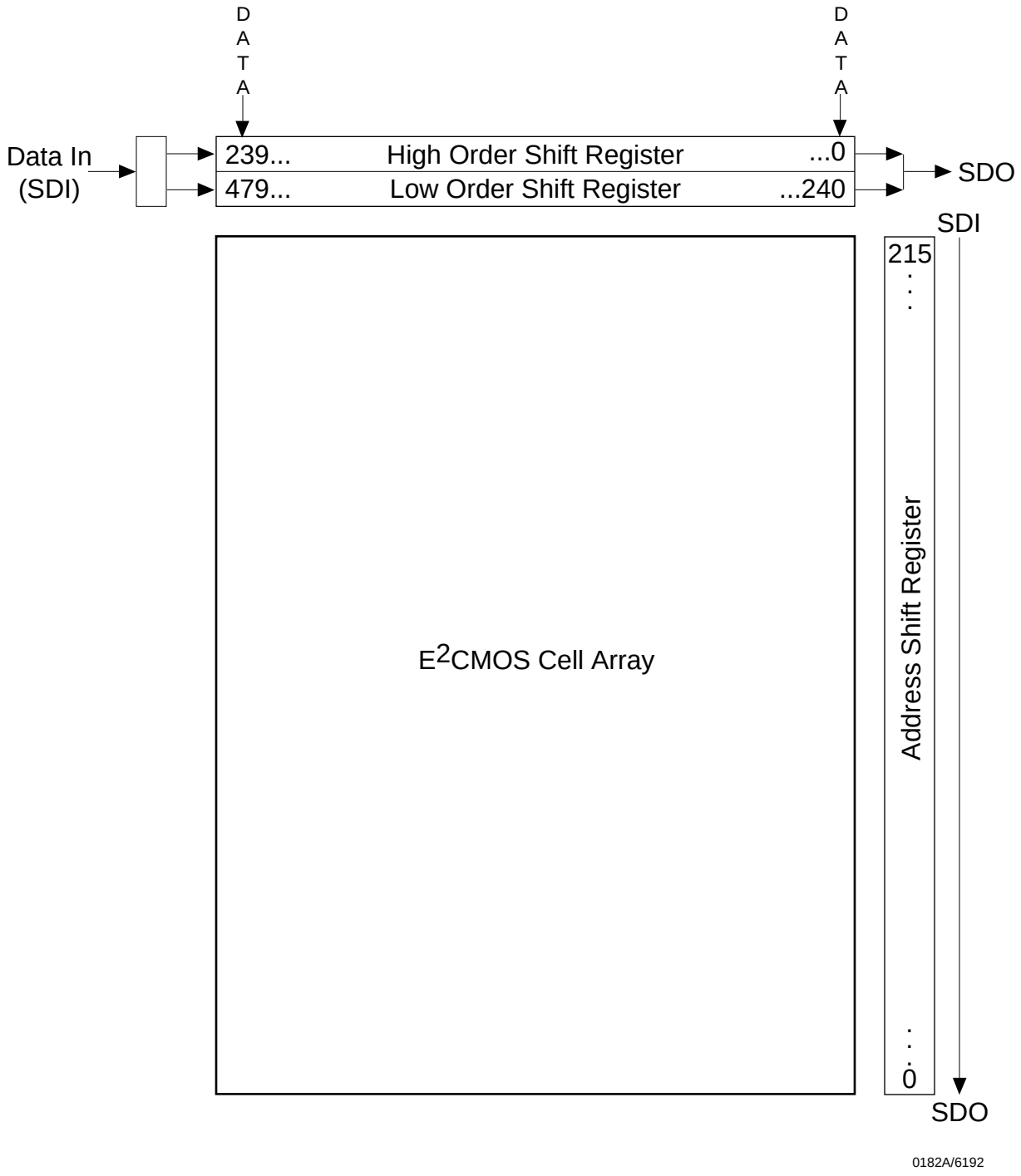
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for interface include isp™ Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section in this Data Book.

The device identifier for the ispLSI 3192 is 0010 0001 (21 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 3192 Shift Register Layout



Note: A logic “1” in the address shift register enables the row for programming or verification. A logic “0” disables it.

Boundary Scan

Lattice Semiconductor offers support for the IEEE 1149.1 Boundary Scan specification on the 3000 Family of devices.

The user interfaces to the boundary scan circuitry through the Test Access Port (TAP). The TAP consists of a control state machine, instruction decoder and instruction register.

The TAP is controlled using the test control lines: Test Data IN (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Reset ($\overline{TRST}$) and Test Clock (TCK).

All of the input cells and I/O cells are serially connected together in a long chain. The scan out of one cell is connected to the scan in of the next cell. The cells are connected in the following order: TDI to GOE0, GOE1, Y0, Y1, Y2, Y3, Y4, TOE, $\overline{RESET}$, I/O95 thru I/O0 to I/O96 thru I/O191 to TDO.

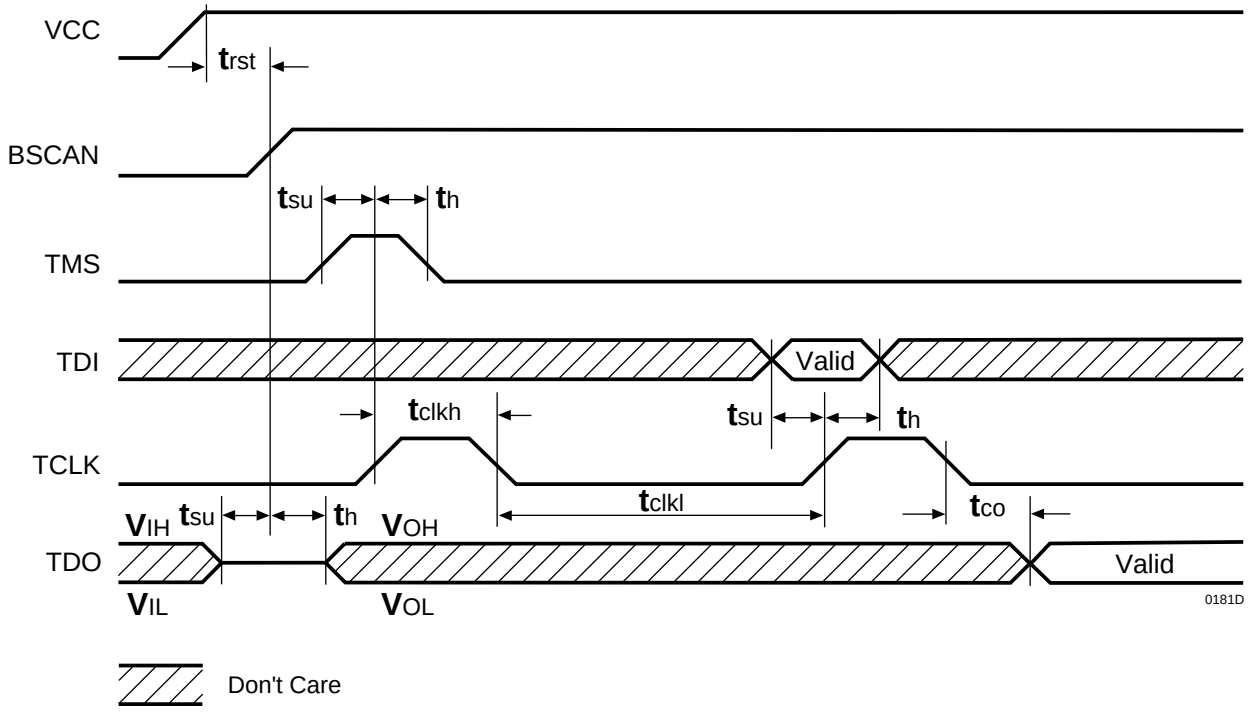
The timing specifications for Boundary Scan are listed below. The waveforms are shown in figure 5.

Boundary Scan Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
t_{rst}	Reset Time from Valid V_{CC}		100	–	–	µs
t_{su}	Setup Time		60	–	–	ns
t_h	Hold Time		10	–	–	ns
t_{co}	Clock to Output		–	–	60	ns
t_{clkh}	Clock Pulse Duration, High		60	–	–	ns
t_{clkl}	Clock Pulse Duration, Low		60	–	–	ns

Table 2 - 0028Aisp-3192

Figure 5. Boundary Scan Waveforms



Pin Description

NAME	MQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95 I/O 96 - I/O 101 I/O 102 - I/O 107 I/O 108 - I/O 113 I/O 114 - I/O 119 I/O 120 - I/O 125 I/O 126 - I/O 131 I/O 132 - I/O 137 I/O 138 - I/O 143 I/O 144 - I/O 149 I/O 150 - I/O 155 I/O 156 - I/O 161 I/O 162 - I/O 167 I/O 168 - I/O 173 I/O 174 - I/O 179 I/O 180 - I/O 185 I/O 186 - I/O 191	36, 37, 38, 39, 40, 41, 43, 44, 45, 46, 47, 48, 50, 51, 52, 53, 54, 55, 57, 58, 59, 60, 61, 62, 64, 65, 66, 67, 68, 69, 71, 72, 73, 74, 75, 76, 78, 79, 80, 81, 82, 83, 85, 86, 87, 88, 89, 90, 92, 93, 94, 95, 96, 97, 99, 100, 101, 102, 103, 104, 106, 107, 108, 109, 110, 111, 113, 114, 115, 116, 117, 118, 120, 121, 122, 123, 124, 125, 127, 128, 129, 130, 131, 132, 134, 135, 136, 137, 138, 139, 141, 142, 143, 144, 145, 146, 156, 157, 158, 159, 160, 161, 163, 164, 165, 166, 167, 168, 170, 171, 172, 173, 174, 175, 177, 178, 179, 180, 181, 182, 184, 185, 186, 187, 188, 189, 191, 192, 193, 194, 195, 196, 198, 199, 200, 201, 202, 203, 205, 206, 207, 208, 209, 210, 212, 213, 214, 215, 216, 217, 219, 220, 221, 222, 223, 224, 226, 227, 228, 229, 230, 231, 233, 234, 235, 236, 237, 238, 240, 1, 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0 and GOE1 TOE	152 and 153 154	Global Output Enable input pins. Test output enable pin.
$\overline{\text{RESET}}$ Y0, Y1 and Y2 Y3 and Y4	33 35, 34, 148 149, 151	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device. Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device. Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the I/O cells in the device.
BSCAN/$\overline{\text{ispEN}}$** TDI/SDI* TCLK/SCLK* TMS/MODE* $\overline{\text{TRST}}$ TDO/SDO*	32 30 29 28 155 27	Boundary Scan Enable. Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active. Input - This pin performs two functions. It is the Test Data input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the isp state machine. Input - This pin performs two functions. It is the Test Clock input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. Input - This pin performs two functions. It is the Test Mode Select input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine. Input - Test Reset, active low to reset the Boundary Scan State Machine. Output - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the isp data. When $\overline{\text{ispEN}}$ is high it functions as Test Data Out.
GND VCC	13, 31, 49, 63, 77, 91, 105, 119, 133, 150, 169, 183, 197, 211, 225, 239 6, 20, 42, 56, 70, 84, 98, 112, 126, 140, 162, 176, 190, 204, 218, 232	Ground (GND) V_{CC}

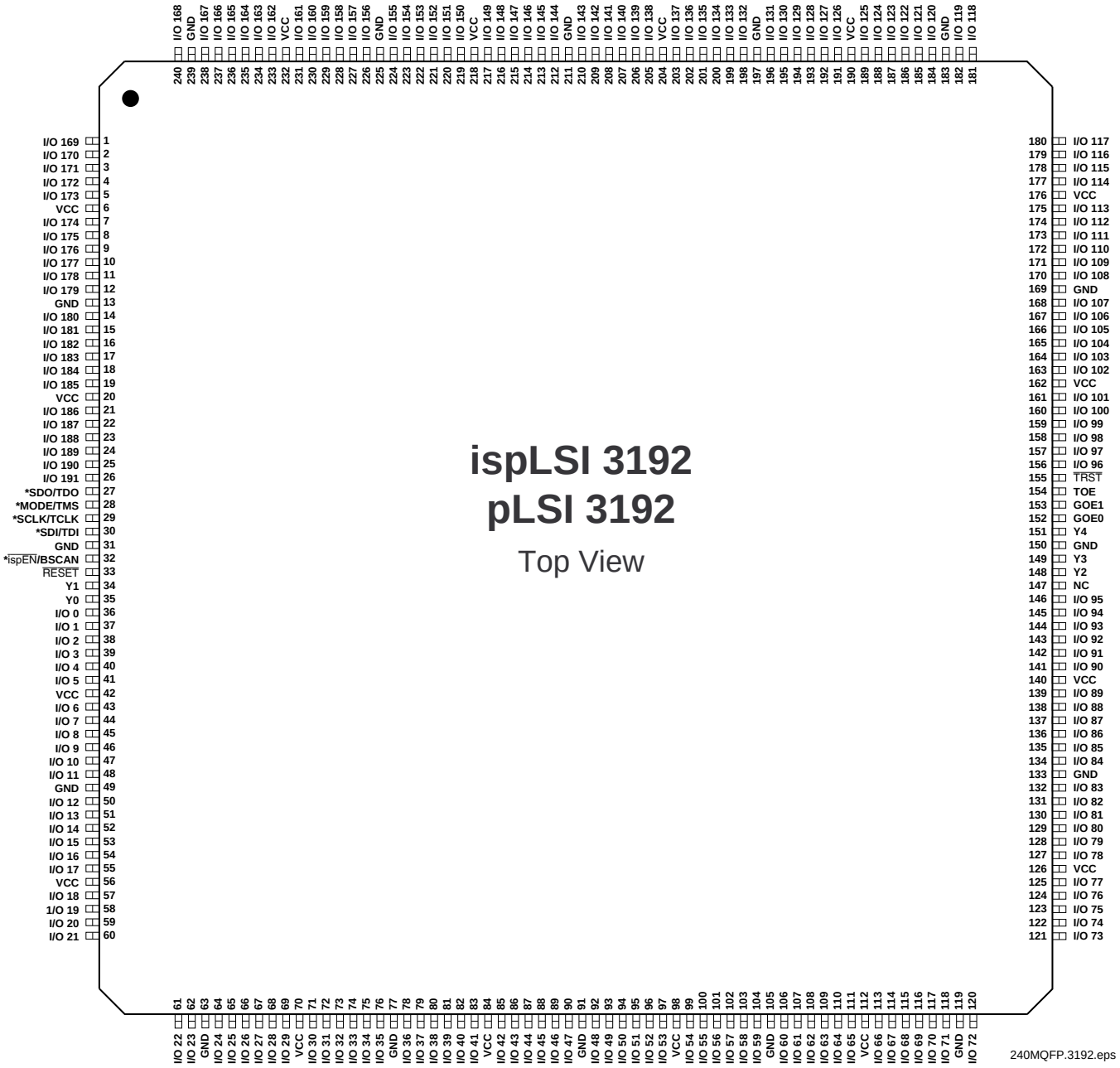
Table 2 - 0002/3192

* ispLSI 3192 only

** $\overline{\text{ispEN}}$ for ispLSI 3192 only, NC for pLSI 3192 must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

Pin Configuration

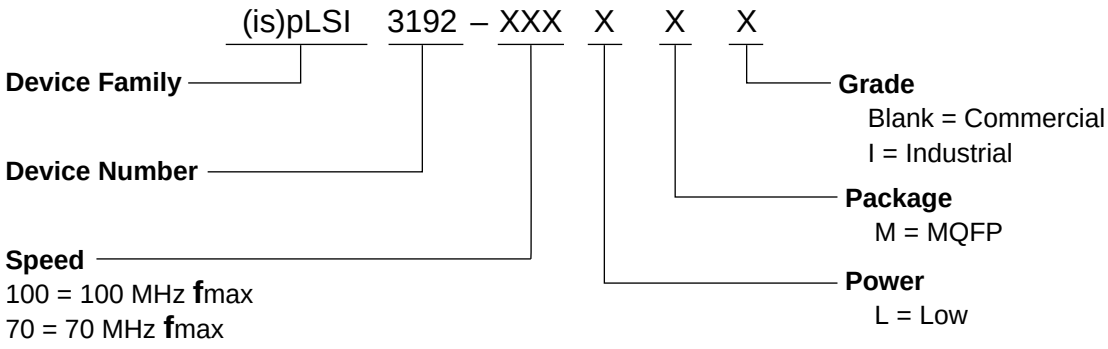
ispLSI and pLSI 3192 240-pin MQFP



240MQFP.3192.eps

*Pins have dual function capability for ispLSI 3192 only.

Part Number Description



0212/3192

Ordering Information

COMMERCIAL

Family	fmax	tpd	Ordering Number	Package
ispLSI	100	10	ispLSI 3192-100LM	240-Pin MQFP
	70	15	ispLSI 3192-70LM	240-Pin MQFP
pLSI	100	10	pLSI 3192-100LM	240-Pin MQFP
	70	15	pLSI 3192-70LM	240-Pin MQFP

Table 2- 0041/3192

INDUSTRIAL

Family	fmax	tpd	Ordering Number	Package
ispLSI	70	15	ispLSI 3192-70LMI	240-Pin MQFP

Table 2- 0042/3192

ispLSI® and pLSI® 3256

High Density Programmable Logic

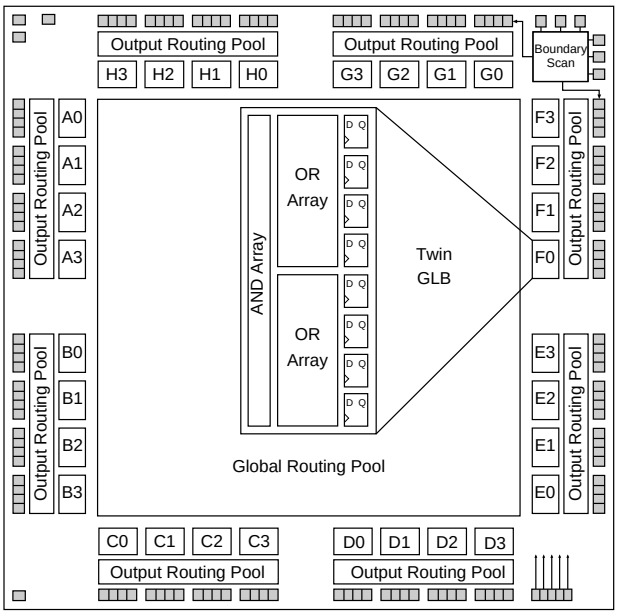
Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— 128 I/O Pins**
  - **— 11000 PLD Gates**
  - **— 384 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 77 MHz Maximum Operating Frequency**
  - **— t_{pd} = 15 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ (ISP™) 5-Volt Only**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **100% IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Five Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispLSI AND pLSI DEVELOPMENT TOOLS**

  pDS® Software
  - **— Easy to Use PC Windows™ Interface**
  - **— Boolean Logic Compiler**
  - **— Manual Partitioning**
  - **— Automatic Place and Route**
  - **— Static Timing Table**

  pDS+™ Software
  - **— Industry Standard, Third Party Design Environments**
  - **— Schematic Capture, State Machine, HDL**
  - **— Automatic Partitioning and Place and Route**
  - **— Comprehensive Logic and Timing Simulation**
  - **— PC and Workstation Platforms**

Functional Block Diagram



0139A

Description

The ispLSI and pLSI 3256 are High Density Programmable Logic Devices which contain 384 Registers, 128 Universal I/O pins, five Dedicated Clock Input Pins, eight Output Routing Pools (ORP), and a Global Routing Pool (GRP) which allows complete inter-connectivity between all of these elements. The ispLSI 3256 features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 3256 offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 3256 devices.

The basic unit of logic on the ispLSI and pLSI 3256 devices is the Twin Generic Logic Block (Twin GLB) labelled A0, A1...H3. There are a total of 32 of these Twin GLBs in the ispLSI and pLSI 3256 devices. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays, and eight outputs which can be configured to be either combinatorial or registered. All Twin GLB inputs come from the GRP.

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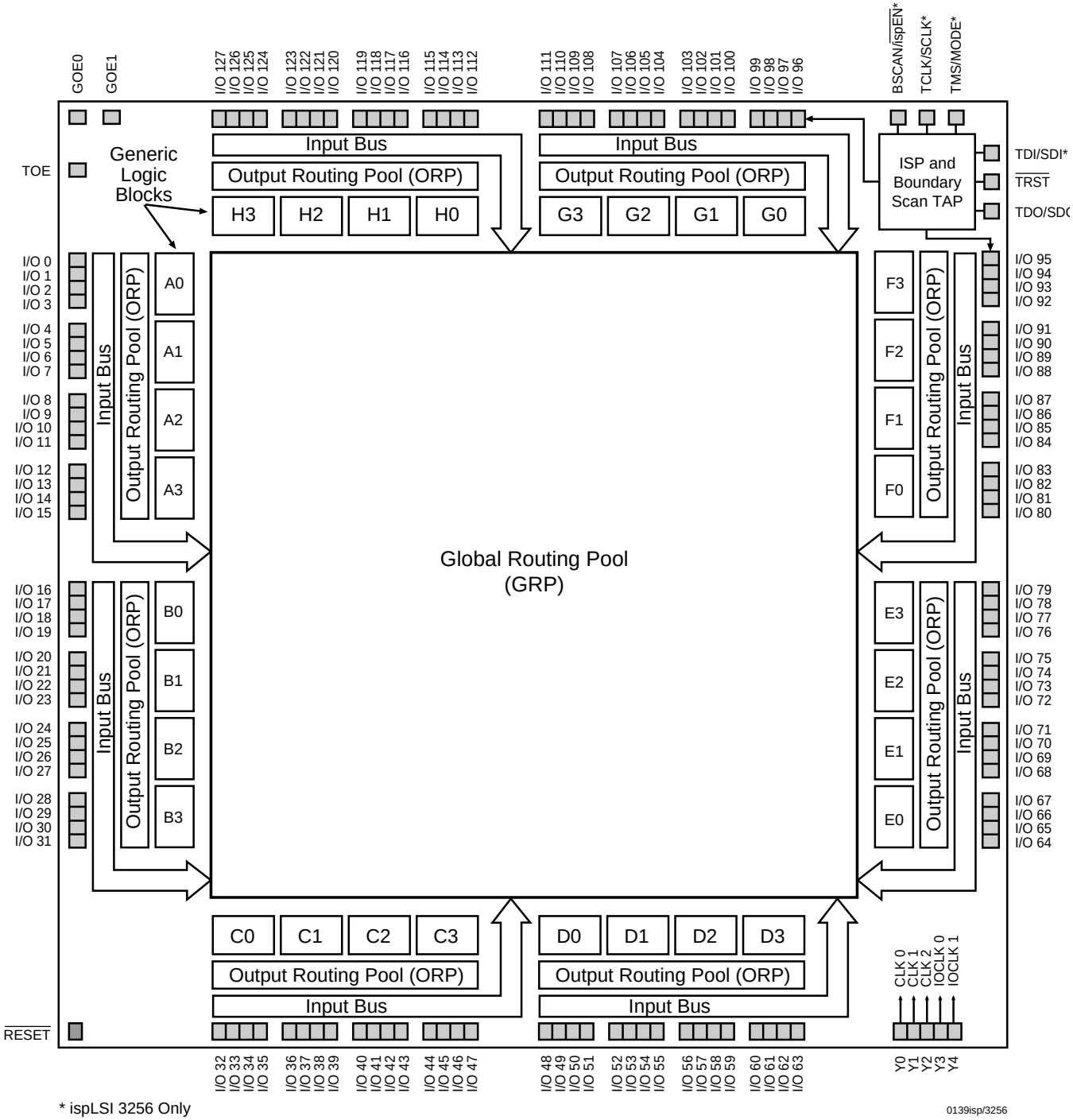
Functional Block Diagram

Figure 1. ispLSI and pLSI 3256 Functional Block Diagram



Description (continued)

All local logic block outputs are brought back into the GRP so they can be connected to the inputs of any other logic block on the device. The device also has 128 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a registered input, a latched input, an output or a bidirectional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

The 128 I/O Cells are grouped into eight sets of 16 bits. Each of these I/O groups is associated with a logic Megablock through the use of the ORP. These groups of 16 I/O cells share one Product Term Output Enable which is associated with a specific pair of Megablocks and two Global Output Enables.

Four Twin GLBs, 16 I/O Cells and one ORP are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of the four Twin GLBs are connected to a set of 16 I/O cells by the ORP. The ispLSI and pLSI 3256 Device contains eight of these Megablocks.

The GRP has as its inputs the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the ispLSI and pLSI 3256 devices are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

The table below lists key attributes of the device along with the number of resources available.

An additional feature of the ispLSI and pLSI 3256 is the Boundary Scan capability, which is composed of cells connected between the on-chip system logic and the device's input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one.

The ispLSI and pLSI 3256 supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

Key Attributes of the ispLSI and pLSI 3256

Attribute	Quantity
Twin GLBs	32
Registers	384
I/O Pins	128
Global Clocks	5
Global OE	2
Test OE	1

Table - 003Aisp/3256

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2 - 0005/3256

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	12	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2 - 0006/3256

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2- 0008B

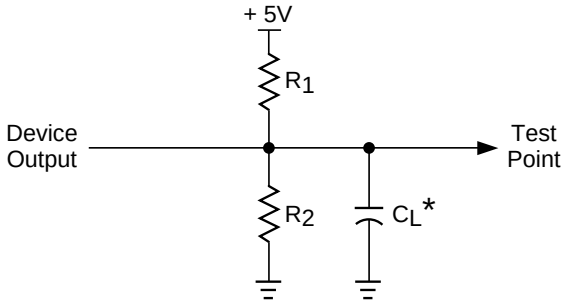
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Ouput Timing Reference Levels	1.5V
Output Load	See figure 2

Table 2 - 0003

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A

Output Load conditions (See figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
$I_{IL\text{-}isp}$	Bscan/$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V f_{TOGGLE} = 1 MHz	–	150	270	mA

Table 2 - 0007isp/3256

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using sixteen 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

PARAMETER	TEST COND.[5]	#[2]	DESCRIPTION[1]	-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	15.0	–	20.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	18.0	–	24.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	77	–	57	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	50	–	37	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle[4]	83	–	63	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	9.5	–	12.5	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	9.0	–	12.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	11.0	–	15.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	10.5	–	14.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	15.0	–	20.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10.0	–	13.5	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	18.0	–	24.5	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	18.0	–	24.5	ns
t_{goeen}	B	16	Global OE Output Enable	–	11.0	–	13.5	ns
t_{goedis}	C	17	Global OE Output Disable	–	11.0	–	13.5	ns
t_{toeen}	B	18	Test OE Output Enable	–	17.0	–	23.0	ns
t_{toedis}	C	19	Test OE Output Disable	–	17.0	–	23.0	ns
t_{wh}	–	20	External Synchronous Clock Pulse Duration, High	6.0	–	8.0	–	ns
t_{wl}	–	21	External Synchronous Clock Pulse Duration, Low	6.0	–	8.0	–	ns
t_{su3}	–	22	I/O Reg. Setup Time before Ext. Sync. Clock (Y3, Y4)	5.0	–	7.0	–	ns
t_{h3}	–	23	I/O Reg. Hold Time after Ext. Sync. Clock (Y3, Y4)	0.0	–	0.0	–	ns

Table 2 - 0030A/3256

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. f_{max} (Toggle) may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{iobp}	24	I/O Register Bypass	–	2.4	–	3.3	ns
t_{iolat}	25	I/O Latch Delay	–	2.4	–	3.3	ns
t_{iosu}	26	I/O Register Setup Time before Clock	6.2	–	8.6	–	ns
t_{ioh}	27	I/O Register Hold Time after Clock	3.9	–	5.3	–	ns
t_{ioco}	28	I/O Register Clock to Out Delay	–	1.9	–	2.6	ns
t_{ior}	29	I/O Register Reset to Out Delay	–	3.6	–	4.9	ns
GRP							
t_{grp}	30	GRP Delay	–	3.0	–	4.1	ns
GLB							
t_{4ptbp}	31	4 Product Term Bypass Path Delay	–	5.9	–	7.6	ns
t_{1ptxor}	32	1 Product Term/XOR Path Delay	–	6.4	–	8.8	ns
$t_{20ptxor}$	33	20 Product Term/XOR Path Delay	–	7.4	–	10.1	ns
t_{xoradj}	34	XOR Adjacent Path Delay[3]	–	8.1	–	11.1	ns
t_{gbp}	35	GLB Register Bypass Delay	–	0.1	–	0.1	ns
t_{gsu}	36	GLB Register Setup Time before Clock	1.8	–	2.4	–	ns
t_{gh}	37	GLB Register Hold Time after Clock	6.0	–	8.2	–	ns
t_{gco}	38	GLB Register Clock to Output Delay	–	1.8	–	2.2	ns
t_{gro}	39	GLB Register Reset to Output Delay	–	2.8	–	3.8	ns
t_{ptre}	40	GLB Product Term Reset to Register Delay	–	10.5	–	14.2	ns
t_{ptoe}	41	GLB Product Term Output Enable to I/O Cell Delay	–	5.4	–	7.3	ns
t_{ptck}	42	GLB Product Term Clock Delay	3.2	6.3	4.3	8.5	ns
ORP							
t_{orp}	43	ORP Delay	–	2.7	–	3.6	ns
t_{orpbp}	44	ORP Bypass Delay	–	1.2	–	1.6	ns

Table 2 - 0036A/3256

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters[1]

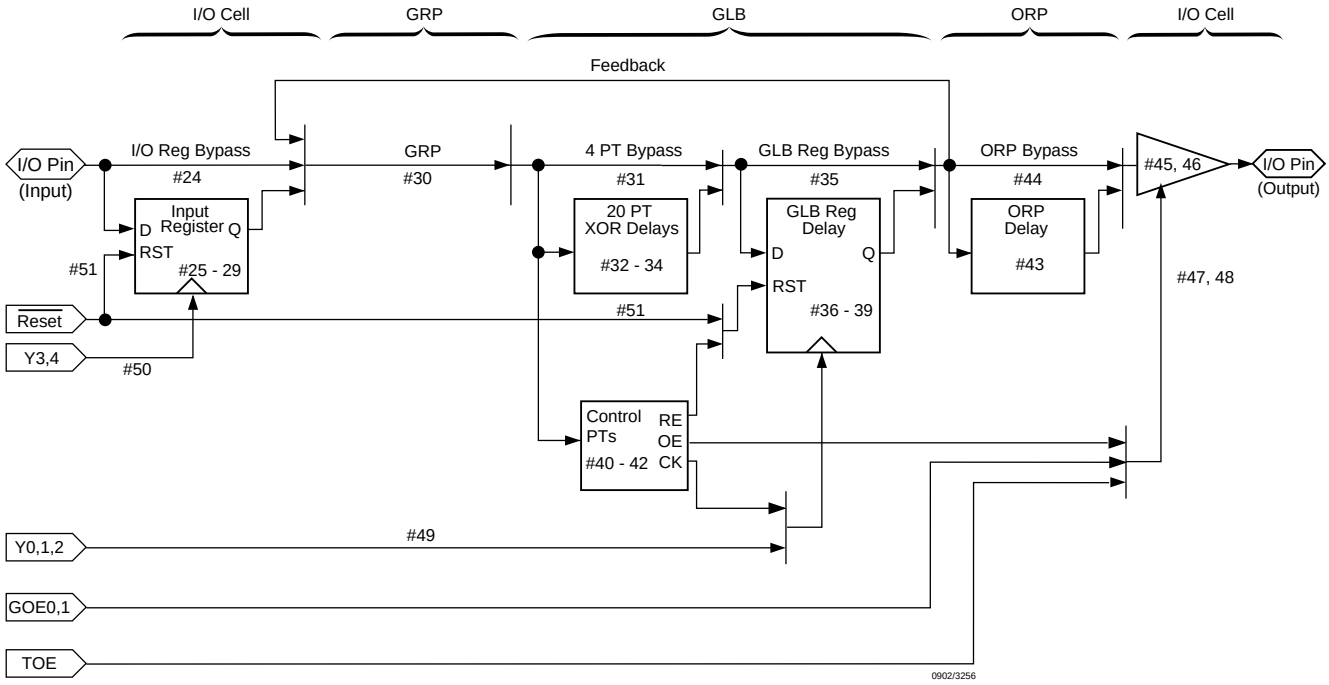
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	45	Output Buffer Delay	–	2.4	–	3.3	ns
t_{obs}	46	Output Buffer Delay, Slow Slew	–	12.4	–	13.3	ns
t_{oen}	47	I/O Cell OE to Output Enabled	–	7.2	–	9.8	ns
t_{odis}	48	I/O Cell OE to Output Disabled	–	7.2	–	9.8	ns
Clocks							
$t_{gy0/1/2}$	49	Clock Delay, Y0 or Y1 or Y2 to Global GLB Clock Line	3.6	3.6	4.9	4.9	ns
$t_{ioy3/4}$	50	Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line	1.2	5.2	1.6	7.0	ns
Global Reset							
t_{gr}	51	Global Reset to GLB and I/O Registers	–	7.1	–	9.6	ns

Table 2 - 0037A/3256

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI and pLSI 3256 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (**t**iobp + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp + **t**ptck(min))
= (#24+ #30+ #33) + (#36) - (#24+ #30+ #42)
8.0 ns = (2.4 + 3.0 + 9.4) + (1.8) - (2.4 + 3.0 + 3.2)

th = Clock (max) + Reg h - Logic
= (**t**iobp + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp + **t**20ptxor)
= (#24+ #30+ #42) + (#37) - (#24+ #30+ #33)
2.9 ns = (2.4 + 3.0 + 6.3) + (6.0) - (2.4 + 3.0 + 9.4)

tco = Clock (max) + Reg co + Output
= (**t**iobp + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#24 + #30 + #42) + (#38) + (#43 + #45)
2.9 ns = (2.4 + 3.0 + 6.3) + (1.8) + (2.7 + 2.4)

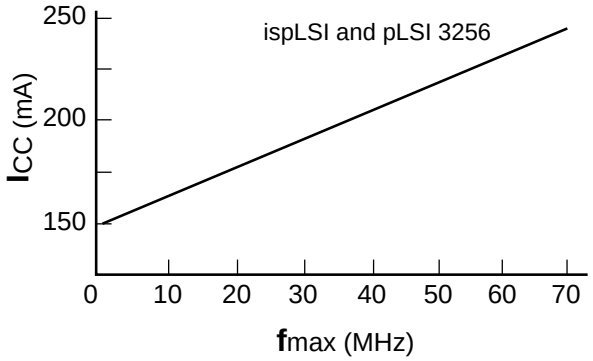
Table 2- 0042-16/3256

Note: Calculations are based on timing specs for the ispLSI 3256-70L.

Power Consumption

Power Consumption in the ispLSI and pLSI 3256 device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of 16 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI and pLSI 3256 using the following equation:

I_{CC} = 44 + (# of PTs * 0.18) + (# of nets * Max. freq * 0.013) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

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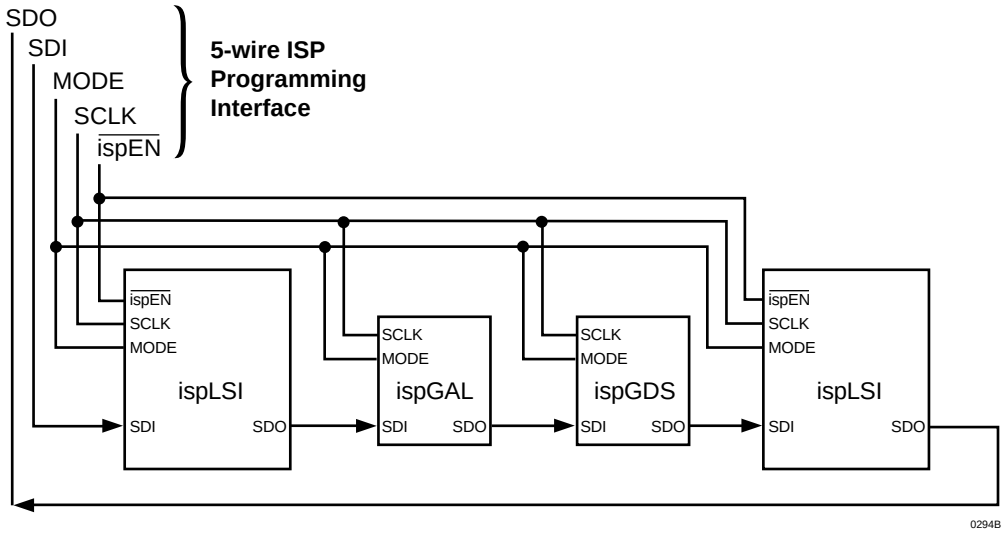
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

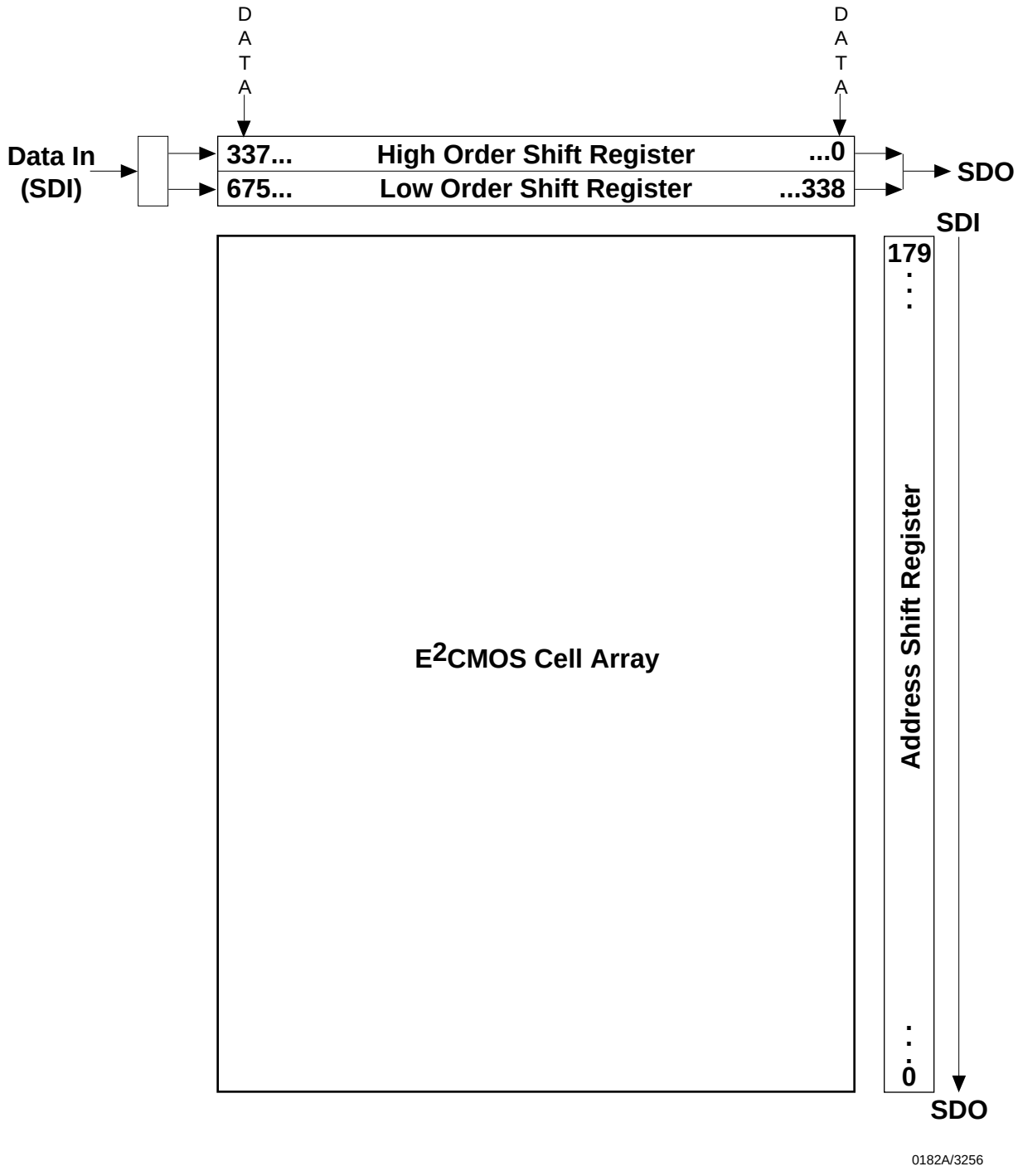
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for interface include isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section in this Data Book.

The device identifier for the ispLSI 3256 is 0010 0010 (22 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 3256 Shift Register Layout



Note: A logic “1” in the address shift register enables the row for programming or verification. A logic “0” disables it.

Boundary Scan

Lattice Semiconductor offers support for the IEEE 1149.1 Boundary Scan specification on the 3000 Family of devices.

The user interfaces to the boundary scan circuitry through the Test Access Port (TAP). The TAP consists of a control state machine, instruction decoder and instruction register.

The TAP is controlled using the test control lines: Test Data IN (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Reset ($\overline{TRST}$) and Test Clock (TCK).

All of the input cells and I/O cells are serially connected together in a long chain. The scan out of one cell is connected to the scan in of the next cell. The cells are connected in the following order: TDI to IO63 thru IO32 to Y4, Y3, Y2, Y1, RESET, TOE, GOE1, GOE0, Y0, IO31 thru IO0 to IO64 thru IO127 to TDO.

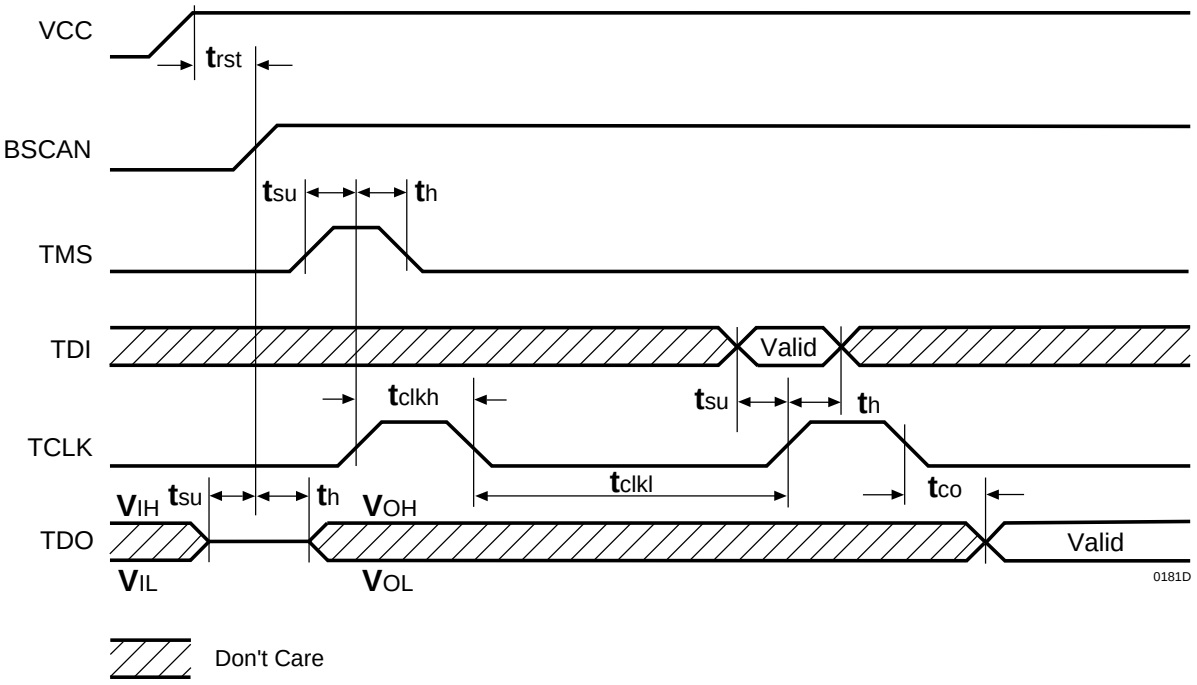
The timing specifications for Boundary Scan are listed below. The waveforms are shown in figure 5.

Boundary Scan Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
t_{rst}	Reset Time from Valid V_{CC}		100	–	–	µs
t_{su}	Setup Time		60	–	–	ns
t_h	Hold Time		60	–	–	ns
t_{co}	Clock to Output		–	–	60	ns
t_{clkh}	Clock Pulse Duration, High		60	–	–	ns
t_{clkl}	Clock Pulse Duration, Low		60	–	–	ns

Table 2 - 0028Aisp-3256

Figure 5. Boundary Scan Waveforms



Pin Description

NAME	MQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 4 I/O 5 - I/O 9 I/O 10 - I/O 14 I/O 15 - I/O 19 I/O 20 - I/O 24 I/O 25 - I/O 29 I/O 30 - I/O 34 I/O 35 - I/O 39 I/O 40 - I/O 44 I/O 45 - I/O 49 I/O 50 - I/O 54 I/O 55 - I/O 59 I/O 60 - I/O 64 I/O 65 - I/O 69 I/O 70 - I/O 74 I/O 75 - I/O 79 I/O 80 - I/O 84 I/O 85 - I/O 89 I/O 90 - I/O 94 I/O 95 - I/O 99 I/O 100 - I/O 104 I/O 105 - I/O 109 I/O 110 - I/O 114 I/O 115 - I/O 119 I/O 120 - I/O 124 I/O 125 - I/O 127	25, 26, 28, 29, 30, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 46, 47, 48, 49, 50, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 64, 65, 66, 67, 68, 69, 70, 72, 73, 74, 75, 76, 77, 78, 79, 80, 82, 83, 84, 85, 86, 87, 88, 89, 90, 92, 93, 94, 95, 96, 105, 106, 108, 109, 110, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 126, 127, 128, 129, 130, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 144, 145, 146, 147, 148, 149, 150, 152, 153, 154, 155, 156, 157, 158, 159, 160, 2, 3, 4, 5, 6, 7, 8, 9, 11, 13, 14, 15, 16, 17	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0 and GOE1 TOE	100 and 99 98	Global Output Enable input pins. Test output enable pin.
$\overline{\text{RESET}}$ Y0, Y1 and Y2 Y3 and Y4	20 18, 19, 103 102, 101	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device. Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device. Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the I/O cells in the device.
BSCAN/$\overline{\text{ispEN}}$** TDI/SDI* TCLK/SCLK* TMS/MODE* $\overline{\text{TRST}}$ TDO/SDO*	21 22 23 24 97 104	Boundary Scan Enable. Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active. Input - This pin performs two functions. It is the Test Data input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the isp state machine. Input - This pin performs two functions. It is the Test Clock input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. Input - This pin performs two functions. It is the Test Mode Select input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine. Input - Test Reset, active low to reset the Boundary Scan State Machine. Output - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the isp data. When $\overline{\text{ispEN}}$ is high it functions as Test Data Out.
GND VCC	1, 10, 27, 45, 63, 81, 107, 125, 143 12, 31, 51, 71, 91, 111, 131, 151	Ground (GND) V_{CC}

Table 2 - 0002Bisp/3256

* ispLSI 3256 only

** $\overline{\text{ispEN}}$ for ispLSI 3256 only, NC for pLSI 3256 must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

Pin Description

NAME	CPGA PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 4 I/O 5 - I/O 9 I/O 10 - I/O 14 I/O 15 - I/O 19 I/O 20 - I/O 24 I/O 25 - I/O 29 I/O 30 - I/O 34 I/O 35 - I/O 39 I/O 40 - I/O 44 I/O 45 - I/O 49 I/O 50 - I/O 54 I/O 55 - I/O 59 I/O 60 - I/O 64 I/O 65 - I/O 69 I/O 70 - I/O 74 I/O 75 - I/O 79 I/O 80 - I/O 84 I/O 85 - I/O 89 I/O 90 - I/O 94 I/O 95 - I/O 99 I/O 100 - I/O 104 I/O 105 - I/O 109 I/O 110 - I/O 114 I/O 115 - I/O 119 I/O 120 - I/O 124 I/O 125 - I/O 127	G1, G2, G3, E1, F2, F3, C1, E2, E3, D2, D3, B2, C3, C4, B3, B1, B4, C5, A3, B5, C6, A4, B6, A5, C7, A6, A7, C8, B8, B9, C9, A9, A10, B10, A11, B11, A12, C11, A13, B12, A14, A15, A16, C13, B14, B15, C14, B16, C15, D15, A17, D16, E15, B17, C17, E16, F15, D17, E17, F17, G16, G17, H15, H16, L16, M17, N17, M16, P17, R17, N16, S17, N15, P16, P15, S16, R15, R14, S15, T17, S14, R13, T15, S13, R12, T14, S12, T13, R11, T12, T11, R10, S10, S9, R9, T9, T8, S8, T7, S7, T6, R7, T5, S6, T4, T3, T2, R5, S4, S3, R4, S2, R3, P3, T1, P2, N3, S1, R1, N2, M3, P1, N1, M1, L2, L1, K3, K2	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0 and GOE1 TOE	J17 and J15 J16	Global Output Enable input pins. Test output enable pin.
$\overline{\text{RESET}}$ Y0, Y1 and Y2 Y3 and Y4	J3 K1, J2, K15 K16, K17	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device. Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device. Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the I/O cells in the device.
BSCAN/$\overline{\text{ispEN}}$** TDI/SDI* TCLK/SCLK* TMS/MODE* $\overline{\text{TRST}}$ TDO/SDO*	J1 H1 H2 H3 H17 L17	Boundary Scan Enable. Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active. Input - This pin performs two functions. It is the Test Data input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the isp state machine. Input - This pin performs two functions. It is the Test Clock input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. Input - This pin performs two functions. It is the Test Mode Select input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine. Input - Test Reset, active low to reset the Boundary Scan State Machine. Output - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the isp data. When $\overline{\text{ispEN}}$ is high it functions as Test Data Out.
GND VCC	F1, C2, A2, B7, C10, B13, C16, F16, L15, R16, T16, S11, S5, R8, R2, M2 D1, A8, G15, C12, M15, T10, L3, R6	Ground (GND) V_{CC}

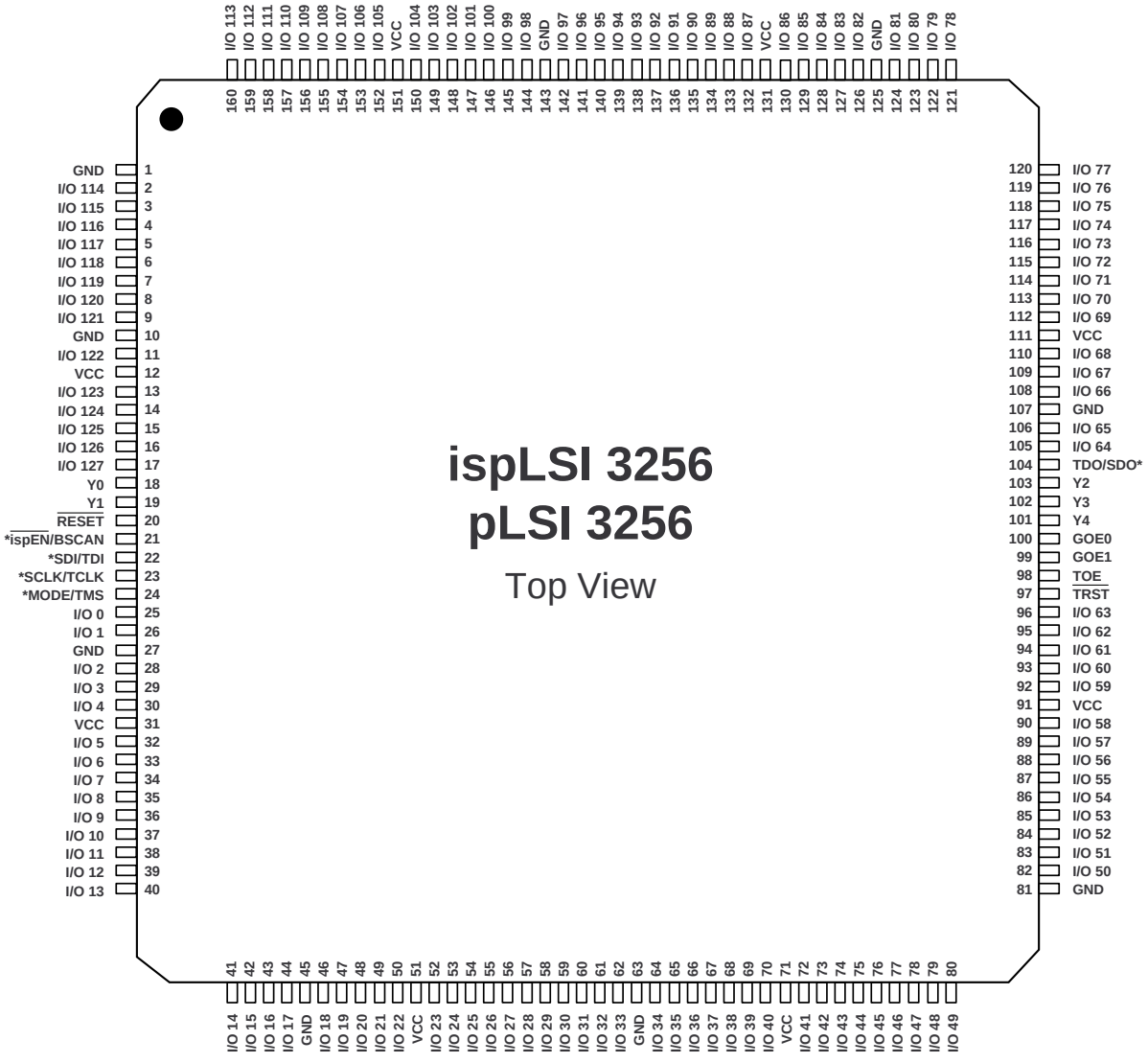
Table 2 - 0002isp/3256

* ispLSI 3256 only

** $\overline{\text{ispEN}}$ for ispLSI 3256 only, NC for pLSI 3256 must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

Pin Configuration

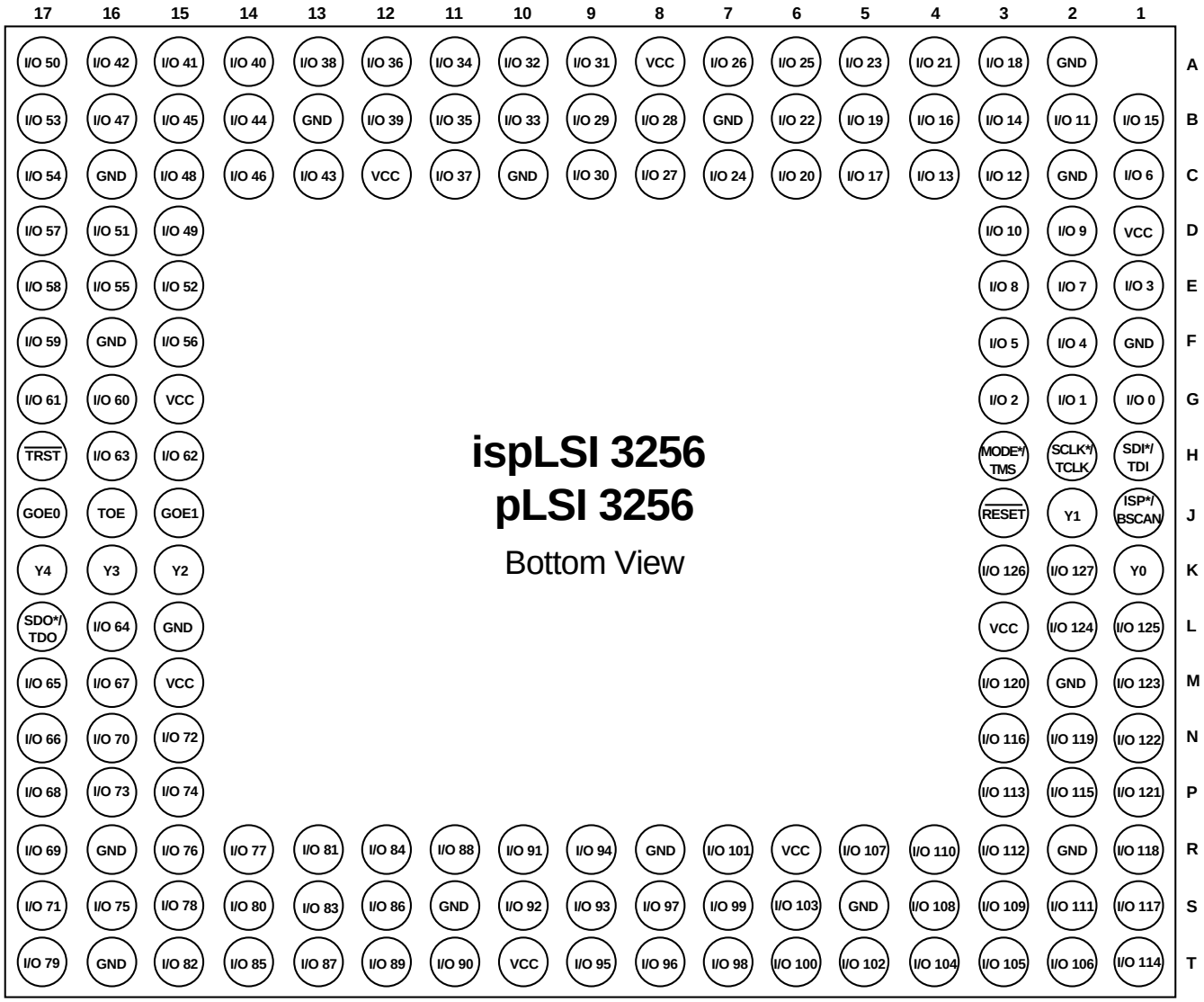
ispLSI and pLSI 3256 160-pin MQFP



*Pins have dual function capability for ispLSI 3256 only.

Pin Configuration

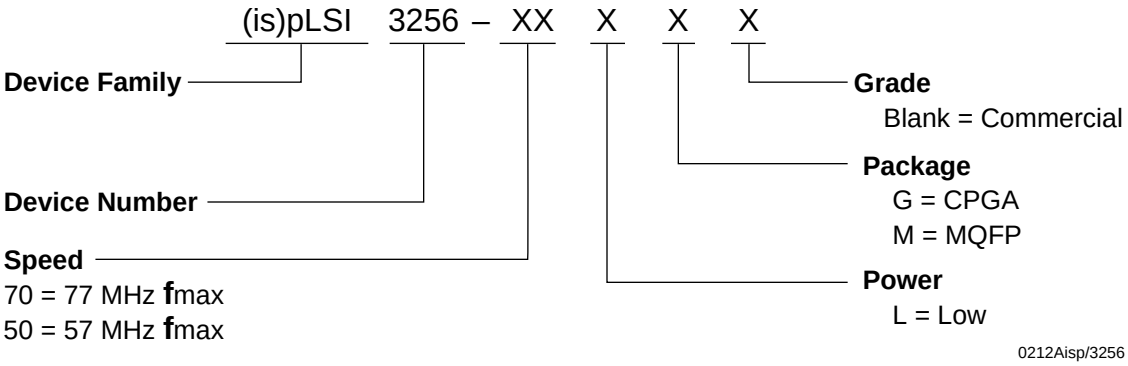
ispLSI and pLSI 3256 167-Pin CPGA



*Pins have dual funtion capability for ispLSI 3256 only.

0123Bisp

Part Number Description



0212Aisp/3256

Ordering Information

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	77	15	ispLSI 3256-70LM	160-Pin MQFP
	77	15	ispLSI 3256-70LG	167-Pin CPGA
	57	20	ispLSI 3256-50LM	160-Pin MQFP
	57	20	ispLSI 3256-50LG	167-Pin CPGA
pLSI	77	15	pLSI 3256-70LM	160-Pin MQFP
	77	15	pLSI 3256-70LG	167-Pin CPGA
	57	20	pLSI 3256-50LM	160-Pin MQFP
	57	20	pLSI 3256-50LG	167-Pin CPGA

Table 2 - 0041A-08isp/3256

Introduction to ispLSI® and pLSI® 6000 Family

Introduction

Lattice Semiconductor Corporation's ispLSI® and pLSI® families are high-density, cell-based E^2CMOS® programmable logic devices. These devices provide design engineers with a superior system solution for integrating high-speed logic on a single chip.

The Lattice Semiconductor Corporation (LSC) ispLSI and pLSI 6000 Family combines high-density, general-purpose programmable logic with dedicated memory and register/counter modules. The result is a family of devices that support system-level integration of memory and logic functions with enhanced performance.

The ispLSI and pLSI 6000 family is ideal for high-density designs, where integration of complete logic subsystems into a single device is necessary. System applications include intelligent DMA controllers, serial controllers/ LAN controllers/UARTS, multimedia video/audio processors, video controllers, master bus interfaces and data acquisition controllers.

The ispLSI family incorporates Lattice Semiconductor's innovative in-system programmable™ (ISP™) technology. ISP technology allows for real-time programming, less expensive manufacturing and end-user feature reconfiguration.

LSC's E^2CMOS technology features reprogrammability, the ability to program a device again and again, to easily incorporate any design modifications. This capability allows full parametric testability during manufacturing, guaranteeing 100 percent programming and functional yield.

All necessary development tools are available from Lattice Semiconductor and third-party vendors. Development tools offered range from LSC's low-cost pDS® software, featuring Boolean entry in a graphical Windows™-based environment, to the pDS+™ family of Fitters that interface with third-party development software packages. pDS+ systems support schematic capture, state machine, Boolean, and HDL Design entry. Designs can now be completed in hours as opposed to days or weeks.

ispLSI and pLSI 6000 Family

- ❑ 70 MHz System Performance
- ❑ 15 ns Pin-to-Pin Delay
- ❑ 20 ns Memory Access Time
- ❑ High Density General Purpose Programmable Logic Module (8,000 PLD Gates)
- ❑ 4K-Bit Memory FIFO/Dual-Port/Single-Port Memory Module
- ❑ 8 x 16-Bit Register/Counter Module
- ❑ 208-Pin Package with 157 User I/Os
- ❑ In-System Programmable (ispLSI)
- ❑ Boundary Scan Test (IEEE 1149.1 Standard)

ispLSI and pLSI Technology

- ❑ UltraMOS E^2CMOS — the PLD Technology of Choice
- ❑ Electrically Erasable/Programmable/ Reprogrammable
- ❑ 100% Tested During Manufacture
- ❑ 100% Programming Yield
- ❑ Fast Programming

ispLSI and pLSI Development Tools

- ❑ Low Cost, Fully Integrated pDS Design System for the PC
- ❑ HDL, VHDL, Boolean Equation, State Machine and Schematic Capture Entry
- ❑ pDS+ Support for Industry-Standard Third-Party Design Environments and Platforms*
- ❑ Timing and Functional Simulation
- ❑ PC and Workstation Platforms

*Note: pDS+ support in third-party CAE environments is scheduled for 1996 introduction. Contact Lattice Semiconductor for availability.

6000 Family Overview

The ispLSI and pLSI 6000 family of high-density devices address high-performance system integration needs, including registers, counters, multiplexers, complex state machines and memory all on a single device.

The first series of devices in the ispLSI and pLSI 6000 Family consists of the ispLSI and pLSI 6192FF, 6192DM and 6192SM. These devices vary only in the dedicated memory configuration: the 6192FF has a programmable 4K-Bit FIFO, the 6192DM has a dual-port memory, and the 6192SM has a single-port memory. Each device includes an 8 x 16-Bit programmable register/counter module and a 24 Twin GLB/192 macrocell programmable logic module based on the ispLSI and pLSI 3000 Family architecture.

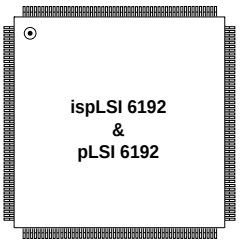
Each device contains multiple Generic Logic Blocks (GLBs) in the programmable logic module, which are designed to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provides the optimum combination of internal logic and external connections. A global interconnect scheme ties all logic and memory together. An abundance of general-purpose and dedicated module I/O pins gives easy access to all resources externally. Table 1 describes the family attributes.

Table 1. ispLSI and pLSI 6000 Family Attributes

Family Member	6192FF	6192SM	6192DM
Memory Module	FIFO	Single-Port SRAM	Dual-Port SRAM
	Organization: 512 x 9 or 256 x 18 (FF, SM, DM); 256 x 9 or 128 x 18 (SM Only) Speed: 20 ns Access Time		
Register/Counter Module	Organization: 8 x 16-Bit Register/Counter/Timer/Shift Register Speed: 125 MHz Counter Frequency		
Programmable Logic Module	Organization: 192 Macrocell/24 Twin GLB Speed: 15 ns Tpd/70 MHz Fmax		

6K Attributes

Figure 1. 6000 Family Package



208-Pin MQFP

0288-160C/6K

ispLSI® and pLSI® 6192

High Density Programmable Logic with Dedicated Memory and Register/Counter Modules

Features

- **A FAMILY OF HIGHLY INTEGRATED, CELL-BASED, PROGRAMMABLE LOGIC DEVICES CONSISTING OF:**
  - **— Memory Module**
  - **— Register/Counter Module**
  - **— Programmable Logic Module**
  - **— 159 User Logic/Memory/Register/Counter Pins**
  - **— 25000-Gate Overall Density**
- **MEMORY MODULE OPTIONS**
  - **— FIFO (6192FF), Single-Port RAM (6192SM) or Dual-Port RAM (6192DM)**
  - **— Programmable Organizations:**
    - **Single 256 x 18 or 512 x 9**
    - **Dual 128 x 18 or 256 x 9 (6192SM)**
  - **— 31 Dedicated Data and Control Interface Pins**
  - **— Programmable Almost Empty and Almost Full Flags (FIFO)**
  - **— Dedicated Arbitration/Busy Logic (Dual-Port RAM)**
- **REGISTER/COUNTER MODULE**
  - **— 8 Cascadable 16-Bit Functions**
  - **— 9 Programmable Modes Including Counter, Timer, Shift Register and Register Options**
  - **— 24 Dedicated Module Data and Control Pins Including Terminal Count Flags**
  - **— Automatic Preload, Count Up/Down Options**
- **HIGH DENSITY PROGRAMMABLE LOGIC MODULE**
  - **— 8000-Gate General Purpose Programmable Logic Block**
  - **— 192 General Purpose Logic Registers**
  - **— 24-Input, Twin Generic Logic Blocks (GLBs) Implement Any Registered or Combinatorial Functions**
  - **— High-Speed Global Interconnects**
  - **— 96 I/O Pins with Input Registers**
  - **— Security Cell Prevents Unauthorized Design Copying**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 77 MHz Maximum Operating Frequency**
  - **— t_{pd} = 15 ns Propagation Delay**
  - **— f_{cnt} = 125 MHz Counter Frequency**
  - **— 50MHz FIFO Data Rate**
  - **— 20ns Memory Access Time**
  - **— Electrically Erasable and Reprogrammable**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - **— In-System Programmable™ 5-Volt Only**
  - **— Change Logic and Interconnects "On-the-Fly" in Seconds**
  - **— Reprogram Soldered Devices for Debugging**
- **IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**

Functional Block Diagram

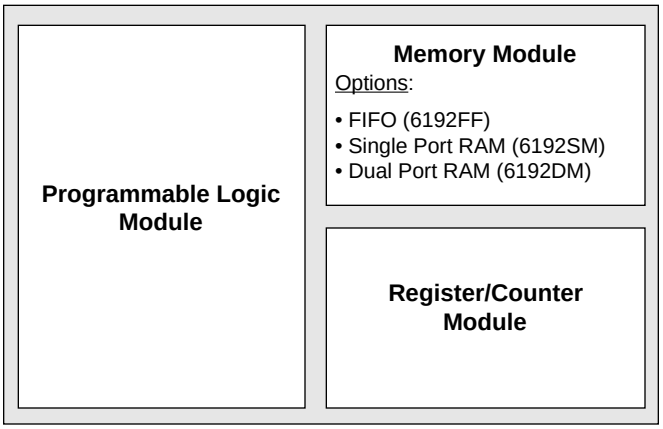


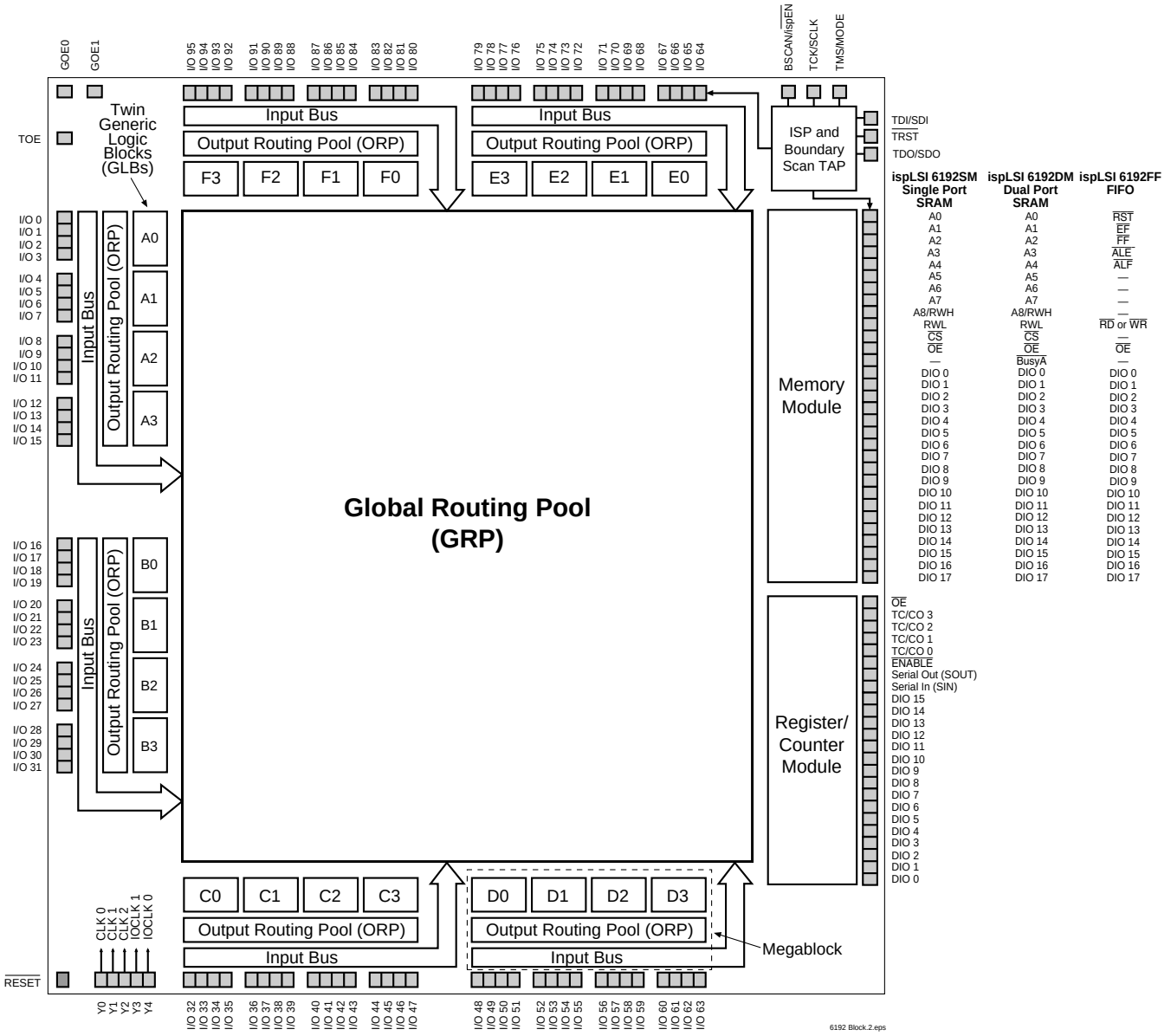
Table 1. ispLSI and pLSI 6192 Device Features

	Memory Module Options			Register/Counter Module	General Programmable Logic Module
Functions	FIFO 6192FF	Single-Port SRAM 6192SM	Dual-Port SRAM 6192DM	Programmable Register / Counter / Timer / Shift Register	Universal: Registered or Combinatorial
Organization (Programmable)	Single: 512 x 9 or 256 x 18 Dual: 128 x 18 or 256 x 9 (6192SM Only)			Cascadeable 8 x 16 Bit Words	192 Macrocells
External Interface	18 I/O & 13 Control Pins			16 I/O & 8 Control Pins	96 I/O / 5 Clocks / 2 Global Output Enables
Performance	20ns Memory Access Time (Tacc)			125MHz Counter Frequency (Fcnt)	15ns Logic Delay (Tpd) 77MHz Frequency (Fmax)
Programmability	In-System Programmable				
Testability	IEEE 1149.1 Boundary Scan Test				
Package	208-Pin Metal Quad Flat Pack (MQFP)				

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Functional Block Diagram

Figure 1. ispLSI and pLSI 6192 Functional Block Diagram



ispLSI 6192SM Single Port SRAM	ispLSI 6192DM Dual Port SRAM	ispLSI 6192FF FIFO
A0	A0	$\overline{RST}$
A1	A1	$\overline{EF}$
A2	A2	$\overline{FF}$
A3	A3	$\overline{ALE}$
A4	A4	$\overline{ALF}$
A5	A5	—
A6	A6	—
A7	A7	—
A8/RWH	A8/RWH	—
RWL	RWL	$\overline{RD}$ or $\overline{WR}$
$\overline{CS}$	$\overline{CS}$	—
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
—	$\overline{BusyA}$	—
DIO 0	DIO 0	DIO 0
DIO 1	DIO 1	DIO 1
DIO 2	DIO 2	DIO 2
DIO 3	DIO 3	DIO 3
DIO 4	DIO 4	DIO 4
DIO 5	DIO 5	DIO 5
DIO 6	DIO 6	DIO 6
DIO 7	DIO 7	DIO 7
DIO 8	DIO 8	DIO 8
DIO 9	DIO 9	DIO 9
DIO 10	DIO 10	DIO 10
DIO 11	DIO 11	DIO 11
DIO 12	DIO 12	DIO 12
DIO 13	DIO 13	DIO 13
DIO 14	DIO 14	DIO 14
DIO 15	DIO 15	DIO 15
DIO 16	DIO 16	DIO 16
DIO 17	DIO 17	DIO 17

$\overline{OE}$
TC/CO 3
TC/CO 2
TC/CO 1
TC/CO 0
$\overline{ENABLE}$
Serial Out (SOUT)
Serial In (SIN)
DIO 15
DIO 14
DIO 13
DIO 12
DIO 11
DIO 10
DIO 9
DIO 8
DIO 7
DIO 6
DIO 5
DIO 4
DIO 3
DIO 2
DIO 1
DIO 0

Note:
Since certain signal names are duplicated on Memory Module and Register/Counter Module pins ($\overline{OE}$, DIO), the notation:

$\overline{OE}$ (RAM)
$\overline{OE}$ (RC)
DIO (RAM)
DIO (FIFO)
DIO (RC)

will be used periodically in this data sheet to differentiate signals.

Description

The ispLSI and pLSI 6192 devices are High Density, Cell-Based Programmable Logic Devices that contain a dedicated Memory Module, a dedicated Register/Counter Module and an 8000-gate general-purpose Programmable Logic block. Output Routing Pools (ORP) and a Global Routing Pool (GRP) give complete interconnectivity between these elements. The Cell-Based architecture with dedicated modules have been added to enhance the functionality, performance and utilization of the devices.

The ispLSI and pLSI 6192 families are each offered in three versions: the 6192FF (FIFO), 6192SM (Single Port RAM) and 6192DM (Dual Port RAM). All three devices employ the same general-purpose programmable logic module and register/counter module, with only the memory module functionality changing. The pinouts of the three devices are different only in the memory module control interface pins.

Memory Module

Lattice Semiconductor offers a dedicated dual-port FIFO module in the 6192FF device. The FIFO is user configurable as a 256 x 18 or 512 x 9 block and is connected to the external world through dedicated FIFO I/O pins. The other data port of the FIFO goes to the GRP. A variety of FIFO control flags such as Full ($\overline{FF}$), Almost Full ($\overline{ALF}$), Almost Empty ($\overline{ALE}$) and Empty ($\overline{EF}$) are available as dedicated device outputs. These signals are also available as inputs to the GRP to facilitate use by on-chip logic. The FIFO operation is discussed at length in the following sections.

The 6192SM features a single-port memory module. The module can be organized either as a single 256 x 18 or 512 x 9 single port memory or as two smaller 128 x 18 or 256 x 9 single port memories. The external interface features memory address input pins (A0-A8), Read/Write (RWL, RWH), Chip Select ($\overline{CS}$), Output Enable ($\overline{OE}$) control lines, and 18 bidirectional data lines. The memory can be accessed from this external interface or from the internal GRP based on the user's design.

The 6192DM has functionality similar to the 6192SM, but access from the GRP or external pins is supported concurrently. Dedicated arbitration logic and Busy flags help to resolve issues arising from simultaneous access from both ports of the same memory location. The Busy signal from the external port ($\overline{BusyA}$) is available at a dedicated device pin. The dual-port memory is configurable as a single 256 x 18 or 512 x 9 memory.

Register/Counter Module

An additional feature of the 6192 devices is a dedicated Register/Counter module. Eight 16-bit blocks are available to function as registers or shift registers. In addition, four of these blocks can be programmed to operate as loadable Up/Down counters. These four blocks include carry-in and carry-out connections to allow counter cascading up to 64 bits. The Register/Counter block also has a 16-bit data port connected to the GRP along with a variety of control inputs and status flag outputs.

Programmable Logic Module

The basic unit of general-purpose programmable logic on the 6192 devices is the Twin Generic Logic Block (Twin GLB). There are a total of 24 of these Twin GLBs in the 6192 devices. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays as well as eight outputs which can be configured independently to be combinatorial or registered. All Twin GLB logic inputs come from the GRP.

Four Twin GLBs, 16 I/O cells and one ORP form a logic Megablock. The 16 I/O cells within a Megablock share one Product Term Output Enable and two Global Output Enable signals. The outputs of four Twin GLBs are connected to a set of 16 I/O cells by the ORP. The ispLSI and pLSI 6192 devices each contain six of these Megablocks.

The GRP has, as its inputs, the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells as well as independent bidirectional data bus ports from the FIFO and Register/Counter blocks. Flag outputs from these modules as well as control inputs are also connected to the GRP. All these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

All GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other logic block on the device. The device has 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a latched input, an output or a bidirectional I/O pin with 3-state control. Output signal levels are TTL compatible and the output drivers can source 4mA and sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. The devices are packaged in space saving 208-pin Metal Quad Flat Pack (MQFP) packages.

Clocks in the ispLSI and pLSI 6192 devices are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

In-System Programmability

The ispLSI 6192 devices also feature 5-Volt in-system programmability and in-system diagnostic capabilities. Through this capability, the devices offer non-volatile “on-the-fly” reprogrammability of logic and memory to support truly reconfigurable systems.

Boundary Scan

The 6192 families also have Boundary Scan capability, consisting of dedicated cells connected between the on-chip system logic and the device’s input and the output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one. The device supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

General Purpose Programmable Logic Module

The following is a brief description of the general purpose programmable logic module. For additional information on this module see the 1000/E Family Architectural Description in Section 2 of this Data Book.

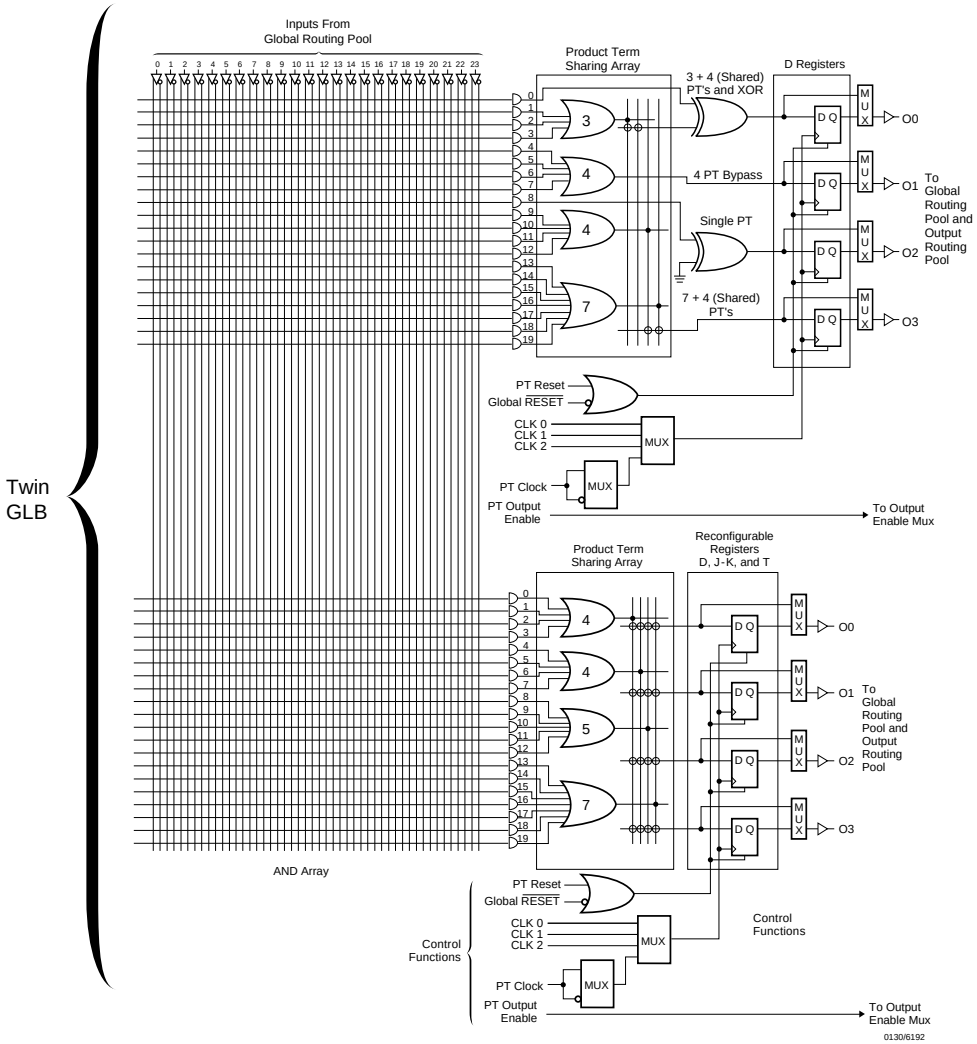
Generic Logic Block

The Twin GLB is the standard logic block of the Lattice Semiconductor ispLSI and pLSI 6192 families. This Twin GLB has 24 inputs, eight outputs and the logic necessary to implement most standard logic functions. The internal logic of the Twin GLB is divided into four separate sections: the AND Array, Product Term Sharing Array, Reconfigurable Registers, and Control section.

The AND array consists of two sets of 20 product terms which are the logical product of any of the 24 Twin GLB inputs. These inputs all come from the GRP, and are either feedback signals from any of the 24 Twin GLBs, inputs from the external I/O Cells or outputs from the memory or Register/Counter Modules. All Twin GLB input signals are available to the product terms in both the logical true and complemented forms which makes Boolean logic reduction easier.

The two Product Term Sharing Arrays (PTSA) take the 20 product terms each and allocate them to two groups of four Twin GLB outputs. There are four OR gates, with four, four, five and seven product term inputs respectively. The output of any of these OR gates can be routed to any of the four Twin GLB outputs, and if more product

Figure 2. ispLSI and pLSI 6192 Twin GLB



terms are needed, the PTSA can combine them as necessary. If the user's main concern is speed, the PTSA can use a bypass circuit with four Product Terms to increase the performance of the cell. This can be done to any or all of the eight outputs of the Twin GLB.

The Reconfigurable Registers consist of four D-type flip-flops with an XOR gate on the input. The XOR gate in the GLB can be used either as a logic element or to reconfigure the D-type flip-flop to emulate a J-K or T-type flip-flop. This greatly simplifies the design of counters, comparators and ALU type functions. The registers can be bypassed if the user needs a combinatorial output. Each register output is brought back into the Global Routing Pool and is also brought to the I/O cells via the Output Routing Pool. Reconfigurable registers are not available when the four product term bypass is used. Figure 2 illustrates the mixed mode configurations of the Twin GLB.

Various signals which control the operation of the GLB outputs are driven from the Control Functions. The clock for the registers can come from any of three CLK0-2 inputs or from a product term within the GLB. The Reset Signal for the GLB can come from the Global Reset pin ($\overline{\text{RESET}}$) or from a product term within the block. The Global Reset pin is always connected and is logically "ORed" with the PT reset (if used). An active reset signal always sets the Q of the registers to the logic 0 state. The Output Enable for the I/O cells associated with the GLB comes form a product term within the block. Use of a product term for output enable makes it unavailable for use as a general-purpose logic term.

Megablock Structure

Four Twin GLBs, 16 I/O cells and one ORP make up a Megablock. Each Twin GLB has a maximum fan-in of 24 inputs, and no dedicated inputs associated with any Megablock. Each Twin GLB has eight associated outputs. A total of 32 GLB outputs are fed to the ORP. However, only 16 out of the 32 outputs feed to 16 I/O cells. The Megablock structure is shown in figure 3.

Figure 3. ispLSI and pLSI 6192 Family Megablock Block Diagram

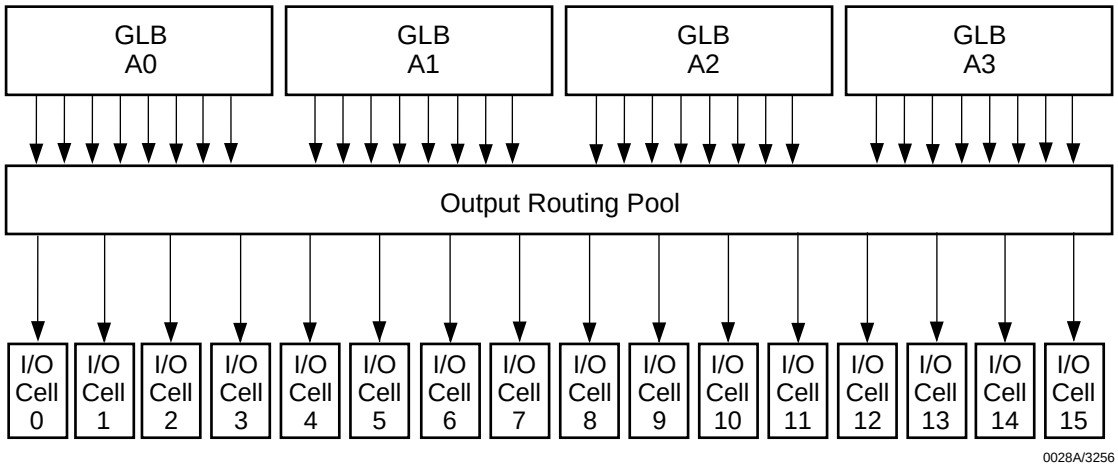


Figure 4. ispLSI and pLSI 6192 Family Global Clock Structure

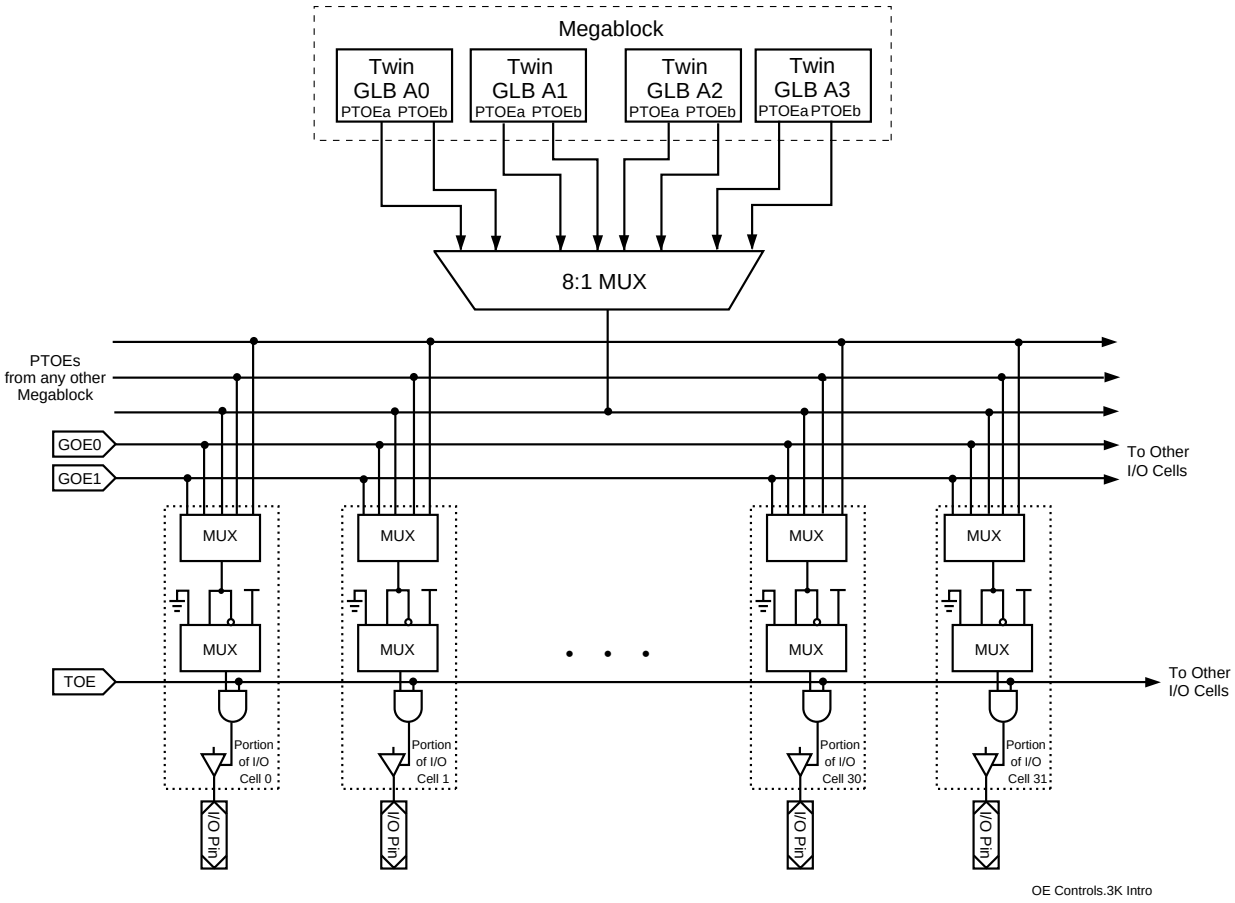
Global Clock Structure

The global clock structure is made up of five global clock input pins, Y0, Y1, Y2, Y3, and Y4. This is shown in figure 4. Three of the clock pins are dedicated for GLB clocks and the remaining two clock pins are dedicated for I/O register clocks. All input clock signals are fed directly to the GLB clock input via a clock multiplexer. The GLB global clocks do not have inversion capability, but the product term clock does have inversion capability before it reaches the clock multiplexer.

Output Enable Controls

A global test OE signal (TOE) is hardwired to all I/O cells and is useful to perform static testing of all the 3-state output buffers within the device. In addition to the test OE signal, two global OEs (GOE0 and GOE1) are connected to all I/O pins. The product term OE is shared between two Megablocks resulting in twice the GLBs being able to use a single OE signal. The Megablock OE signal and global OE signals are fed to an OE multiplexer. The OE signals, with the exception of the test OE, have inversion capability after going through the OE multiplexer as shown in figure 5.

Figure 5. ispLSI and pLSI 6192 Family Output Enable Controls



Boundary Scan

Boundary Scan (IEEE 1149.1 compatible) is a test feature incorporated within the device to provide on-chip test capabilities during PCB testing. Five input signal pins, BSCAN, TDI, TCK, TMS, $\overline{TRST}$, and one output signal pin, TDO, are associated with the boundary scan logic cells. These signals share the same dedicated signal pins used for ISP programming. The signal BSCAN is associated with the $\overline{ispEN}$ pin, TDI corresponds to the SDI pin, TCK corresponds to the SCLK pin, TMS corresponds to the MODE pin, and TDO corresponds to the SDO pin. When $\overline{ispEN}$ is asserted low, the MODE, SDI, SDO, and SCLK options become active for ISP programming. Otherwise, BSCAN, TDI, TCK, TMS, TDO, and $\overline{TRST}$ options become active for boundary scan testing of the device. The boundary scan block diagram is shown in figure 6. TDI is the test data serial input, TCK is the boundary scan clock associated with the serial shift register, TMS is the test mode select input, TDO is the test data output, and finally $\overline{TRST}$ is the reset signal pin.

The user interfaces to the boundary scan circuitry through the Test Access Port (TAP). The TAP consists of a control state machine, instruction decoder and instruction register.

The TAP is controlled using the test control lines: Test Data IN (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Reset ($\overline{TRST}$) and Test Clock (TCK).

The TAP controls the operation of the Boundary Scan Registers after decoding the instruction code sent to the instruction register (see table 3).

The Boundary Scan Registers for the I/O cells are shown in figure 7. As illustrated in the figure, each General-Purpose I/O cell contains 3 registers, 2 latches and 5 multiplexers to implement the ability to capture the state of the I/O cell or set the state of the output path of the cell or function as a conventional I/O cell. Module I/O cells eliminate the output enable registers (OE control comes from OE pins).

The Boundary Scan Registers required for an input only cell are shown in figure 8. An input only cell can only have its state captured, which only requires one MUX and one register. Output-only cells are shown in figure 9. Here, two registers control the output and output enable.

All of the input, output and I/O cells are serially connected together in a long chain. The SCAN OUT of one cell is connected to the SCAN IN of the next cell. The cells are connected in the following order: TDI to I/O47 through I/O32, Y4, Y3, Y2, Y1, $\overline{RESET}$, TOE, GOE1, GOE0, Y0, I/O31 through I/O0, $\overline{BusyA}$, A0/$\overline{RST}$(FIFO), A1/$\overline{EF}$, A2/$\overline{FF}$, A3/$\overline{ALE}$, A4/$\overline{ALF}$, A6, A7, A8/RWH, RWL/$\overline{RD}$ or $\overline{WR}$, $\overline{CS}$, $\overline{OE}$(RAM), DI/O0 through DI/O17(RAM or FIFO), DI/O0 through DI/O15(RC), $\overline{OE}$(RC), SIN, SOUT, ENABLE, TC/CO0 through TC/CO3, I/O48 through I/O95, to TDO.

Note that input-only pins add only one register to control the inputs to the Boundary Scan chain (A0, A5, A6, A7, A8, RWL, $\overline{CS}$, SIN, ENABLE, Y0-Y4, $\overline{RESET}$, TOE, GOE0, GOE1). Output-only pins add two registers to the chain ($\overline{BusyA}$, SOUT, TC/C0-3) to control the output and output enable. Pins that function as input or output add three registers to the chain (I/O0-95, A1/$\overline{EF}$, A2/$\overline{FF}$, A3/$\overline{ALE}$, A4/$\overline{ALF}$) to control inputs, outputs and enables. DI/O0-17(RAM or FIFO) and DI/O0-15(RC) add two registers to the chain per pin for input/output control (output enable for these pins is generated from the respective $\overline{OE}$ pin register. $\overline{OE}$(RC) adds two registers to control its input and the output enable for DI/O0-15(RC). $\overline{OE}$(RAM) adds three registers: one to control its input and two to control the output enables for the high and low bytes of the DI/O(RAM) pins.

Figure 6. Boundary Scan Block Diagram

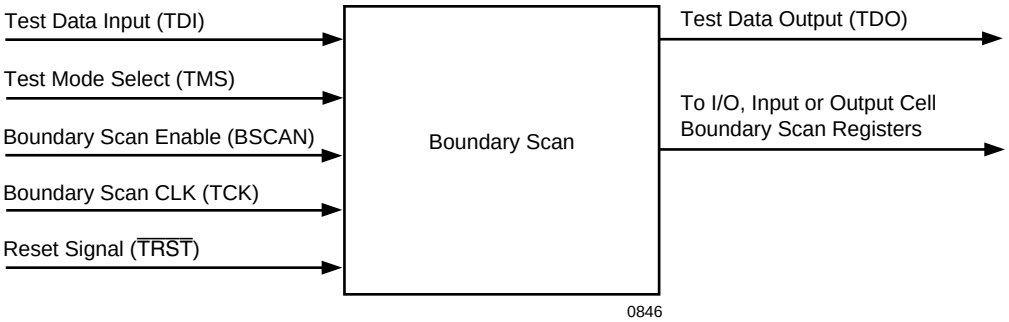


Figure 7. Boundary Scan Registers for I/O Cells

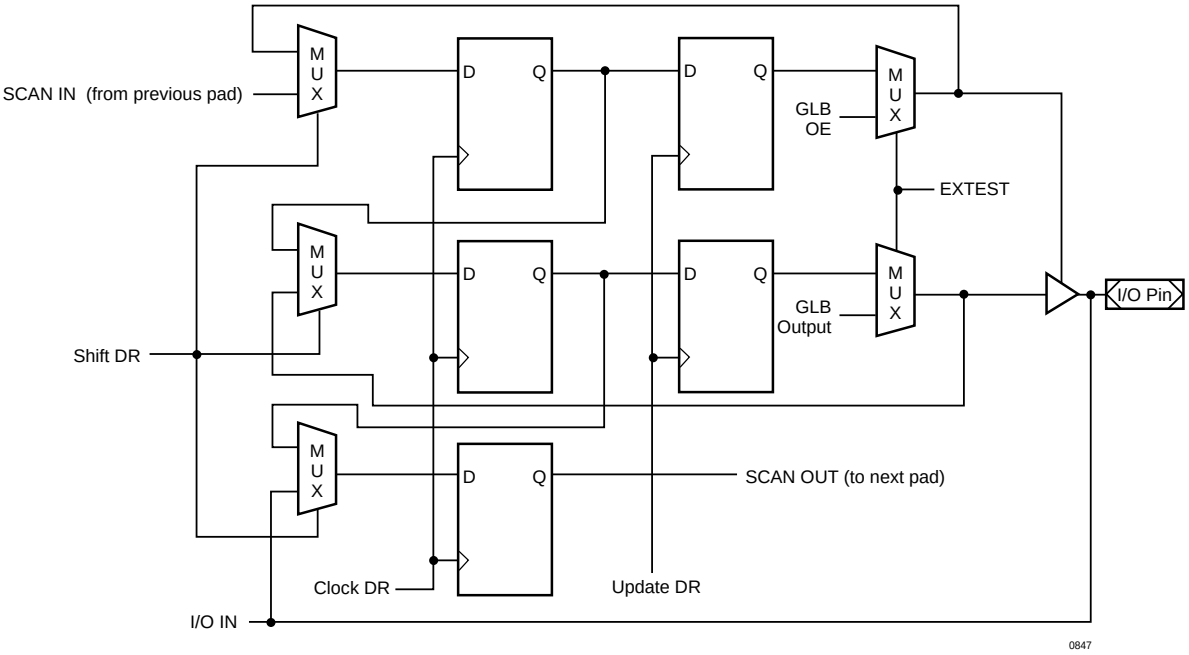


Figure 8. Boundary Scan Registers for an Input Only Cell

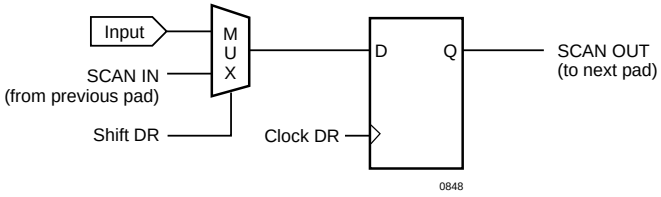


Figure 9. Boundary Scan Registers for Output-Only Cell

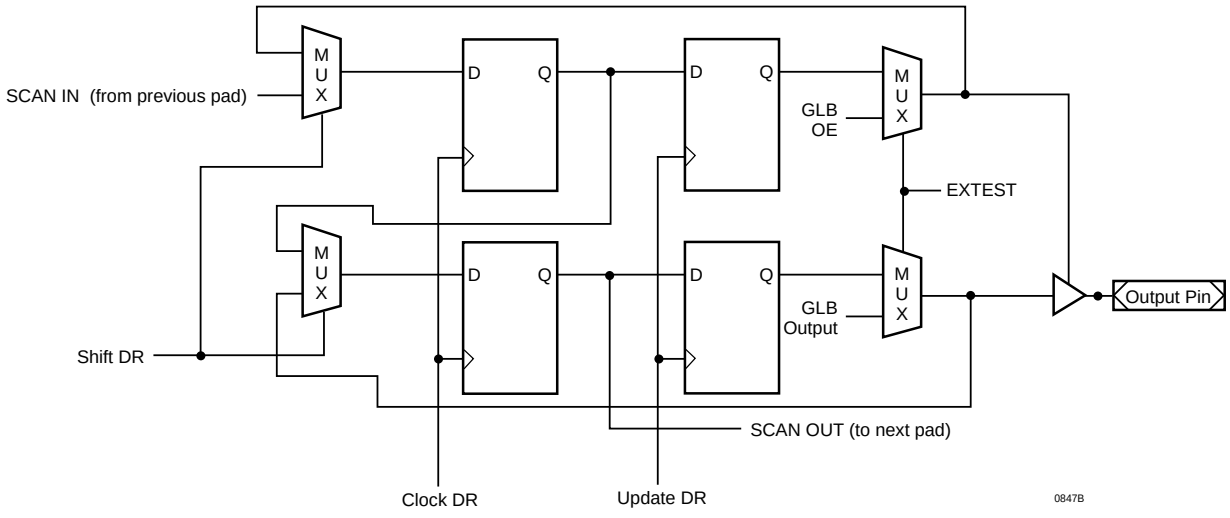


Table 2. Boundary Scan Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
t_{rst}	Reset Time from Valid V_{CC}		100	–	–	µs
t_{su}	Setup Time		60	–	–	ns
t_h	Hold Time		60	–	–	ns
t_{co}	Clock to Output		–	–	60	ns
t_{clkh}	Clock Pulse Duration, High		60	–	–	ns
t_{clkl}	Clock Pulse Duration, Low		60	–	–	ns

Table 2 - 0028Aisp-3256

Figure 10. Boundary Scan Waveforms

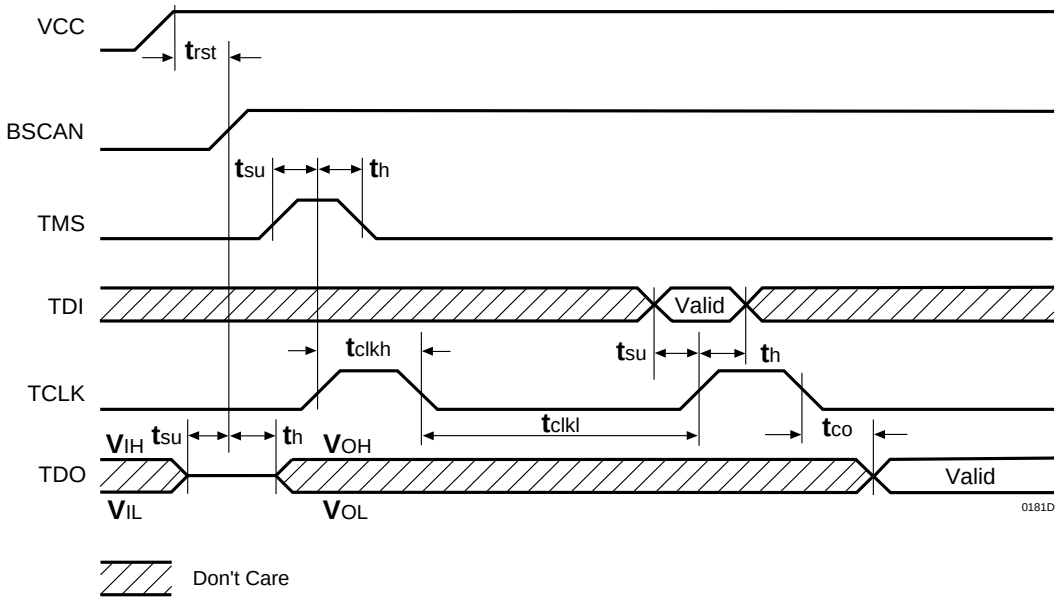


Table 3. Boundary Scan Instruction Codes

Instruction Name	Code	Description
SAMPLE/ PRELOAD	11100	Loads and shifts data into BScan registers
EXTEST	00000	Drives external I/O with BScan registers
BYPASS	11111	Bypasses registers of selected device(s)

Note: LSB shifts in first.

Table 10- 0007

FIFO Description (6192FF)

Integration of high-speed static RAM technology with dedicated internal support logic yields a high-performance, high-density FIFO memory module on the ispLSI and pLSI 6192FF. A FIFO is a First-In/First-Out buffer that acts as an elastic buffer between two synchronous or asynchronous systems with simultaneous read/write accesses. The data rate between the two systems can be regulated by monitoring the status flags and throttling the read and write accesses.

Because data is produced and accepted at different rates, it is important to monitor the boundary conditions (Full or Empty) of the data buffer. Failure to act on the boundary conditions will result in data overflow or underflow. The Empty and Full flags can also be fed back internally to inhibit further Read and Write operations until the FIFO is no longer empty or full.

While offering the basic features of a FIFO, the dedicated FIFO module in the 6192FF device also provides two new user-programmable flags: Almost-Empty and Almost-Full. These flags can be used as early warning flags in critical real-time applications such as data acquisition, high-speed data link and pipeline Digital Signal Processing applications. In a multi-tasking environment, the Almost-Empty and Almost-Full Flags can also be used to set the interrupt request in advance, so that the CPU has sufficient time to perform the switching task.

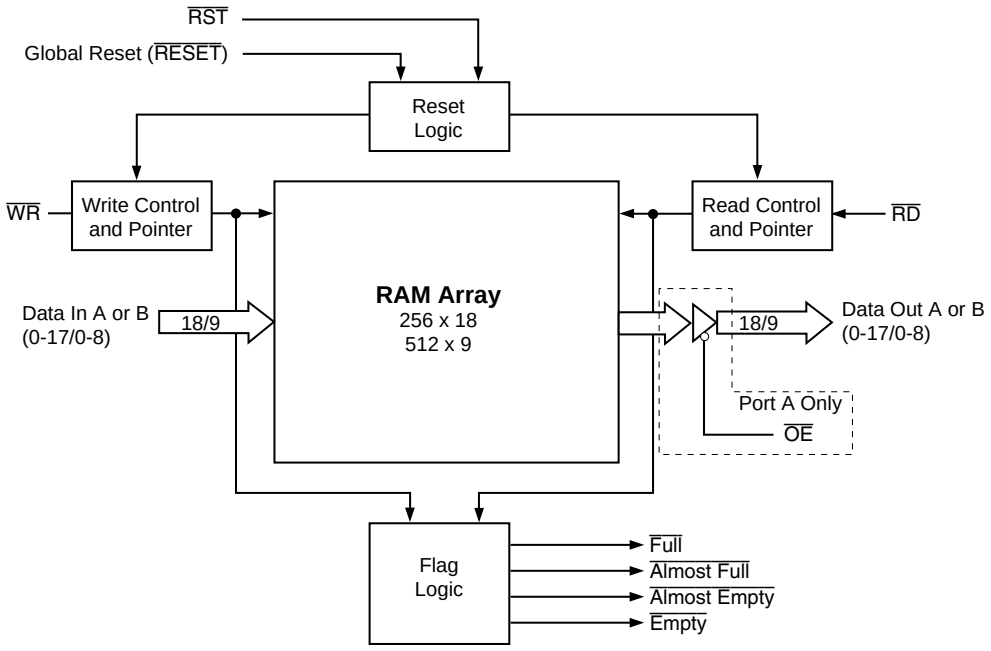
Figure 11 illustrates the functionality of the FIFO. Data In, Write ($\overline{WR}$), Read ($\overline{RD}$) and Reset ($\overline{RST}$) form the inputs and Data Out, Full ($\overline{FF}$), Almost Full ($\overline{ALF}$), Almost Empty ($\overline{ALE}$) and Empty ($\overline{EF}$) constitute the Outputs of the FIFO module. When $\overline{WR}$ is active, data can be written into the RAM array sequentially, independent of Read. When $\overline{RD}$ is active, data can be read from the RAM array sequentially, again, independent of Write. The dedicated module reset or global reset pin of the device can be used to reset the internal address pointers to the first location of RAM array, and all the flags to an empty state. The FIFO signals the empty and full condition by asserting the Empty and Full flags, respectively. The Almost Empty and Almost Full flags can be used to set the interrupt request in advance.

Read, Write and Reset inputs into the FIFO also have user-programmable polarity control so these normally active low signals can be individually defined as active high or active low.

The FIFO is user configurable and can be configured as:

Description	Ports Used
256 x 18 FIFO	A to B
256 x 18 FIFO	B to A
512 x 9 FIFO	A to B
512 x 9 FIFO	B to A

Figure 11. FIFO Module Functional Block Diagram



FIFO Operation

The FIFO can be configured in two directions: Port A to B, where data flows from the dedicated FIFO I/O pins to the GRP, and Port B to A, where data flows from GRP to I/O pins. Accesses between ports can be asynchronous. The module utilizes an 18- or 9-bit wide data bus to make it user configurable as a 256 x 18 or 512 x 9 block.

A write cycle is initiated on the falling edge of the Write ($\overline{WR}$) provided the Full Flag ($\overline{FF}$) is not set. Data is stored in the RAM array sequentially and independently of any ongoing read operation. When the FIFO is full, the Full Flag goes low (becomes active), and further write operations are inhibited to prevent data overflow, i.e., the external Write ($\overline{WR}$) is blocked internally from going low. Upon the completion of a valid read operation, the Full Flag will go high allowing a valid write to begin. If the FIFO is not read after a Reset, the Full Flag will go low after 256 (256 x 18) or 512 (512 x 9) writes. The Almost Full Flag ($\overline{ALF}$) is programmable via E^2CMOS cells on the device. It can be programmed to go low at any given location. It does not, however, inhibit further write operations. The Almost Full location must be above the Almost Empty Flag location.

A read cycle is initiated on the falling edge of Read ($\overline{RD}$) if the Empty Flag ($\overline{EF}$) is not set. The data is accessed from the RAM array sequentially, independent of any ongoing write operations. After Read goes high, the Data Outputs (Data Out 0-17) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting the further read operations. The data outputs will remain in a high impedance state while the FIFO is empty. When the FIFO is empty, the internal read pointer is blocked from going low. Once a valid write operation has been accomplished, the Empty Flag will go high and a valid read can then begin. The Almost Empty Flag can be programmed to go low at any given point but does not inhibit further read operations. This location has to be below the Almost Full Flag location.

Figure 12. Full Flag from Last Write Timing Waveform

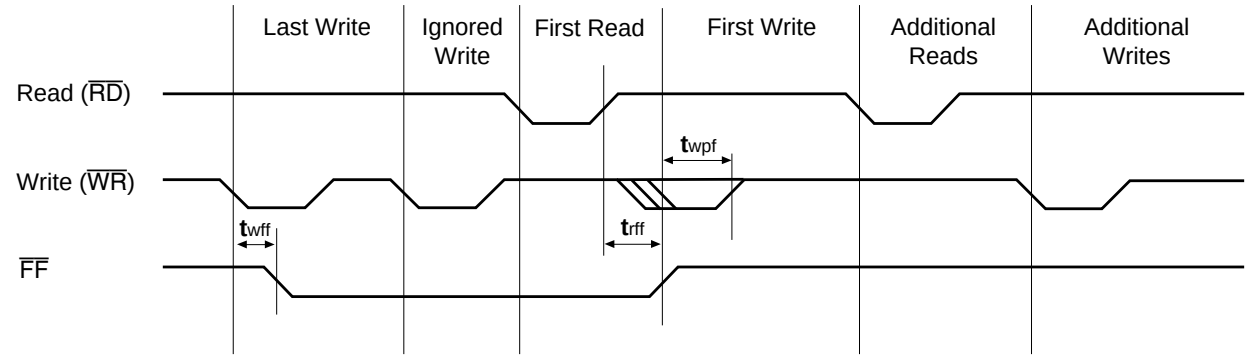
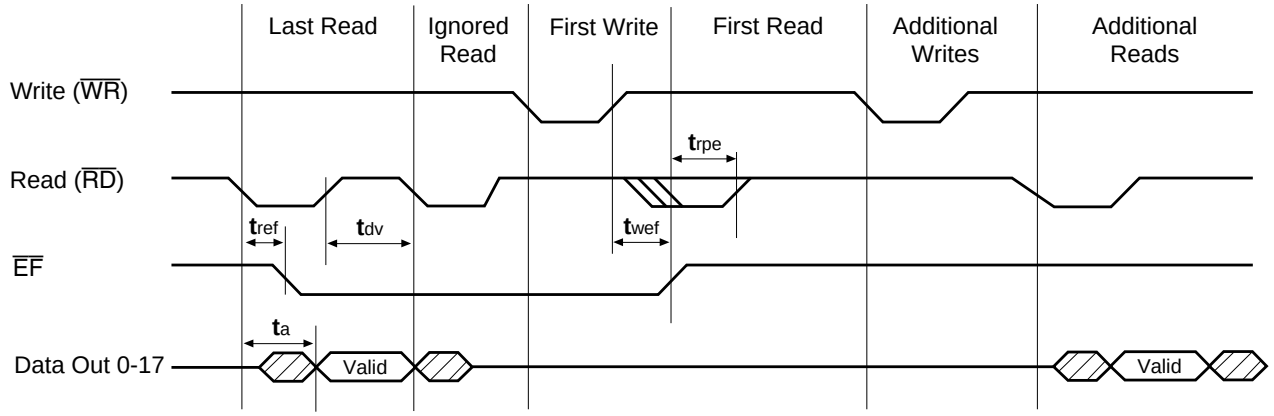


Figure 13. Empty Flag from Last Read Timing Waveform



Reset is accomplished whenever the FIFO Reset ($\overline{RST}$) input is taken to a low state. During reset, internal read and write pointers are set to the first location of the FIFO memory array. Almost Full and Full Flags are cleared (high), and Almost Empty and Empty Flags are set (low). A reset is required after power up before a write operation can take place.

Figure 14. Almost-Empty/Almost-Full Flag Timing Waveform

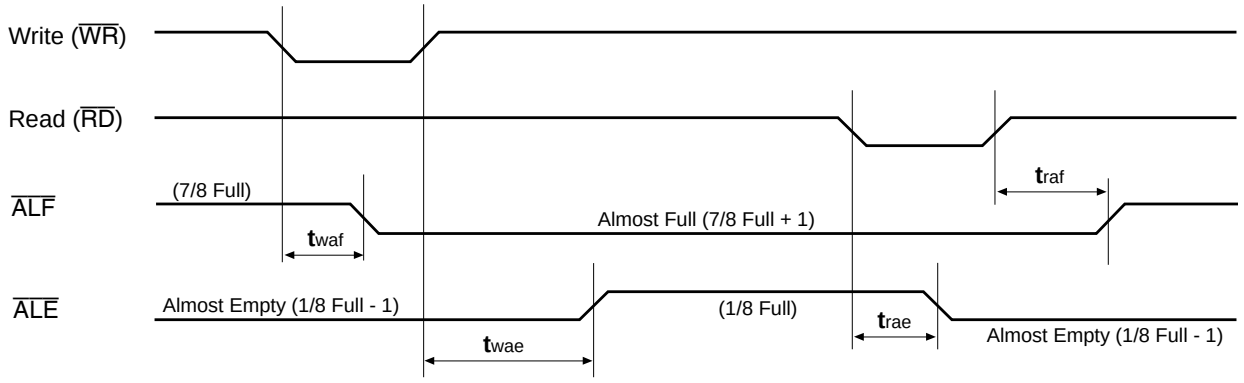


Figure 15. Asynchronous Write and Read Operation Timing Waveform

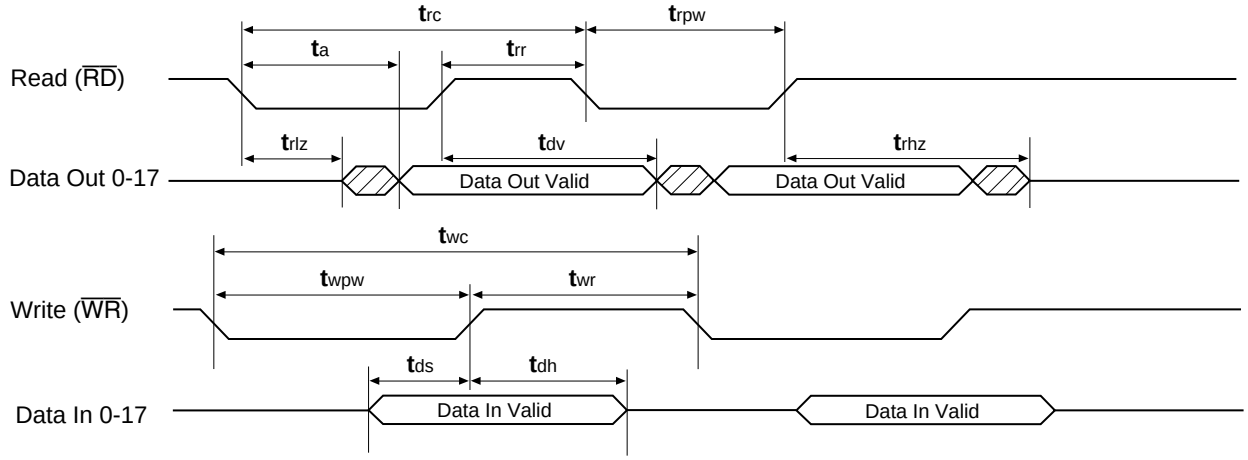
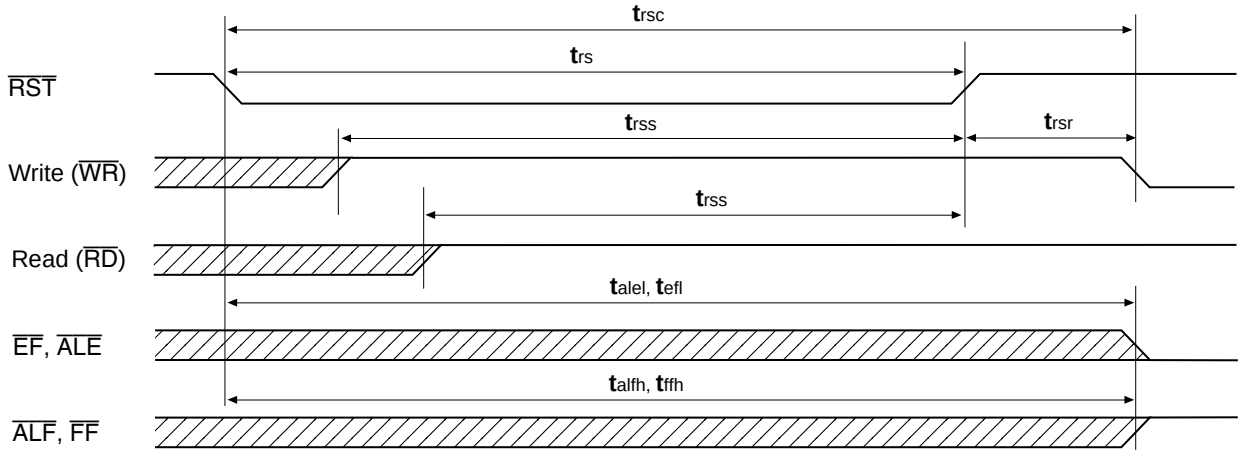


Figure 16. FIFO Reset Timing Waveform



FIFO Interfaces

Port A to B Configuration

Figure 17 below shows the port A to B configuration of the FIFO. Port A is connected to the I/O cells and port B to the GRP of the device. I/O cells (Port A) are used to write data into the FIFO when the Write signal goes low. The GRP (Port B) is driven with the data from the FIFO when the Read signal goes low. The status of the various control flags is passed to the I/O cells and GRP.

In the 512 x 9 FIFO configuration, the high-order 9 bits (Data In A9-17) are used for writing in data. The remaining data I/O pins are pulled high.

Port B to A Configuration

Figure 18 below shows the port B to A configuration of the FIFO. The GRP inputs (Port B) provide data to the FIFO when the Write signal goes low. I/O cells read data from the FIFO when the Read signal goes low. The I/O cells are in the high impedance state when the Read signal is high. The status of various control flags is passed to the I/O cells and GRP.

When not used for memory interfacing, the DIO 0-17 (FIFO) and $\overline{ALE}$ and $\overline{ALF}$ pins may be used for general-pupose logic inputs into the GRP.

Figure 17. Port A to B Configuration

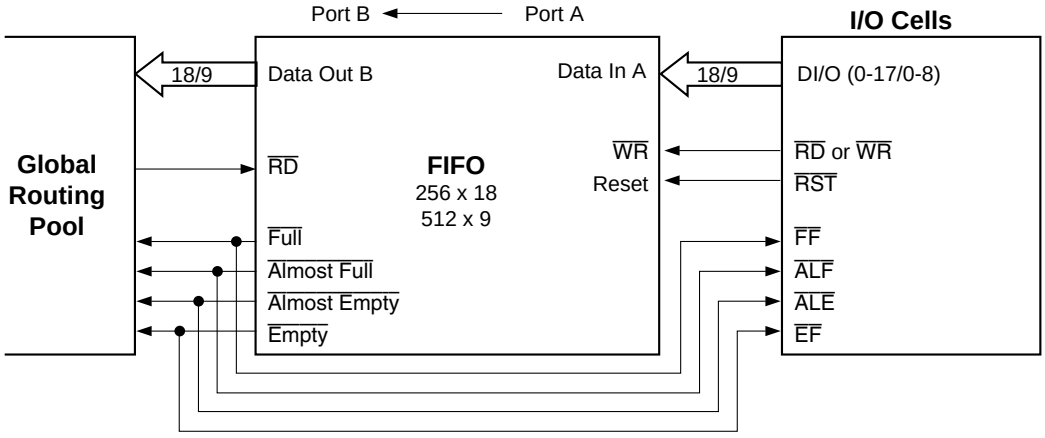
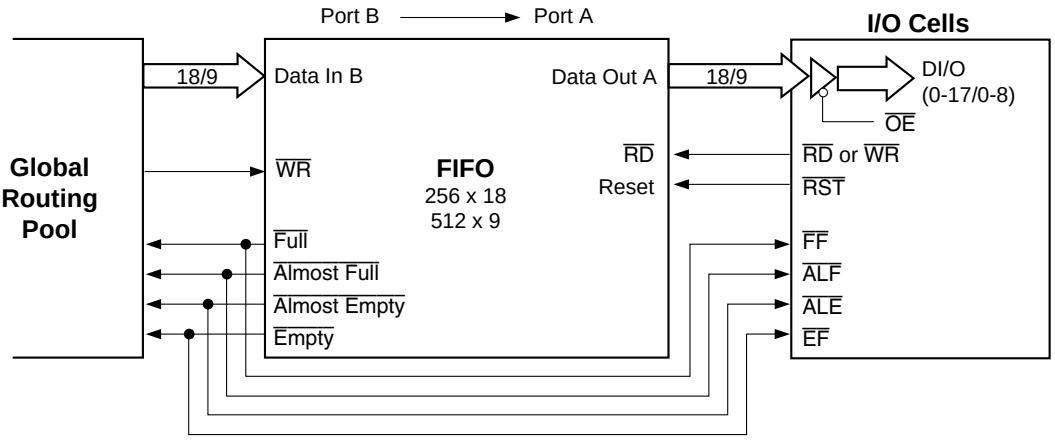


Figure 18. Port B to A Configuration



Dual Port RAM Module Description (6192DM)

A dual port static RAM constitutes the memory module in the ispLSI and pLSI 6192DM devices. The dual port RAM is organized as a 512 x 9 memory module with a parity bit added to each byte of data. The memory module can be accessed for read or write concurrently via two separate ports as long as both ports do not access the same memory location at the same time.

Figure 19 illustrates the functionality of the Dual Port RAM. It can be sub-divided into 3 parts: Memory Array, Address Decoders and the Control and Arbitration Logic.

The 18-bit data bus is bidirectional and can be used to read data from the memory array or write data to the memory array. A byte read/write operation involves 8-bits of data and a parity bit. 8 address bits (ADDR 0-7) are used to access a particular word location in memory array. RWH is associated with the higher 9 data bits and RWL is used for lower 9 data bits. There are 2 RWH and 2 RWL lines, one pair for each port. These are inputs to the Control logic to select the type of operation to be performed. Depending on the configuration. It can be a word read/write operation, or byte read and/or write operation. $\overline{CS}$ is the Chip Select line. There is a separate $\overline{CS}$ for each port. The $\overline{CS}$ line has to be active in order to perform a read/write operation on the memory module.

All the input signals, control as well as the data lines, are user selectable to be active high or low. The Dual Port RAM has a default configuration of active low for the $\overline{CS}$.

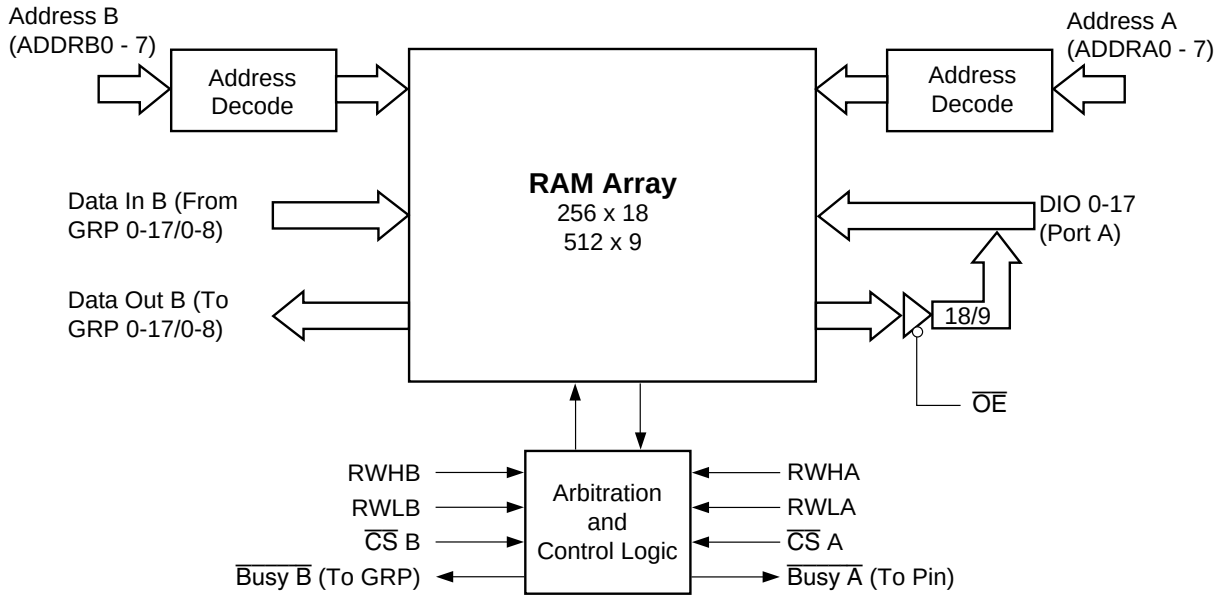
When not used for memory interfacing, the DIO 0-8 (RAM) and A3-A7 pins may be used for general-purpose logic inputs into the GRP.

The Dual Port RAM is user configurable and can be configured as any of the following:

Description	Ports Used
256 x 18 Dual Port RAM	A & B
256 x 18 Dual Port RAM w/Byte Write (9 Bit Write)	A & B
512 x 9 Dual Port RAM	A & B

Port A interfaces with the external world through DIO pins and Port B is internal to the device via the GRP.

Figure 19. Dual Port RAM Functional Block Diagram



Dual Port RAM Configurations

256 x 18 Dual Port RAM

Figure 20 below shows the 256 x 18 and 512 x 9 configurations of the Dual Port RAM. ADDRA 0-7 form the 8-bit address bus used to access one of the 256 locations from Port A which is connected to the external pins. ADDRB 0-7 form the 8-bit address bus used to access one of the 256 locations from Port B which is connected to the GRP. RWLA is the control line which determines the type of operation to be performed with the 18-bit data bus from the DIO pins. A high RWLA signal reads 18-bits of data from the memory location pointed to by the address bus. A low RWLA signal writes 18-bits of data to the location pointed by the address bus. The $\overline{CSA}$ line has to be low to have port A respond to a read/write operation. In this configuration, RWHA and RWHB are not used.

The same operations on the B Port are controlled by RWLB and $\overline{CSB}$. For this port, control signals and data interface with the GRP.

256 x 18 Dual Port RAM w/Byte (9-bit) Write

In this mode, RWL is the control line which determines the type of operation to be performed on the lower 9 bits of the memory location. RWH is the control line used to select the type of operation to be performed on the higher 9 bits of the memory location. All other operating characteristics are similar to the previous mode.

This mode is an ideal way to pack 9-bit data into 18-bit memory by simply alternating the RWL and RWH states. This mode can also be used to perform bus width conversion whereby one port operates at 9-bits and the second port operates at 18-bits

512 x 9 Dual Port RAM

This mode uses 9 address bits to select one of 512 locations. ADDRA 0-7 form the 8 address bits and RWH is used as the 9th address bit (MSB). In this configuration, the high order bits (bits 9-17) of the 18-bit data bus are used to transfer data to the RAM. RWL is the control line used to select the type of operation to be performed on the specified memory location.

Arbitration

The two ports may act like independent RAMs, however the arbitration and control logic as well as the Memory core are shared by both ports as shown previously. When the $\overline{CS}$ is inactive the RAM will ignore any operation, read or write on that port.

The dual port RAM can be written to or read from asynchronously and simultaneously by each port at the same time (except for the same address). If the same address location is accessed by both ports, the arbitration logic evaluates which port will win out. The port that wins will have a logic 1 or a busy inactive on its Busy Flag. Busy will go low for the port that loses. If the address is the same for both ports and there is >5ns between the port accesses, the Busy signal is activated and which port has to wait is determined on a first-come, first-served basis.

When the addresses on Port A and B are the same and the $\overline{CSA}$ and $\overline{CSB}$ both go low within 5ns of each other or if $\overline{CSA}$ and $\overline{CSB}$ are both low and the address for both ports change to the same location within 5ns, the arbitration is unpredictable: either port may win.

Figure 20. Dual Port RAM Configurations

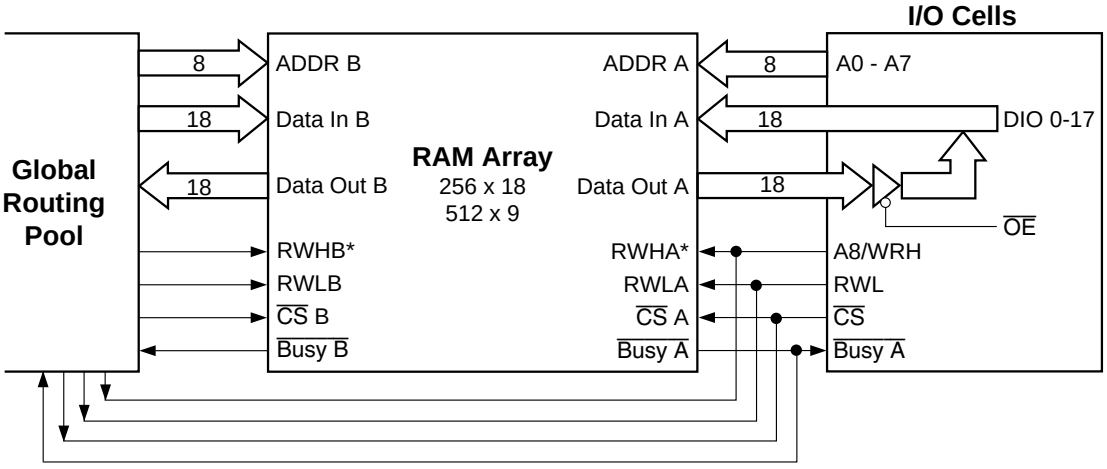


Figure 21. Dual Port RAM with $\overline{\text{Busy}}$ Timing Diagram

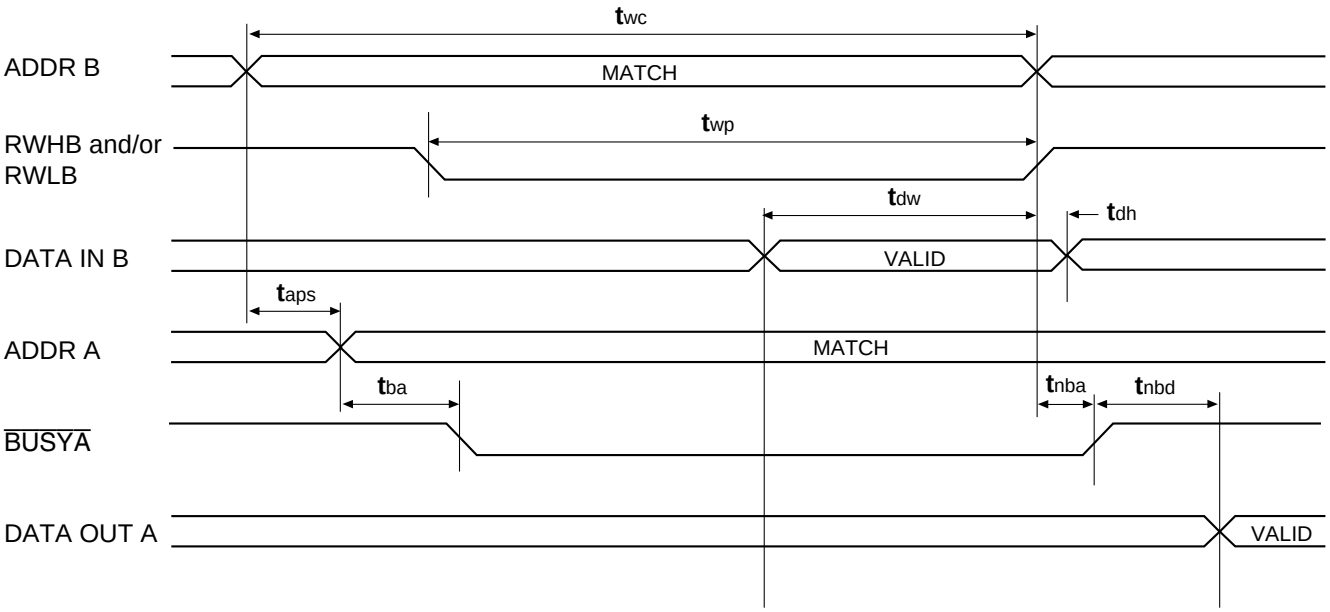


Figure 22. Dual Port RAM Contention Cycle ($\overline{\text{CS}}$ Arbitration) Timing Diagram

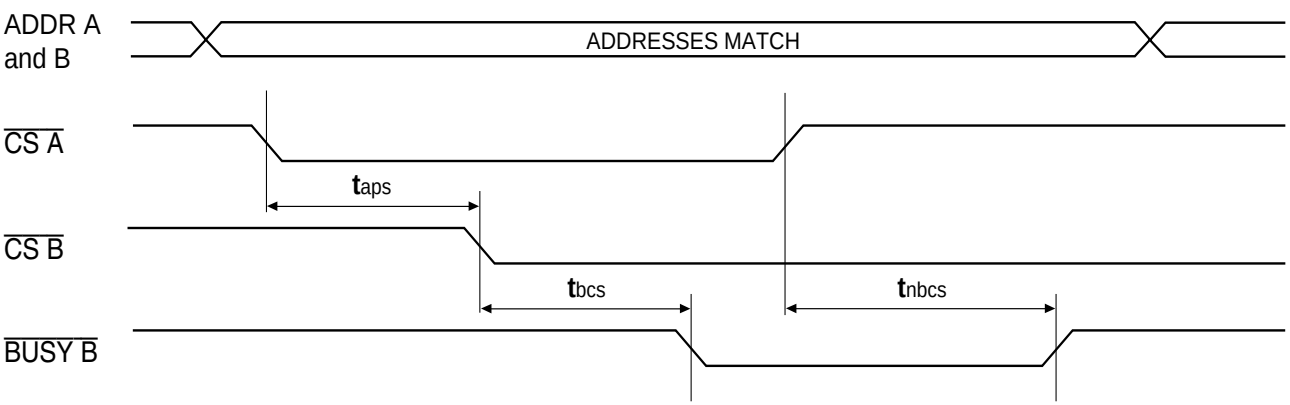


Figure 23. Dual Port RAM Contention Cycle (Address Valid Arbitration) Timing Diagram

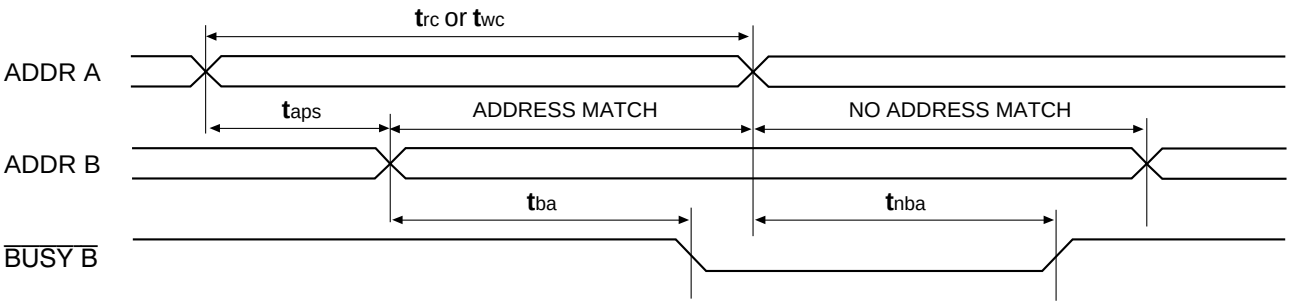


Figure 24. Dual Port RAM Write Cycle (RW Controlled) Timing Diagram

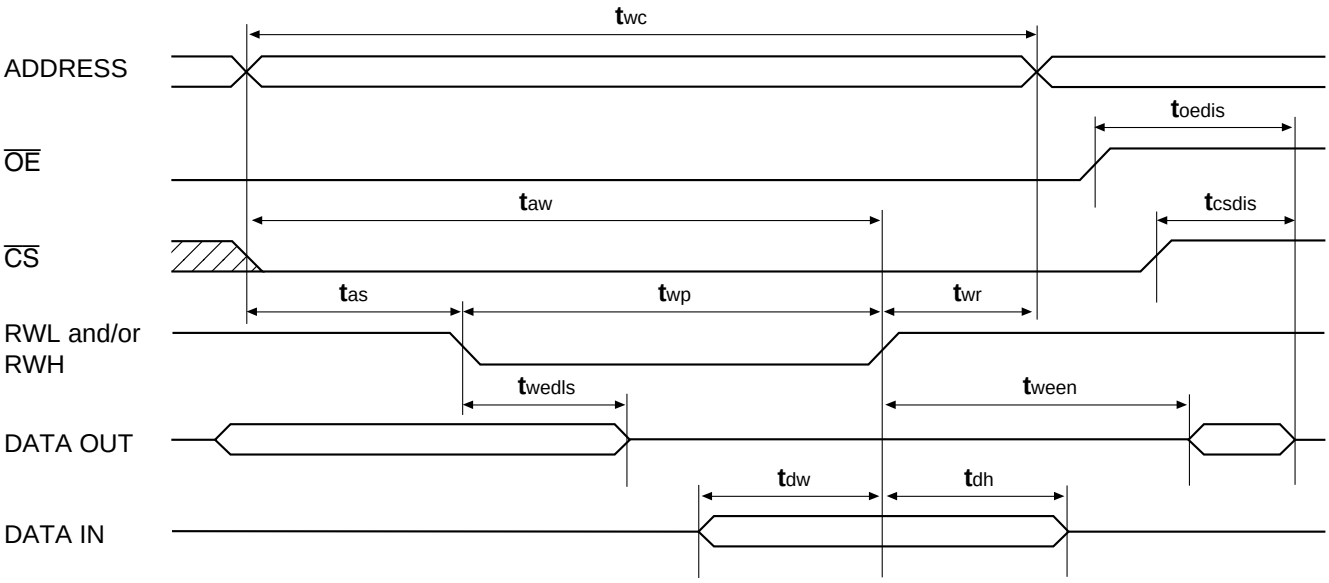
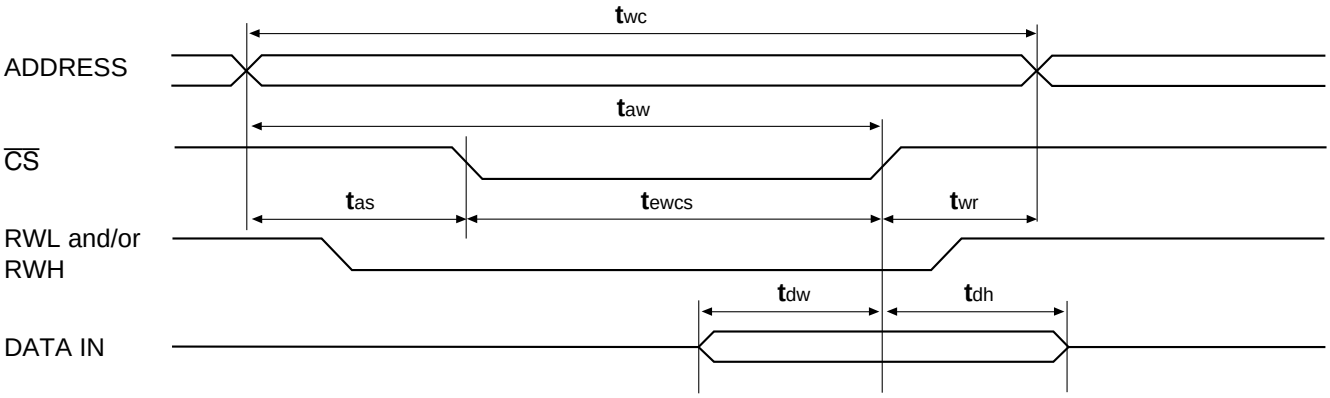


Figure 25. Dual Port RAM Write Cycle ($\overline{CS}$ Controlled) Timing Diagram



Single Port RAM Description (6192SM)

Single port Static RAM constitutes the memory module in the 6192SM device. As a single-port memory, only one port is used to access the memory for data reads and writes. The 6192SM can be configured to operate either as one large single-port memory or as two smaller single-port memories.

When used as a large single-port RAM, the memory can be organized as 256 x 18 or 512 x 9. Either Port A or Port B can be used to control the single-port RAM as shown in Figure 26. A byte read/write mode similar to that of the dual-port RAM is also provided to allow independent control of the upper and lower 9-bit banks of the memory.

When used as two independent smaller single-port memories, each memory can be organized as 128 x 18 or 256 x 9. The two memories, however, must have identical configurations. Port A, therefore controls one single-port memory and Port B controls the other single-port memory as shown in Figure 27. Both memories can operate simultaneously and independently. Byte read/write mode also applies to the dual single-port RAM configuration.

When not used for memory interfacing, the DIO0-8 (RAM) and A3-A7 pins may be used for general purpose inputs into the GRP.

The RAM is user configurable and can be configured as:

Description	Single Memory Port Used	Dual Memory Ports Used
128 x 18 Single Port RAM	—	A and B
128 x 18 Single Port RAM w/Byte Write (9 Bit Write)	—	A and B
256 x 9 Single Port RAM	—	A and B
256 x 18 Single Port RAM	A or B	—
256 x 18 Single Port RAM w/Byte Write (9 Bit Write)	A or B	—
512 x 9 Single Port RAM	A or B	—

Figure 26. Single Port RAM Functional Block Diagram (Single RAM Block)

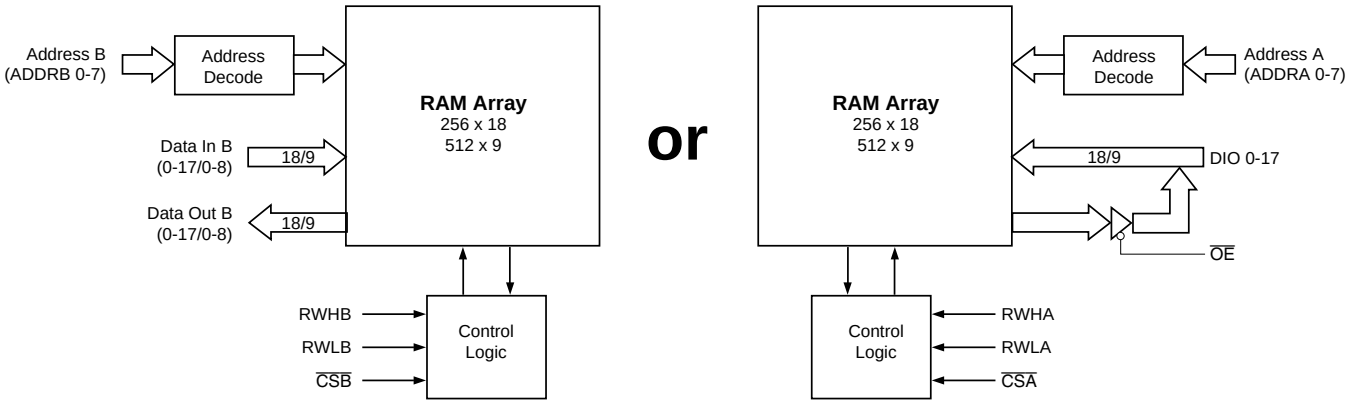
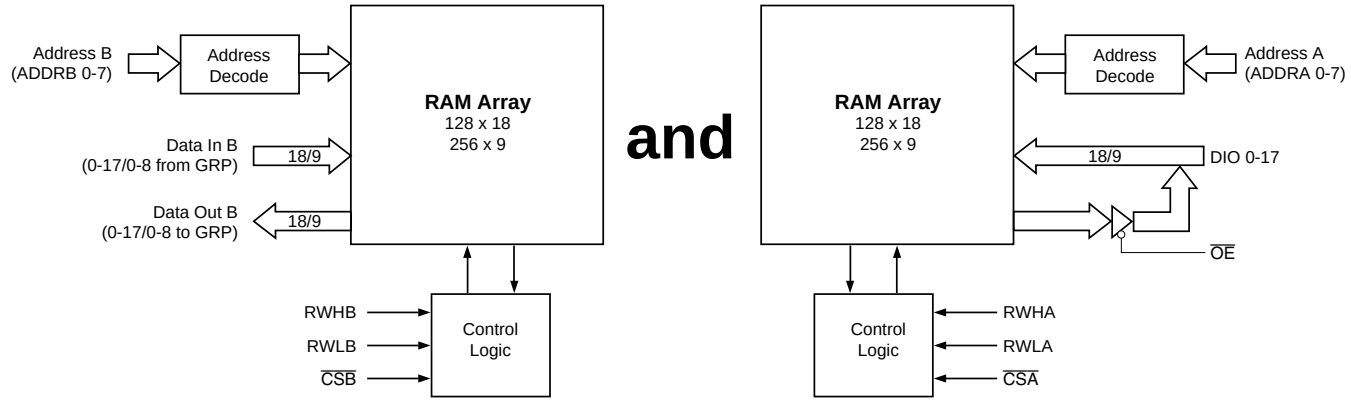


Figure 27. Single Port RAM Functional Block Diagram (Dual RAM Blocks)



Port A interfaces with the external world through the dedicated I/O pins and Port B is internal to the device, through the GRP.

Single Port RAM Configurations

256 x 18 Single Port RAM (Port A or B)

Figure 28 shows the port A configuration of the Single Port RAM. A0-7 form the 8-bit address bus used to select one of the 256 locations. RWLA is the control line which determines the type of operation to be performed with the 18-bit data bus. A high RWLA signal reads out 18-bits of data from the location pointed to by the address bus. A low RWLA signal writes in 18-bits of data to the location pointed to by the address bus. The $\overline{CS}$ line has to be low (active-low) to have the RAM respond to a read/write operation. As shown below, the control lines can come from the I/O cells and/or from the GRP, as defined by the software.

When in port B configuration (figure 29), the GRP drives the address bus, data bus and the various control lines.

256 x 18 Single Port RAM w/Byte (9-bit) Write (Port A or B)

In this mode, RWL is the control line which determines the type of operation to be performed on the lower 9 bits of the memory location using the lower 9-bits of the 18-bit data bus. Similarly, RWH is the control line to select the type of operation to be performed using the higher 9 bits of the memory location with the higher 9 bits of the 18-bit data bus. All other operating characteristics are similar to the previous mode.

512 x 9 Single Port RAM (Port A or B)

This mode uses 9 address bits to select one of the 512 locations. A0-A7 form the 8 address bits and RWH is used as the 9th address bit (MSB). In this configuration, the higher 9 bits of the 18-bit data bus are used to transfer data. RWL is the control line used to select the type of operation to be performed on the specified memory location.

The 6192SM can also be configured as two separate smaller single port RAMs with Port A controlling one and Port B controlling the other. Both RAMs can operate simultaneously. Each smaller memory operates exactly the same way as the larger memory except for the address bit A7.

Dual 128 x 18 Single Port RAM (Port A and B)

This mode uses A0-A6 address bits to select one of the 128 locations. A7 is not used in this mode. RWLA and $\overline{CSA}$ control the operations for Port A. RWLB and $\overline{CSB}$ determine the operations for Port B.

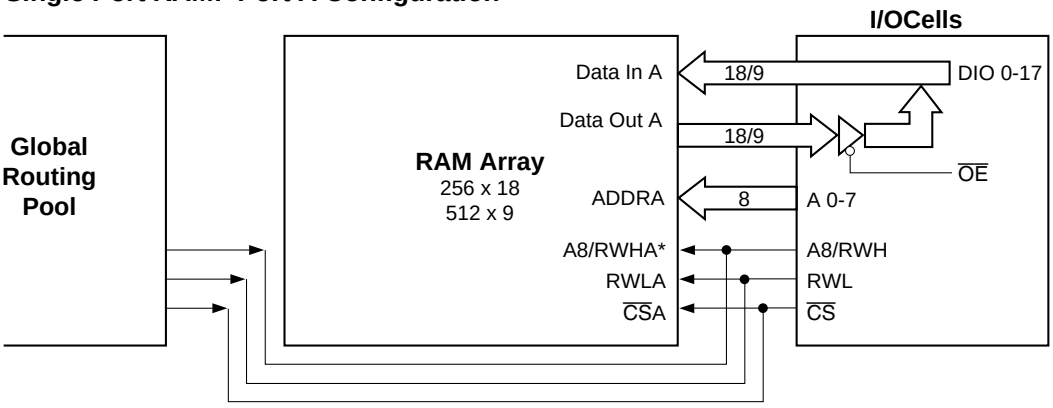
Dual 128 x 18 Single Port RAM with Byte Write (Port A and B)

RWLA and RWLB control the read/write operations for the lower order 9 bits of their respective memories. RWHA and RWHB control the operation for the higher order 9 bits.

Dual 256 x 9 Single Port RAM (Port A and B)

A7 is used as the most significant address bit required to access the 256 locations in the memory. The higher order 9 bits of the 18-bit bus are used to transfer data. RWL is the control line used to select the type of operation to be performed.

Figure 28. Single Port RAM: Port A Configuration



Note (*)
1. In 256 x 18 Single Port RAM configuration, A8/RWH is left unconnected.
2. In 256 x 18 Single Port RAM configuration with Byte Write configuration, A8/RWH acts as a control line to select the type of operation to be performed with the high 9 bits of the 18 bit data bus.
3. In 512 x 9 Single Port RAM configuration, A8/RWH is used as the most significant Address bit

Figure 29. Single Port RAM: Port B Configuration

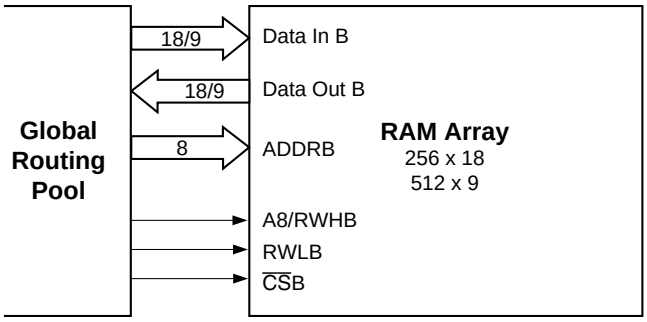


Figure 30. Single Port RAM Read Cycle Timing Diagram

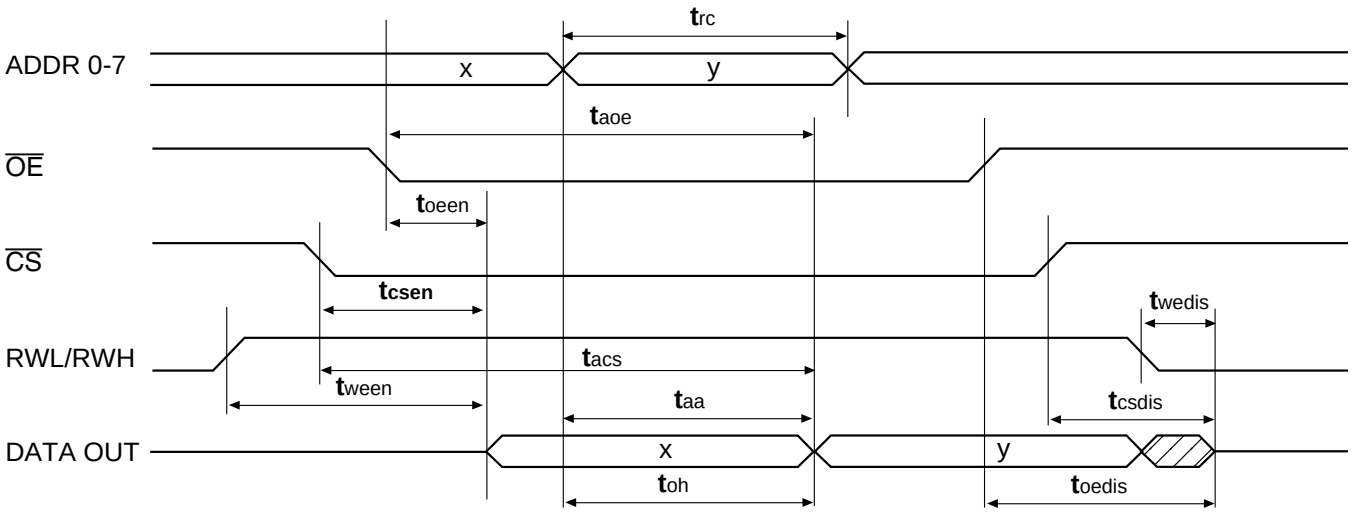
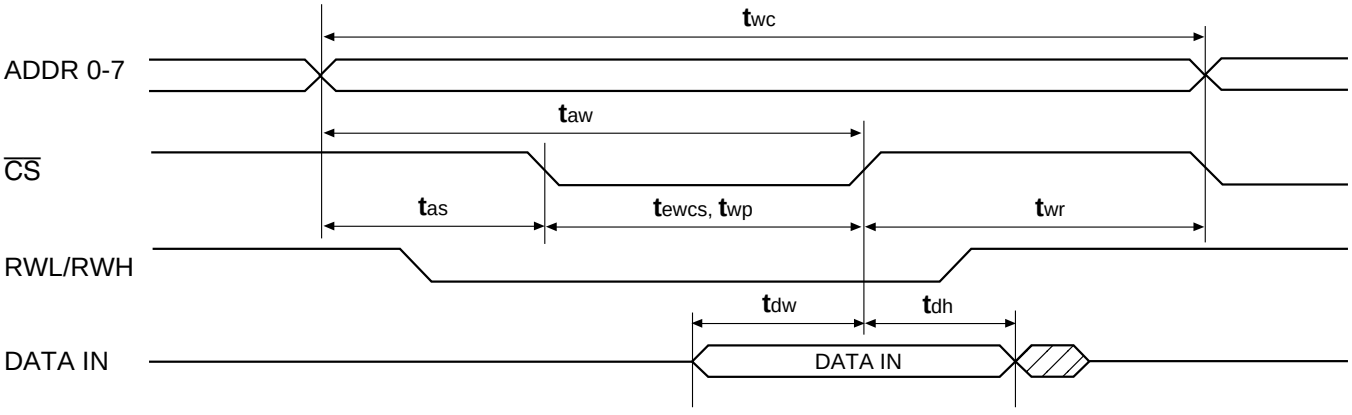


Figure 31. Single Port RAM Write Cycle ($\overline{CS}$ Controlled) Timing Diagram



Register/Counter Module Description

The Register/Counter module consists of a group of eight 16-bit Banks with control and data interfaces to both the GRP and a dedicated group of device pins. The Register File/Counter has a 16-bit bidirectional parallel data interface, Serial Data In (SIN), Serial Data Out (SOUT), and Output Enable ($\overline{OE}$) pins along with four Carry Out (COUT) pins that correspond to the counter/timer functions described below. The Banks in the Register/Counter Module can be configured by the user to implement:

- •Registers
- •Counters
- •Timers (Modulo Counter)
- •Shift Registers

In addition, Banks can be cascaded to form larger functions; for example, eight Banks can be cascaded in the Parallel-to-Serial mode to form a 128-bit parallel-to-serial shift register.

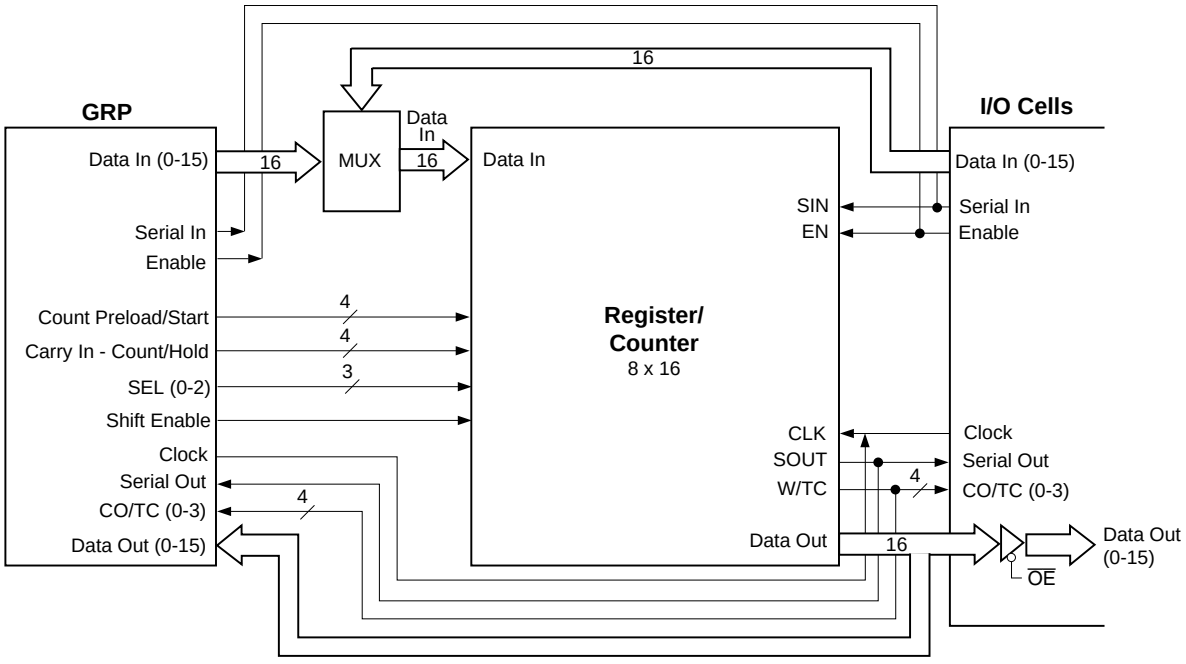
The pDS design software allows the designer to choose one of nine predefined configurations or Modes for the Register/Counter module. Depending on the Mode chosen (discussed later), the Data Interfaces to the module can be configured as:

- •Parallel to Parallel
- •Serial to Parallel
- •Parallel to Serial
- •Serial to Serial

The Banks are addressed independently for read and write operations by using the three Select (SEL0-2) lines. These signals are driven from the 6192 GRP. All eight banks can be configured as register files, but only four of them (Banks 1,3,5,7) can be configured as 16 bit loadable up/down counters or as 16 bit loadable up/down Modulo counters. Each counter/timer Bank can be individually configured by the user. The up/down mode and 8 or 16 bit operation of the counter/timer are configured when the device is programmed based upon the user's design inputs. All the eight word banks can be configured as shift registers.

Select Inputs			Bank Selected
SEL 2	SEL 1	SEL 0	Bank #
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Figure 32. Register/Counter Module Connectivity



When the dedicated Register/Counter I/O pins (DIO 0-15) are not used for the Register/Countert module, they can be used as input-only pins for the general-purpose programmable logic block. In this mode, the data pins of the unused module feed directly into the device's Global Routing Pool (GRP).

The data inputs, data outputs and the control signals for the Register/Counter Module can be either active high or active low. Other control signals (SEN, SEL0-2, etc.) come only from the GRP. Data inputs and SIN and Enable control signals can come from I/O cells or the GRP. Data output signals can go to I/O and the GRP to be used in other logic.

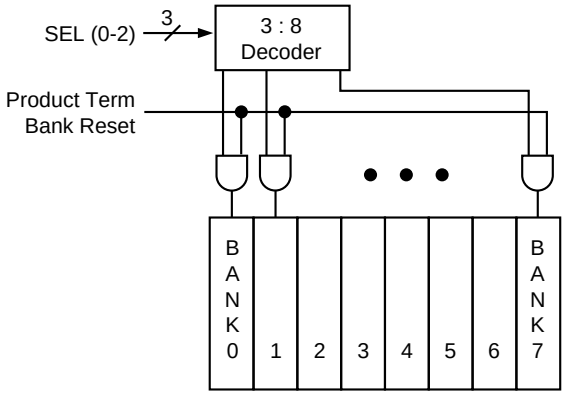
Each Bank can use a unique Clock configuration. The Clock is selectable from either one of the three GLB clocks, the I/O clock 0 (Y4) or a product term clock (PTCK). The user has the ability to select the true or complement of the selected clock.

There are two Reset functions within the Register/Counter Module, the Global Reset and PT Bank Reset. The Global Reset resets all the registers in programmable logic module and register/counter module. The Global Reset is active low. The Product Term (PT) Bank Reset, in conjunction with the Select lines, is used to individually reset the banks. The PT Bank Reset is active high.

The Register/Counter Module I/O pins (DIO 0-15 (RC))can be controlled by either the Global Output Enable (GOE) or the Module Output Enable ($\overline{OE}$) through a user-programmable option. The user has the choice of selecting either of these signals on an I/O by I/O basis. The OE can also be selected to be active high or low on an I/O by I/O basis.

Register/Counter Module Configuration

Figure 33. Product Term Bank Reset



Options

There are nine pre-defined Register/Counter configurations or modes which are supported by Lattice Semiconductor's pDS software. These are:

1. 8-Bank Register File
2. 8-Bank Parallel to Serial Shift Register
3. 8-Bank Serial to Parallel Shift Register
4. 8-Bank Serial to Serial Shift Register
5. 4-Bank Parallel Load Up/Down Counter with 4-Bank Register File
6. 4-Bank Adjacent Load Up/Down Counter with 4-Bank Adjacent Register File
7. 4-Bank Parallel Load Up/Down Timer with 4-Bank Register File
8. 4-Bank Adjacent Load Up/Down Timer with 4-Bank Adjacent Register File
9. 4-Bank Custom Preset Load Up/Down Timer with 4-Bank Register File

In the above modes, counters and timers can be loaded either 8 or 16 bits at a time.

The following sections will discuss each of these operating modes in detail.

Configuration #1: 8-Bank Register File

The register file is organized as eight words of 16 bits each. Sixteen data inputs are available to supply the data to be stored. The Select lines permit direct access to read or write the data to any of these words. In order to write data to a location in the file, the SEL0-2 lines must point to the correct location and the Enable input must go active. The write operation is synchronous to the clock. Data must be stable at the Register/Counter module inputs a minimum set-up time (tensu) prior to Enable going inactive and Low to High transition on the Clock for it to be correctly written into the file. Data from the location pointed to by SEL0-2 is always presented at the multiplexer outputs (Data Out 0-15). However, to insure the data is valid, the read operation should be done when the Enable is inactive or after the falling edge of the clock.

For example, if the Select line Address is 011(binary) and the Enable signal is low, the data is clocked into the Bank 3.

Figure 34. Register/Counter Option #1: 8-Bank Register File

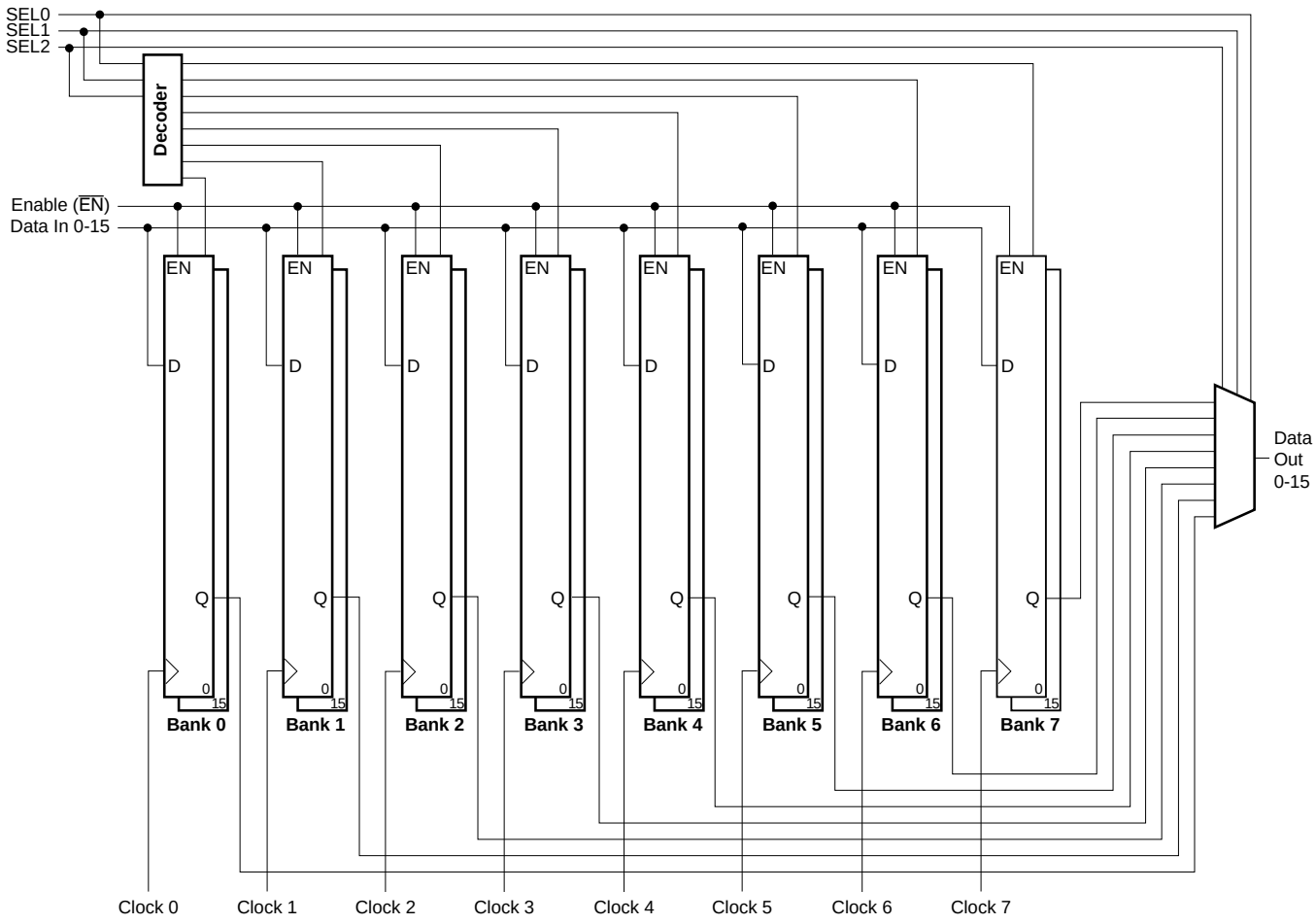
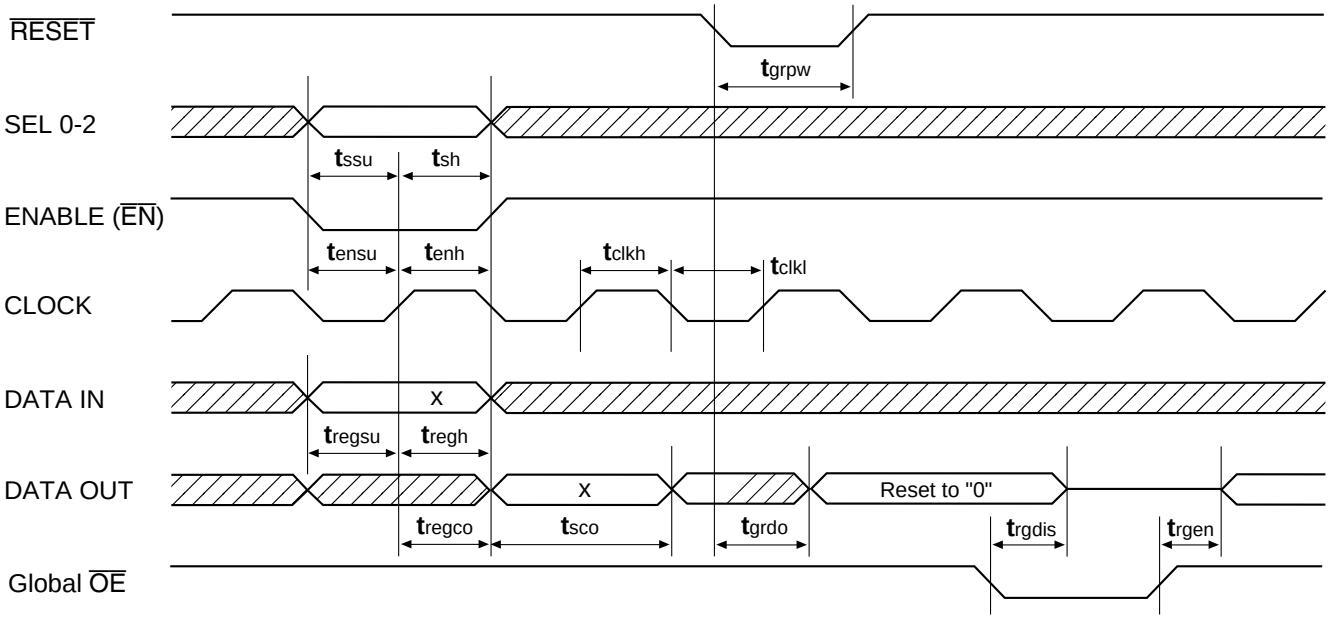


Figure 35. Register Parallel Read/Write Timing Diagram



Configuration #2: 8-Bank Parallel to Serial Shift Register

This configuration is used to convert data from a parallel to serial format. In this mode, each bank functions as a 16-bit shift register with all 8 Bank s serially cascaded from Bank 0 to Bank 7 to form a 128-bit shift register chain. Here, the parallel data write operation is the same as with the Register File configuration. As previously discussed, the Enable line must be low for the Write operation to be performed. Depending on the parallel load operation, the chain can be used as a 1-bit to 128-bit shift register. Data is read out of the Serial Out (SOUT) pin (connected to the LSB of Bank 7) serially on each Clock transition when the Shift Enable ($\overline{SEN}$) is Low.

Figure 36. Register/Counter Option #2: 8-Bank Parallel to Serial Shift Register

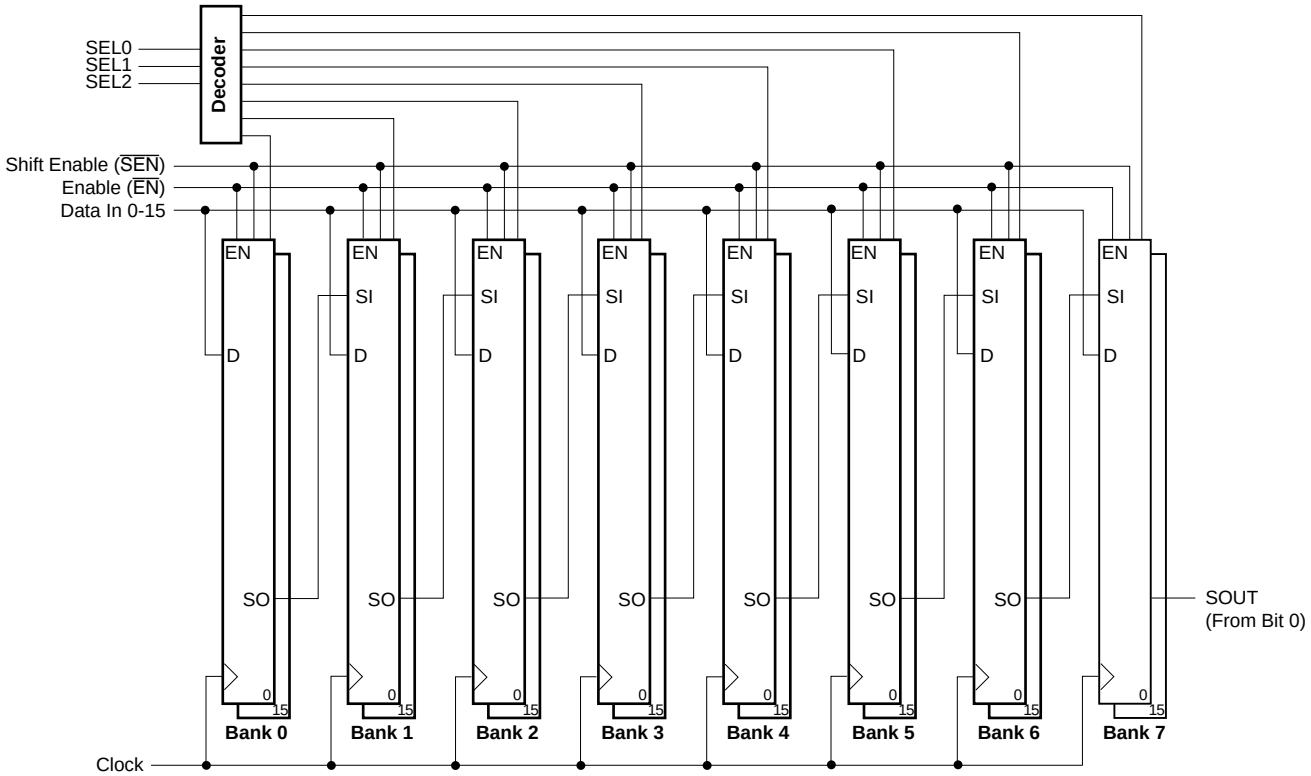


Figure 37. Shift Register Parallel Load/Shift Timing Diagram

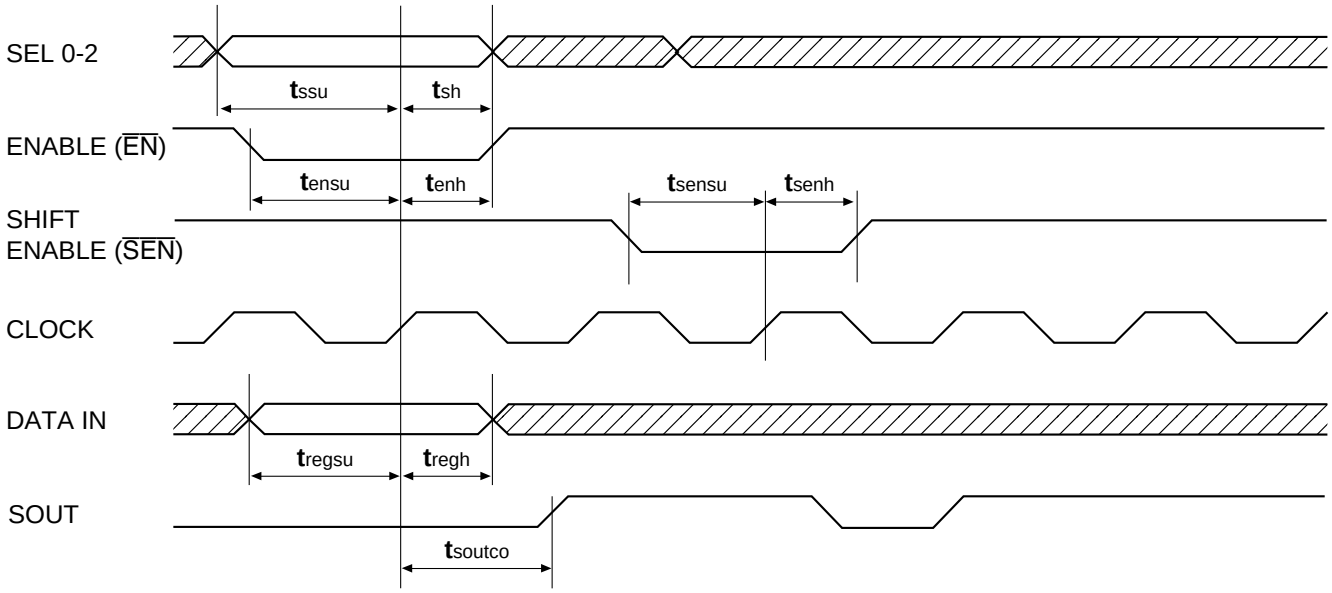
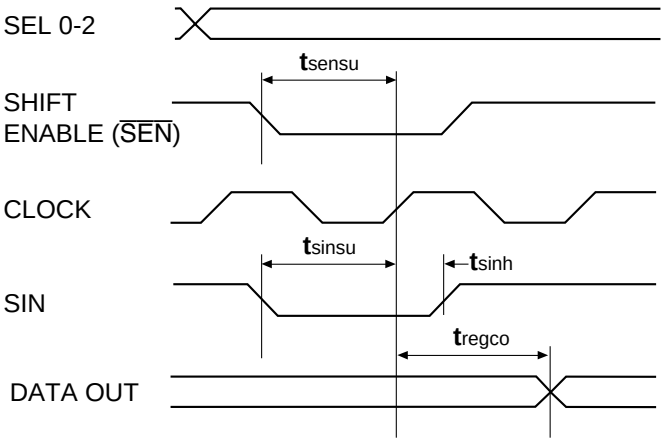


Figure 38. Shift Register Serial Load/Shift Timing Diagram



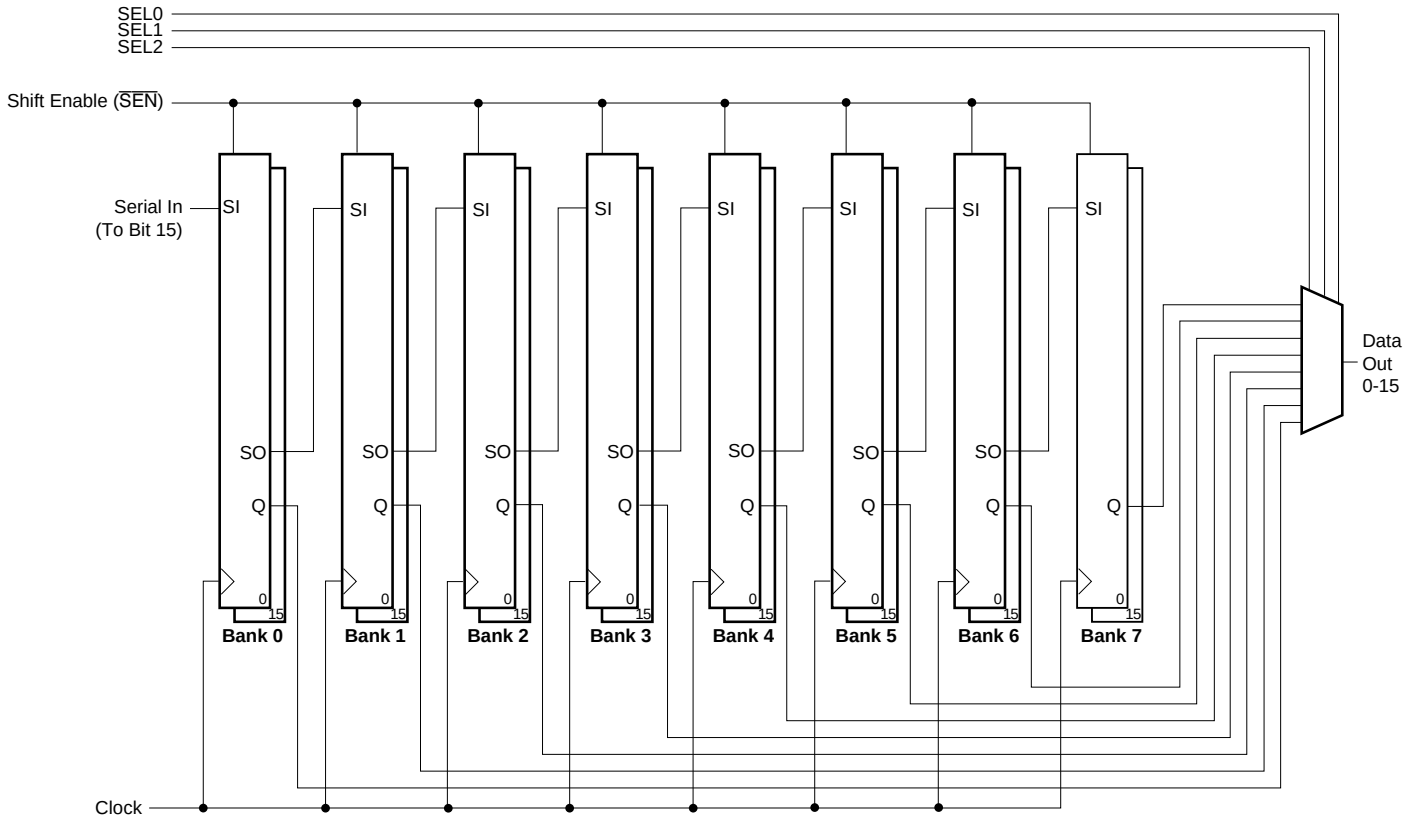
Configuration #3: 8-Bank Serial to Parallel Shift Register

This configuration is used to convert the data presented on the SIN input from serial to parallel format. All 8 banks are cascaded together. The serial out line(LSB) of one bank is automatically connected to the next bank's serial in line (MSB) and so on to form a 128-bit shift register. Depending on the use of SEL0-2, the shift register chain can be used as a 1-bit to 128-bit shift register.

The serial write operation takes place when Shift Enable ($\overline{SEN}$) is Low. The serial data is clocked into Bank 0 (see figure 38).

The Read operation is same as Parallel-to-Parallel configuration. Here also, the read operation should be performed when the Enable is inactive or after the falling edge of the clock.

Figure 39. Register/Counter Option #3: 8-Bank Serial to Parallel Shift Register

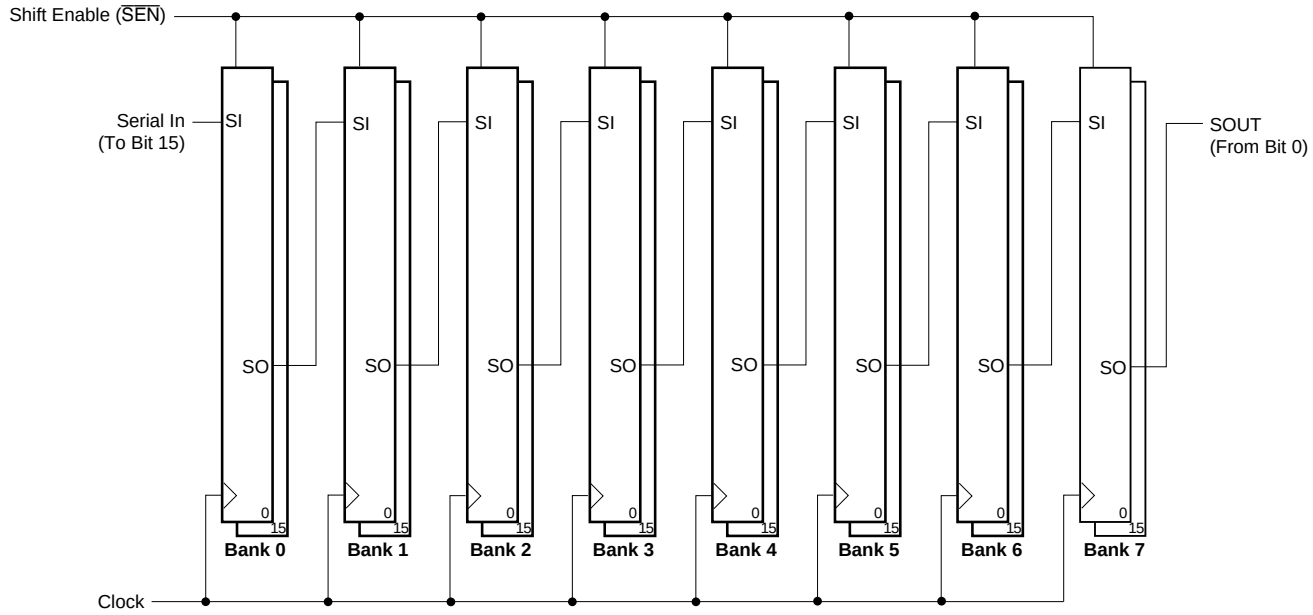


Configuration #4: 8-Bank Serial to Serial Shift Register

This configuration is used to shift data in and serially shift data out. The bank are cascaded together to form a 128 bit shift register. The data flow is from the Most Significant Bit (MSB) to the Least Significant Bit of each bank. The LSB of Bank 0 is connected to the (MSB) of Bank 1 and so on. The Serial Data In (SIN) is on Bank 0 and the Serial data out (SOUT) is on Bank 7.

Both the read and write operations are serial in this mode of operation in this configuration. The Shift Enable signal controls the Shift or Hold activity of the data. When the Shift Enable is low, the banks will begin shifting data (MSB to LSB) synchronously. When the signal is High, the banks retain the last data without shifting.

Figure 40. Register/Counter Option #4: 8-Bank Serial to Serial Shift Register



Configuration #5: 4 Bank Parallel Load Up/Down Counter with 4-Bank Register File

Four of the eight banks can be configured as 8- or 16-bit loadable, up or down counters. These word banks are Bank 1, Bank 3, Bank 5 and Bank 7. The counters are addressed for read and write operations in the same manner as the Register File by using SEL (0-2) and Enable. The counters are parallel loaded from the Data In (DIN) lines and are read out to the Data Out (DOUT) lines. The 8 or 16 bit data is loaded into the counter bank selected by the select lines. Whether 8 or 16 bit data is transferred is determined by the operating mode defined for the specific counter when the device is programmed. Load (Write) occurs when Enable (EN) signal is low and a there is a low-to-high clock edge.

Each counter has independent Carry In-Count/Hold (CICH) and Carry Out (COUT) lines, which allow the designer to have independent control of each counter, thus giving more flexibility in his design. These lines can have several alternative uses. The Carry In and Carry Out lines can be used to cascade counters to form very large counters, up to 64 bits. The Carry In can also be used as a Count/Hold control: when the signal is High, the counter will count. When low, it will hold the counter at the present count. The Carry Out line can also be used to tell when the counter has reached its maximum or terminal count (TC).

The count operation will only take place when the Carry In-Count/hold is high and there is a low-to-high clock edge. When the counters reach FFFFH during counting up or 0000H when counting down, their contents "roll-over" on the next clock pulse to 0000H and FFFFH respectively, and counting continues, assuming Carry-In is active (see figure 42).

In Mode #5, 4 Banks (1,3,5,7) are configured as counters which operate as described immediately above, and 4 Banks (0,2,4,6) operate as Register files as described in Mode #1 above.

Figure 41. Register/Counter Option #5: 4 Bank Parallel Load Up/Down Counter with 4 Bank Register File

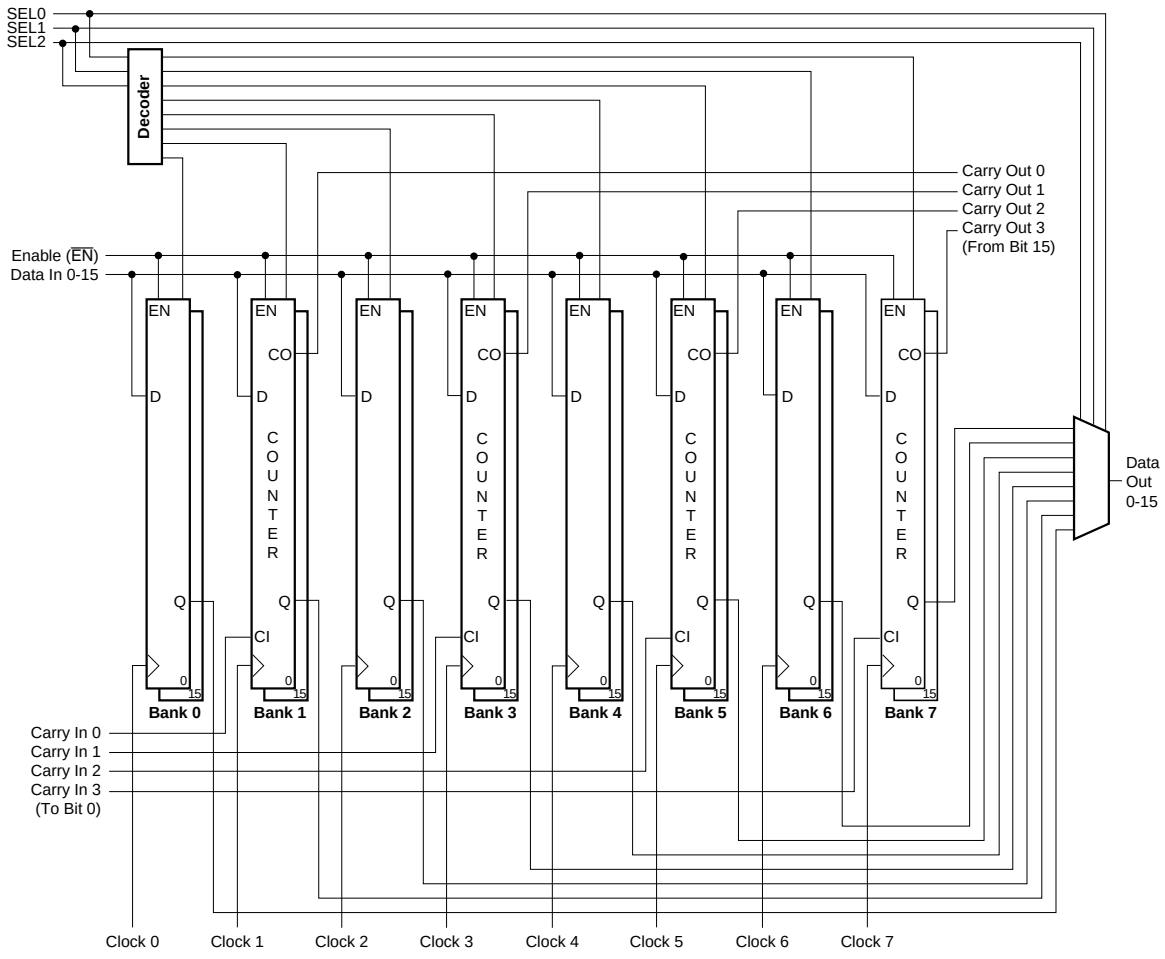
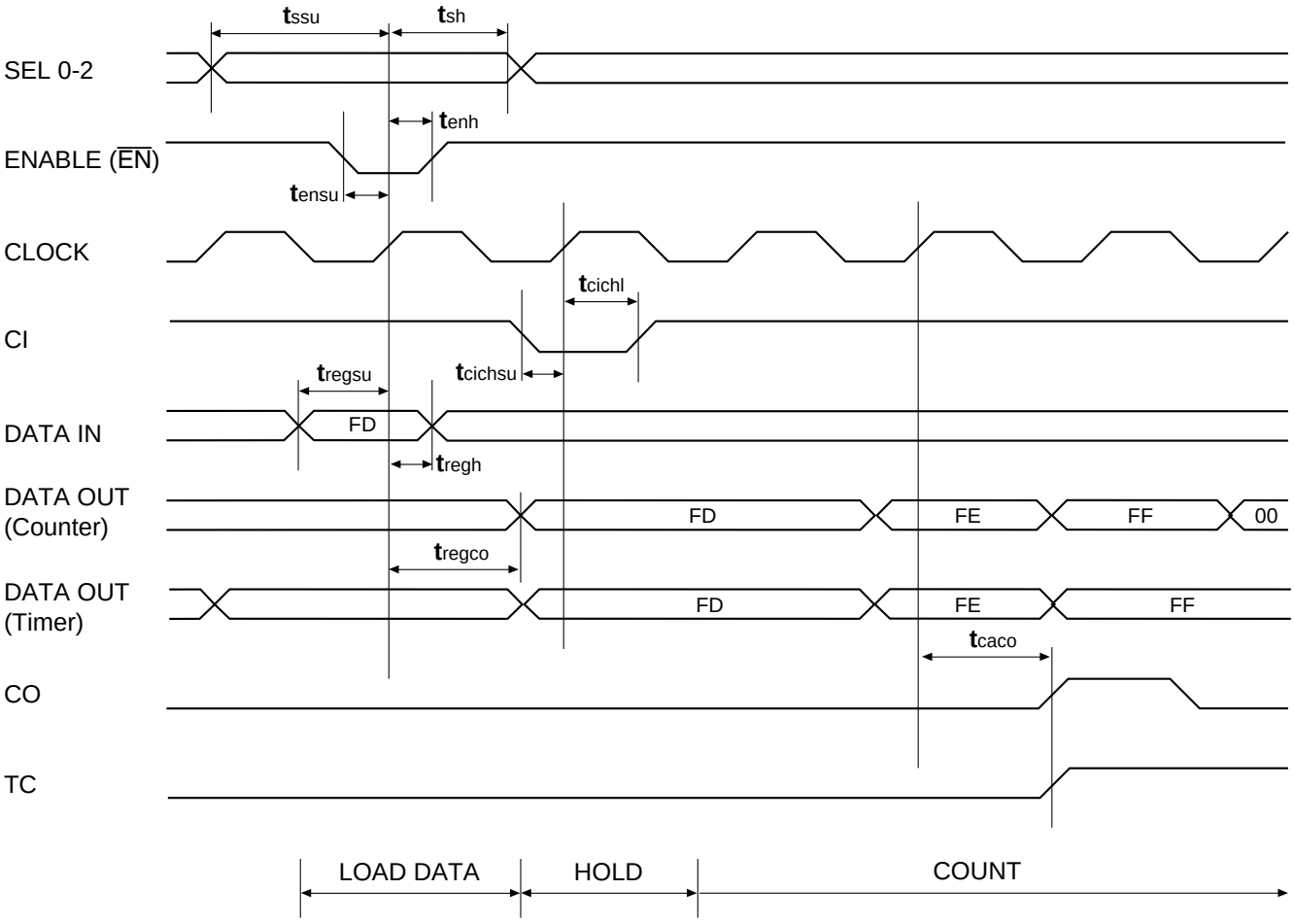


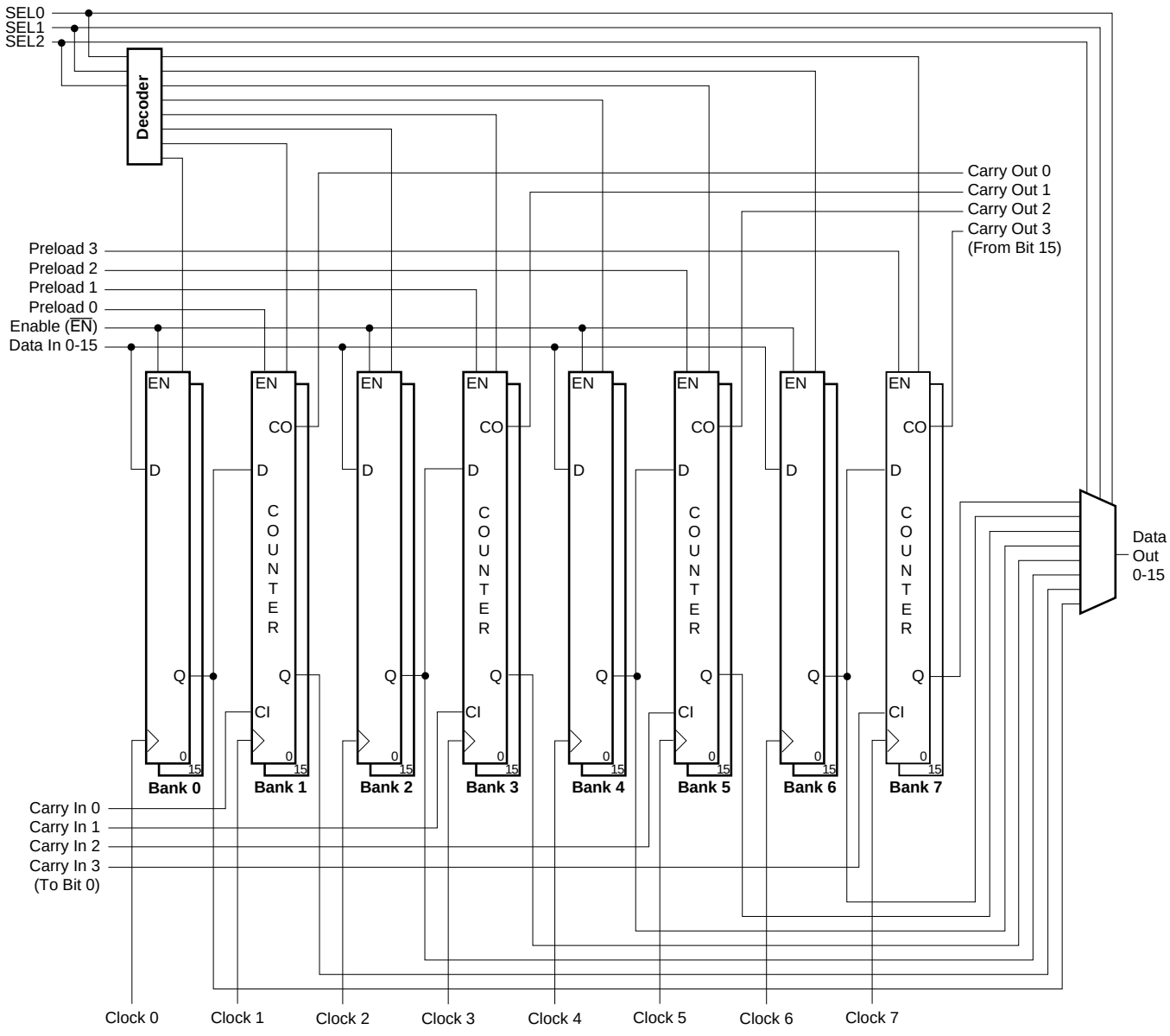
Figure 42. Counter/Timer Timing Diagram



Configuration #6: 4 Bank Adjacent Load Up/Down Counter with 4 Bank Adjacent Register File

In this mode, the counters function as described in Mode #5 above. However, rather than being parallel loaded from the Data In lines when Enable is low, the counters are loaded from the adjacent registers during a load. Banks 0, 2, 4, 6 are used to hold the preload data for counter Banks 1, 3, 5, and 7, respectively. The preload data is loaded into the selected register file bank in the usual manner when a clock occurs and the Enable is low. Data is loaded into the adjacent counter when th corresponding Preload is low and there is a rising clock edge.

Figure 43. Register/Counter Option #6: 4 Bank Adjacent Load Up/Down Counter with 4 Bank Adjacent Register File



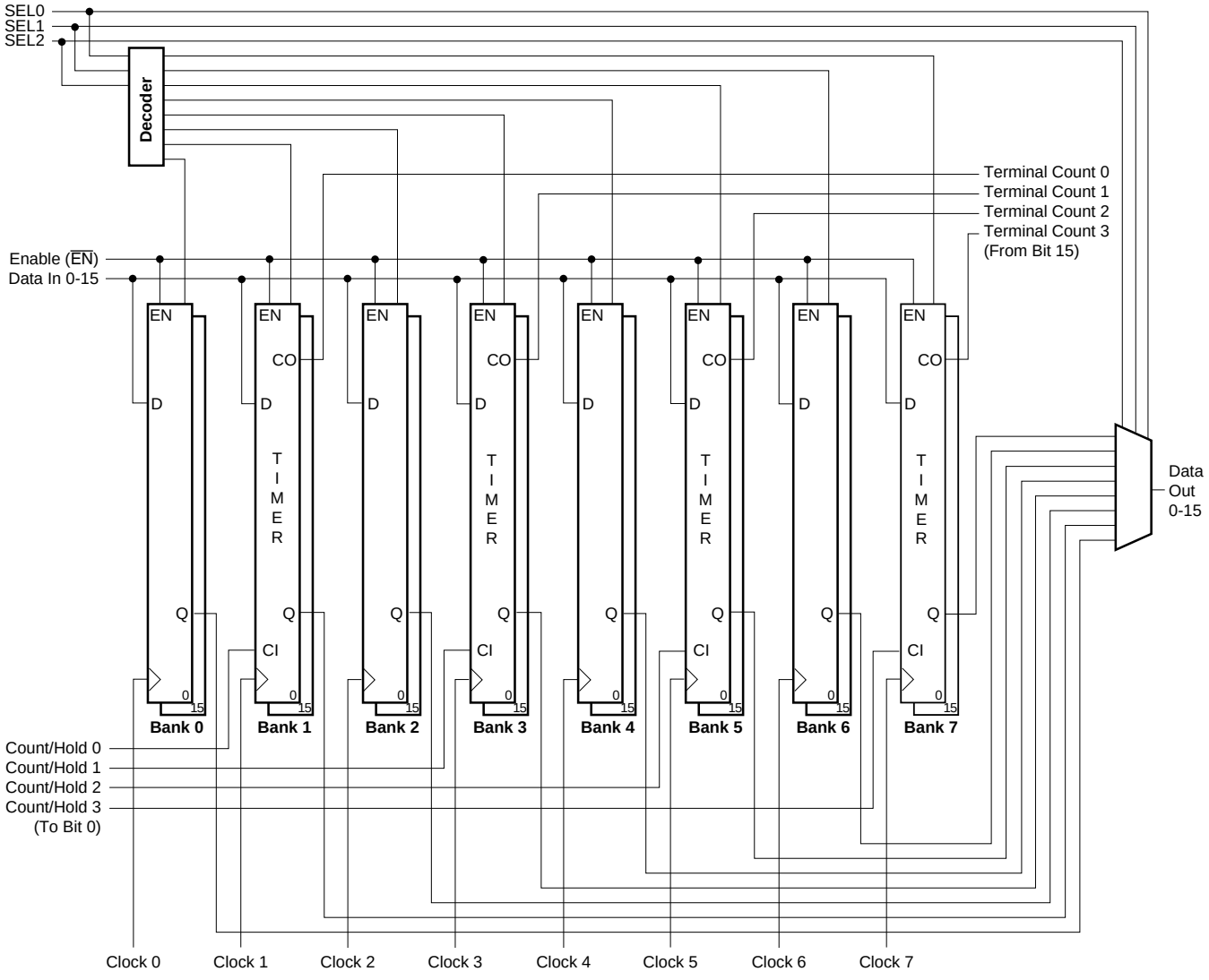
Configuration #7: 4 Bank Parallel Load Up/Down Timer with 4 Bank Register File

Four of the eight banks in the Register/Counter module can be configured as 8- or 16-bit loadable, up or down timers. These word banks are Bank 1, Bank 3, Bank 5 and Bank 7. The timers are addressed for loading and reading in the same manner as the Register File (Mode #1). The counters are parallel loaded from the Data In (DIN) lines and are read out to the Data Out (DOUT) lines. The 8 or 16 bit data is loaded into the timer bank selected based on the operating mode specified for the timer and programmed into the device. The load occurs when the Enable signal is low and there is a rising clock edge.

Each timer has an independent Carry In-Count/Hold line which allows the designer to have independent control of each timer, thus giving more flexibility. Timer operation is different from counter operation in that a timer will stop counting once the terminal count (FFFFH for an Up Timer and 0000H for a Down Timer) is reached. The Timer will begin counting again only after the timer is reloaded using the Enable and SEL0-2 lines. Also, each timer has a independent Carry Out/Terminal Count output. The carryin-count/hold and the count preload/start signals must be high for the timer to operate.

In Mode #7, 4 Banks (1,3,5,7) are configured as timers which operate as described immediately above, and 4 Banks (0,2,4,6) operate as Registers as described in Mode #1 above.

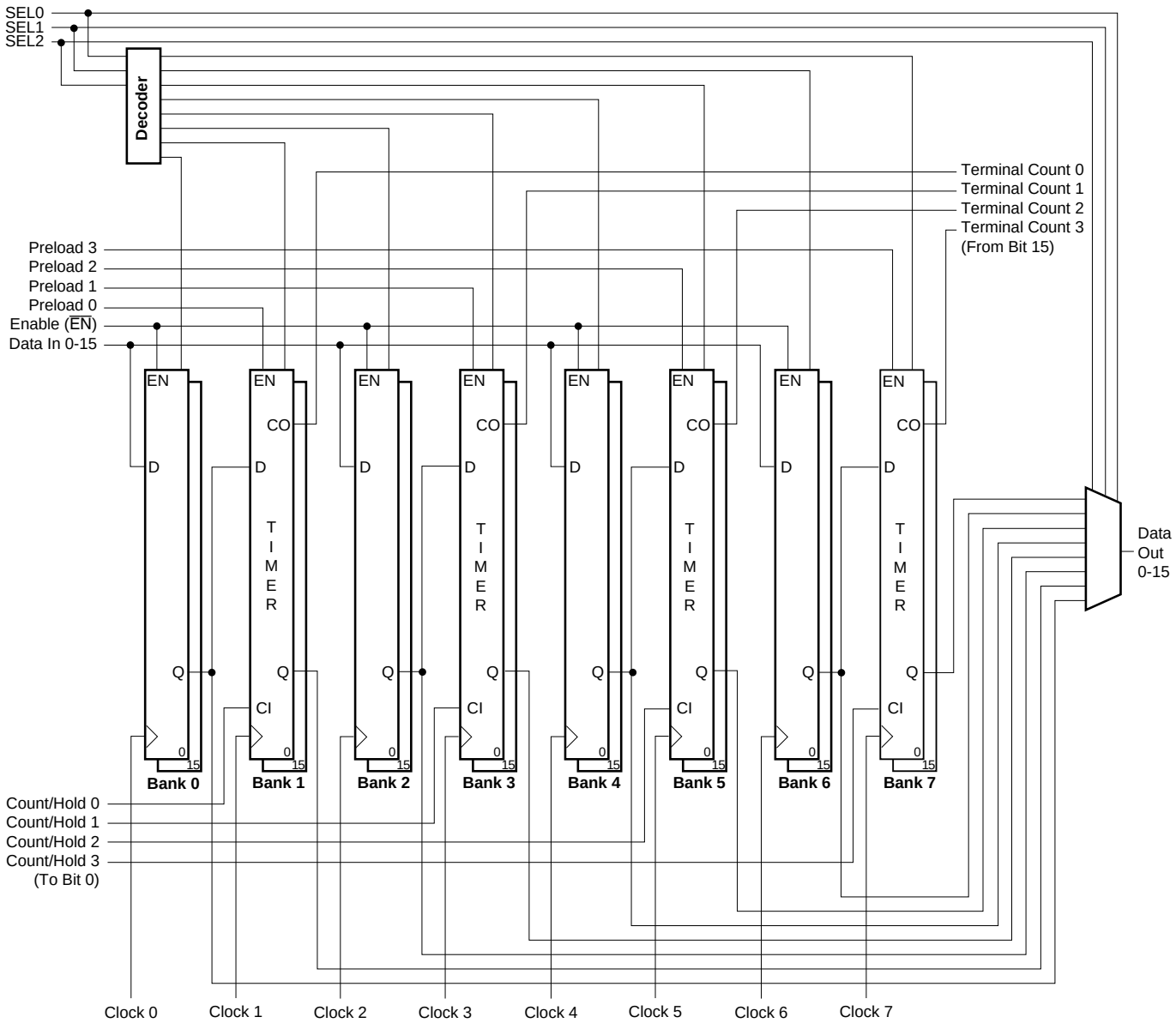
Figure 44. Register/Counter Option #7: 4 Bank Parallel Load Up/Down Timer with 4 Bank Register File



Configuration #8: 4 Bank Adjacent Load Up/Down Timer with 4 Bank Adjacent Register File

In this mode, the timers function as described in Mode #7 above. However, rather than being parallel loaded from the DIN lines when Enable is low, the counters are loaded from the adjacent registers during a load. Banks 0, 2, 4, 6 are used to hold the preload data for counter Banks 1, 3, 5, and 7, respectively. The preload data is loaded into the selected register file bank in the usual manner when a clock occurs and the Enable is low. Data is loaded into the adjacent counter when Preload is low and there is a rising clock edge.

Figure 45. Register/Counter Option #8: 4 Bank Adjacent Load Up/Down Timer with 4 Bank Adjacent Register File

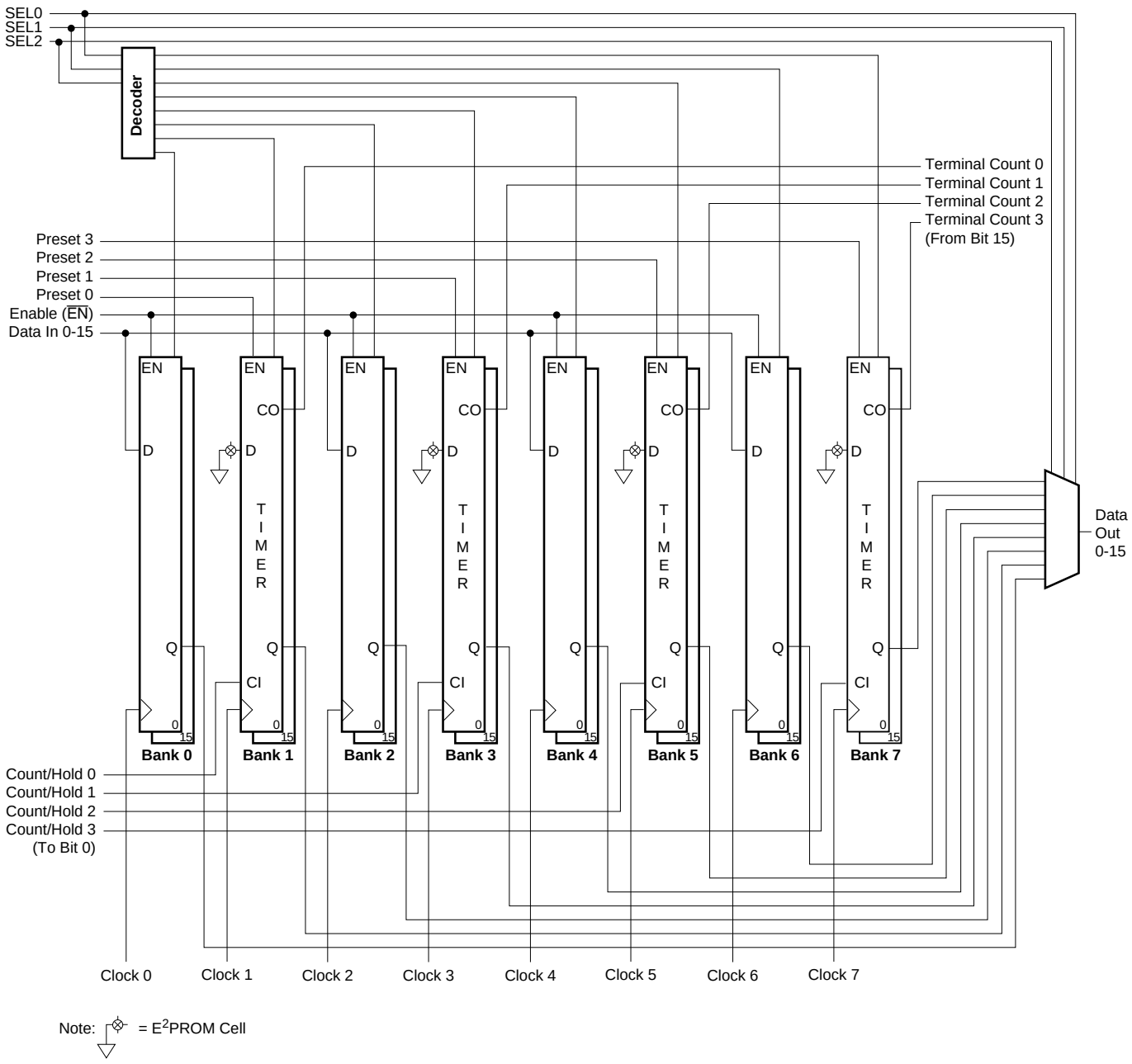


Configuration #9: 4 Bank Custom Preset Load Up/Down Timer with 4 Bank Register File

In this mode, the timers function as described in Mode #7 above. However, rather than being parallel loaded from the DIN lines, or from the adjacent registers, in Mode #9 the Timers are loaded from dedicated E^2PROM (Read-Only Memory) locations. The preset data in these locations is determined by the user when the logic is designed using the pDS software and is programmed into the device using non-volatile technology. The data from these locations is loaded into the counter whenever Preset is low and there is a clock edge.

In Mode #9, 4 Banks (1,3,5,7) are configured as timers which operate as described immediately above, and 4 Banks (0,2,4,6) operate as Registers as described in Mode #1 above.

Figure 46. Register/Counter Option #9: 4 Bank Custom Preset Load Up/Down Timer with 4 Bank Register File



I/O Cells

The 6192 family of devices has 3 types of programmable I/O cells. They can be classified as:

- General Bidirectional I/O Cell
- Module Bidirectional I/O Cell
- Module I/O Cell

General Bidirectional I/O Cell

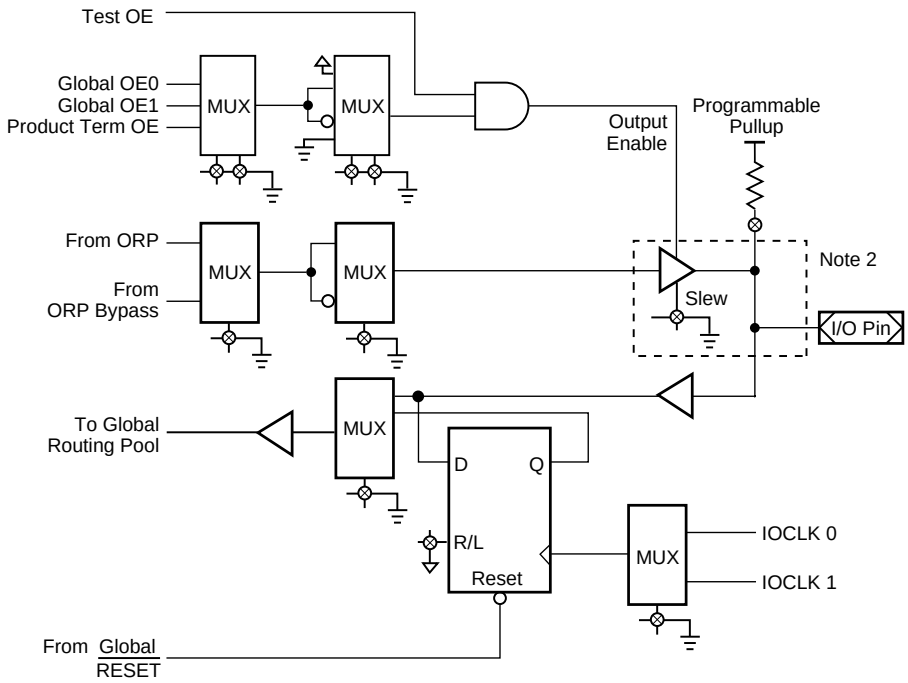
The general bidirectional I/O cell structure, associated with Megablocks A, B, C, D, E and F is similar to Lattice Semiconductor's 3000 family I/O cells (see figure 47). They are used to route input, output or bi-directional signals connected to the I/O pin. Each I/O cell contains Boundary Scan Registers (see Boundary Scan section). A global Test OE signal is hardwired to all I/O cells and is used to 3-state all output buffers within the device. In addition to the test OE signal, two software selectable global OEs are connected to each of these I/O cells. A Product Term OE and global OE signals are fed to an OE multiplexer to allow one of the three signals to control the output. This OE signal can also be inverted.

The output signal can come from one of two sources, the ORP or the faster ORP bypass. A pair of multiplexers selects which signal will be used, and its polarity. There is also a software programmable slew rate control. Slew rate control allows non-timing-critical signals to run at a slower rate which improves system noise immunity. The software has the capability to enable and disable the slew rate control bit on an individual I/O basis.

When the I/O cell is used as an input, the data goes to the input register and a selection multiplexer which selects either the direct data input or the input register output. The output of the multiplexer then goes to the GRP. The input register can be configured as a level sensitive transparent latch or an edge triggered D-type flip-flop to store the incoming data. Each I/O cell can individually select one of the two clock signals (IOCLK 0 or IOCLK 1). The input register reset signal is hard wired to the global reset ($\overline{\text{RESET}}$) signal which is driven by the active low chip reset pin.

There is an active pull-up resistor on the I/O pins which is automatically used when the pin is not used in the design. This improves the noise immunity and reduces I_{cc} for the device. An option exists to have active pull-up resistors connected to all pins.

Figure 47. General-Purpose Bidirectional I/O Cell



Note:

1. Represents an E^2CMOS Cell.
2. See Boundary Scan section for details.

Module Bidirectional I/O Cell

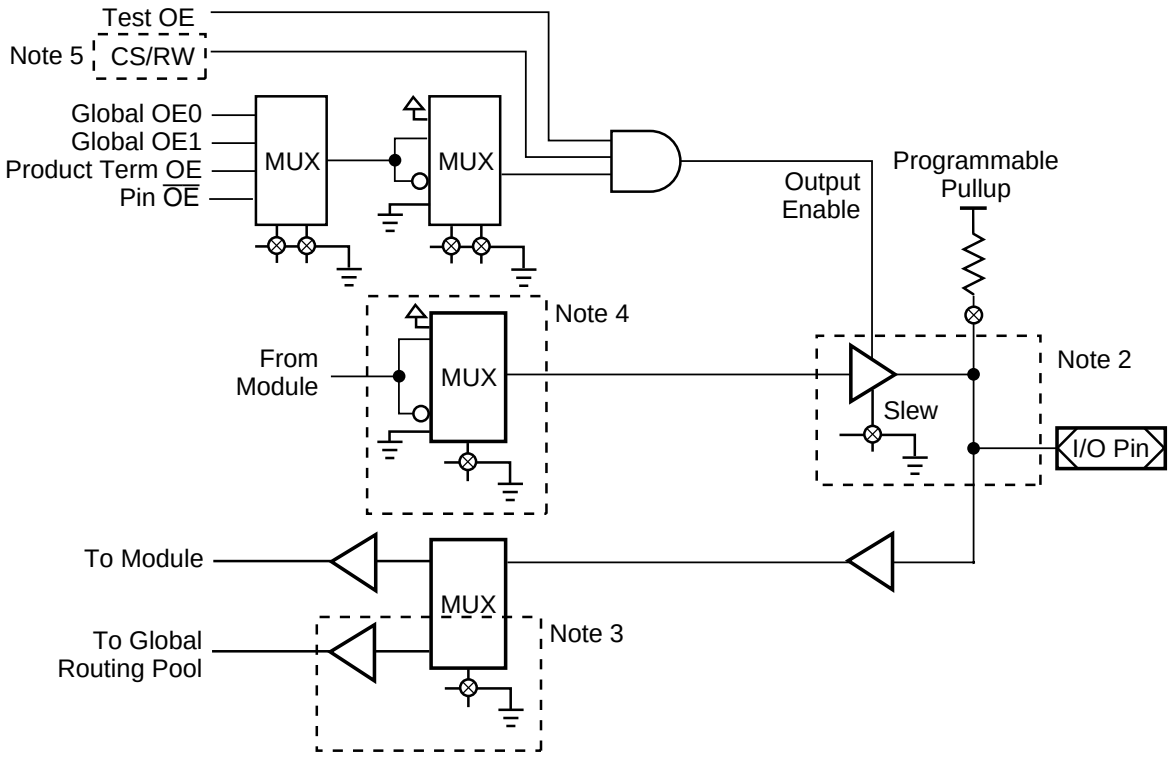
Module bidirectional I/O cells are associated with the bidirectional data bus in the memory module and the register/counter module. The structure of these cells is similar to that of the general bi-directional I/O cells, with some differences. Figure 48 illustrates two signals that are hard-wired to module data I/O cells: Test OE and CS/RW. Test OE is driven by the TOE pin and is wired to all the module data I/O cells. CS/RW is generated by logic internal to the memory module and is only wired to the data I/O cells associated with this module. CS/RW is high only when the chip is selected and the memory is to be read. Thus, an inactive Chip Select forces the pin driver in each of these I/O cells to the high impedance state.

Figure 48 shows Pin $\overline{OE}$, Product Term OE, and two Global OE signals. These are fed to an OE multiplexer to allow one of these four signals or its inversion to control the output driver. The logic output from the Register/Counter module has an inversion capability in the I/O cell while the memory module does not (see figure 48, note 4).

Selected data I/O cells (0-8) in the memory module have an alternative use: these pins can be used as general-purpose inputs to the GRP when the memory module is used in 512 x 9 configuration or left unused in the design. The data I/O cells (0-15) in the register/counter module can also be used as general-purpose inputs to the GRP provided the register/counter module is left unused in the design (see figure 48, note 3).

In the module bidirectional I/O cell, unlike in the general bidirectional I/O cell where the slew rate is individually controllable for each outputs, either all or none of the output data bits can be programmed to have slew rate control.

Figure 48. Module Bidirectional I/O cell



Note:

1. Represents an E^2CMOS Cell.
2. See Boundary Scan section for details.
3. Selected Module I/O pins only (DIO0-8(MEM) and DIO0-15(RC))
4. Register/Counter Module data I/O cell only.
5. Memory Module data I/O cell only.

Module I/O Cell

Module I/O cells are associated with the logic control signals of the memory module and register/counter module. They are controlled by the software and can be programmed as simple inputs or outputs. A multiplexer is used to select the polarity of the output signal coming from the module.

The control signals (TC/CO(0-3), SOUT) of the register/counter module use output pins. The slew rate is individually controllable for each output. SIN and ENABLE are input pins.

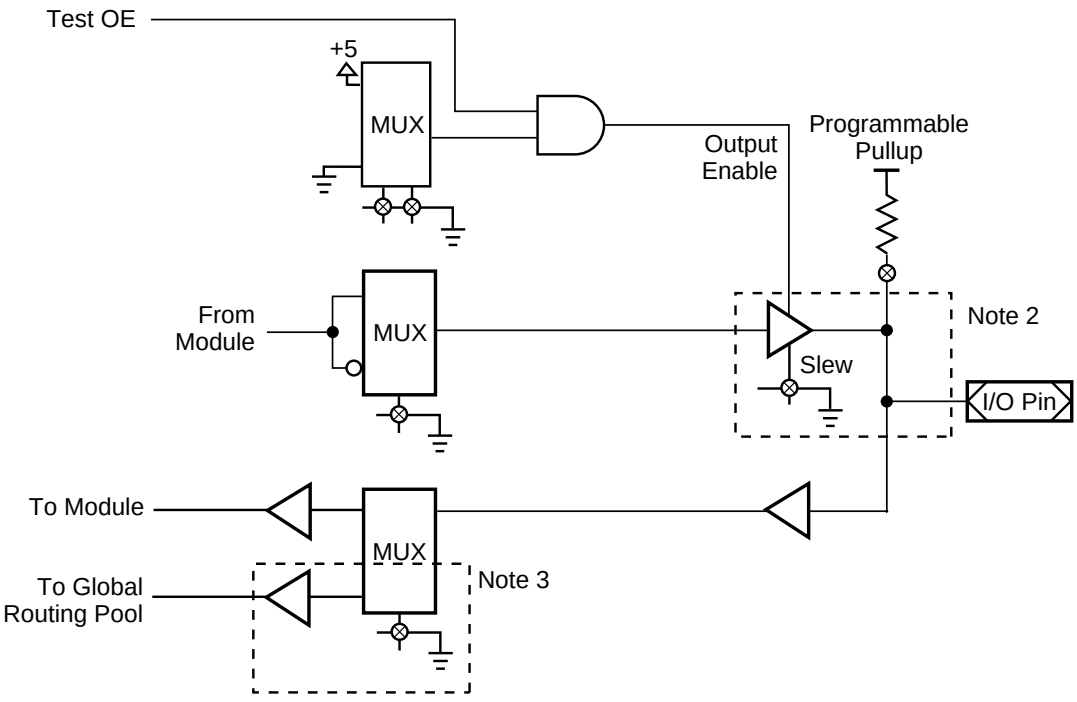
Selected I/O cells in the memory module can be used as general-purpose logic inputs if the memory module is left unused (see figure 49, note 3).

The table below summarizes various types of I/O cells used by the module. They are classified as Module Bidirectional I/O cells and Module Unidirectional I/O cells.

The output signals come from the module. Some of them can be configured with the help of a polarity selection multiplexer. When the I/O cell is used as an input, the data goes to the module. Some of the I/O cells have an additional capability of being used as inputs to the GRP when the module is left unused in the design.

Module Unidirectional I/O cells can be used either as an input or an output. When used as an output cell, TOE will always 3-state the output buffer. It also has a programmable slew rate control. When used as an input cell as shown in the table there are two versions: one that drives the module only, and a second version which can drive the GRP if the module is not used.

Figure 49. Module I/O Cell



Note:

1. Represents an E^{2}CMOS Cell.
2. See Boundary Scan section for details.
3. Only in Memory Module ($\overline{ALE}$ & $\overline{ALF}$ in FIFO and A3 - A7 in RAM).

Module I/O Cell Connectivity

	Signal Name	Module Bidirectional I/O Cell				Module Unidirectional I/O Cell			
		Basic	Input to		Output From Module	Basic	Input to		Output From Module
			Module	GRP			Module	GRP	
Register/ Counter Interface	DIO 0-15	√[2]	√	√	√[3]				
	TC/CO 0-3, SOUT					√[1]			√[3]
	$\overline{OE}$, SIN, $\overline{ENABLE}$						√		
FIFO Interface	DIO 0-8	√[2]	√	√	√				
	DIO 9-17	√[2]	√		√				
	$\overline{EF}$, $\overline{FF}$					√[1]	√		√[3]
	$\overline{ALE}$, $\overline{ALF}$					√[1]	√	√	√[3]
	$\overline{RST}$, $\overline{OE}$, $\overline{RD}$ or $\overline{WR}$						√		
RAM Interface	DIO 0-8	√[2]	√	√	√				
	DIO 9-17	√[2]	√		√				
	A0, $\overline{OE}$, RWL						√		
	A1, A2					√[1]	√		
	A3, A4					√[1]	√	√	
	A5, A6, A7						√	√	
	A8/RWH, $\overline{CS}$						√	√	

Note:
1. TOE and programmable slew rate controls.
2. GOE, PTOE, TOE and programmable slew rate controls.
3. Output polarity selection multiplexer.

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2 - 0005/3256

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	Typical [1]	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC}= 5.0V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	15	pf	V_{CC}= 5.0V, V_Y = 2.0V

1. Guaranteed but not 100% tested.

Table 2 - 0006/6192

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2- 0008B

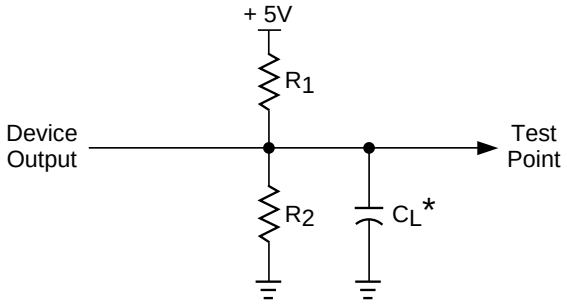
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Ouput Timing Reference Levels	1.5V
Output Load	See figure 2

Table 2 - 0003

3-state levels are measured 0.5V from steady-state active level.

Figure 50. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A

Output Load conditions (See figure 50)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	—	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{OL} \le V_{IL}$ (Max.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
I_{IL-PU}	I/O Active Pull-Up Current	$0V \le V_{IN} \le V_{IL}$ (Max.)	—	—	-150	µA
I_{IL-isp}	BSCAN/$\overline{ispEN}$ Input Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (Max.)	—	—	-150	µA
I_{OS}	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	—	—	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0V, V_{IH} = 3.0V, f_{TOGGLE} = 1MHz	—	150	—	mA

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using sixteen 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Switching Characteristics: Programmable Logic Module[1, 2, 3]

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	
tpd1	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	—	15	—	20	ns
tpd2	A	2	Data Propagation Delay	—	18	—	24.5	ns
fmax (Int.)	A	3	Clock Frequency with Internal Feedback[3]	77	—	57	—	MHz
fmax (Ext.)	—	4	Clock Frequency with External Feedback	50	—	37	—	MHz
fmax (Tog.)	—	5	Clock Frequency, Max Toggle[4]	83	—	63	—	MHz
tsu1	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	9.5	—	12.5	—	ns
tco1	A	7	GLB Reg. Clock to Output Delay, ORP bypass	—	9	—	12	ns
th1	—	8	GLB Reg. Hold Time after Clock, 4PT bypass	0	—	0	—	ns
tsu2	—	9	GLB Reg. Setup Time before Clock	11	—	15	—	ns
tco2	—	10	GLB Reg. Clock to Output Delay	—	10.5	—	14	ns
th2	—	11	GLB Reg. Hold Time after Clock	0	—	0	—	ns
tr1	A	12	Ext. Reset Pin to Output Delay	—	15	—	20	ns
trw1	—	13	Ext. Reset Pulse Duration	10	—	13.5	—	ns
tptoeen	B	14	Input to Output Enable	—	18	—	24.5	ns
tptoedis	C	15	Input to Output Disable	—	18	—	24.5	ns
tgoeen	B	16	Global OE Output Enable	—	11	—	13.5	ns
tgoedis	C	17	Global OE Output Disable	—	11	—	13.5	ns
ttoeen	B	18	Test OE Output Enable	—	17	—	23	ns
ttoedis	C	19	Test OE Output Disable	—	17	—	23	ns
twh	—	20	Ext. Sync. Clock Pulse Duration, High	4	—	5	—	ns
twl	—	21	Ext. Sync. Clock Pulse Duration, Low	4	—	5	—	ns
tsu3	—	22	I/O Reg. Setup Time before Ext. Sync. Clock (Y3, Y4)	6	—	8	—	ns
th3	—	23	I/O Reg. Hold Time after Ext. Sync. Clock (Y3, Y4)	0	—	0	—	ns

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit loadable counter using GRP feedback.
4. fmax (toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Internal Timing Parameters: Programmable Logic Module[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{iobp}	24	I/O Register Bypass	–	2.4	–	3.3	ns
t_{iolat}	25	I/O Latch Delay	–	2.4	–	3.3	ns
t_{iosu}	26	I/O Register Setup Time before Clock	7.2	–	9.6	–	ns
t_{ioh}	27	I/O Register Hold Time after Clock	3.9	–	5.3	–	ns
t_{ioco}	28	I/O Register Clock to Out Delay	–	1.9	–	2.6	ns
t_{ior}	29	I/O Register Reset to Out Delay	–	3.6	–	4.9	ns
GRP							
t_{grp}	30	GRP Delay	–	3.0	–	4.1	ns
GLB							
t_{4ptbp}	31	4 Product Term Bypass Path Delay	–	5.9	–	7.6	ns
t_{1ptxor}	32	1 Product Term/XOR Path Delay	–	6.4	–	8.8	ns
$t_{20ptxor}$	33	20 Product Term/XOR Path Delay	–	7.4	–	10.1	ns
t_{xoradj}	34	XOR Adjacent Path Delay[3]	–	8.1	–	11.1	ns
t_{gbp}	35	GLB Register Bypass Delay	–	0.1	–	0.1	ns
t_{gsu}	36	GLB Register Setup Time before Clock	1.8	–	2.4	–	ns
t_{gh}	37	GLB Register Hold Time after Clock	6.0	–	8.2	–	ns
t_{gco}	38	GLB Register Clock to Output Delay	–	1.8	–	2.2	ns
t_{gro}	39	GLB Register Reset to Output Delay	–	2.8	–	3.8	ns
t_{ptre}	40	GLB Product Term Reset to Register Delay	–	10.5	–	14.2	ns
t_{ptoe}	41	GLB Product Term Output Enable to I/O Cell Delay	–	5.4	–	7.3	ns
t_{ptck}	42	GLB Product Term Clock Delay	3.2	6.3	4.3	8.5	ns
ORP							
t_{orp}	43	ORP Delay	–	2.7	–	3.6	ns
t_{orpbp}	44	ORP Bypass Delay	–	1.2	–	1.6	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters: Programmable Logic Module[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	45	Output Buffer Delay	–	2.4	–	3.3	ns
t_{obs}	46	Output Buffer Delay, Slow Slew	–	12.4	–	13.3	ns
t_{oen}	47	I/O Cell OE to Output Enabled	–	7.2	–	9.8	ns
t_{odis}	48	I/O Cell OE to Output Disabled	–	7.2	–	9.8	ns
Clocks							
$t_{gy0/1/2}$	49	Clock Delay, Y0 or Y1 or Y2 to Global GLB Clock Line	3.6	3.6	4.9	4.9	ns
$t_{ioy3/4}$	50	Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line	1.2	5.2	1.6	7.0	ns
Global Reset							
t_{gr}	51	Global Reset to GLB and I/O Registers	–	7.1	–	9.6	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

External Switching Characteristics: FIFO Module[1]

Over Recommended Operating Conditions

PARAMETER	TEST[2] COND.	#[1]	DESCRIPTION	-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	
ts	—	52	Shift Frequency	—	50	—	33.3	MHz
trc	A	53	Read Cycle Time	20	—	30	—	ns
ta	A	54	Read Pulse to Data Access Time	—	12	—	20	ns
trr	A	55	Read Recovery Time	5	—	10	—	ns
trpw	—	56	Read Pulse Width	15	—	20	—	ns
tdv	A	57	Data Held Valid from Read Pulse Inactive	3	—	3	—	ns
twc	—	58	Write Cycle Time	20	—	30	—	ns
twpw	—	59	Write Pulse Width	15	—	20	—	ns
twr	—	60	Write Recovery Time	5	—	10	—	ns
tds	—	61	Data Setup Time	13	—	18	—	ns
tdh	—	62	Data Hold Time	0	—	0	—	ns
trsc	—	63	Reset Cycle Time	20	—	30	—	ns
trs	—	64	Reset Pulse Width	15	—	20	—	ns
trsr	A	65	Reset Recovery Time	5	—	10	—	ns
tefl	A	66	Reset Active to Empty Flag Active	—	20	—	25	ns
tffh	A	67	Reset Active to Full Flag Inactive	—	20	—	25	ns
talel	A	68	Reset Active to Almost Empty Flag Active	—	25	—	30	ns
talfh	A	69	Reset Active to Almost Full Flag Inactive	—	25	—	30	ns
trff	A	70	Read Inactive to Full Flag Inactive	—	20	—	25	ns
traf	A	71	Read Inactive to Almost Full Flag Inactive	—	25	—	30	ns
trhz	A	72	Read Inactive to Data Out Disable	—	15	—	20	ns
trlz	A	73	Read Active to Data Out Enable	0	—	0	—	ns
trss	A	74	Read or Write Inactive to Reset Inactive	15	—	20	—	ns
trae	A	75	Read Active to Almost Empty Flag Active	—	25	—	30	ns
tref	A	76	Read Active to Empty Active	—	20	—	25	ns
trpe	A	77	Read Pulse Width after Empty Flag Inactive	15	—	20	—	ns
twff	—	78	Write Active to Full Flag Active	—	20	—	25	ns
twaf	—	79	Write Active to Almost Full Flag Active	—	25	—	30	ns
twae	—	80	Write Inactive to Almost Empty Flag Inactive	—	25	—	30	ns
twef	—	81	Write Inactive to Empty Flag Inactive	—	20	—	25	ns
twpf	—	82	Write Pulse Width after Full Flag Inactive	15	—	20	—	ns

1. Refer to Timing Model in this data sheet for further details.
2. Reference Switching Test Conditions section.

Internal TIming Parameters: FIFO Module[1]

Over Recommended Operating Conditions

PARAMETER	#	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
ts	83	Shift Frequency	—	50	—	28.5	MHz
trc	84	Read Cycle Time	25	—	35	—	ns
terdv	85	End Read Pulse to Next Data Valid	—	12	—	20	ns
trr	86	Read Recovery Time	10	—	15	—	ns
trpw	87	Read Pulse Width	15	—	20	—	ns
twc	88	Write Cycle Time	20	—	30	—	ns
twpw	89	Write Pulse Width	15	—	20	—	ns
twr	90	Write Recovery Time	5	—	10	—	ns
tds	91	Data Setup Time	18	—	23	—	ns
tdh	92	Data Hold Time	0	—	0	—	ns
trsc	93	Reset Cycle Time	25	—	30	—	ns
trs	94	Reset Pulse Width	15	—	20	—	ns
trsr	95	Reset Recovery Time	10	—	10	—	ns
tefl	96	Reset Active to Empty Flag Active	—	15	—	18	ns
tffh	97	Reset Active to Full Flag Inactive	—	15	—	18	ns
talel	98	Reset Active to Almost Empty Flag Active	—	20	—	23	ns
talfl	99	Reset Active to Almost Full Flag Inactive	—	20	—	23	ns
trff	100	Read Inactive to Full Flag Inactive	—	15	—	18	ns
traf	101	Read Inactive to Almost Full Flag Inactive	—	20	—	23	ns
trss	102	Read or Write Inactive to Reset Inactive	15	—	20	—	ns
trae	103	Read Active to Almost Empty Flag Active	—	20	—	23	ns
tref	104	Read Active to Empty Active	—	15	—	18	ns
trpe	105	Read Pulse Width after Empty Flag Inactive	15	—	20	—	ns
twff	106	Write Active to Full Flag Active	—	15	—	18	ns
twaf	107	Write Active to Almost Full Flag Active	—	20	—	23	ns
twae	108	Write Inactive to Almost Empty Flag Inactive	—	20	—	23	ns
twef	109	Write Inactive to Empty Flag Inactive	—	15	—	18	ns
twpf	110	Write Pulse Width after Full Flag Inactive	15	—	20	—	ns
Generic Path							
tmemmio	111	Delay Added for Memory Out to MIO	—	1	—	2	ns
fmemgrp	112	Delay Added for Memory Out to GRP	—	1	—	2	ns
tmiomem	113	Delay Added for MIO to Memory	—	4	—	5	ns
tgrpmem	114	Delay Added for GRP to Memory	—	4	—	5	ns

1. Internal Timing Parameters are not tested and are for reference only.

External Switching Characteristics: RAM Module (Port A Only)[1]

Over Recommended Operating Conditions

PARAMETER	TEST[2] COND.	#[1]	DESCRIPTION	-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	
Read Cycle								
trc	—	115	Read Cycle Time	20	—	25	—	ns
taa	A	116	Address Access Time	—	20	—	25	ns
tacs	A	117	Chip Select Access Time	—	15	—	20	ns
taoe	A	118	OE Pin Access Time	—	12	—	15	ns
toh	A	119	Output Hold from Address Change	2	—	2	—	ns
toeen	B	120	OE Pin to Data Output Enable	0	—	0	—	ns
toedis	C	121	OE Pin to Data Output Disable	—	12	—	15	ns
tcsen	B	122	Chip Select to Data Output Enable	0	—	0	—	ns
tcsdis	C	123	Chip Select to Data Output Disable	—	15	—	20	ns
Write Cycle								
twc	—	124	Write Cycle Time	20	—	25	—	ns
taw	—	125	Address Valid to Write End	15	—	20	—	ns
tas	—	126	Address Setup to Write Start	0	—	0	—	ns
tewcs (tcw)	—	127	Chip Select to End of Write	15	—	20	—	ns
twp	—	128	Write Pulse Width	15	—	20	—	ns
twr	—	129	Write Recovery Time	0	—	0	—	ns
tdw	—	130	Data Valid to Write End	15	—	20	—	ns
tdh	—	131	Data Hold from Write End	0	—	0	—	ns
tween	—	132	RW High to Data Output Enable	0	—	0	—	
twedis	—	133	RW Low to Data Output Disable	—	15	—	20	ns
Busy Timing								
tba	—	134	Busy from Address Match	—	15	—	20	ns
tnba	—	135	Not Busy from Address Mismatch	—	15	—	20	ns
tbcs	—	136	Busy from Chip Select Active	—	15	—	20	ns
tnbcs	—	137	Not Busy from Chip Select Inactive	—	15	—	20	ns
taps	—	138	Arbitration Priority Setup Time	5	—	8	—	ns
tnbd	—	139	Not Busy to Read Data Valid	—	20	—	30	ns

1. Refer to Timing Model in this data sheet for further details.
2. Reference Switching Test Conditions section.

Internal TIming Parameters: RAM Module (Port B Only)

Over Recommended Operating Conditions

PARAMETER	#	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Read Cycle							
trc	140	Read Cycle Time	25	—	30	—	ns
taa	141	Address Access Time	—	20	—	28	ns
toh	142	Output Hold from Address Change	0	—	0	—	ns
Write Cycle							
twc	143	Write Cycle Time	25	—	30	—	ns
taw	144	Address Valid to Write End	17	—	22	—	ns
tas	145	Address Setup to Write Start	0	—	0	—	ns
tewcs (tcw)	146	Chip Select to End of Write	17	—	22	—	ns
twp	147	Write Pulse Width	15	—	20	—	ns
twr	148	Write Recovery Time	0	—	0	—	ns
tdw	149	Data Valid to Write End	17	—	22	—	ns
tdh	150	Data Hold from Write End	0	—	0	—	ns
Busy Timing							
tba	151	Busy from Address Match	—	10	—	13	ns
tnba	152	Not Busy from Address Mismatch	—	10	—	13	ns
tbcs	153	Busy from Chip Select Active	—	10	—	13	ns
tnbcs	154	Not Busy from Chip Select Inactive	—	10	—	13	ns
taps	155	Arbitration Priority Setup Time	5	—	8	—	ns
tnbd	156	Not Busy to Read Data Valid	—	20	—	30	ns
Generic Path							
tmemmio	157	Delay Added for Memory Out to MIO	—	1	—	2	ns
fmemgrp	158	Delay Added for Memory Out to GRP	—	1	—	2	ns
tmiomem	159	Delay Added for MIO to Memory	—	4	—	5	ns
tgrpmem	160	Delay Added for GRP to Memory	—	4	—	5	ns

External Switching Characteristics: Register/Counter Module[1]

Over Recommended Operating Conditions

PARAMETER	TEST[2] COND.	#[1]	DESCRIPTION	-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	
tregco	A	161	Clock to Parallel Data Out	—	15	—	20	ns
tregsu	—	162	Parallel Data In Setup to Clock	8	—	12	—	ns
tregh	—	163	Parallel Data In Hold from Clock	0	—	0	—	ns
tgrdo	A	164	Global Reset to Data Out	—	20	—	25	ns
tgrpw	—	165	Global Reset Pulse Duration	12	—	15	—	ns
trgen	B	166	Global OE Output Enable	—	15	—	20	ns
trgdis	C	167	Global OE Output Disable	—	15	—	20	ns
tclkh	—	168	Clock High Period	4	—	5	—	ns
tclkl	—	169	Clock Low Period	4	—	5	—	ns
Shift Register								
tsft	—	170	Clock Frequency, Max. Shift Rate	125	—	100	—	MHz
tsoutco	—	171	Clock to SOUT	—	17	—	20	ns
tsinsu	—	172	SIN Setup to Clock	8	—	12	—	ns
tsinh	—	173	SIN Hold from Clock	0	—	0	—	ns
Counter/Timer								
fmax	—	174	16-bit Counter	125	—	100	—	MHz
fmax	—	175	16-bit Timer	125	—	100	—	MHz
tcaco	A	176	Clock to Carry Out/TC (16-bit)	—	18	—	22	ns

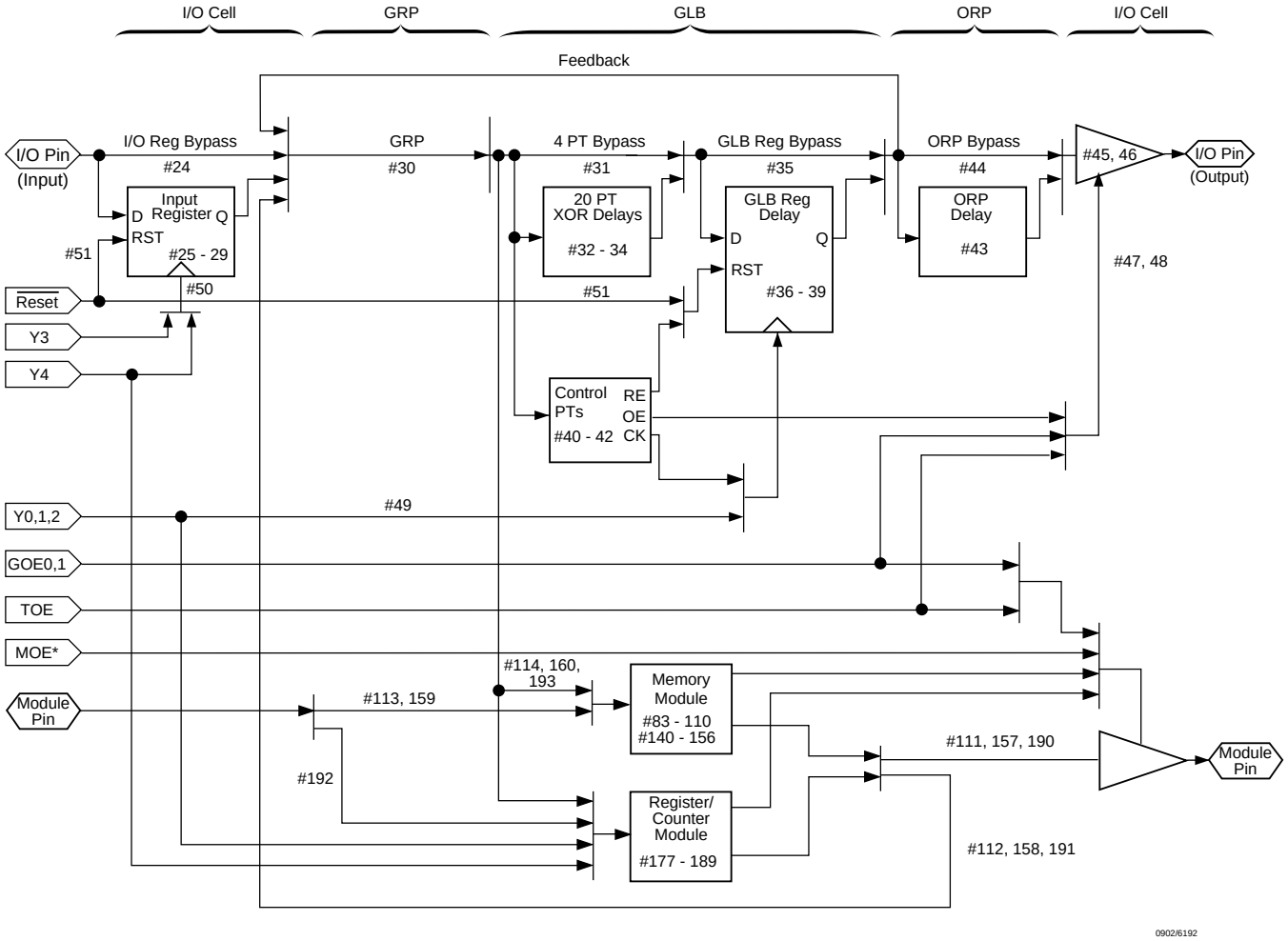
1. Refer to Timing Model in this data sheet for further details.
2. Reference Switching Test Conditions section.

Internal TIming Parameters: Register/Counter Module

Over Recommended Operating Conditions

PARAMETER	#	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Generic Timings							
tsco	177	Select to Parallel Data Out	—	14.6	—	17.6	ns
tssu	178	Select Setup to Clock	7.6	—	11.9	—	ns
tsh	179	Select Hold to Clock	0	—	0	—	ns
tensu	180	Enable/Preload/Preset Setup to Clock	7.6	—	11.9	—	ns
tenh	181	Enable/Preload/Preset Hold from Clock	0	—	0	—	ns
tptrdo	182	Product Term Reset to Data Out	—	11.9	—	13.4	ns
tptrpw	183	Product Term Reset Pulse Duration	12	—	15	—	ns
Shift Register							
tsensu	184	ShiftEn Setup to Clock	7.6	—	11.9	—	ns
tsenh	185	ShiftEn Hold to Clock	0	—	0	—	ns
Counter/Timer							
tcaco	186	Clock to Carry Out/TC (16-bit)	—	13.4	—	15.1	ns
tcichsu	187	Carry In/Count Hold Setup to Clock	7.6	—	11.9	—	ns
tcichh	188	Carry In/Count Hold Hold to Clock	0	—	0	—	ns
tcichco	189	Carry In/Count Hold to Carry Out/TC					ns
Generic Path							
trcmio	190	Delay Added for Reg./Counter Out to MIO	—	1	—	2	ns
frcgrp	191	Delay Added for Reg./Counter Out to GRP	—	1	—	2	ns
tmiorc	192	Delay Added for MIO to Reg./Counter	—	4	—	5	ns
tgrprc	193	Delay Added for GRP to Reg./Counter	—	4	—	5	ns

ispLSI and pLSI 6192 Timing Model

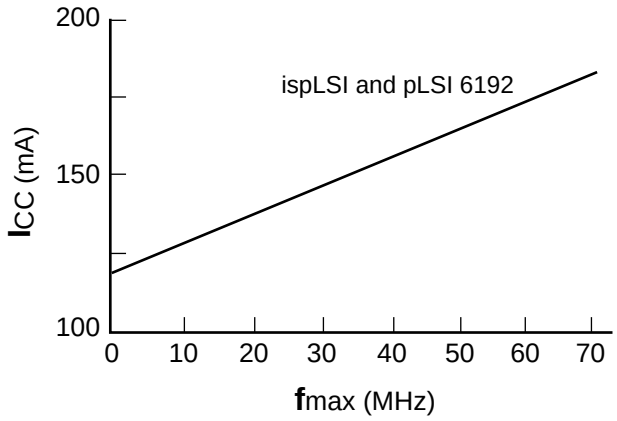


* = Dedicated Module Output Enable

Power Consumption

Power Consumption in the ispLSI and pLSI 6192 device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 51 shows the relationship between power and operating speed.

Figure 51. Typical Device Power Consumption vs fmax



Notes: Typical Current at 5V, 25° C

0127A/6192

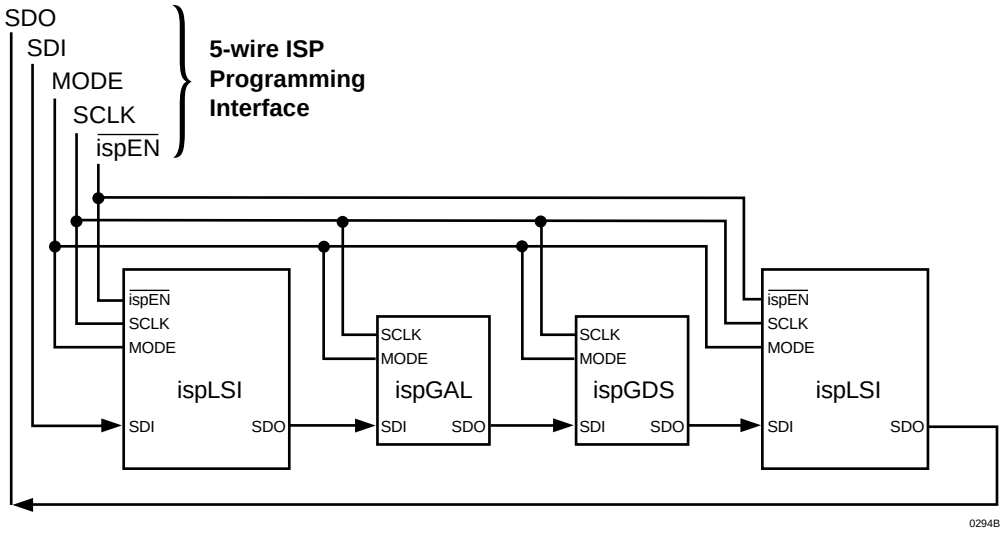
In-System Programmability™

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

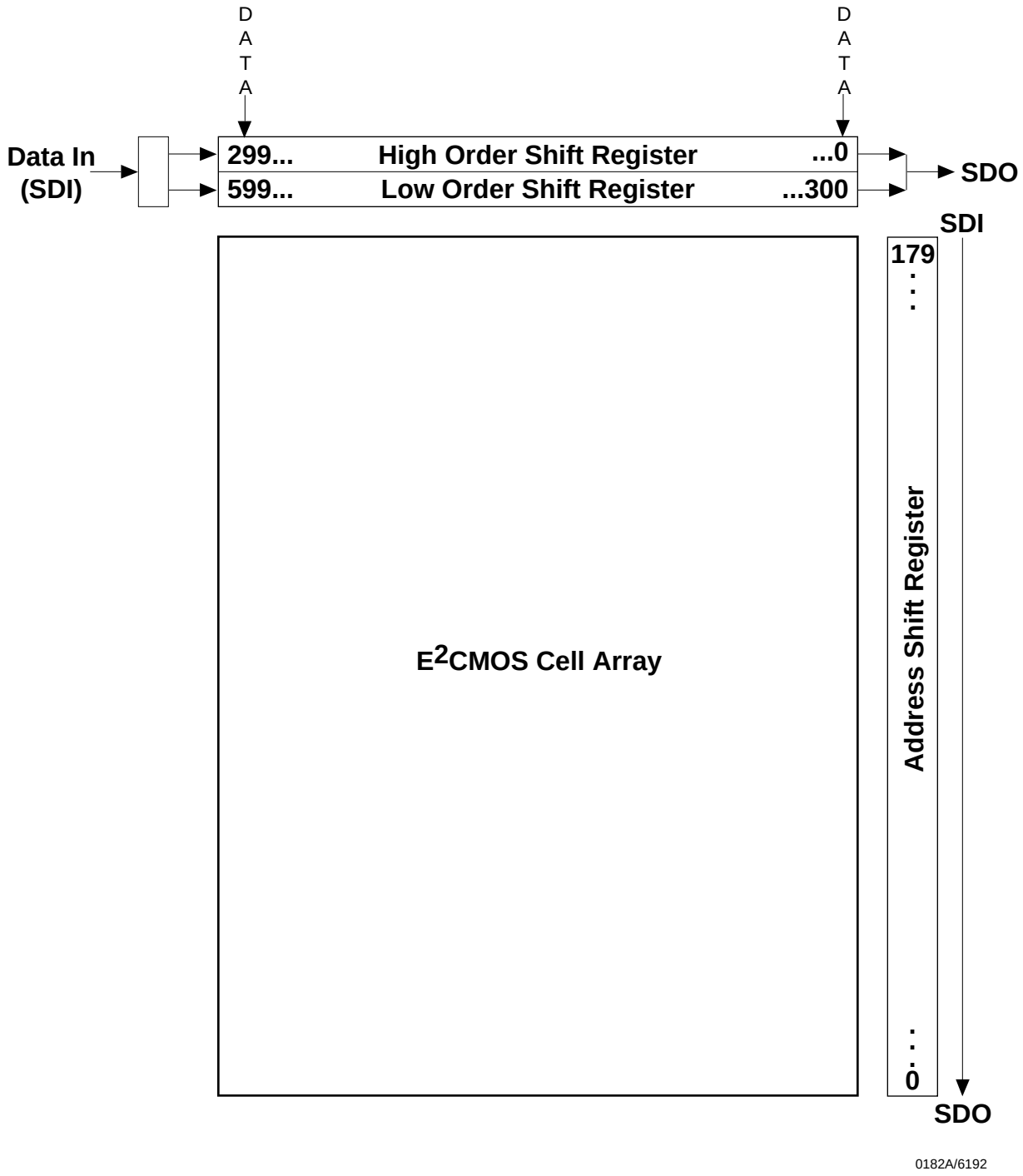
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for interface include isp Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 52 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section in this Data Book.

The device identifier for the ispLSI 6192 is 0011 0010 (32 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 52. ISP™ Programming Interface



ispLSI 6192 Shift Register Layout



Note: A logic “1” in the address shift register enables the row for programming or verification. A logic “0” disables it.

Pin Description: Programmable Logic Module

NAME	MQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 4 I/O 5 - I/O 9 I/O 10 - I/O 14 I/O 15 - I/O 19 I/O 20 - I/O 24 I/O 25 - I/O 29 I/O 30 - I/O 34 I/O 35 - I/O 39 I/O 40 - I/O 44 I/O 45 - I/O 49 I/O 50 - I/O 54 I/O 55 - I/O 59 I/O 60 - I/O 64 I/O 65 - I/O 69 I/O 70 - I/O 74 I/O 75 - I/O 79 I/O 80 - I/O 84 I/O 85 - I/O 89 I/O 90 - I/O 94 I/O 95	32, 33, 34, 36, 37, 38, 40, 41, 42, 43, 44, 45, 47, 48, 49, 51, 52, 53, 54, 55, 56, 58, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 79, 80, 82, 83, 84, 85, 86, 87, 88, 89, 90, 92, 94, 95, 96, 97, 169, 170, 171, 172, 173, 175, 176, 177, 179, 181, 182, 183, 184, 186, 187, 188, 189, 190, 192, 193, 194, 196, 198, 199, 200, 201, 203, 204, 205, 206, 207, 1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 15, 16, 17, 18, 19, 20	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0 and GOE1	75 and 73	Input - Global Output Enable input pins.
TOE	72	Input - Test Output Enable pin.
$\overline{\text{RESET}}$	25	Input - Active Low Global Reset pin which resets all of the GLB and I/O registers in the device.
Y0, Y1 and Y2	22, 24, 78	Input - Dedicated Clock pins - These clock inputs are connected to one of the clock inputs of all the GLBs on the device.
Y3 and Y4	77, 76	Input - Dedicated Clock pins - These clock inputs are connected to one of the clock inputs of all the I/O cells in the device.
**$\overline{\text{ispEN}}$/BSCAN	26	Input - Boundary Scan Enable. Dedicated in-system programming Enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
*SDI/TDI	27	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is low, this is the Serial Data In pin to load programming data into the device. When $\overline{\text{ispEN}}$ is high, this pin is used as the Test Data In for the Boundary Scan operation
*SCLK/TCLK	28	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is low, this is the Serial Clock input pin for device programming. When $\overline{\text{ispEN}}$ is high, this is the Test Clock pin used for the Boundary Scan operation.
*MODE/TMS	29	Input - This pin performs two functions. When $\overline{\text{ispEN}}$ is low, this is the Mode pin to control the isp state machine operations. When $\overline{\text{ispEN}}$ is high, this is the Test Mode Select input for the Boundary Scan operation.
$\overline{\text{TRST}}$	71	Input - Test Reset, active low to reset the Boundary Scan State Machine.
*SDO/TDO	136	Output - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it is the Serial Data Out pin used to read the isp data. When $\overline{\text{ispEN}}$ is high it functions as Test Data Out pin for the Boundary Scan operation.
GND	11, 23, 35, 46, 59, 70, 81, 93, 104, 116, 128, 141, 152, 158, 164, 174 180, 185, 191, 197, 202, 208	Ground (GND)
Vcc	13, 21, 31, 39, 57, 74, 91, 118 126, 137, 145, 162, 178, 195	Vcc

Table 2 - 0002/6192

* ispLSI versions only

** $\overline{\text{ispEN}}$ for ispLSI versions only, NC for pLSI versions must be left floating or tied to Vcc, must not be grounded or tied to any other signal.

Pin Description: Register/Counter Module

NAME	MQFP PIN NUMBERS	DESCRIPTION
DI/O 0 - DI/O 4 (RC) DI/O 5 - DI/O 9 (RC) DI/O 10 - DI/O 14 (RC) DI/O 15 (RC)	139, 140, 142, 143, 144, 146, 147, 148, 149, 150, 151, 153, 154, 156, 157, 159	Input/Output Pins - These are the external data pins used by the Register/Counter module. They are tristated when the $\overline{OE}$(RC) pin is inactive (high). They can be used as general-purpose logic inputs if the Register/Counter module does not use the external data interface.
TC/CO0 - TC/CO3	165, 166, 167, 168,	Output Pins - Terminal count (timers) or Carry Out (counters) outputs. Used only in timer or counter modes for Register/Counter module.
$\overline{ENABLE}$	163	Input Pin - Active low Enable pin used to write data from DI/O(RC) pins to selected bank of Register/Counter.
SIN	160	Input Pin - Serial data input to Bit 15 of Bank 0. Used only in shift register configuration.
SOUT	161	Output Pin - Serial data output from Bit 0 of Bank 7. Used only in shift register configurations.
$\overline{OE}$ (RC)	138	Input Pin - Register/Counter Output Enable pin. Enables the DI/O(RC) pins when active low.

Table 2 - 0002/6192 Reg/Ctr

Pin Description: FIFO Module

NAME	MQFP PIN NUMBERS	DESCRIPTION
DI/O 0 - DI/O 4 (FIFO) DI/O 5 - DI/O 9 (FIFO) DI/O 10 - DI/O 14 (FIFO) DI/O 15 - DI/O 17 (FIFO)	113, 114, 115, 117, 119, 120, 121, 122, 123, 124, 125, 127, 129, 130, 131, 132, 133, 134	Input/Output Pins - These are the external data I/O pins used by the FIFO. For the 512 x 9 FIFO configuration, the higher 9 bits are used. These pins tristate when $\overline{RD}$ goes inactive (high).
$\overline{RST}$	99	Input Pin - Active low $\overline{Reset}$ input used to reset the internal read and write pointers to the first location of the RAM array.
$\overline{RD}$ or $\overline{WR}$	110	Input Pin - Active Low. This is a dual function pin. When data is read from the FIFO to the external pins it acts as a read enable pin ($\overline{RD}$) for Port B to A configuration. When data is written to the FIFO from the external pins it acts as a write control pin ($\overline{WR}$) for Port A to B configuration. When $\overline{RD}$ is low, data is read from the RAM array sequentially. When $\overline{WR}$ is low, data is written to the RAM array
$\overline{FF}$	101	Output Pin - Active low Full Flag pin to indicate that the FIFO is full and further write operation is inhibited.
$\overline{EF}$	100	Output Pin - Active low Empty Flag pin to indicate the FIFO is empty and further read operation is inhibited.
$\overline{ALF}$	103	Output Pin - Active low Almost Full Flag. It can be programmed to activate at any location. Can be used as a general-purpose logic input if not used for external FIFO interfacing.
$\overline{ALE}$	102	Output Pin - Active low Almost Empty Flag. It can be programmed to activate at any location. It has to be below the Almost Full Flag. Can be used as a general-purpose logic input if not used for external FIFO interfacing.

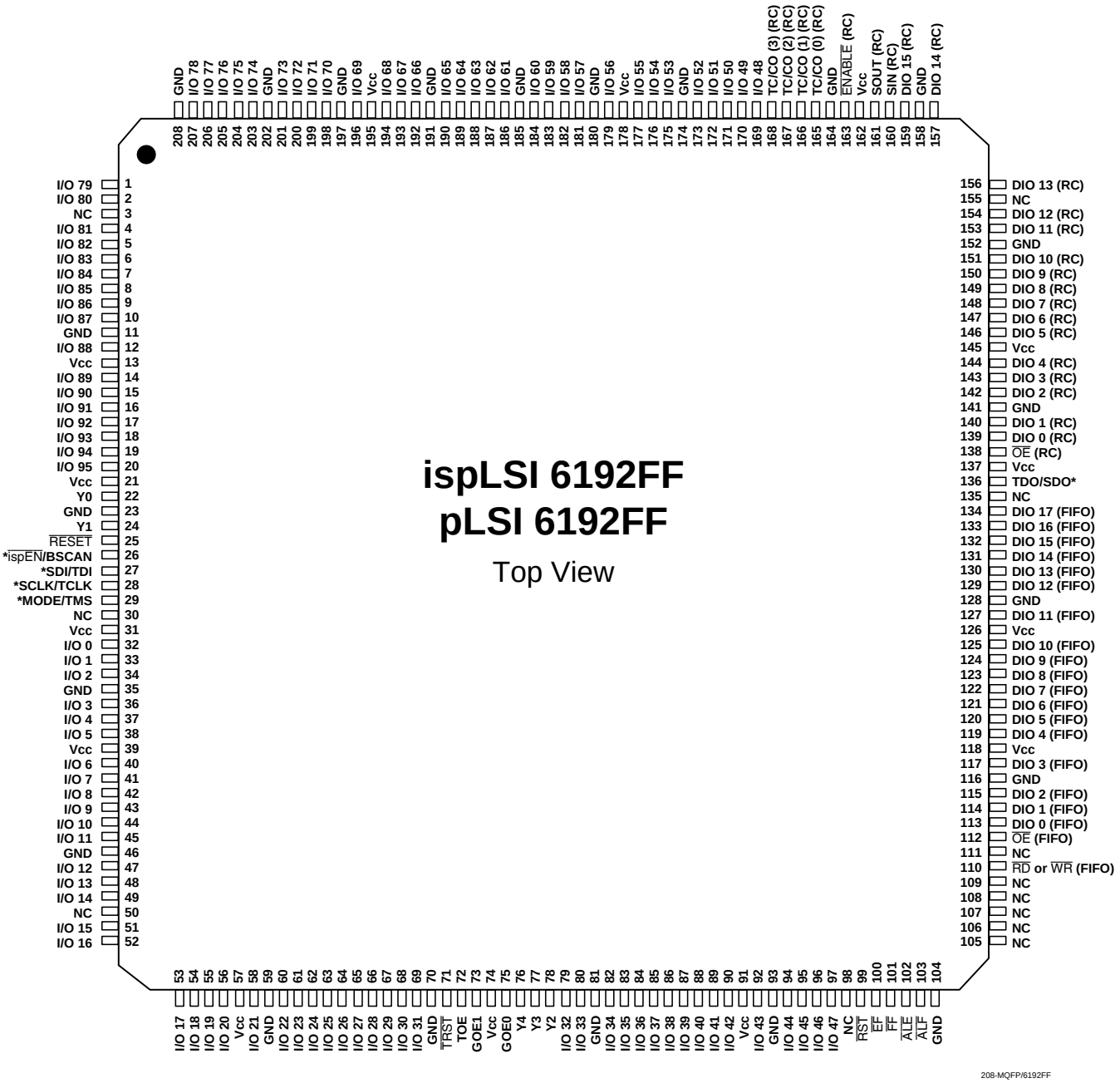
Table 2 - 0002/6192FF

Pin Description: Dual Port and Single Port RAM Module

NAME	MQFP PIN NUMBERS	DESCRIPTION
DI/O 0 - DI/O 4 (RAM) DI/O 5 - DI/O 9 (RAM) DI/O 10 - DI/O 14 (RAM) DI/O 15 - DI/O 17 (RAM)	113, 114, 115, 117, 119, 120, 121, 122, 123, 124, 125, 127, 129, 130, 131, 132, 133, 134	Input/Output Pins - These are the data I/O pins used by the RAM. For the 512x9 RAM configuration, the high order 9 bits are used. These pins tristate when $\overline{OE}$(RAM) or $\overline{CS}$(RAM) goes inactive. In addition, if the RWH and/or RWL pin are in the write state (low), the appropriate byte(s) of DI/O will tristate. DI/O 0-8 can also be used for general-purpose logic inputs if not needed for RAM interfacing from the I/O cellls (Single Port RAM only).
A0 - A3 A4 - A7	99, 100, 101, 102, 103, 105, 106, 108	Input Pins - Address inputs to access locations in the RAM array. A3 - A7 can also be used as general-purpose logic inputs if not needed for RAM interfacing from the I/O cells.
A8/RWH	109	Input Pin - Used as read/write control line for upper byte RAM when in byte write mode. The RAM performs a read operation when RWH is high and write operation when RWH is low. Used as 9th address bit when RAM is configured as 512x9. Can be used as a general-pupose logic input if not needed for external RAM interfacing.
RWL	110	Input Pin - Controls the read/write operation of the memory module. When operating in the byte write mode, RWL controls the read/write of the lower order byte while RWH controls the read/write operation of the higher order byte.
$\overline{CS}$	111	Input Pin - Chip select. Must be active low to perform read or write from external RAM interface. Can be used as a general-pupose logic input if not needed for external RAM interfacing.
$\overline{OE}$	112	Input Pin - RAM output enable. Controls DI/O(RAM) pin tristating. Pins tristate when $\overline{OE}$ is inactive (high). Outputs enabled when $\overline{OE}$ active (low).
$\overline{BusyA}$ (Dual Port RAM Only)	98	Output Pin - Active low busy pin indicating that Port A has lost the arbitration when both Port A and Port B are attempting to access the same RAM location simultaneously.

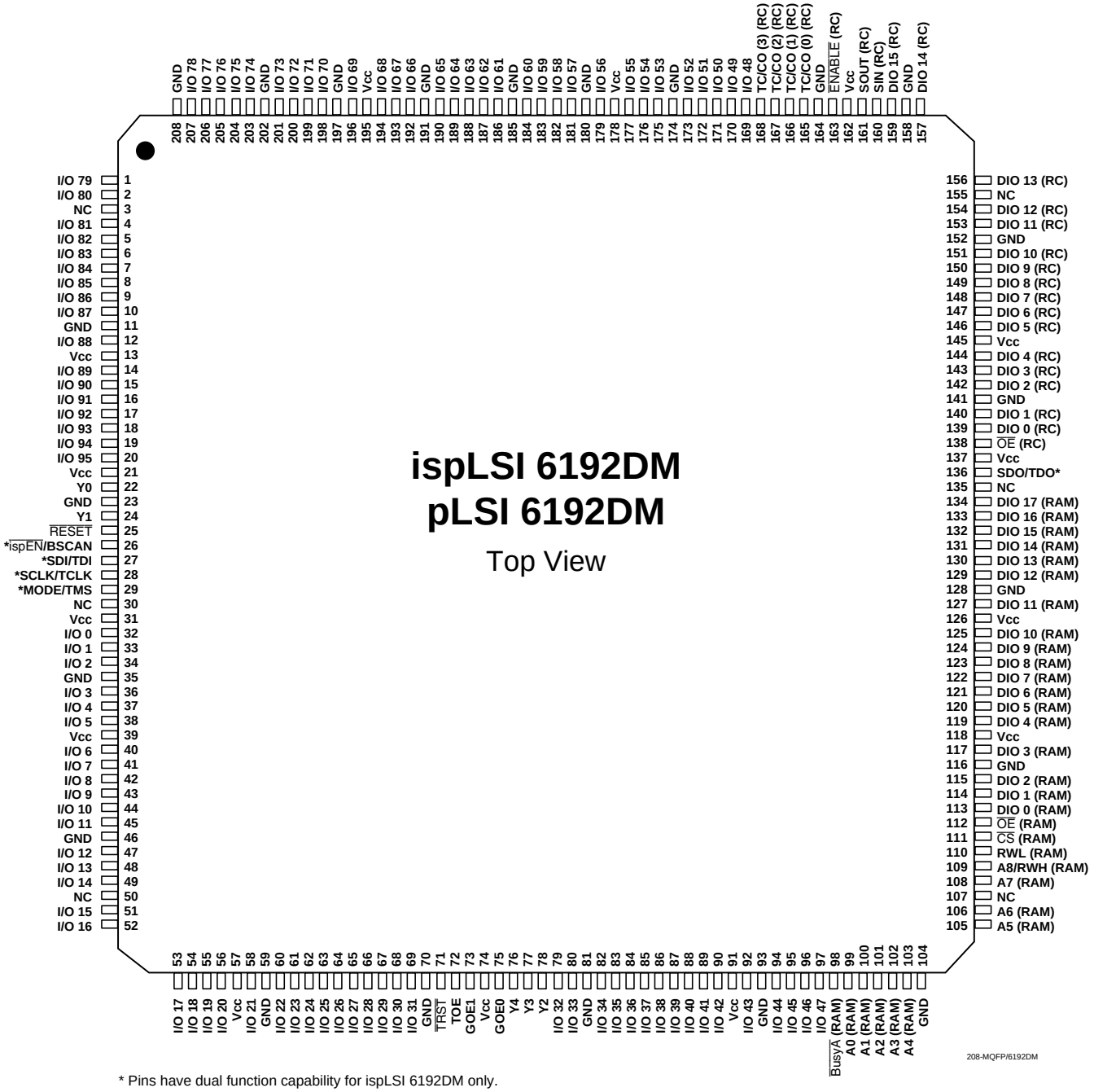
Table 2 - 0002/6192DP/SP

Pin Configuration: ispLSI and pLSI 6192FF



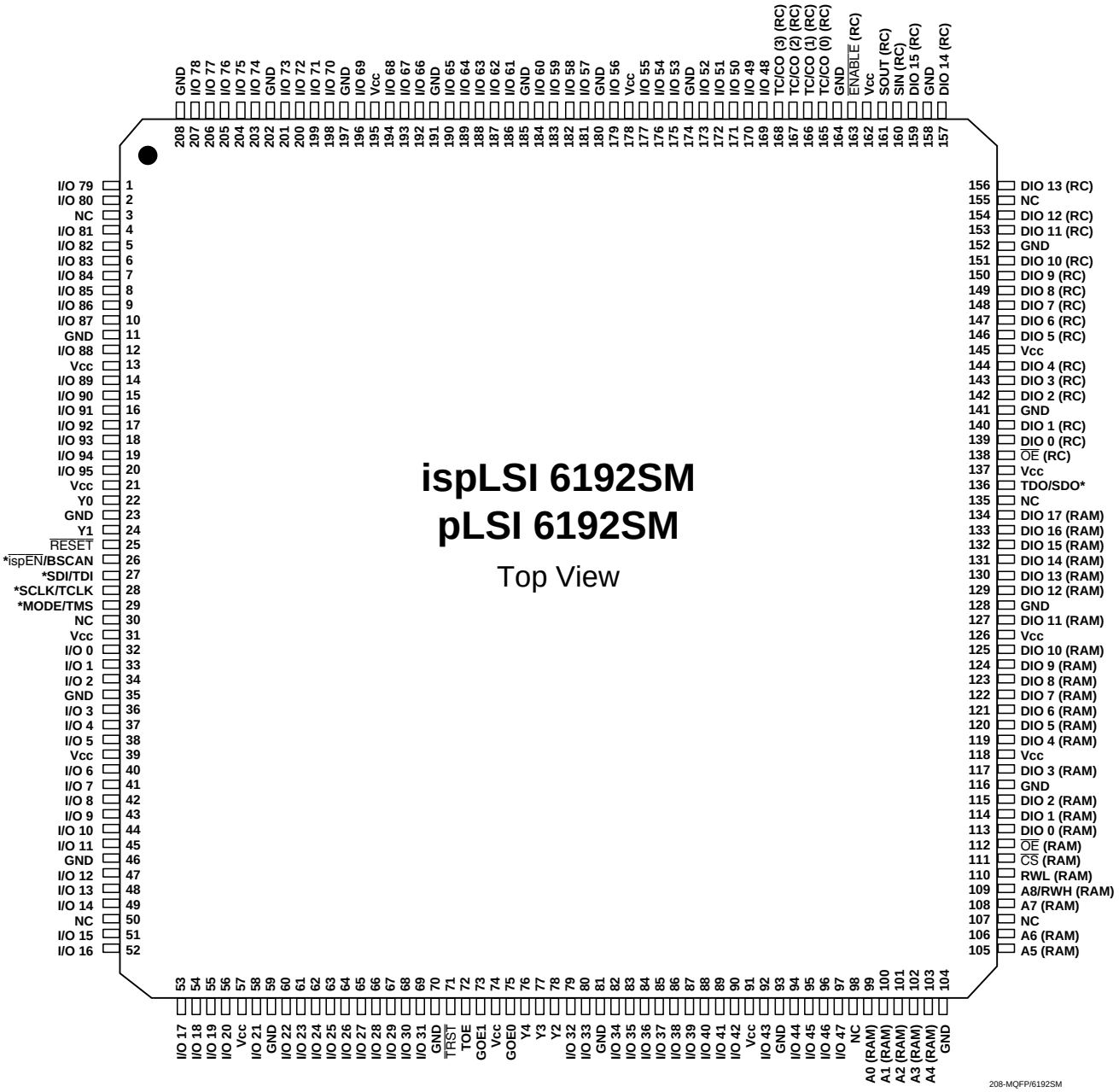
* Pins have dual function capability for ispLSI 6192FF only.

Pin Configuration: ispLSI and pLSI 6192DM



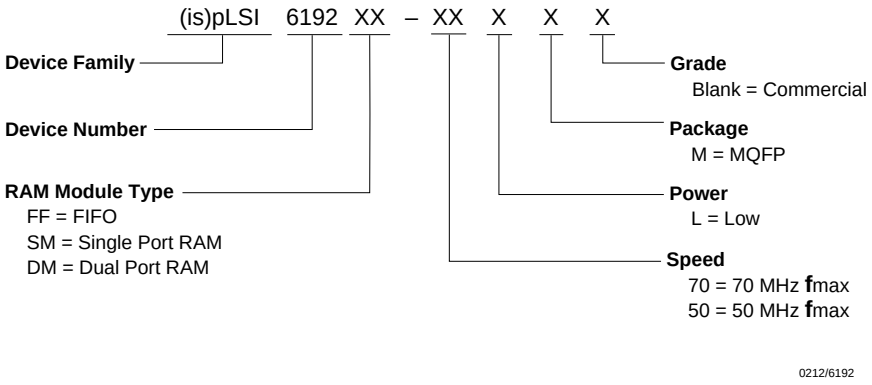
* Pins have dual function capability for ispLSI 6192DM only.

Pin Configuration: ispLSI and pLSI 6192DM



* Pins have dual function capability for ispLSI 6192SM only.

Part Number Description



Ordering Information

RAM Module	Family	fmax	tpd	Ordering Number	Package
FIFO	ispLSI	70	15	ispLSI 6192FF-70LM	208-Pin MQFP
		50	20	ispLSI 6192FF-50LM	208-Pin MQFP
	pLSI	70	15	pLSI 6192FF-70LM	208-Pin MQFP
		50	20	pLSI 6192FF-50LM	208-Pin MQFP
Single Port RAM	ispLSI	70	15	ispLSI 6192SM-70LM	208-Pin MQFP
		50	20	ispLSI 6192SM-50LM	208-Pin MQFP
	pLSI	70	15	pLSI 6192SM-70LM	208-Pin MQFP
		50	20	pLSI 6192SM-50LM	208-Pin MQFP
Dual Port RAM	ispLSI	70	15	ispLSI 6192DM-70LM	208-Pin MQFP
		50	20	ispLSI 6192DM-50LM	208-Pin MQFP
	pLSI	70	15	pLSI 6192DM-70LM	208-Pin MQFP
		50	20	pLSI 6192DM-50LM	208-Pin MQFP

Section 3

Introduction to Generic Array Logic

Overview

Lattice Semiconductor Corporation (LSC), the inventor of the Generic Array Logic™ (GAL®) family of low density, E^2CMOS® PLDs is the leading supplier of low density CMOS PLDs in the world. Features such as industry leading performance, full reprogrammability, low power consumption, 100% testability and 100% programming yields make the GAL family the preferred choice among system designers. The GAL family contains 16 product architectures with a variety of performance levels specified across commercial, industrial and military (MIL-STD-883) operating ranges to meet the demands of any system logic design.

A Product for Any System Design Need

Lattice Semiconductor GAL products have the performance, architectural features, low power, and high quality to meet the needs of the most demanding system designs.

Low Voltage Products

This rapidly growing family of 3.3V products support all speed, power and system logic level requirements. Included are the world's fastest PLDs (16LV8D, 20LV8D and 22LV10D) which are ideal for high performance, 3.3V logic applications, the "zero power" (16/20LV8ZD) and the "low power" (16LV8C, 22LV10C) product lines which offer the flexibility of working in mixed 3.3V and 5V systems.

Standard Products

Aimed at providing a superior design alternative to the bipolar PLD, the GAL16V8, GAL20V8, GAL22V10, GAL20RA10 and GAL20XV10 replace over 98% of all bipolar PAL devices. These GAL devices meet, and in most cases, beat bipolar PAL performance specifications while consuming significantly lower power and offering higher quality and reliability via LSC's electrically reprogrammable E^2CMOS technology.

Extension Products

These products provide enhanced functionality including innovative architecture (GAL18V10, GAL26CV12, GAL6001/6002), 64mA high output drive (GAL16VP8 and GAL20VP8), "zero power" operation (GAL16V8Z/ZD and GAL20V8Z/ZD), and in-system programmability (ispGAL22V10).

GAL16LV8 and GAL20LV8

Fastest 3.3V PLDs in the World

- Performance ranging from 3.5ns Tpd and 250MHz Fmax to 15ns Tpd and 62.5MHz Fmax
- Ideal for supporting high performance microprocessors
- 45 mA typical power consumption
- Available in 20-pin and 28-pin PLCC packages

GAL16LV8ZD and GAL20LV8ZD

3.3Volt and Zero Stand-by Power

- 50µA Icc typical stand-by power (100µA MAX)
- 15ns Tpd performance
- Dedicated power-down pin
- Available in 20-pin and 28-pin PLCC packages

GAL22LV10

Fastest 3.3V 22V10 in the World

- Performance from 4 ns Tpd and 250 MHz to 15 ns Tpd and 83 MHz Fmax
- Ideal for high performance systems
- Available in 28-pin PLCC package

GAL16V8 and GAL20V8

Industry Standard Architecture

- Performance ranges from the industry's fastest, at 5ns Tpd to popular 25ns versions
- Low power consumption with low power versions rated at 75mA typical and quarter power versions at 45mA typical
- Eight powerful Output Logic Macrocells (OLMCs) with eight product terms each
- Standard 20-pin (DIP and PLCC) and 24/28-pin (DIP/PLCC) packages

GAL16V8Z/ZD and GAL20V8Z/ZD

Zero Stand-by Power

- 50µA Icc typical stand-by power (100µA MAX)
- 12ns Tpd performance
- Two power-down modes
  - Input transition detection (Z)
  - Dedicated power-down pin (ZD)
- Available in 20-pin DIP/PLCC/SOIC and 24/28-pin DIP/PLCC packages

GAL16VP8 and GAL20VP8

Ideal for Bus Interface or Memory Control Logic

- High output drive versions of the GAL16V8 and GAL20V8
- IOL = 64mA vs standard 24mA
- Combines GAL architecture with high drive of 74XX244 buffer families
- Fast 15ns/80MHz performance
- Available in 20-pin DIP/PLCC and 24/28-pin DIP/PLCC packages

GAL18V10

10 Outputs in a 20-pin Package

- 7.5ns Tpd performance
- 20-pin space-saving subset of the popular GAL22V10
- 8-10 Product Terms per OLMC
- Ideal for space constrained designs
- Only 10 output, 20-pin PLD in the market

GAL20RA10

High Performance Asynchronous Logic

- 10 OLMCs
- 10 independently programmable clocks
- Each macrocell has an independent product term clock
- Fast 7.5ns Tpd performance
- Faster and lower power than bipolar PAL
- Available in 24/28-pin DIP/PLCC packages

GAL20XV10

Perfect for Fast Counters, Decoders or Comparators

- Utilizes powerful XOR function for efficient implementation of arithmetic functions
- Replaces: PAL20L10, 20X10, 20X8 and 20X4, 12L10
- 10ns/100MHz performance significantly outperforms bipolar PALs
- Perfect for video, multimedia and graphics applications
- Available in 24/28-pin DIP/PLCC packages

GAL22V10

Industry Standard Architecture

- Available in industry leading 5ns/200MHz versions through 25ns versions
- Low power consumption with Low Power versions at 90mA and Quarter Power versions at 45mA typical
- 10 OLMCs with variable Product Terms per OLMC ranging from 8 to 16 for increased logic capability
- Standard 24-pin DIP and 28-pin PLCC packages

ispGAL22V10

Offers the Benefits of ISP in a 22V10

- Popular 22V10 architecture
- In-system programmable
- Same 28-pin PLCC footprint as GAL22V10
- Fast 7.5ns/111MHz performance
- Unprecedented design and manufacturing flexibility

GAL26CV12

Expanded Logic Density in a 28-pin DIP/PLCC Package

- 28-pin superset of the popular GAL22V10
- World's fastest 28-pin PLD at 7.5ns
- 26 inputs, 12 outputs
- Flexible 22V10 OLMC
- Fully utilized 28-pin PLCC package gives added functionality over the 22V10 at no space premium!

GAL6001 and GAL6002

The Logic Density of an FPLA Architecture

- Unprecedented logic density in a 24/28-pin DIP/PLCC
- Functional equivalent of two GAL22V10s
- 38 macrocells
  - 10 input macrocells
  - 10 output macrocells
  - 10 I/O macrocells
  - 8 buried logic macrocells
- 15ns/75MHz performance
- Ideal for register-intensive applications

Commercial/Industrial/Military Grades Available

The Lattice Semiconductor GAL family is available in a wide range of commercial, industrial and military grade versions. In the military arena, LSC offers a MIL-STD-883 family as well as a family of Standard Military Drawing (SMD) devices.

Table 1. Lattice Semiconductor Corporation's GAL Product Offering

		Speed Options by Grade (Tpd in ns)		
		Commercial	**Industrial**	**883/Military**
3.3V Products	**GAL16LV8**	3.5, 5, 7.5, 10, 15		
	GAL16LV8ZD Zero Power	15, 25		
	GAL20LV8	3.5, 5, 7.5		
	GAL20LV8ZD Zero Power	15, 25		
	GAL22LV10	4, 5, 7.5, 10, 15		
5V Products	**GAL16V8Z/ZD Zero Power**	12, 15		
	GAL16V8 Low Power	5, 7.5, 10, 15, 25	7.5, 10, 15, 25	7.5, 10, 15, 20, 30
	GAL16V8 Quarter Power	15, 25	20, 25	
	GAL16VP8	15, 25		
	GAL18V10	7.5, 10, 15, 20		
	GAL20RA10	7.5, 10, 15, 20, 30	20	
	GAL20V8Z/ZD Zero Power	12, 15		
	GAL20V8 Low Power	5, 7.5, 10, 15, 25	10, 15, 25	10, 15, 20
	GAL20V8 Quarter Power	15, 25	20, 25	
	GAL20VP8	15, 25		
	GAL20XV10	10, 15, 20		
	GAL22V10 Low Power	5, 7.5, 10, 15, 25	7.5, 10, 15, 20, 25	10, 15, 20, 25, 30
	GAL22V10 Quarter Power	15, 25		
	ispGAL22V10	7.5, 10, 15	15	
	GAL26CV12	7.5, 10, 15, 20	10, 15, 20	
	GAL6001	30		
	GAL6002	15, 20		
	Vcc (3.3V Products)	3.3V ±10%		
	Vcc (5V Products)	5V ±5%	5V ±10%	5V ±10%
	Operating Temperature	0 to 75°C	-40 to 85°C	-55 to 125°C
	Packaging	Plastic DIP, PLCC and SOIC*	Plastic DIP and PLCC	CERDIP and LCC

* SOIC available with GAL16V8Z only.

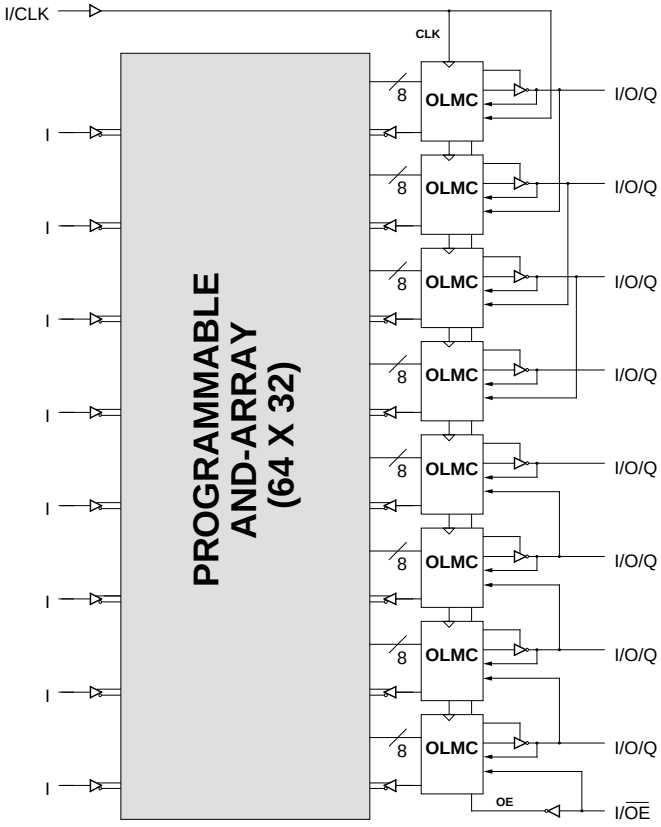
GAL16LV8

Low Voltage E²CMOS PLD Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 3.5 ns Maximum Propagation Delay**
  - **— Fmax = 250 MHz**
  - **— 2.5 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **3.3V LOW VOLTAGE 16V8 ARCHITECTURE**
  - **— JEDEC-Compatible 3.3V Interface Standard**
  - **— Interfaces with Standard 5V TTL Devices (GAL16LV8C)**
- **ACTIVE PULL-UPS ON ALL PINS (GAL16LV8D Only)**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— Glue Logic for 3.3V Systems**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

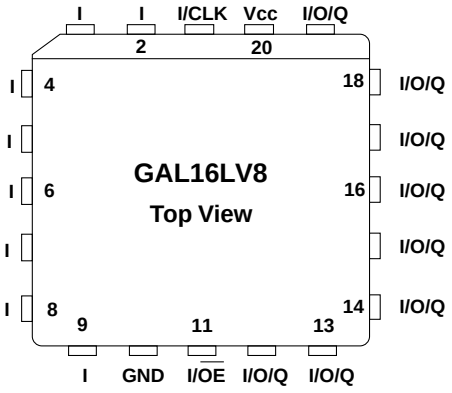
The GAL16LV8D, at 3.5 ns maximum propagation delay time, provides the highest speed performance available in the PLD market. The GAL16LV8C can interface with both 3.3V and 5V signal levels. The GAL16LV8 is manufactured using Lattice Semiconductor's advanced 3.3V E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The 3.3V GAL16LV8 uses the same industry standard 16V8 architecture as its 5V counterpart and supports all architectural features such as combinatorial or registered macrocell operations.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

PIN CONFIGURATION

PLCC



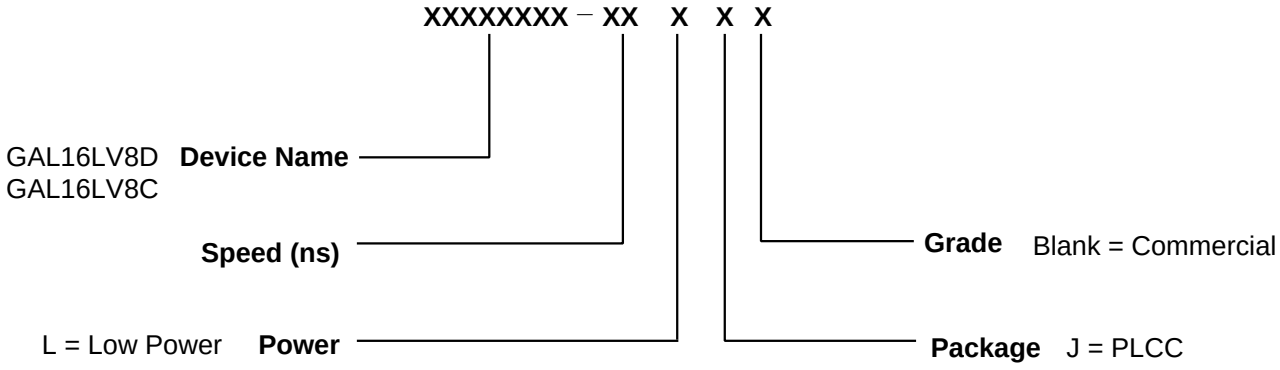
LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL16LV8 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
3.5	3	2.5	70	GAL16LV8D-3LJ	20-Lead PLCC
5	4	3	70	GAL16LV8D-5LJ	20-Lead PLCC
7.5	6	5	65	GAL16LV8C-7LJ	20-Lead PLCC
10	7	7	65	GAL16LV8C-10LJ	20-Lead PLCC
15	12	10	65	GAL16LV8C-15LJ	20-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes are illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL16LV8. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL16LV8 can emulate. It also shows the OLMC mode under which the GAL16LV8 emulates the PAL architecture.

PAL Architectures Emulated by GAL16LV8	GAL16LV8 Global OLMC Mode
16R8	**Registered**
16R6	**Registered**
16R4	**Registered**
16RP8	**Registered**
16RP6	**Registered**
16RP4	**Registered**
16L8	**Complex**
16H8	**Complex**
16P8	**Complex**
10L8	**Simple**
12L6	**Simple**
14L4	**Simple**
16L2	**Simple**
10H8	**Simple**
12H6	**Simple**
14H4	**Simple**
16H2	**Simple**
10P8	**Simple**
12P6	**Simple**
14P4	**Simple**
16P2	**Simple**

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL16V8A
PLDesigner	P16V8R[2]	P16V8C[2]	P16V8C[2]	P16V8A
TANGO-PLD	G16V8R	G16V8C	G16V8AS[3]	G16V8

1) Used with **Configuration** keyword.
2) Prior to Version 2.0 support.
3) Supported on Version 1.20 or later.

REGISTERED MODE

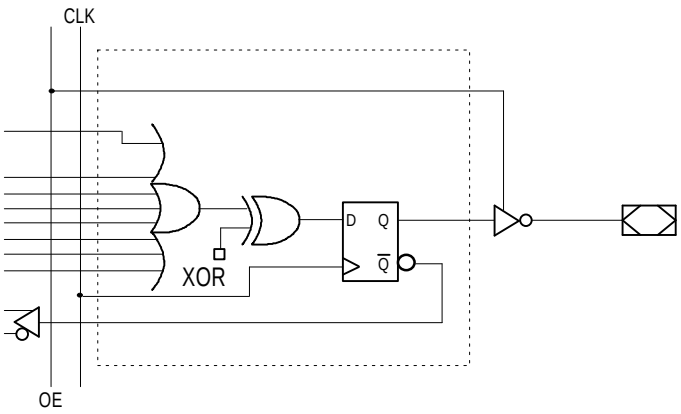
In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

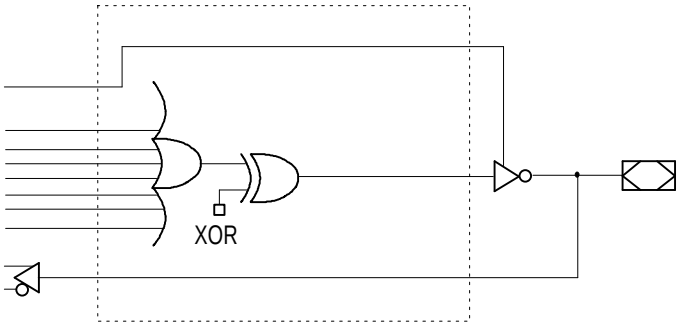
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 11 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$.



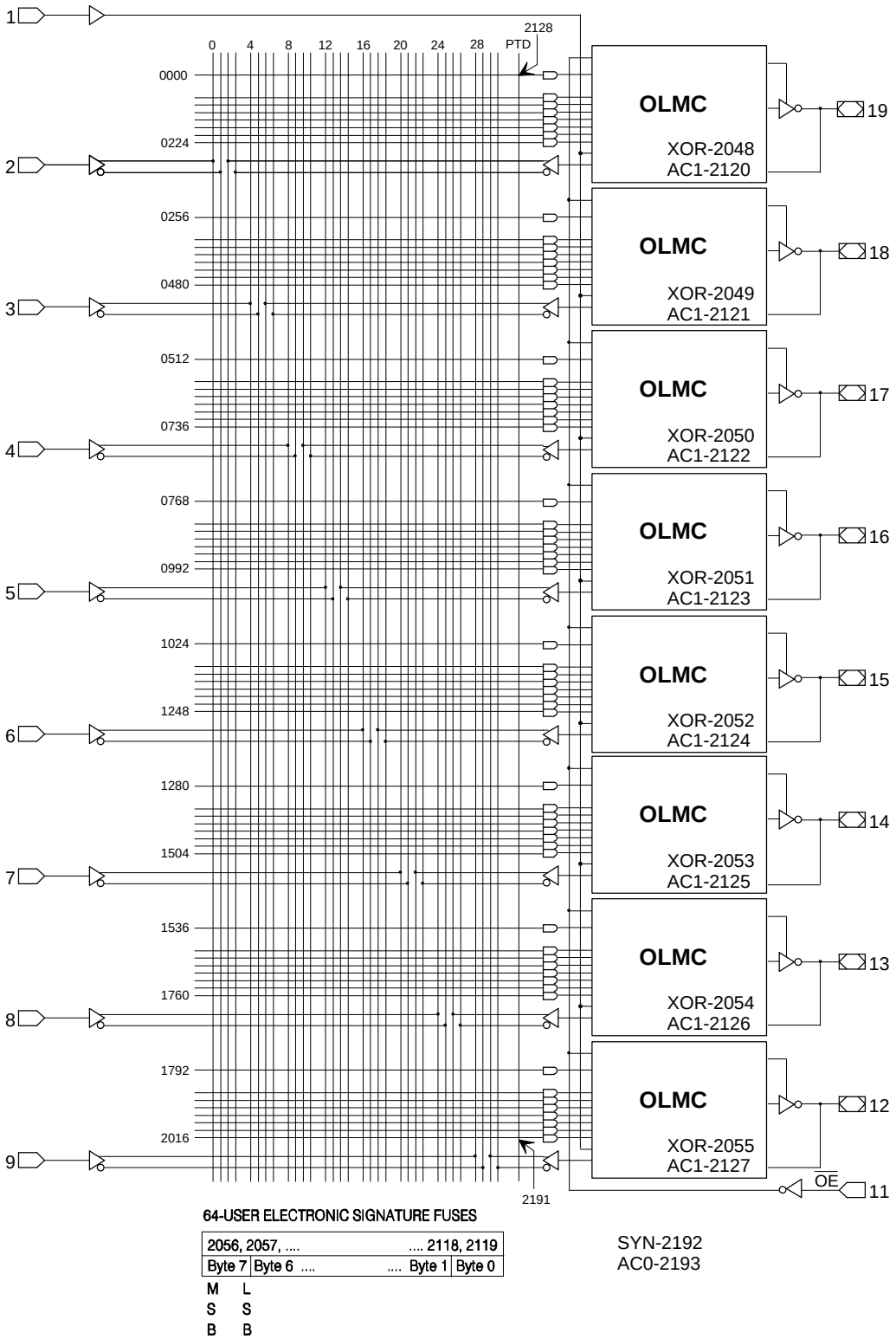
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

PLCC Package Pinout



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...	.... 2118, 2119
Byte 7	Byte 6 .... Byte 1	Byte 0

MSB LSB

SYN-2192
AC0-2193

COMPLEX MODE

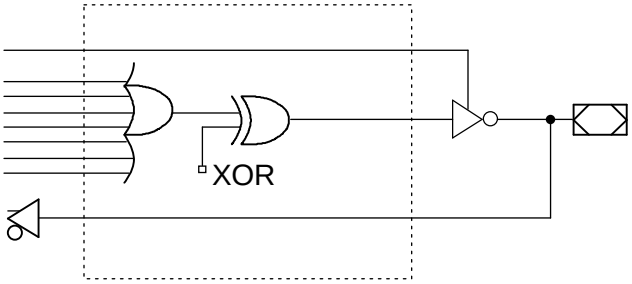
In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 12 & 19) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

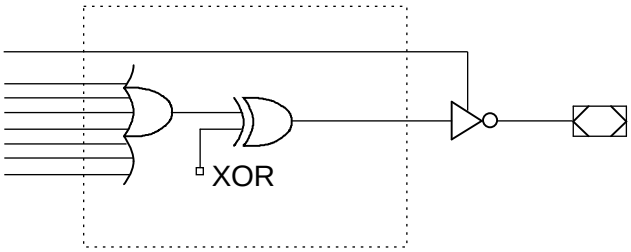
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 11 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 13 through Pin 18 are configured to this function.



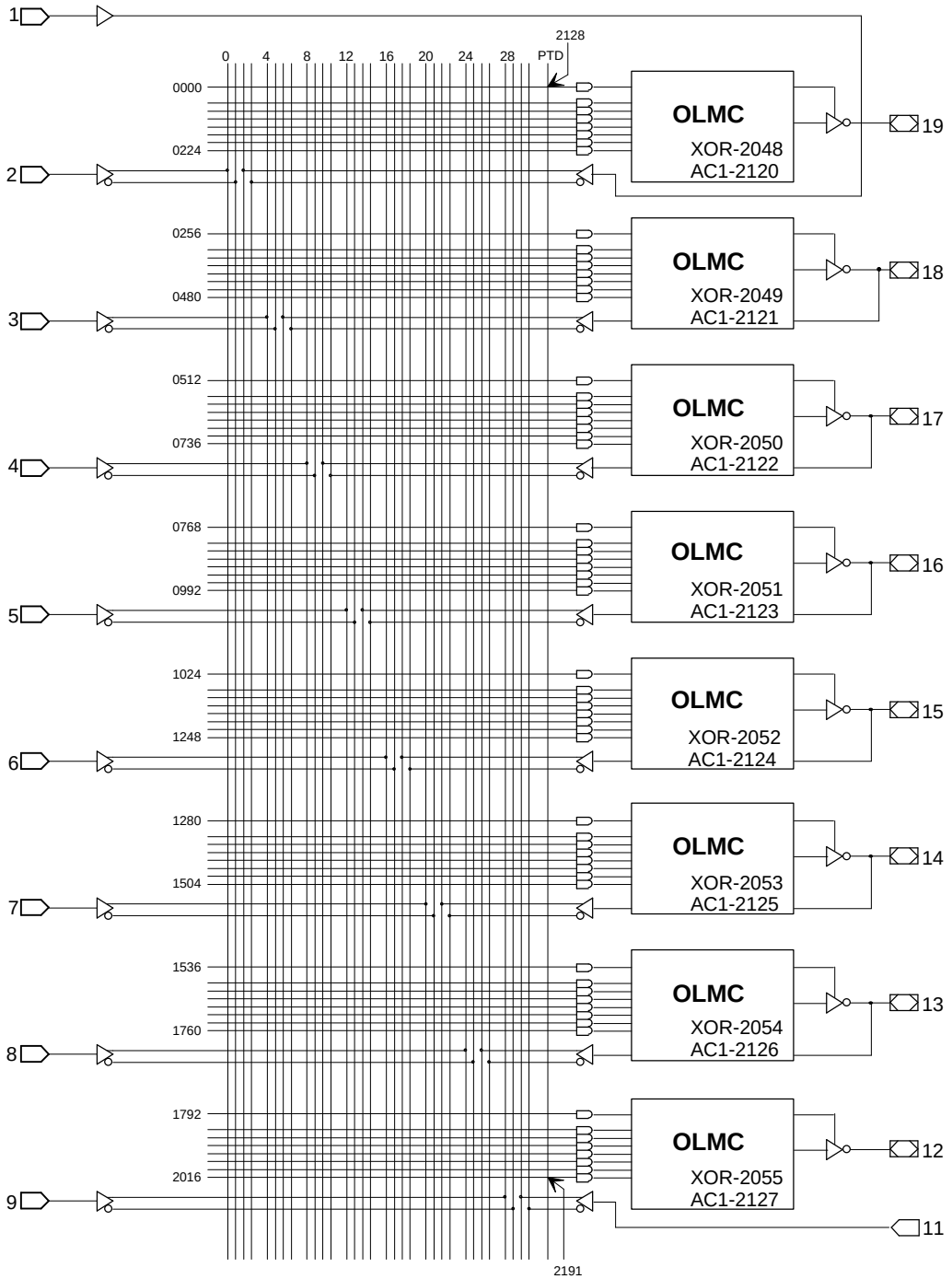
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 12 and Pin 19 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

PLCC Package Pinout



SIMPLE MODE

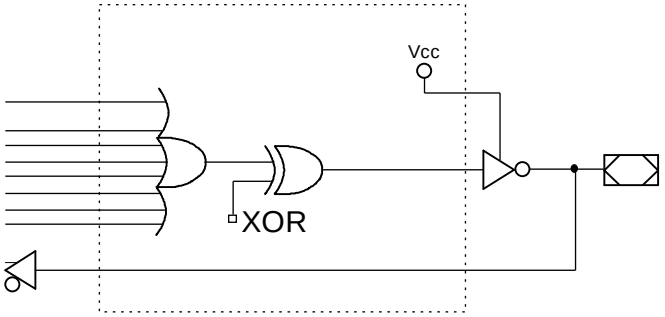
In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

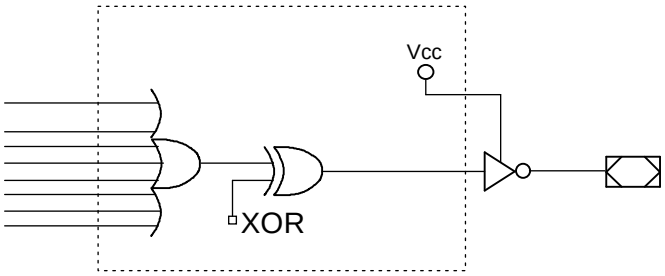
Pins 1 and 11 are always available as data inputs into the AND array. The center two macrocells (pins 15 & 16) cannot be used as input or I/O pins, and are only available as dedicated outputs.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



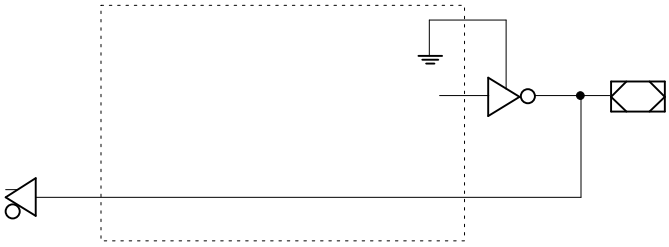
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 15 & 16 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 15 & 16 are permanently configured to this function.



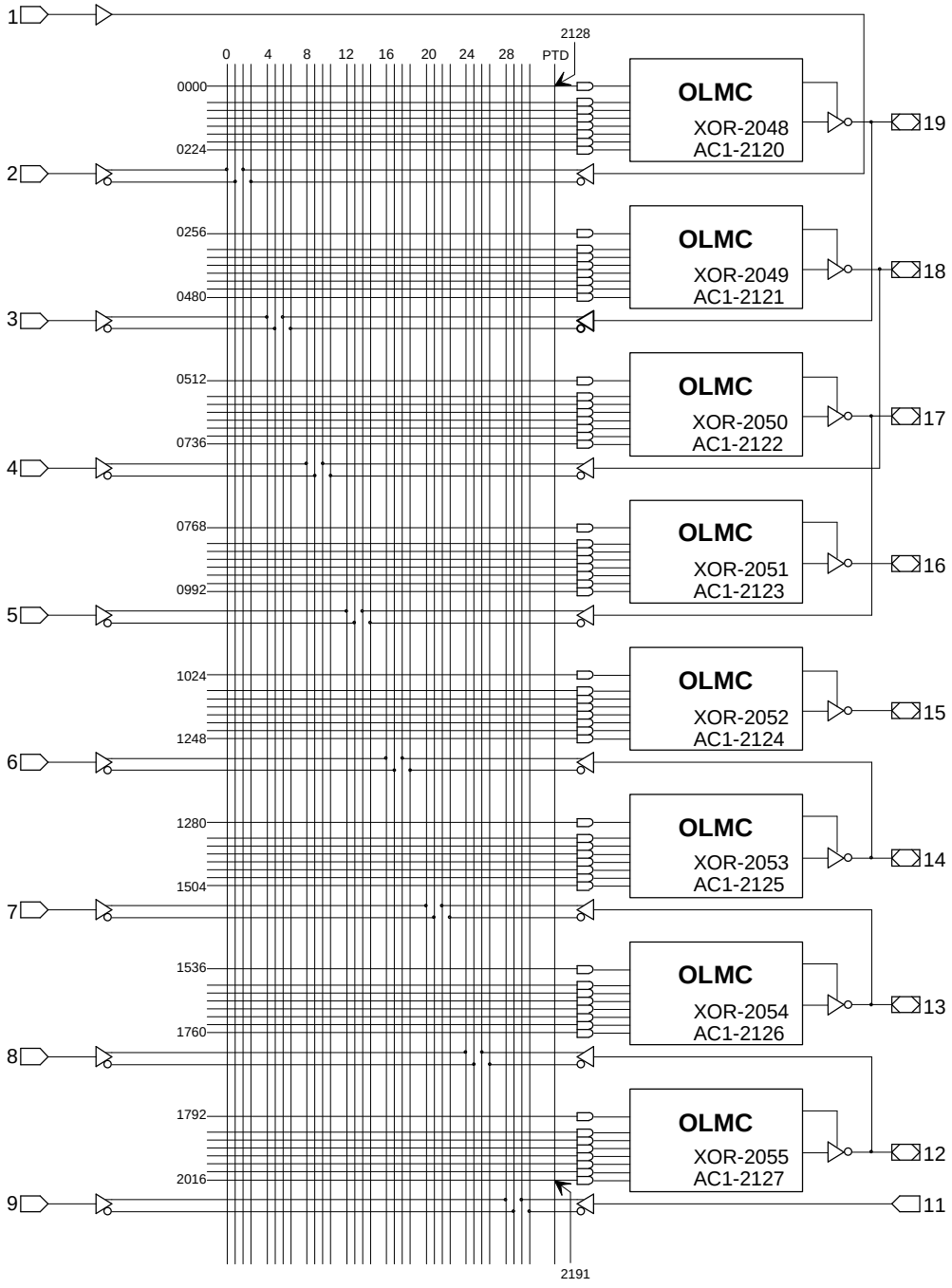
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 15 & 16 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

PLCC Package Pinout



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...			.... 2118, 2119
Byte 7	Byte 6	.... Byte 1	Byte 0

MSB LSB

SYN-2192
AC0-2193

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +4.6V
Input voltage applied ..... –0.5 to +4.6V
Off-state output voltage applied ..... –0.5 to +4.6V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.3	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+0.5	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$(Vcc\text{-}0.2)V \le V_{IN} \le V_{CC}$	—	—	10	µA
		$Vcc \le V_{IN} \le 4.6V$	—	—	20	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.4	V
		I_{OL} = 500µA Vin = V_{IL} or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -100µA Vin = V_{IL} or V_{IH}	Vcc-0.2V	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	–8	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = 0.5V T_A = 25°C	–15	—	–80	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0V V_{IH} = 3.0V Unused Inputs at V_{IL} f_{toggle} = 1MHz Outputs Open	—	45	70	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 3.3V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -3 MIN.	COM -3 MAX.	COM -5 MIN.	COM -5 MAX.	UNITS
tpd[2]	A	Input or I/O to Combinational Output	1	3.5	1	5	ns
tco[2]	A	Clock to Output Delay	1	2.5	1	3	ns
tcf[3]	—	Clock to Feedback Delay	—	2	—	2	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	3	—	4	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[4]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	180	—	142.8	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	200	—	166	—	MHz
	A	Maximum Clock Frequency with No Feedback	250	—	166	—	MHz
twh[4]	—	Clock Pulse Duration, High	2	—	3	—	ns
twl[4]	—	Clock Pulse Duration, Low	2	—	3	—	ns
ten	B	Input or I/O to Output Enabled	—	4.5	—	6	ns
	B	$\overline{OE}$ to Output Enabled	—	3.5	—	5	ns
tdis	C	Input or I/O to Output Disabled	—	4.5	—	6	ns
	C	$\overline{OE}$ to Output Disabled	—	3.5	—	5	ns

1) Refer to Switching Test Conditions section.
2) Minimum values for tpd and tco are not 100% tested but established by characterization.
3) Calculated from fmax with internal feedback. Refer to fmax Descriptions section.
4) Refer to fmax Descriptions section. Guaranteed by characterization.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TYPICAL*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	5	pF	V_{CC} = 3.3V, V_I = 0V
$C_{I/O}$	I/O Capacitance	5	pF	V_{CC} = 3.3V, $V_{I/O}$ = 0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +5.6V
Input voltage applied ..... –0.5 to +5.6V
Off-state output voltage applied ..... –0.5 to +5.6V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	5.25	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CC} - 0.2)V \le V_{IN} \le V_{CC}$	—	—	10	µA
		$V_{CC} \le V_{IN} \le 5.25V$	—	—	30	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.4	V
		I_{OL} = 500 µA Vin = V_{IL} or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -500 µA Vin = V_{IL} or V_{IH}	Vcc-0.45	—	—	V
		I_{OH} = -100 µA Vin = V_{IL} or V_{IH}	Vcc-0.2	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-4	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = 0.5V T_A = 25°C	-10	—	-60	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.0V V_{IH} = 3.0V f_{toggle} = 1MHz Outputs Open	—	45	65	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 3.3V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -7		COM -10		COM -15		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd[2]	A	Input or I/O to Combinational Output	1	7.5	1	10	1	15	ns
tco[2]	A	Clock to Output Delay	1	5	1	7	1	10	ns
tcf[3]	—	Clock to Feedback Delay	—	4	—	5	—	8	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	6	—	7	—	12	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
fmax[4]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	90.9	—	71.4	—	45.5	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	100	—	83.3	—	50	—	MHz
	A	Maximum Clock Frequency with No Feedback	100	—	83.3	—	62.5	—	MHz
twh	—	Clock Pulse Duration, High	5	—	6	—	8	—	ns
twl	—	Clock Pulse Duration, Low	5	—	6	—	8	—	ns
ten	B	Input or I/O to Output Enabled	—	9	—	10	—	15	ns
	B	$\overline{OE}$ to Output Enabled	—	6	—	8	—	15	ns
tdis	C	Input or I/O to Output Disabled	—	9	—	10	—	15	ns
	C	$\overline{OE}$ to Output Disabled	—	6	—	8	—	15	ns

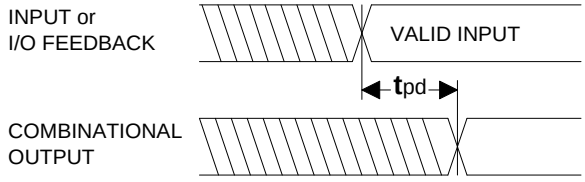
1) Refer to Switching Test Conditions section.
2) Minimum values for **t**pd and **t**co are not 100% tested but established by characterization.
3) Calculated from **f**max with internal feedback. Refer to fmax Descriptions section.
4) Refer to fmax Descriptions section. Guaranteed by characterization.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

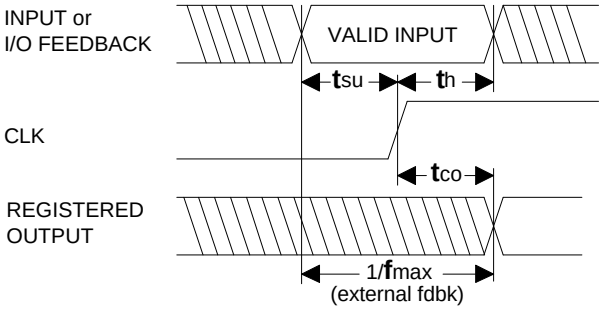
SYMBOL	PARAMETER	TYPICAL*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 3.3V, V_I = 0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 3.3V, $V_{I/O}$ = 0V

*Guaranteed but not 100% tested.

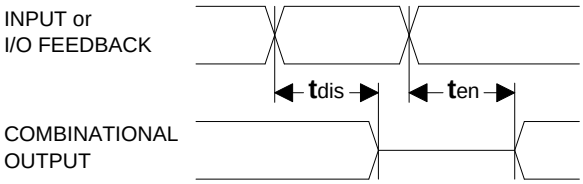
SWITCHING WAVEFORMS



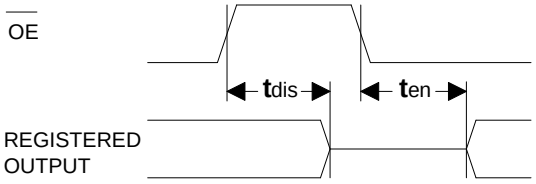
Combinatorial Output



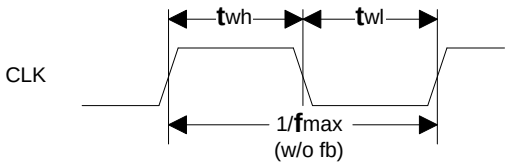
Registered Output



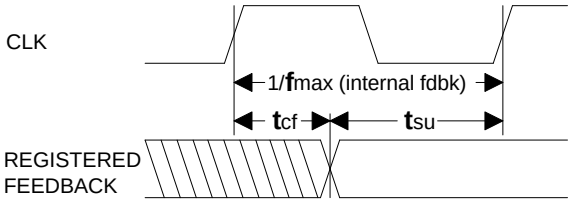
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

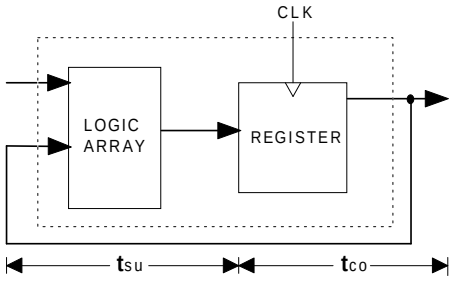


Clock Width



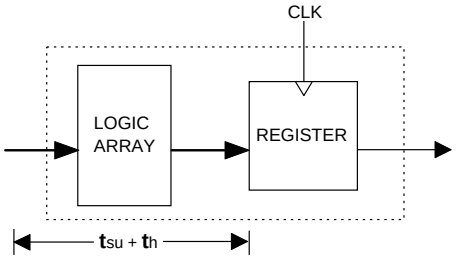
fmax with Feedback

fmax DESCRIPTIONS



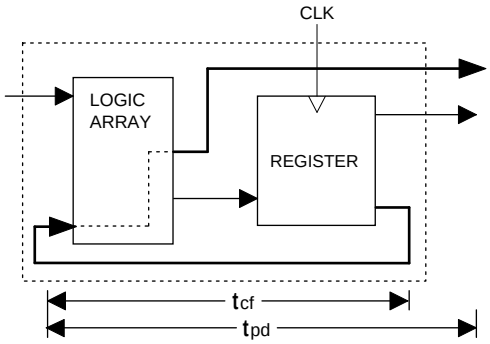
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

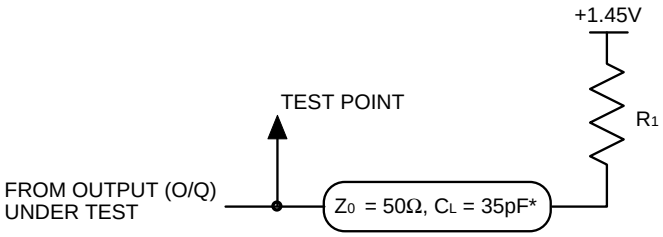
Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

GAL16LV8D: SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	1.5ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

GAL16LV8D Output Load Conditions (see figure)

Test Condition		R_1	C_L
A		50Ω	35pF
B	High Z to Active High at 1.9V	50Ω	35pF
	High Z to Active Low at 1.0V	50Ω	35pF
C	Active High to High Z at 1.9V	50Ω	35pF
	Active Low to High Z at 1.0V	50Ω	35pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

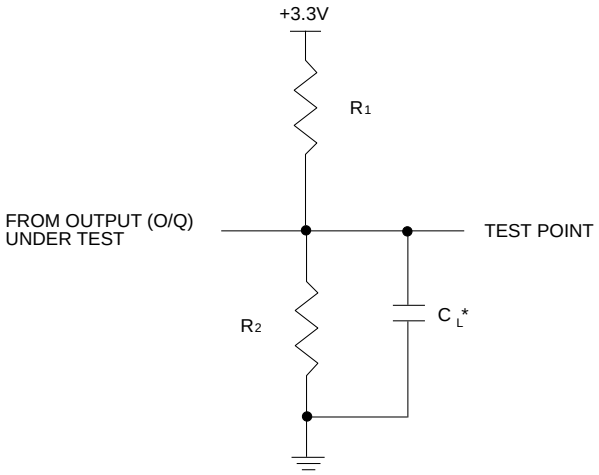
GAL16LV8C: SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	1.5ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

GAL16LV8C Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		316Ω	348Ω	35pF
B	Active High	316Ω	348Ω	35pF
	Active Low	316Ω	348Ω	35pF
C	Active High	316Ω	348Ω	5pF
	Active Low	316Ω	348Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL16LV8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

SECURITY CELL

A security cell is provided in the GAL16LV8 devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL16LV8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias minimizes the potential of latch-up caused by negative input undershoots.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

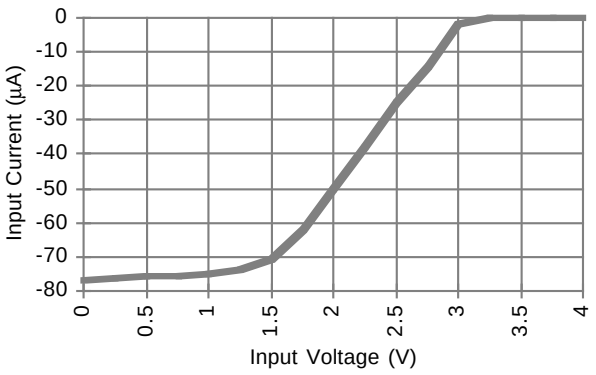
GAL16LV8 devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

INPUT BUFFERS

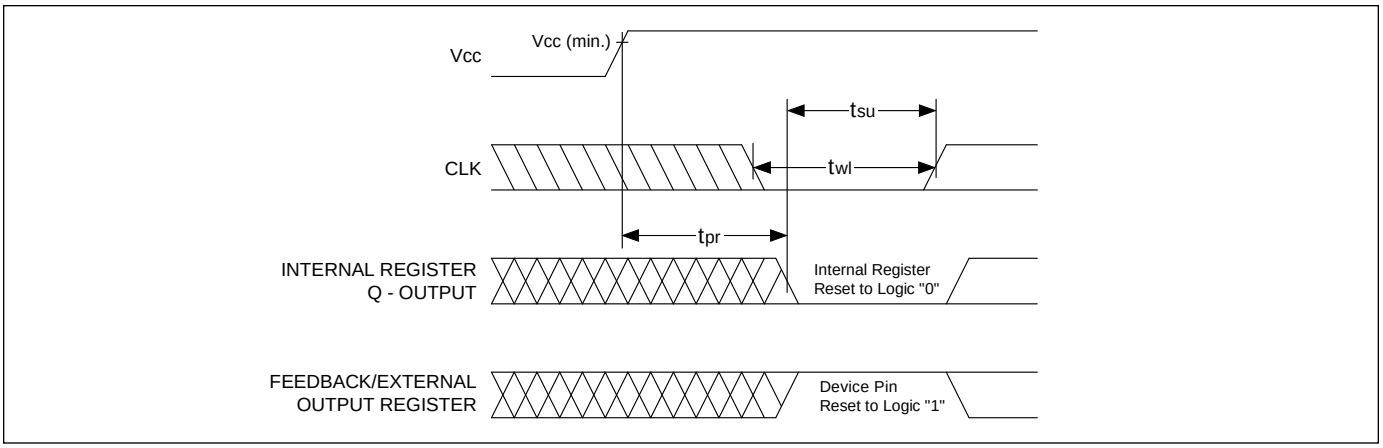
GAL16LV8 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL16LV8D input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or Ground. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Pull-up Characteristic (GAL16LV8D)

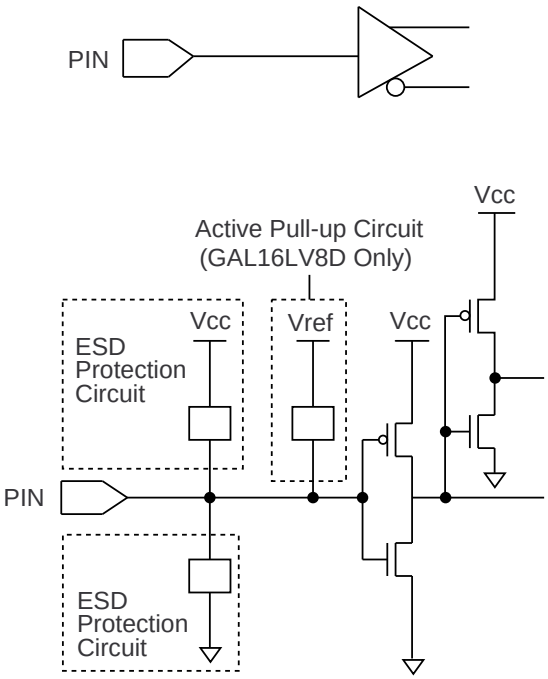


POWER-UP RESET



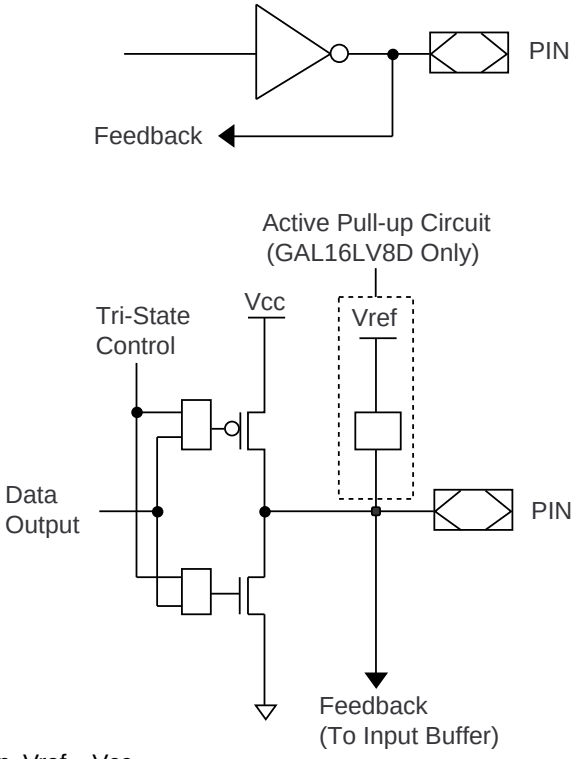
Circuitry within the GAL16LV8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr}, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the device. First, the V_{CC} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typ. Vref = Vcc

Typical Input

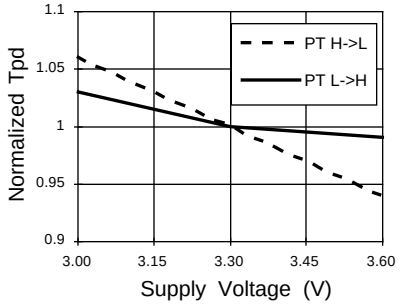


Typ. Vref = Vcc

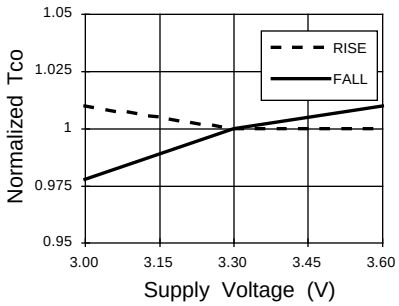
Typical Output

GAL16LV8D: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

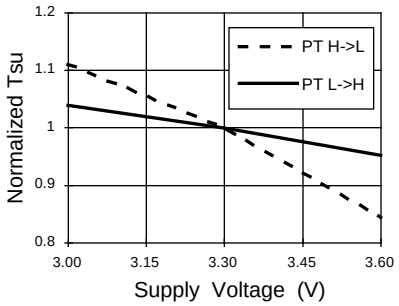
Normalized Tpd vs Vcc



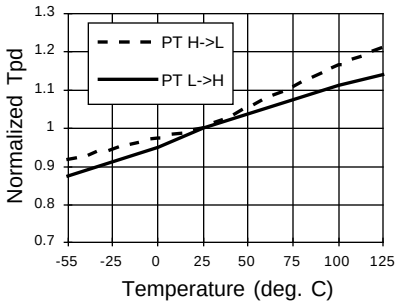
Normalized Tco vs Vcc



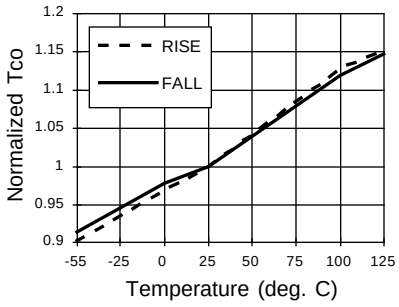
Normalized Tsu vs Vcc



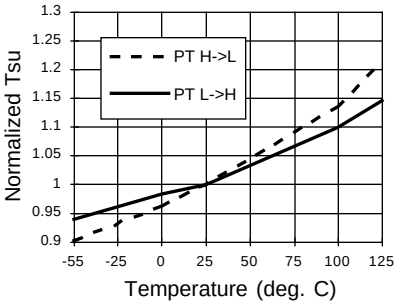
Normalized Tpd vs Temp



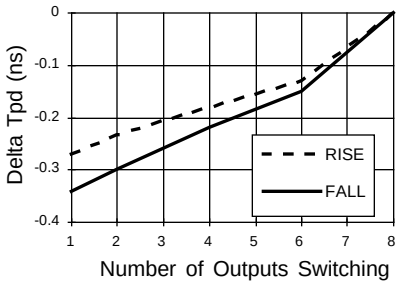
Normalized Tco vs Temp



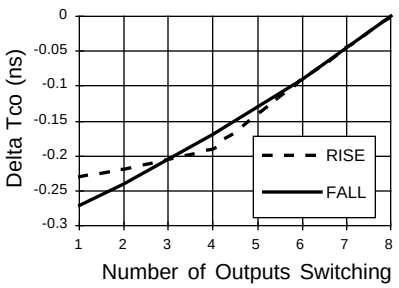
Normalized Tsu vs Temp



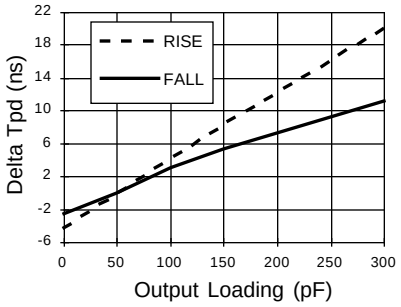
Delta Tpd vs # of Outputs Switching



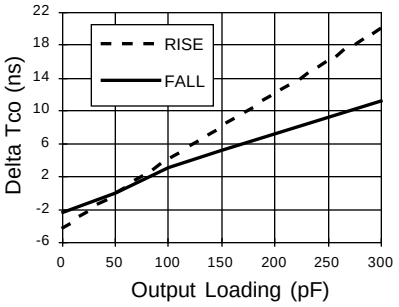
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

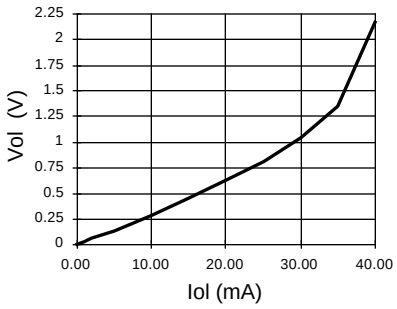


Delta Tco vs Output Loading

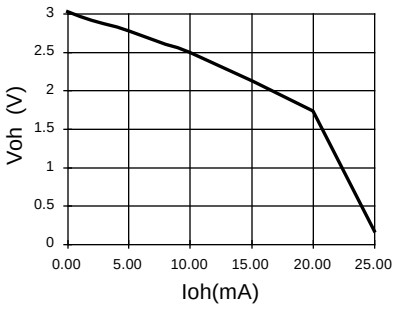


GAL16LV8D: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

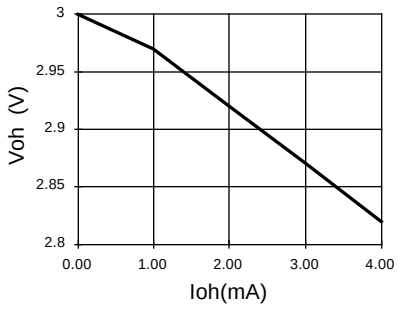
Vol vs Iol



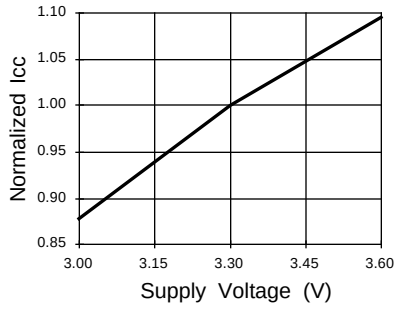
Voh vs Ioh



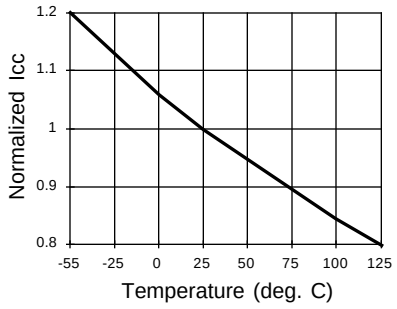
Voh vs Ioh



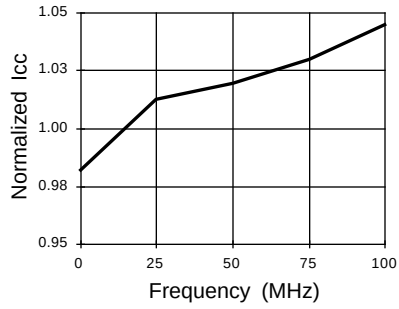
Normalized Icc vs Vcc



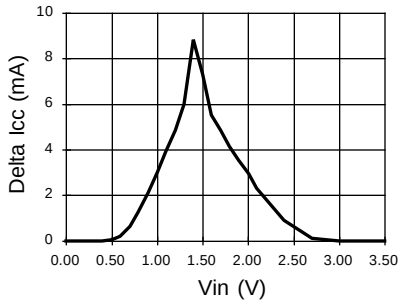
Normalized Icc vs Temp



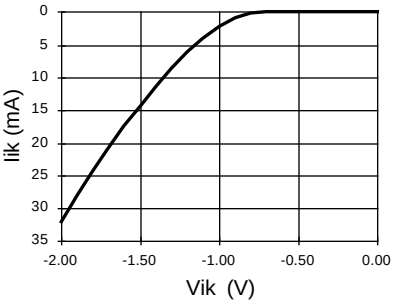
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

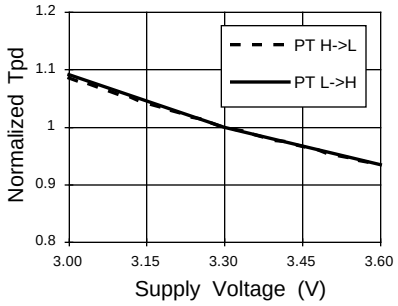


Input Clamp (Vik)

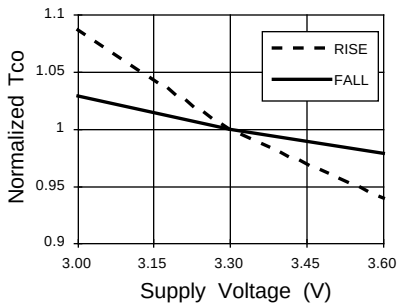


GAL16LV8C: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

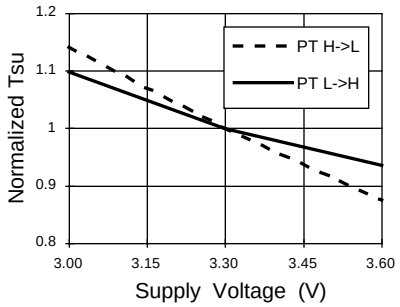
Normalized Tpd vs Vcc



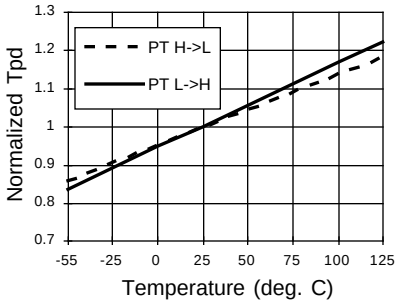
Normalized Tco vs Vcc



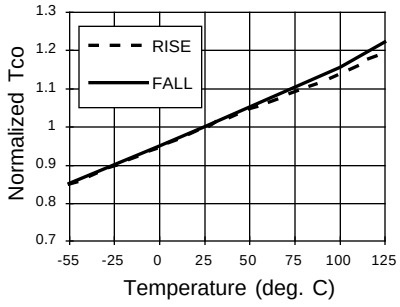
Normalized Tsu vs Vcc



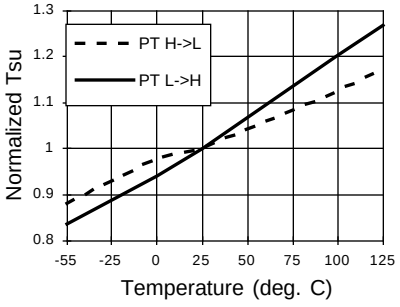
Normalized Tpd vs Temp



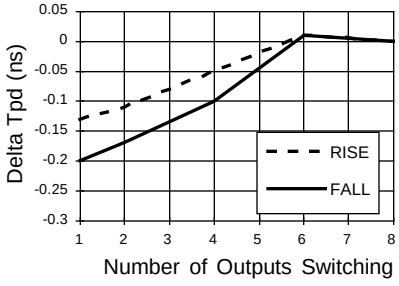
Normalized Tco vs Temp



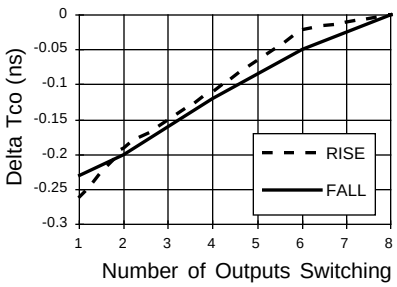
Normalized Tsu vs Temp



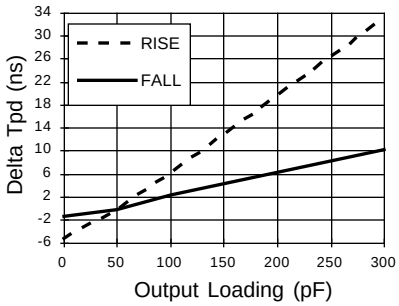
Delta Tpd vs # of Outputs Switching



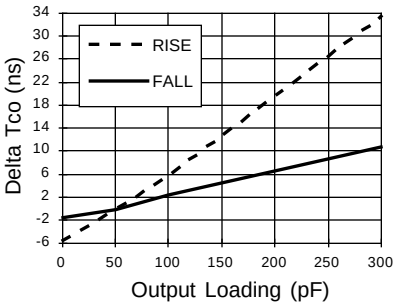
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

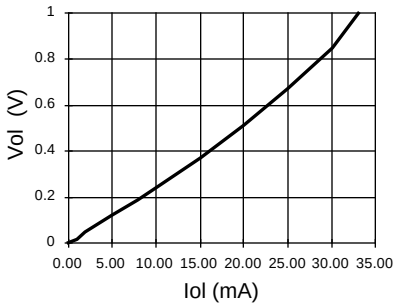


Delta Tco vs Output Loading

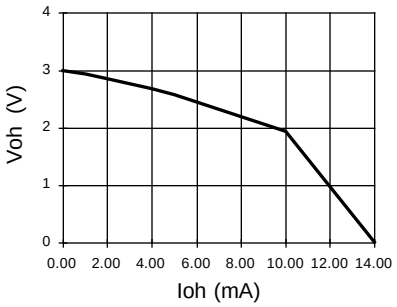


GAL16LV8C: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

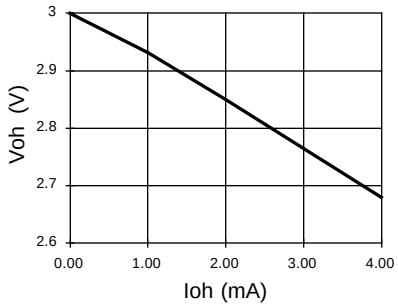
Vol vs Iol



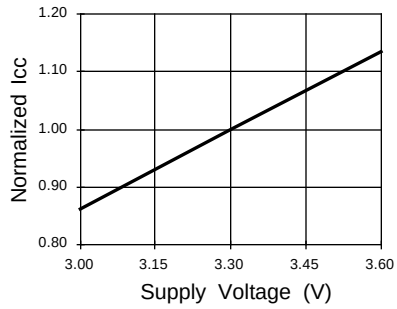
Voh vs Ioh



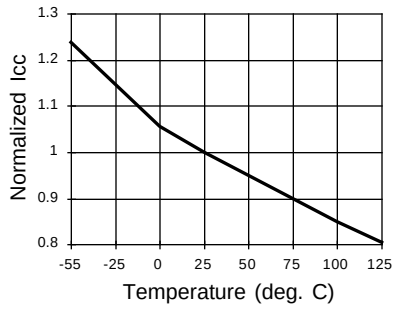
Voh vs Ioh



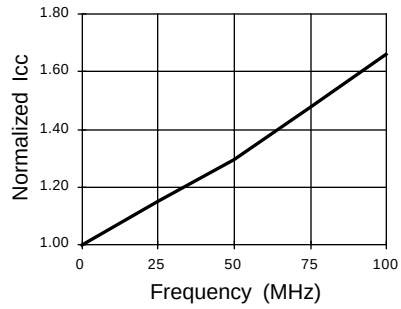
Normalized Icc vs Vcc



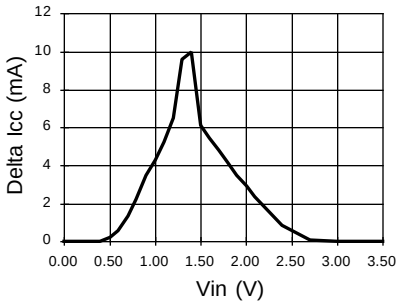
Normalized Icc vs Temp



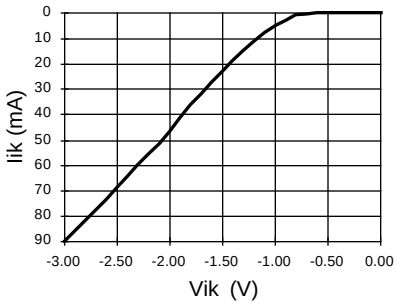
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



GAL16LV8ZD

Low Voltage, Zero Power E²CMOS PLD
Generic Array Logic™

FEATURES

- **3.3V LOW VOLTAGE, ZERO POWER OPERATION**
  - **— JEDEC Compatible 3.3V Interface Standard**
  - **— Interfaces with Standard 5V TTL Devices**
  - **— 50μA Typical Standby Current (100μA Max.)**
  - **— 45mA Typical Active Current (55mA Max.)**
  - **— Dedicated Power-down Pin**
- **HIGH PERFORMANCE E²CMOS TECHNOLOGY**
  - **— TTL Compatible Balanced 8 mA Output Drive**
  - **— 15 ns Maximum Propagation Delay**
  - **— Fmax = 62.5 MHz**
  - **— 10 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— Glue Logic for 3.3V Systems**
  - **— Ideal for Mixed 3.3V and 5V Systems**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

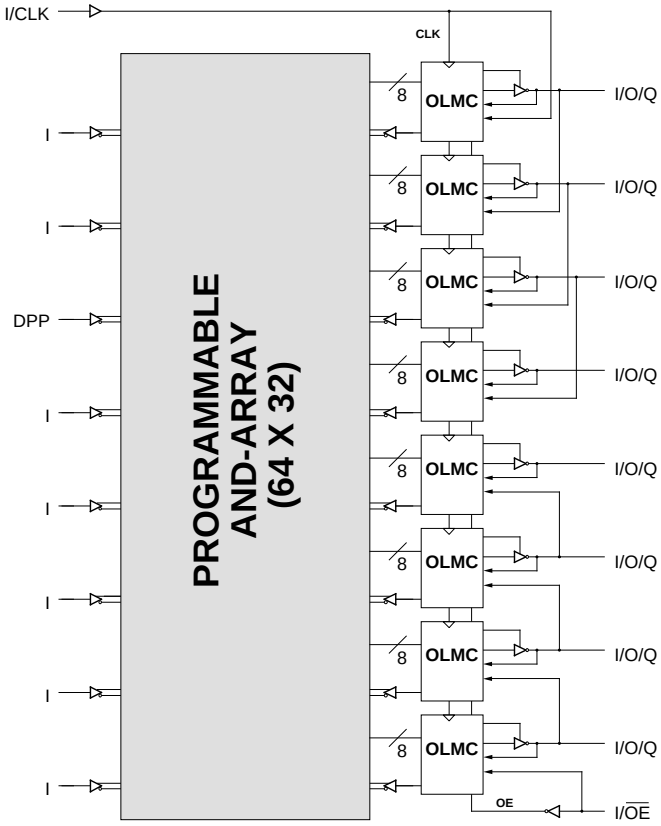
DESCRIPTION

The GAL16LV8ZD, at 100 μA standby current and 15ns propagation delay provides the highest speed low-voltage PLD available in the market. The GAL16LV8ZD is manufactured using Lattice Semiconductor's advanced 3.3V E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology.

The GAL16LV8ZD utilizes a dedicated power-down pin (DPP) to put the device into standby mode. It has 15 inputs available to the AND array and is capable of interfacing with both 3.3V and standard 5V devices.

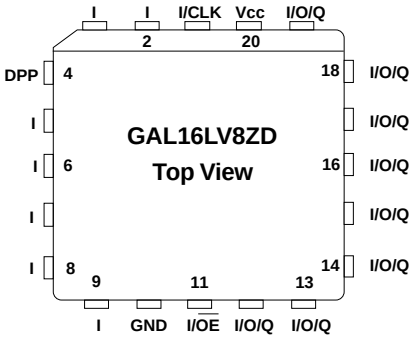
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

PLCC



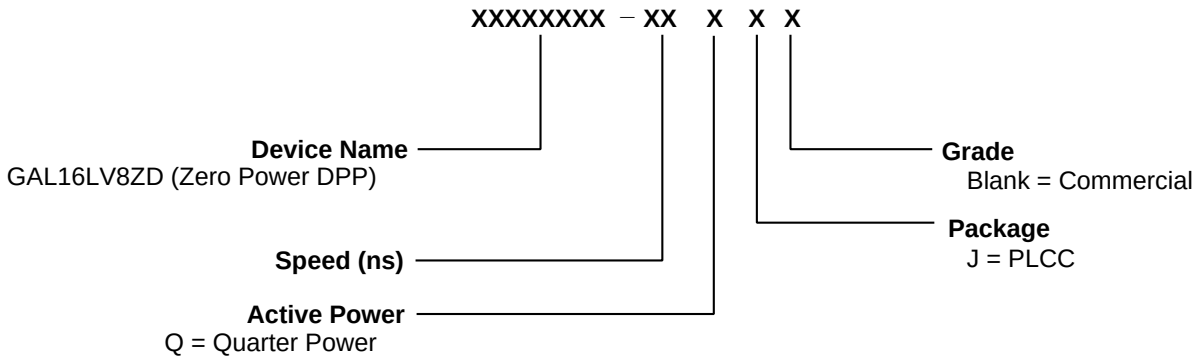
LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL16LV8ZD ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Isb (μA)	Ordering #	Package
15	12	10	55	100	GAL16LV8ZD-15QJ	20-Lead PLCC
25	15	15	55	100	GAL16LV8ZD-25QJ	20-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL16LV8ZD. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. Most compilers also have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

When using the standard GAL16V8 JEDEC fuse pattern generated by the logic compilers for the GAL16LV8ZD, special attention must be given to pin 4 (DPP) to make sure that it is not used as one of the functional inputs.

REGISTERED MODE

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

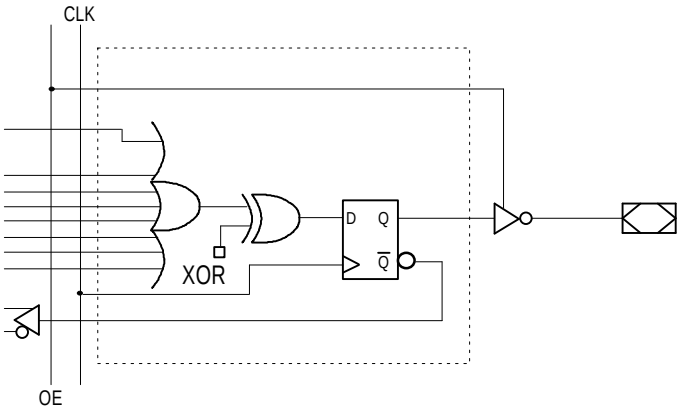
Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

Registered outputs have eight product terms per output. I/O's have seven product terms per output.

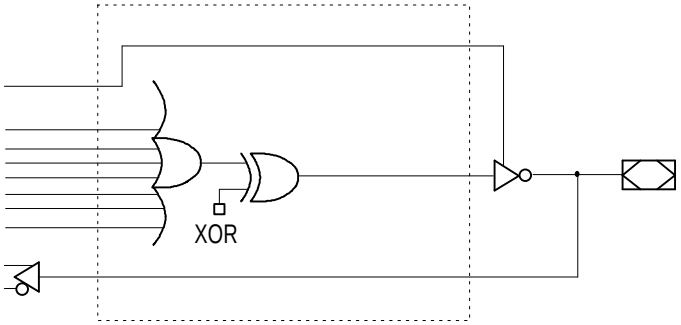
Pin 4 is used as dedicated power-down pin on GAL16LV8ZD. It cannot be used as functional input.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 11 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$.



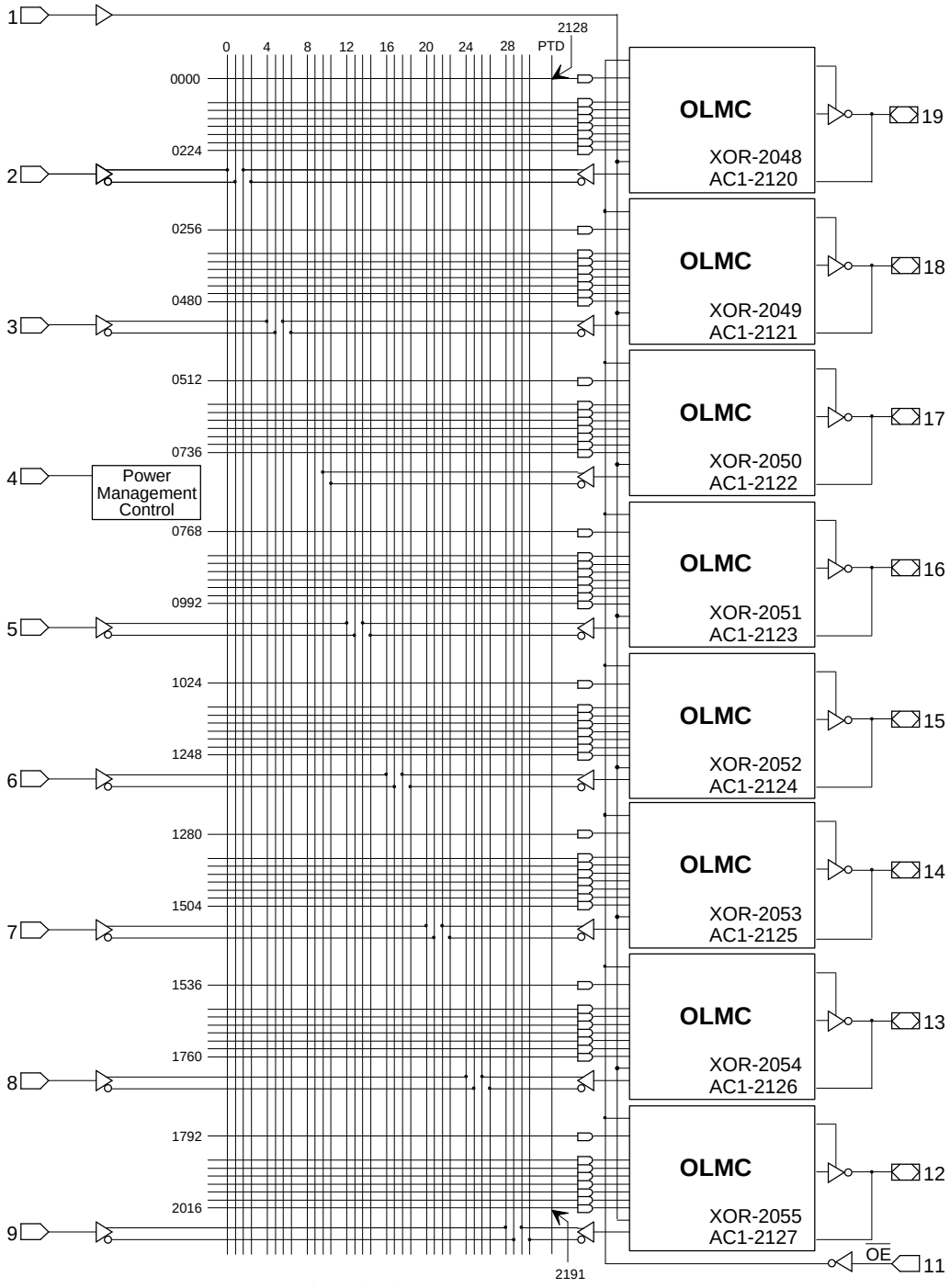
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

PLCC Package Pinout



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...		.... 2118, 2119	
Byte7	Byte6	.... Byte1	Byte0

MSB — LSB

SYN-2192
AC0-2193

COMPLEX MODE

In the Complex mode, macrocells are configured as output only or I/O functions.

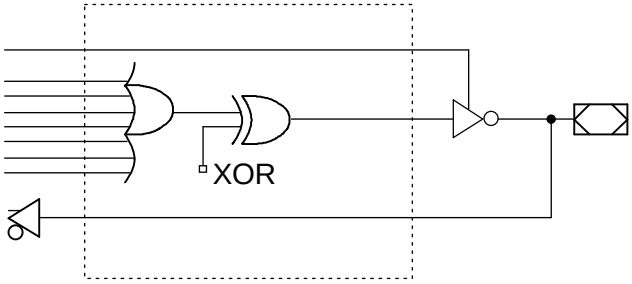
Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 12 & 19) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 11 are always available as data inputs into the AND array.

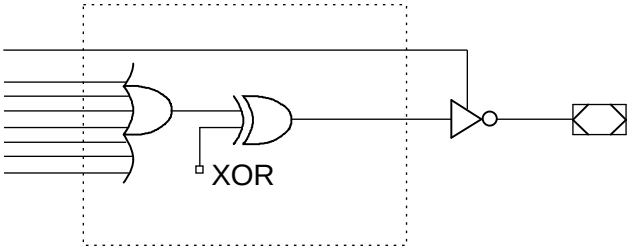
Pin 4 is used as dedicated power-down pin on GAL16LV8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 13 through Pin 18 are configured to this function.



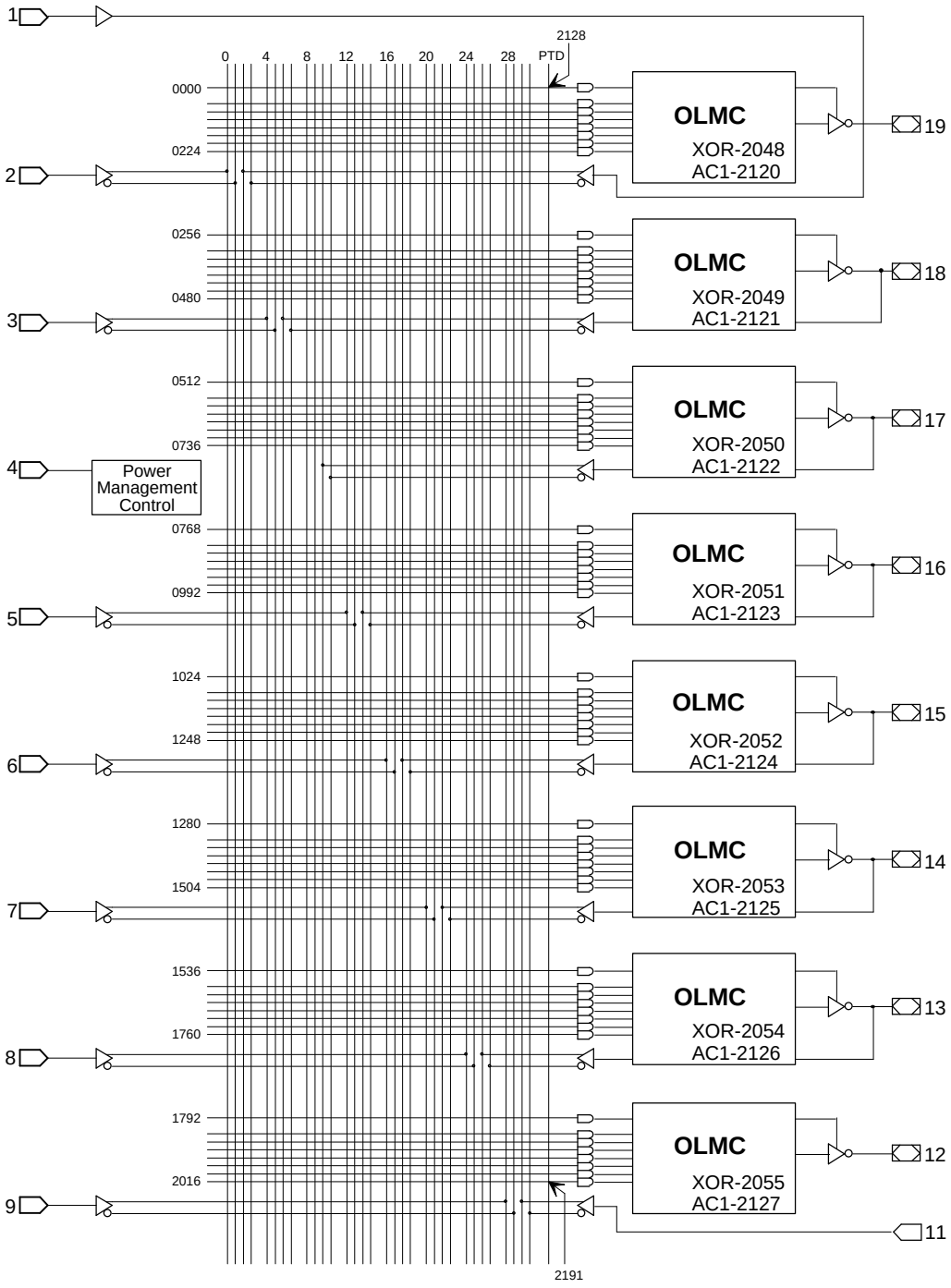
Combinatorial Output Configuration for Complex Mode

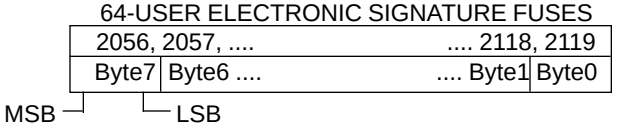
- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 12 and Pin 19 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

PLCC Package Pinout





SYN-2192
AC0-2193

SIMPLE MODE

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

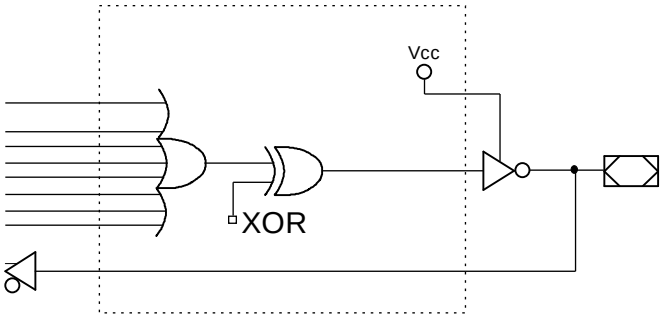
Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

Pins 1 and 11 are always available as data inputs into the AND array. The center two macrocells (pins 15 & 16) cannot be used in the input configuration.

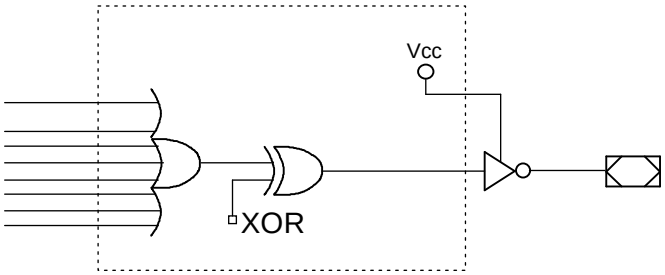
Pin 4 is used as dedicated power-down pin on GAL16LV8ZD. It cannot be used as a functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



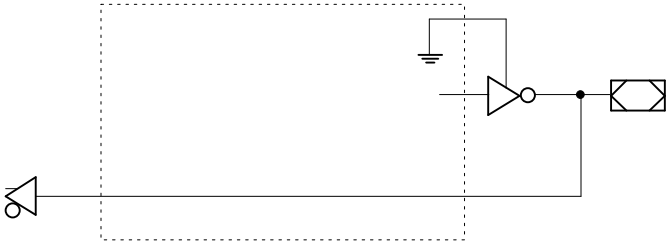
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 15 & 16 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 15 & 16 are permanently configured to this function.



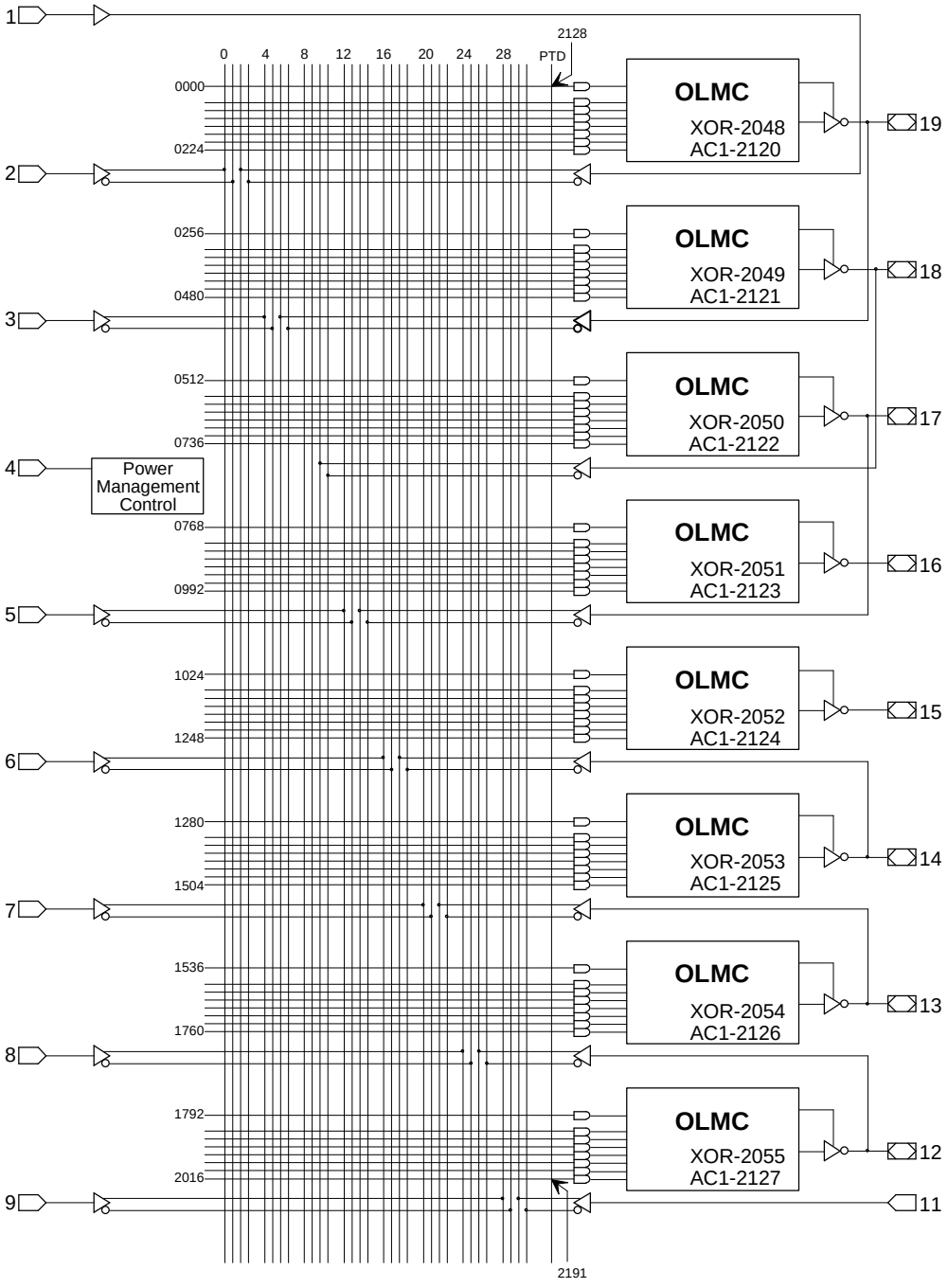
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 15 & 16 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

PLCC Package Pinout



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...	.... 2118, 2119
Byte7 Byte6	.... Byte1 Byte0

MSB — LSB

SYN-2192
AC0-2193

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +5.6V

Input voltage applied ..... -0.5 to +5.6V
Off-state output voltage applied ..... -0.5 to +5.6V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	5.25	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CC}\text{-}0.2)V \le V_{IN} \le V_{CC}$	—	—	10	µA
		$V_{CC} \le V_{IN} \le 5.25V$	—	—	1	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
		I_{OL} = 0.5 mA Vin = V_{IL} or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -0.5 mA Vin = V_{IL} or V_{IH}	Vcc-0.45	—	—	V
		I_{OH} = -100 µA Vin = V_{IL} or V_{IH}	Vcc-0.2	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-8	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = GND T_A = 25°C	-30	—	-130	mA

COMMERCIAL

I_{SB}	Stand-by Power Supply Current	V_{IL} = GND V_{IH} = Vcc Outputs Open	ZD -15/-25	—	50	100	µA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15 MHz Outputs Open	ZD -15/-25	—	45	55	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 3.3V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM	TEST COND.[1]	DESCRIPTION	COM -15 MIN.	COM -15 MAX.	COM -25 MIN.	COM -25 MAX.	UNITS
tpd	A	Input or I/O to Combinatorial Output	3	15	3	25	ns
tco	A	Clock to Output Delay	2	10	2	15	ns
tcf[2]	—	Clock to Feedback Delay	—	8	—	10	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑	12	—	15	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	45.5	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	50	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	62.5	—	41.6	—	MHz
twh	—	Clock Pulse Duration, High	8	—	12	—	ns
twl	—	Clock Pulse Duration, Low	8	—	12	—	ns
ten	B	Input or I/O to Output Enabled	—	17	—	25	ns
	B	$\overline{OE}$↓ to Output Enabled	—	16	—	20	ns
tdis	C	Input or I/O to Output Disabled	—	18	—	25	ns
	C	$\overline{OE}$↑ to Output Disabled	—	17	—	20	ns

1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Description section.
3) Refer to fmax Description section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TYPICAL*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 3.3V, V_I = 0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 3.3V, $V_{I/O}$ = 0V

*Guaranteed but not 100% tested.

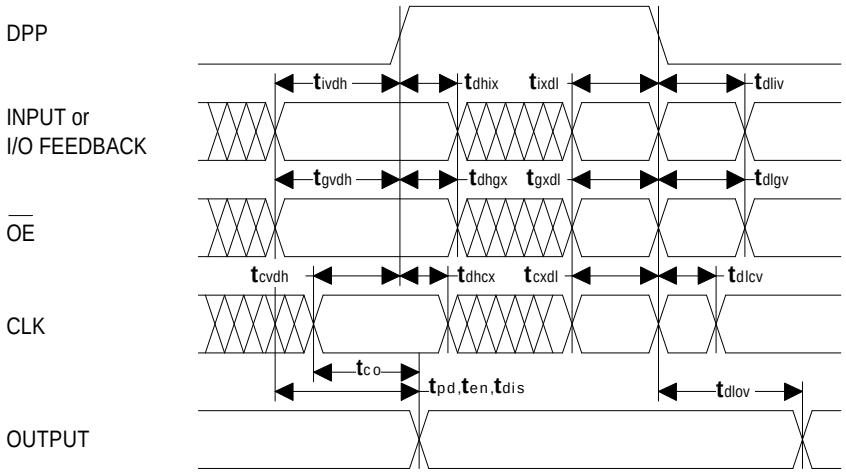
DEDICATED POWER-DOWN PIN SPECIFICATIONS

Over Recommended Operating Conditions

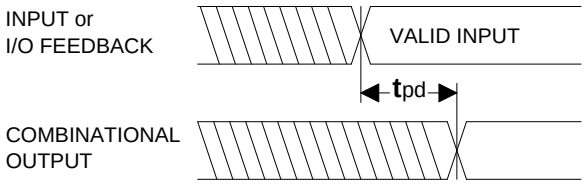
PARAMETER	TEST COND[1].	DESCRIPTION	COM -15		COM -25		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{whd}	—	DPP Pulse Duration High	40	—	40	—	ns
t_{wld}	—	DPP Pulse Duration Low	30	—	40	—	ns
ACTIVE TO STANDBY							
t_{ivdh}	—	Valid Input before DPP High	0	—	0	—	ns
t_{gvdh}	—	Valid OE before DPP High	0	—	0	—	ns
t_{cvdh}	—	Valid Clock before DPP High	0	—	0	—	ns
t_{dhix}	—	Input Don't Care after DPP High	—	15	—	25	ns
t_{dhgx}	—	$\overline{OE}$ Don't Care after DPP High	—	15	—	25	ns
t_{dhcx}	—	Clock Don't Care after DPP High	—	15	—	25	ns
STANDBY TO ACTIVE							
t_{ixdl}	—	Input Don't Care before DPP Low	—	0	—	0	ns
t_{gxdl}	—	$\overline{OE}$ Don't Care before DPP Low	—	0	—	0	ns
t_{cxdl}	—	Clock Don't Care before DPP Low	—	0	—	0	ns
t_{dliv}	—	DPP Low to Valid Input	20	—	25	—	ns
t_{dlgv}	—	DPP Low to Valid OE	20	—	25	—	ns
t_{dlcv}	—	DPP Low to Valid Clock	30	—	35	—	ns
t_{dlov}	A	DPP Low to Valid Output	5	45	5	45	ns

1) Refer to Switching Test Conditions section.

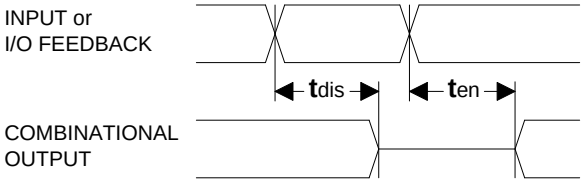
DEDICATED POWER-DOWN PIN (DPP) TIMING WAVEFORMS



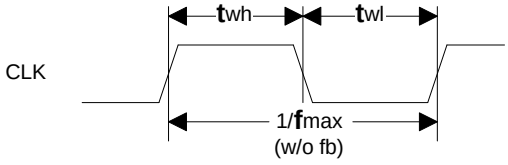
SWITCHING WAVEFORMS



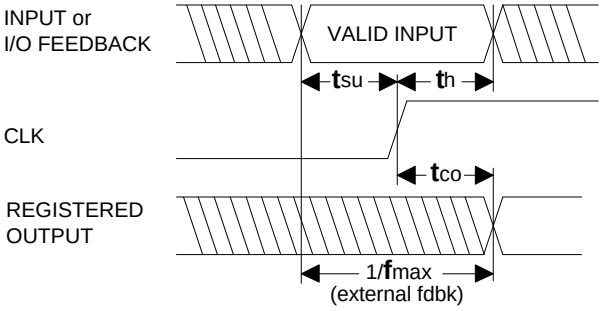
Combinatorial Output



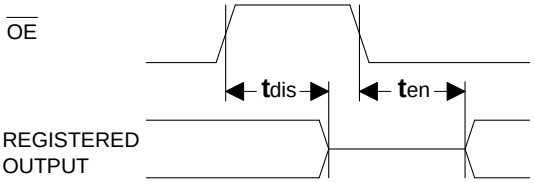
Input or I/O to Output Enable/Disable



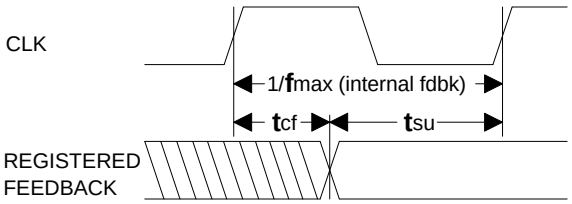
Clock Width



Registered Output

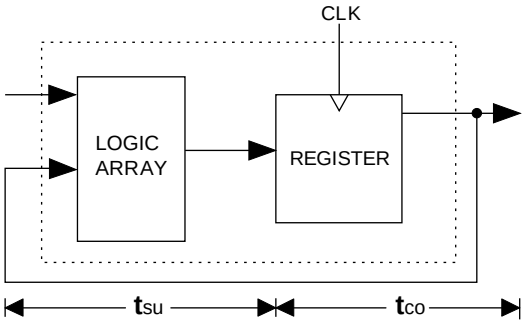


$\overline{OE}$ to Output Enable/Disable



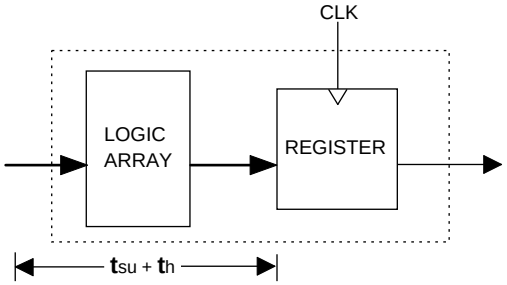
f_{max} with Feedback

fmax SPECIFICATIONS



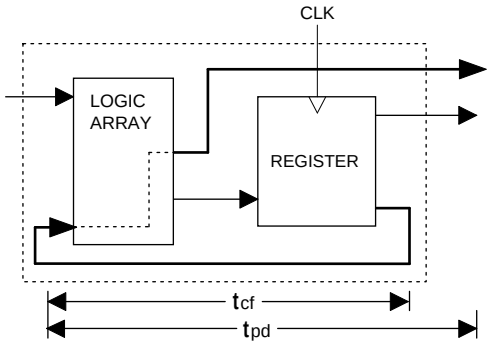
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

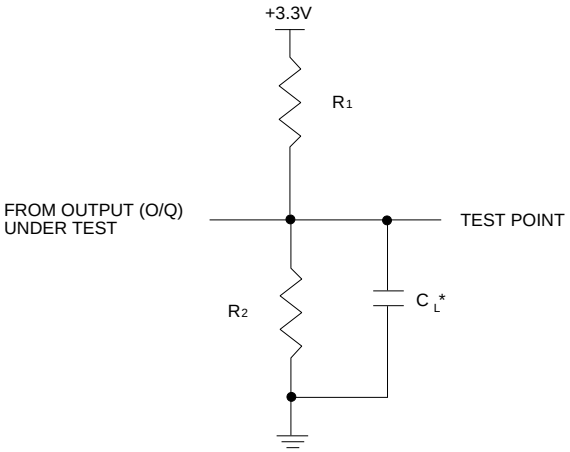
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	2ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level. 3-state to active transitions are measured at (Voh - 0.5) V and (Vol + 0.5) V.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		270Ω	220Ω	35pF
B	Active High	270Ω	220Ω	35pF
	Active Low	270Ω	220Ω	35pF
C	Active High	270Ω	220Ω	5pF
	Active Low	270Ω	220Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL16LV8ZD device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter checksum.

SECURITY CELL

A security cell is provided in the GAL16LV8ZD devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The electronic signature data is always available to the user, regardless of the state of this security cell.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

The GAL16LV8ZD devices includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

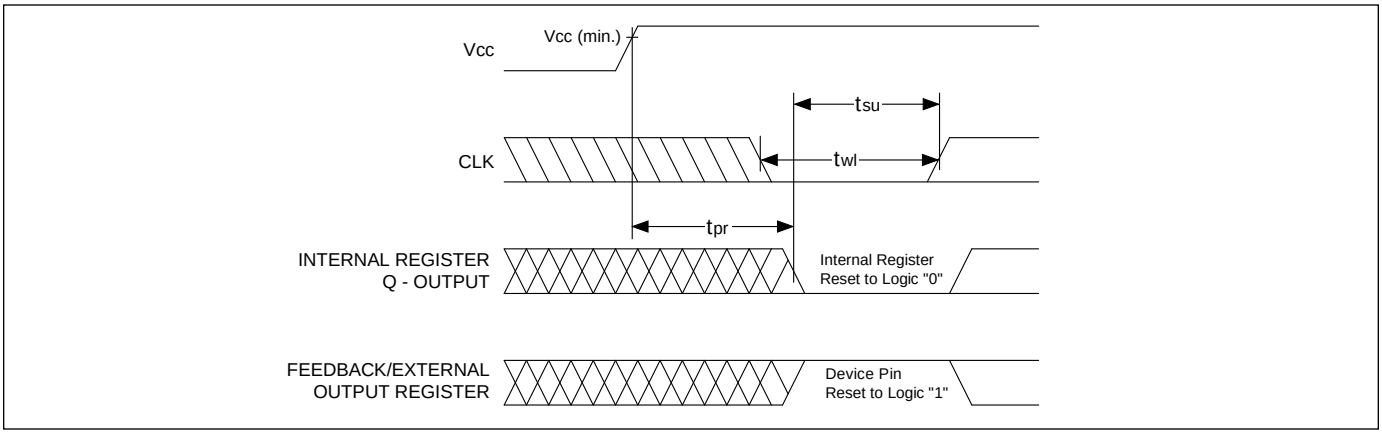
INPUT BUFFERS

GAL16LV8ZD devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

DEDICATED POWER-DOWN PIN (DPP)

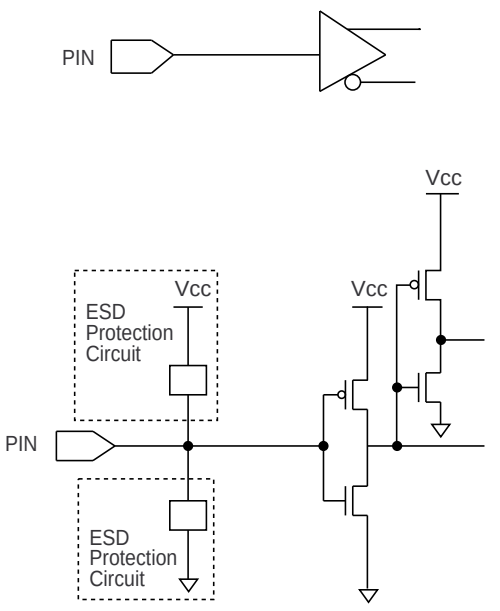
The GAL16LV8ZD uses pin 4 as the dedicated power-down signal to put the device in to the power-down state. DPP is an active high signal where a logic high driven on this signal puts the device into power-down state. Input pin 4 cannot be used as a logic function input on this device.

POWER-UP RESET

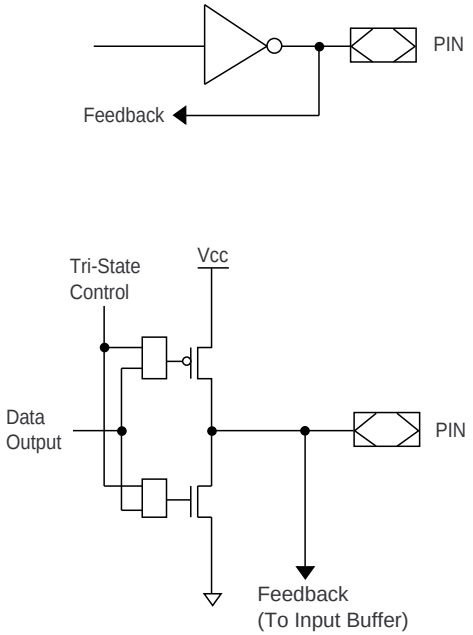


Circuitry within the GAL16LV8ZD provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 10µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL16LV8ZD. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



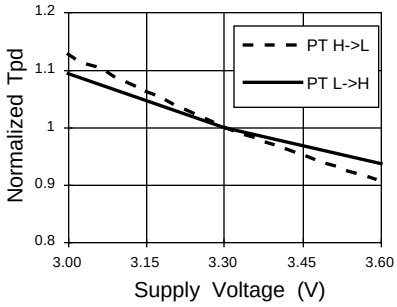
Typical Input



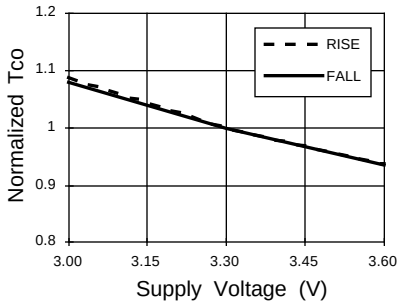
Typical Output

TYPICAL AC AND DC CHARACTERISTICS

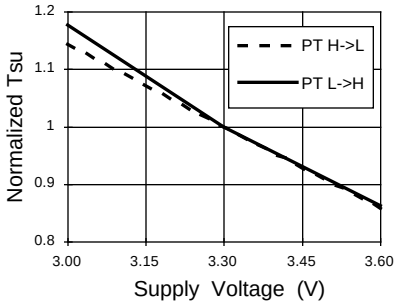
Normalized Tpd vs Vcc



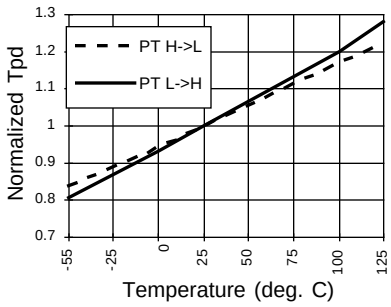
Normalized Tco vs Vcc



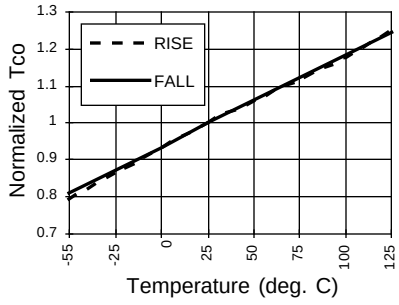
Normalized Tsu vs Vcc



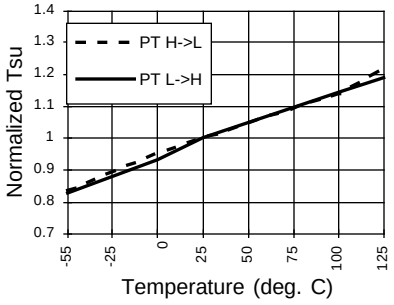
Normalized Tpd vs Temp



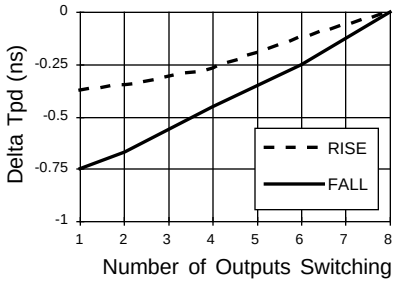
Normalized Tco vs Temp



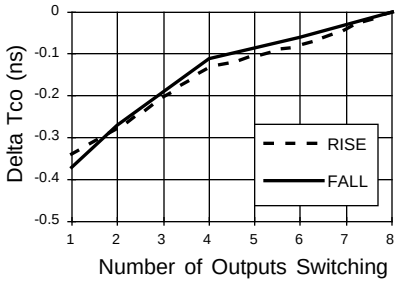
Normalized Tsu vs Temp



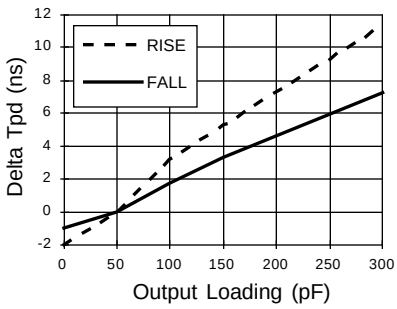
Delta Tpd vs # of Outputs Switching



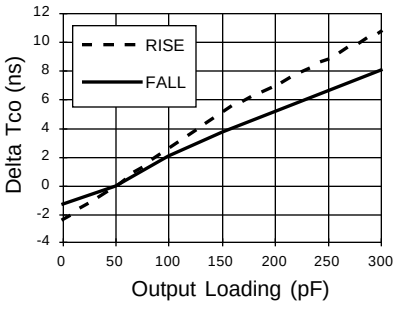
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

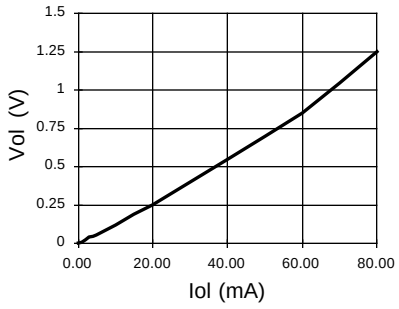


Delta Tco vs Output Loading

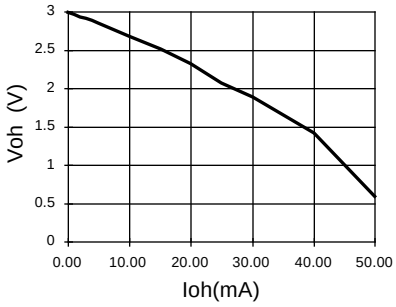


TYPICAL AC AND DC CHARACTERISTICS

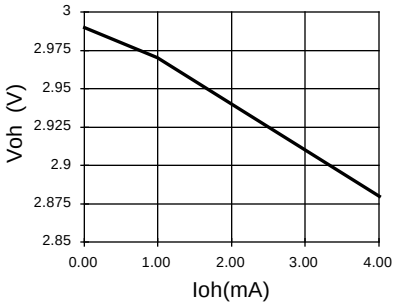
Vol vs Iol



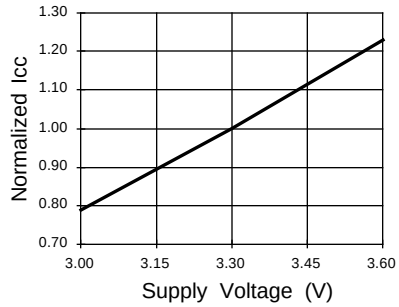
Voh vs Ioh



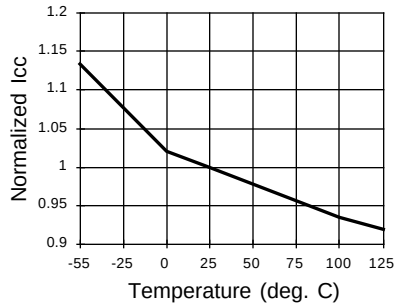
Voh vs Ioh



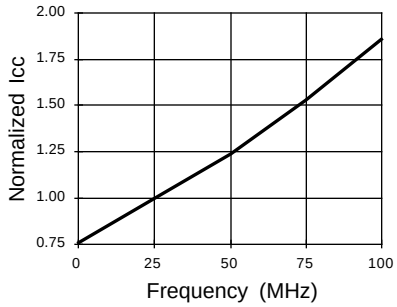
Normalized Icc vs Vcc



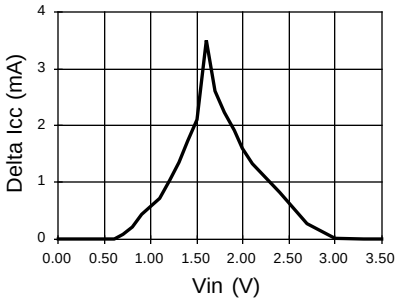
Normalized Icc vs Temp



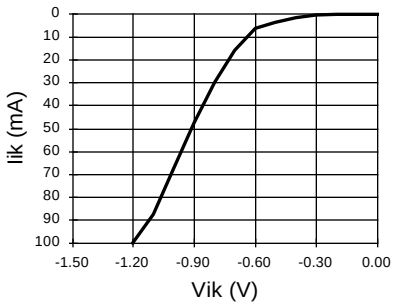
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



GAL16V8Z
GAL16V8ZD

Zero Power E²CMOS PLD

FEATURES

- **ZERO POWER E²CMOS TECHNOLOGY**
  - **— 100µA Standby Current**
  - **— Input Transition Detection on GAL16V8Z**
  - **— Dedicated Power-down Pin on GAL16V8ZD**
  - **— Input and Output Latching During Power Down**
- **HIGH PERFORMANCE E²CMOS TECHNOLOGY**
  - **— 12 ns Maximum Propagation Delay**
  - **— Fmax = 83.3 MHz**
  - **— 8 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 16 mA Output Drive**
  - **— UltraMOS® Advanced CMOS Technology**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Architecturally Similar to Standard GAL16V8**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— Battery Powered Systems**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

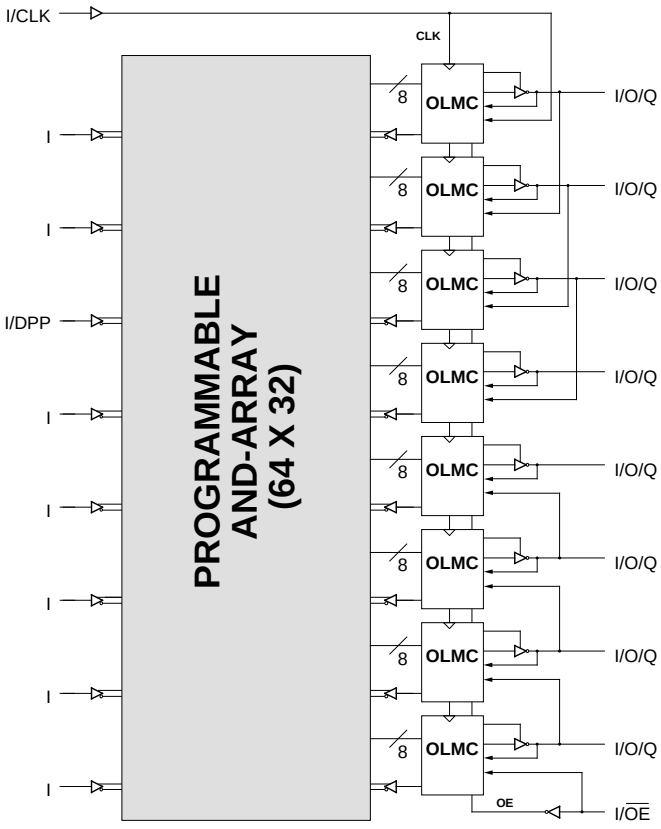
DESCRIPTION

The GAL16V8Z and GAL16V8ZD, at 100 µA standby current and 12ns propagation delay provides the highest speed and lowest power combination PLD available in the market. The GAL16V8Z/ZD is manufactured using Lattice Semiconductor's advanced zero power E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology.

The GAL16V8Z uses Input Transition Detection (ITD) to put the device in standby mode and is capable of emulating the full functionality of the standard GAL16V8. The GAL16V8ZD utilizes a dedicated power-down pin (DPP) to put the device in standby mode. It has 15 inputs available to the AND array.

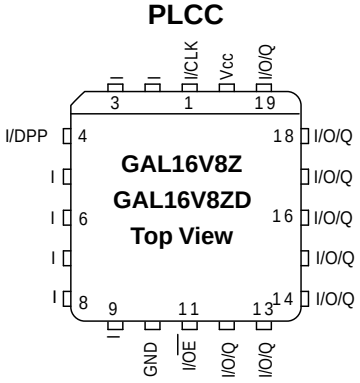
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM

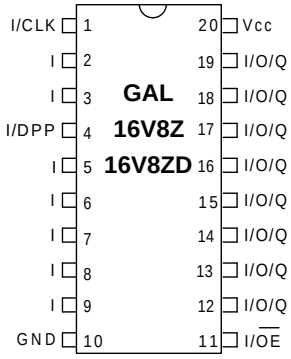


PIN CONFIGURATION

PLCC



DIP/SOIC



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL16V8Z/ZD ORDERING INFORMATION

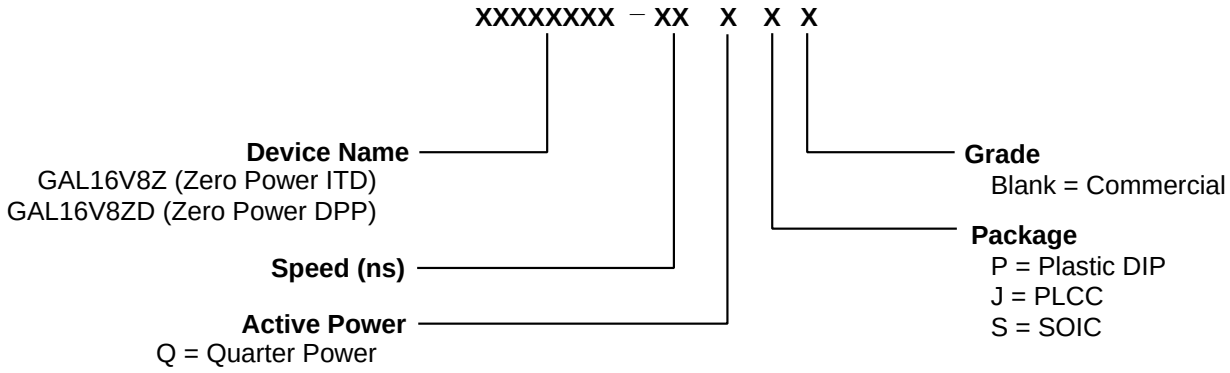
GAL16V8Z: Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Isb (μA)	Ordering #	Package
12	10	8	55	100	GAL16V8Z-12QP	20-Pin Plastic DIP
			55	100	GAL16V8Z-12QJ	20-Lead PLCC
			55	100	GAL16V8Z-12QS	20-Lead SOIC
15	15	10	55	100	GAL16V8Z-15QP	20-Pin Plastic DIP
			55	100	GAL16V8Z-15QJ	20-Lead PLCC
			55	100	GAL16V8Z-15QS	20-Lead SOIC

GAL16V8ZD: Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Isb (μA)	Ordering #	Package
12	10	8	55	100	GAL16V8ZD-12QP	20-Pin Plastic DIP
			55	100	GAL16V8ZD-12QJ	20-Lead PLCC
15	15	10	55	100	GAL16V8ZD-15QP	20-Pin Plastic DIP
			55	100	GAL16V8ZD-15QJ	20-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL16V8Z/ZD. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. Most compilers also have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

When using the standard GAL16V8 JEDEC fuse pattern generated by the logic compilers for the GAL16V8ZD, special attention must be given to pin 4 (DPP) to make sure that it is not used as one of the functional inputs.

REGISTERED MODE

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

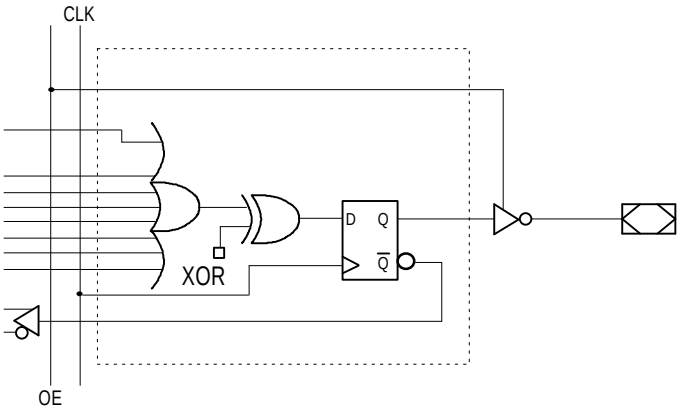
Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

Registered outputs have eight product terms per output. I/O's have seven product terms per output.

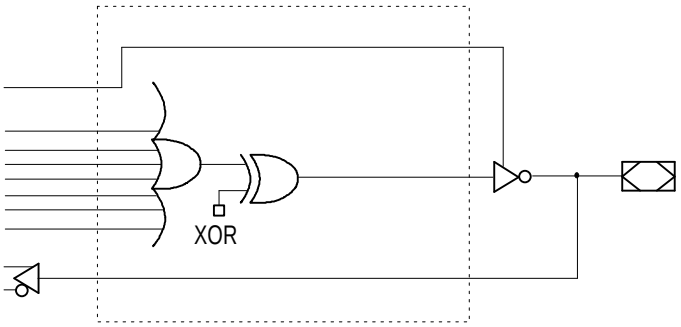
Pin 4 is used as dedicated power-down pin on GAL16V8ZD. It cannot be used as functional input.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 11 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$.



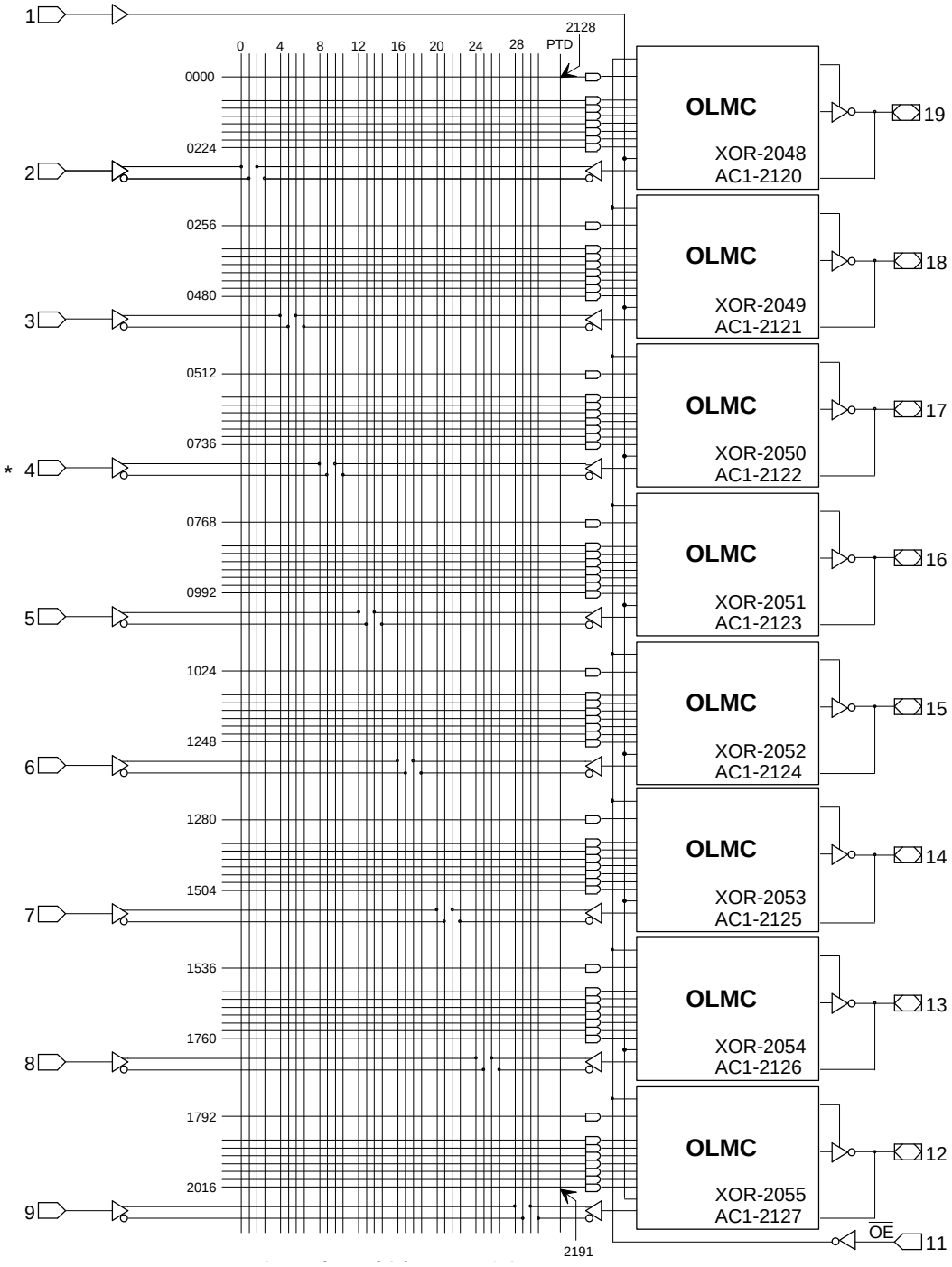
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

DIP, SOIC & PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...		.... 2118, 2119	
Byte7	Byte6	.... Byte1	Byte0

MSB LSB

SYN-2192
AC0-2193

* Note: Input not available on GAL16V8ZD

COMPLEX MODE

In the Complex mode, macrocells are configured as output only or I/O functions.

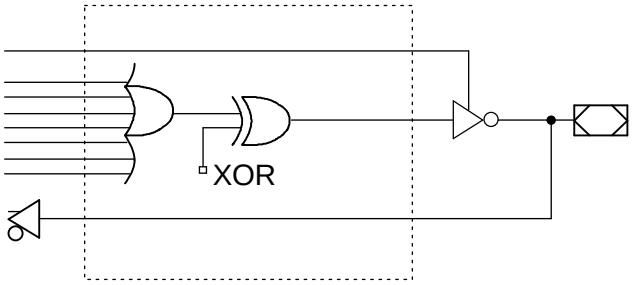
Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 12 & 19) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 11 are always available as data inputs into the AND array.

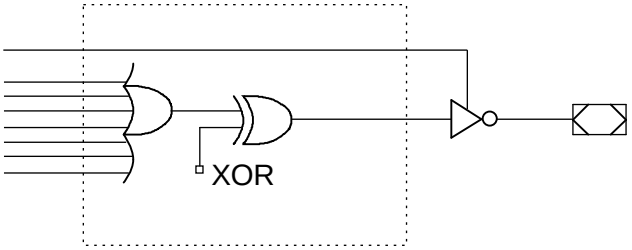
Pin 4 is used as dedicated power-down pin on GAL16V8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 13 through Pin 18 are configured to this function.



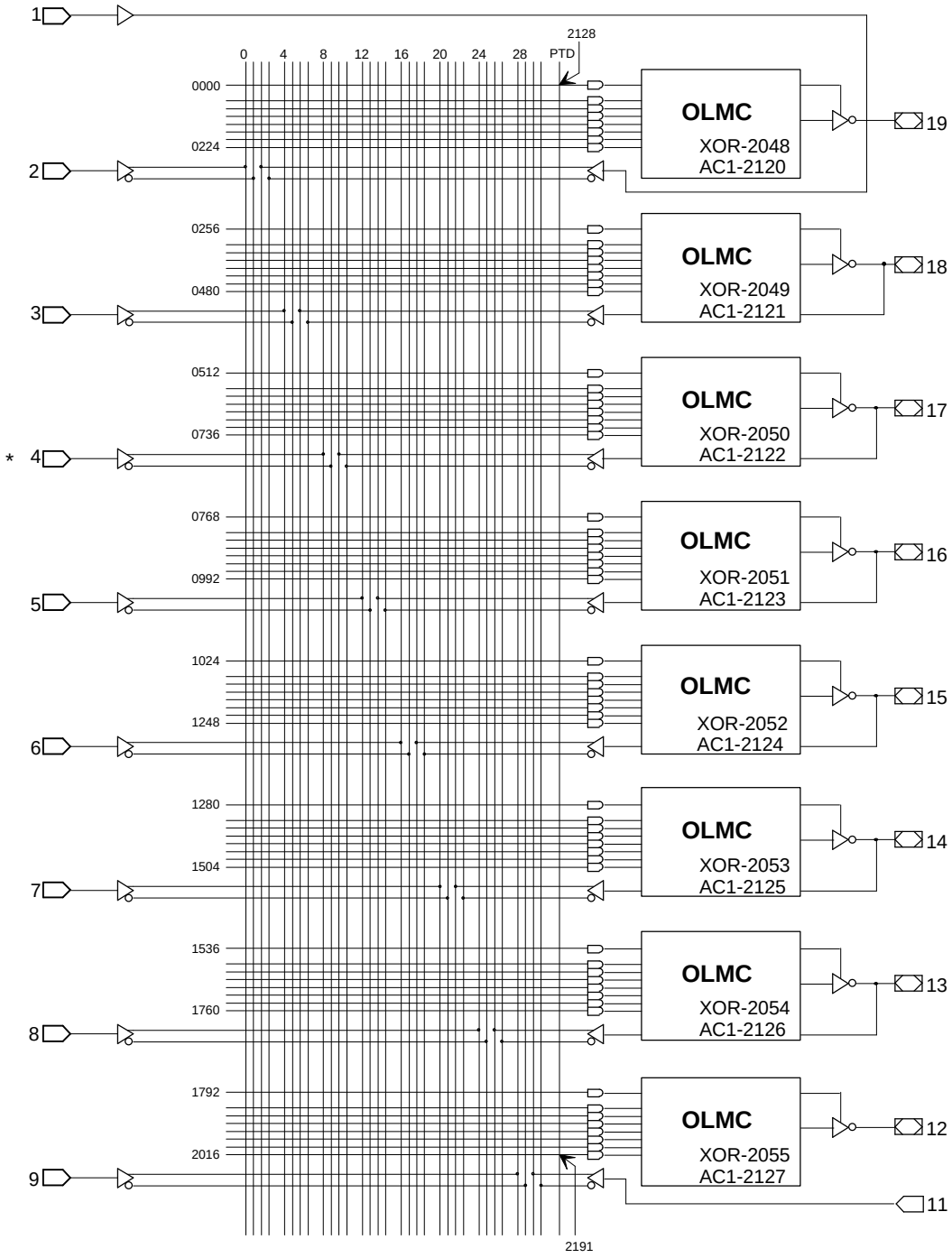
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 12 and Pin 19 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

DIP, SOIC & PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...		.... 2118, 2119
Byte7	Byte6	.... Byte1 Byte0

MSB LSB

SYN-2192
AC0-2193

* Note: Input not available on GAL16V8ZD

SIMPLE MODE

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

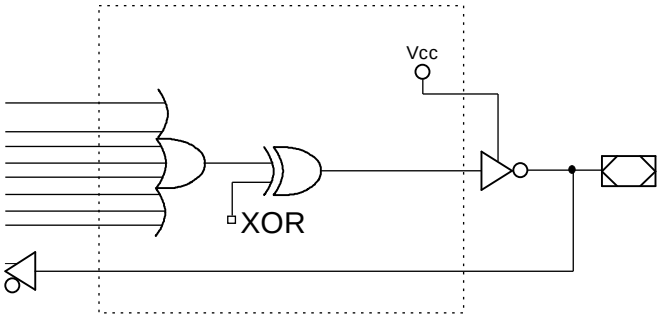
Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight porduct terms that can control the logic. In addition, each output has programmable polarity.

Pins 1 and 11 are always available as data inputs into the AND array. The center two macrocells (pins 15 & 16) cannot be used in the input configuration.

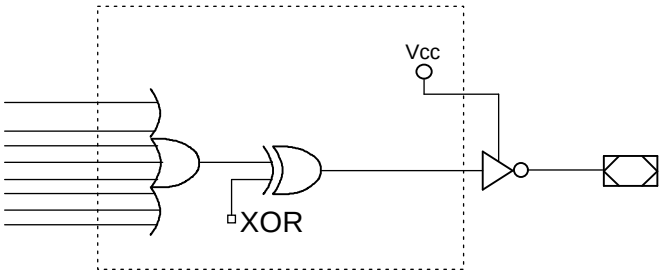
Pin 4 is used as dedicated power-down pin on GAL16V8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



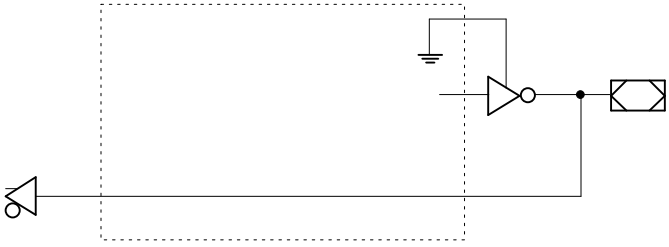
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 15 & 16 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 15 & 16 are permanently configured to this function.



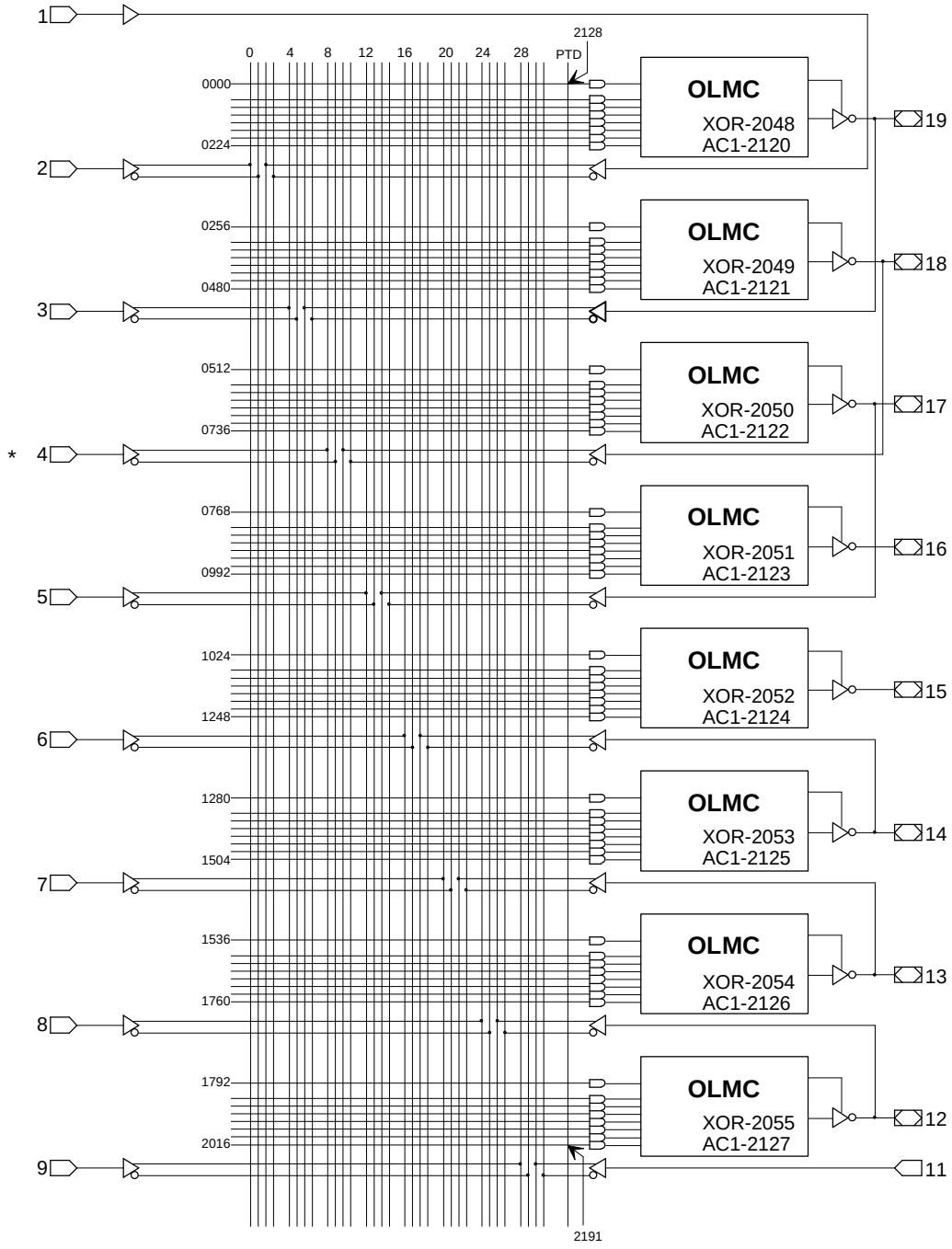
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 15 & 16 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

DIP, SOIC & PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...	.... 2118, 2119
Byte7 | Byte6	.... Byte1 | Byte0

MSB LSB

SYN-2192
AC0-2193

* Note: Input not available on GAL16V8ZD

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -100 µA Vin = V_{IL} or V_{IH}	Vcc-1	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA

COMMERCIAL

I_{SB}	Stand-by Power Supply Current	V_{IL} = GND V_{IH} = Vcc Outputs Open	Z-12/-15 ZD-12/-15	—	50	100	µA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15 MHz Outputs Open	Z-12/-15 ZD-12/-15	—	—	55	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

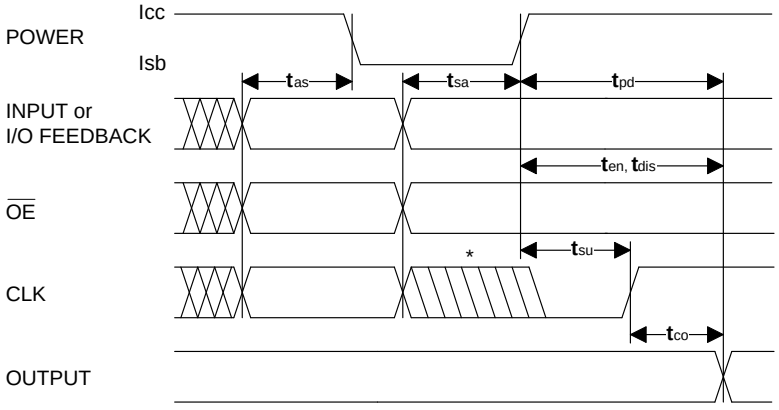
AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -12 MIN.	COM -12 MAX.	COM -15 MIN.	COM -15 MAX.	UNITS
tpd	A	Input or I/O to Combinational Output	3	12	3	15	ns
tco	A	Clock to Output Delay	2	8	2	10	ns
tcf[2]	—	Clock to Feedback Delay	—	6	—	7	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	15	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	55	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	62.5	—	45.5	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	MHz
twh	—	Clock Pulse Duration, High	6	—	8	—	ns
twl	—	Clock Pulse Duration, Low	6	—	8	—	ns
ten	B	Input or I/O to Output Enabled	—	12	—	15	ns
	B	$\overline{OE}$ to Output Enabled	—	12	—	15	ns
tdis	C	Input or I/O to Output Disabled	—	15	—	15	ns
	C	$\overline{OE}$ to Output DIsabled	—	12	—	15	ns
tas	—	Last Active Input to Standby	60	140	50	150	ns
tsa[4]	—	Standby to Active Output	6	13	5	15	ns

1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Specification section.
3) Refer to fmax Specification section.
4) Add **t**sa to **t**pd, **t**su, **t**en and **t**dis when the device is coming out of standby state.

STANDBY POWER TIMING WAVEFORMS



* Note: Rising clock edges are allowed during **t**sa but outputs are not guaranteed.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -12 MIN.	COM -12 MAX.	COM -15 MIN.	COM -15 MAX.	UNITS
tpd	A	Input or I/O to Combinational Output	3	12	3	15	ns
tco	A	Clock to Output Delay	2	8	2	10	ns
tcf[2]	—	Clock to Feedback Delay	—	6	—	7	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	15	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	55	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	62.5	—	45.5	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	MHz
twh	—	Clock Pulse Duration, High	6	—	8	—	ns
twl	—	Clock Pulse Duration, Low	6	—	8	—	ns
ten	B	Input or I/O to Output Enabled	—	12	—	15	ns
	B	$\overline{OE}$ to Output Enabled	—	12	—	15	ns
tdis	C	Input or I/O to Output Disabled	—	15	—	15	ns
	C	$\overline{OE}$ to Output Disabled	—	12	—	15	ns

1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Specification section.
3) Refer to fmax Specification section.

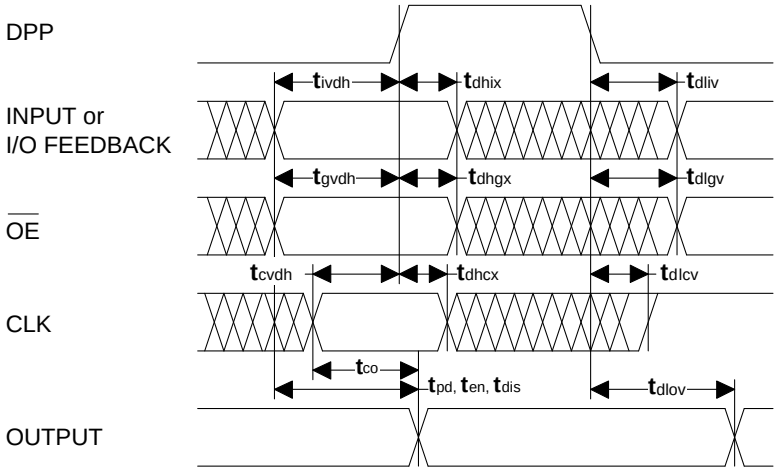
DEDICATED POWER-DOWN PIN SPECIFICATIONS

Over Recommended Operating Conditions

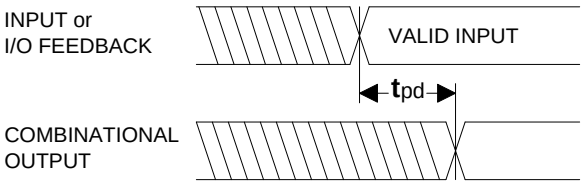
PARAMETER	TEST COND[1].	DESCRIPTION	COM -12		COM -15		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{whd}	—	DPP Pulse Duration High	12	—	15	—	ns
t_{wld}	—	DPP Pulse Duration Low	25	—	30	—	ns
ACTIVE TO STANDBY							
t_{ivdh}	—	Valid Input before DPP High	5	—	8	—	ns
t_{gvdh}	—	Valid OE before DPP High	0	—	0	—	ns
t_{cvdh}	—	Valid Clock Before DPP High	0	—	0	—	ns
t_{dhix}	—	Input Don't Care after DPP High	—	2	—	5	ns
t_{dhgx}	—	$\overline{OE}$ Don't Care after DPP High	—	6	—	9	ns
t_{dhcx}	—	Clock Don't Care after DPP High	—	8	—	11	ns
STANDBY TO ACTIVE							
t_{dliv}	—	DPP Low to Valid Input	12	—	15	—	ns
t_{dlgv}	—	DPP Low to Valid $\overline{OE}$	16	—	20	—	ns
t_{dlcv}	—	DPP Low to Valid Clock	18	—	20	—	ns
t_{dlov}	A	DPP Low to Valid Output	5	24	5	30	ns

1) Refer to Switching Test Conditions section.

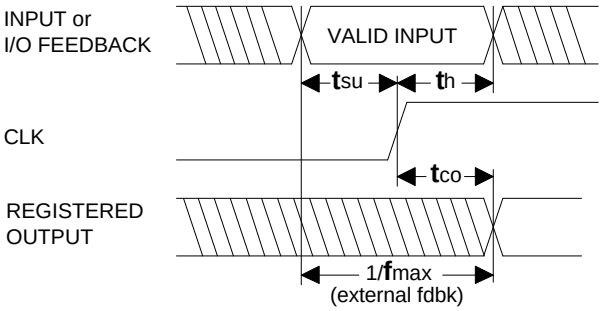
DEDICATED POWER-DOWN PIN (DPP) TIMING WAVEFORMS



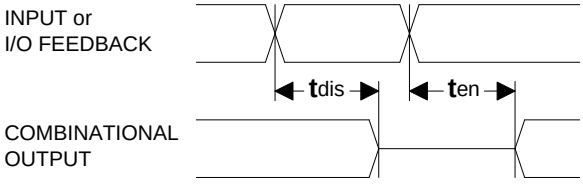
SWITCHING WAVEFORMS



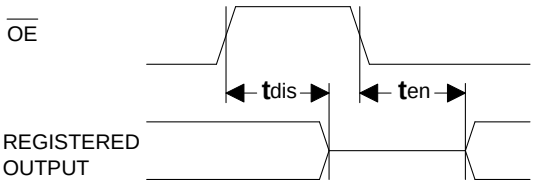
Combinatorial Output



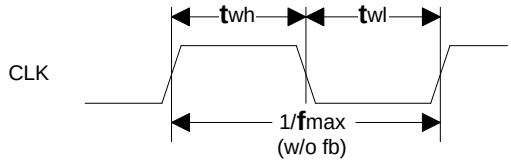
Registered Output



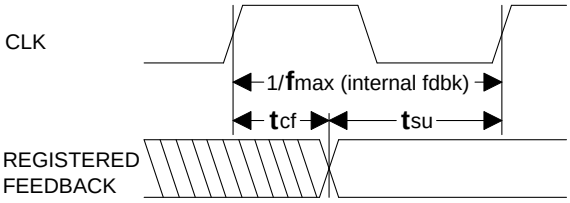
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

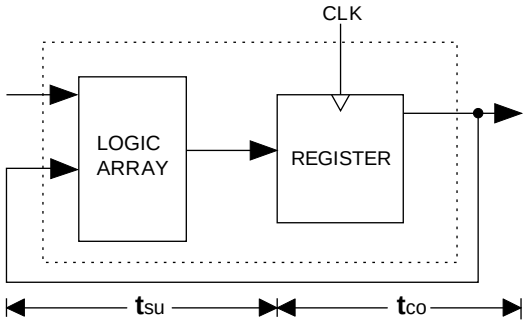


Clock Width



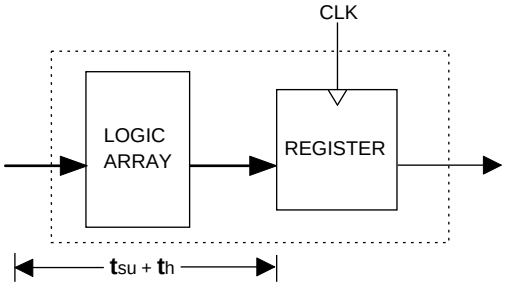
fmax with Feedback

fmax SPECIFICATIONS



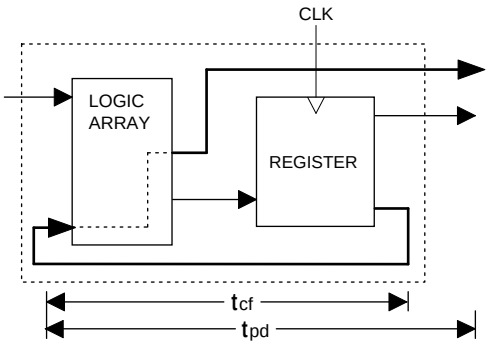
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

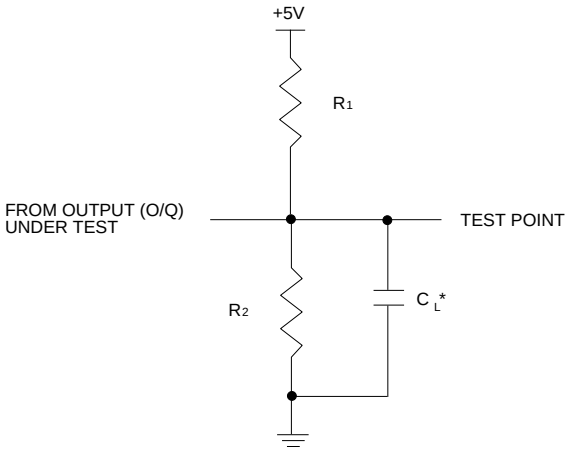
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R1	R2	CL
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL16V8Z/ZD device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter checksum.

SECURITY CELL

A security cell is provided in the GAL16V8Z/ZD devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The electronic signature data is always available to the user, regardless of the state of this security cell.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the Development Tools Section of the Data Book). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle

INPUT TRANSITION DETECTION (ITD)

The GAL16V8Z relies on its internal input detection circuitry to put the device in to power down mode. If there is no input transition for the specified period of time, the device will go into the power down state. Any valid input transition will put the device back into the active state. The first rising clock transition from power-down state only acts as a wake up signal to the device and will not clock the data input through to the output (refer to standby power timing waveform for more detail). Any input pulse widths greater than 5ns at input voltage level of 1.5V will be detected as input transition. The device will not detect any input pulse widths less than 1ns measured at input voltage level of 1.5V as an input transition.

DEDICATED POWER-DOWN PIN (DPP)

The GAL16V8ZD uses pin 4 as the dedicated power-down signal to put the device in to the power-down state. DPP is an active high signal where a logic high driven on this signal puts the device into power-down state. Input pin 4 cannot be used as a functional input on this device.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

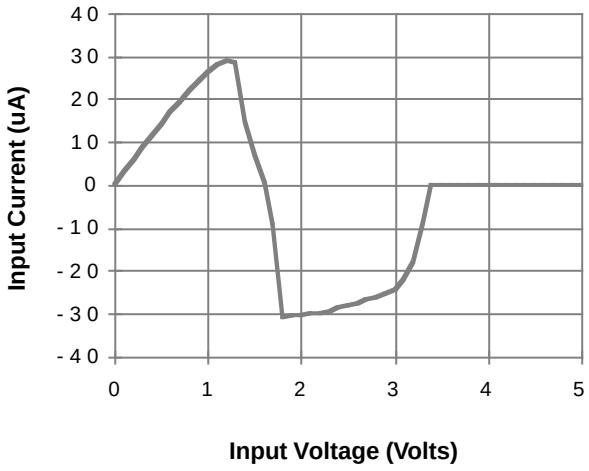
The GAL16V8Z/ZD devices includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

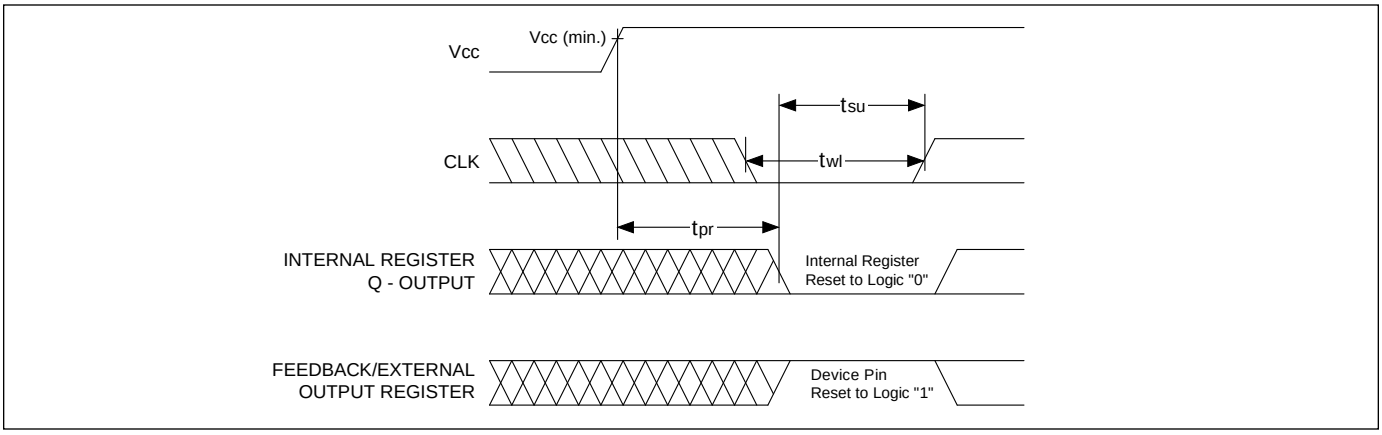
GAL16V8Z/ZD devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL16V8Z/ZD input buffers have latches within the buffers. As a result, when the device goes into standby mode the inputs will be latched to its values prior to standby. In order to overcome the input latches, they will have to be driven by an external source. Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Characteristic

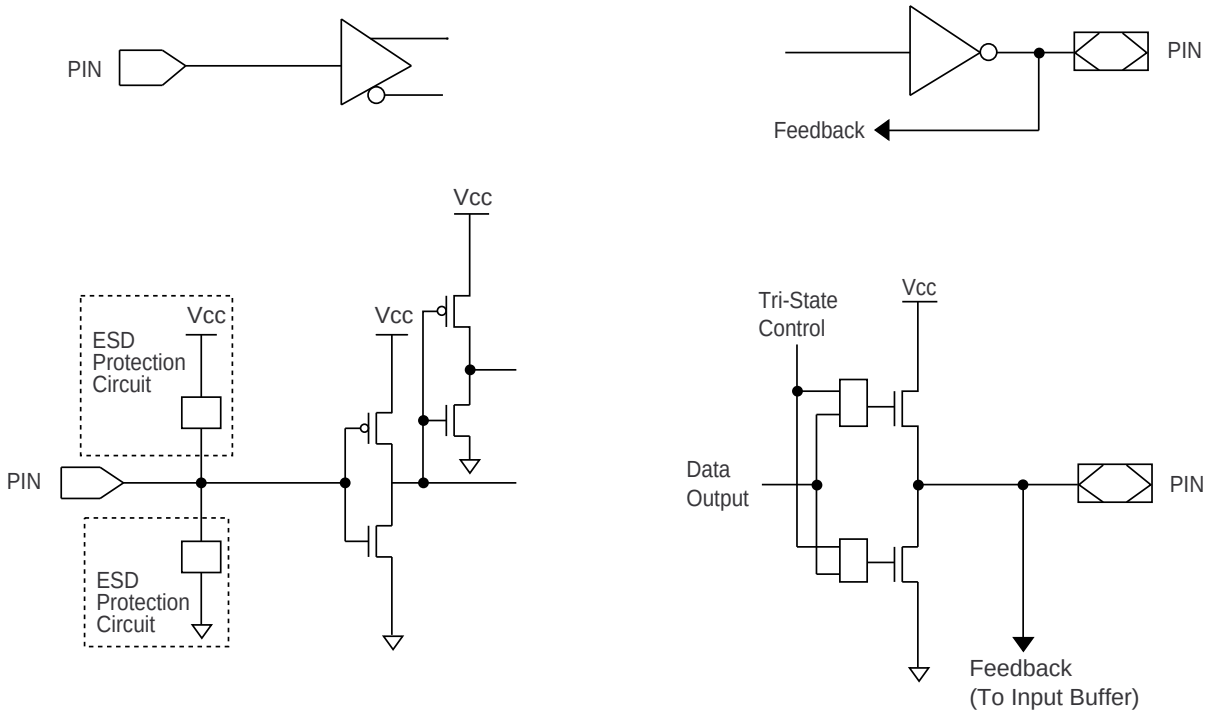


POWER-UP RESET



Circuitry within the GAL16V8Z/ZD provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr}, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL16V8Z/ZD. First, the V_{CC} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

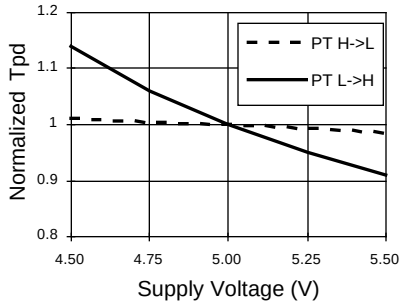
INPUT/OUTPUT EQUIVALENT SCHEMATICS



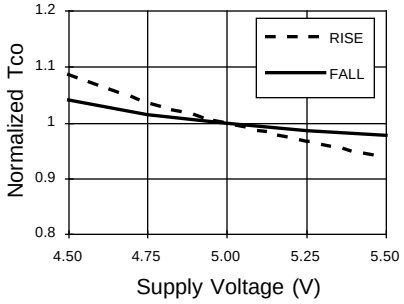
Typical Input **Typical Output**

TYPICAL AC AND DC CHARACTERISTICS

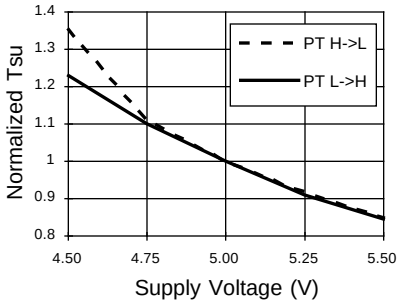
Normalized Tpd vs Vcc



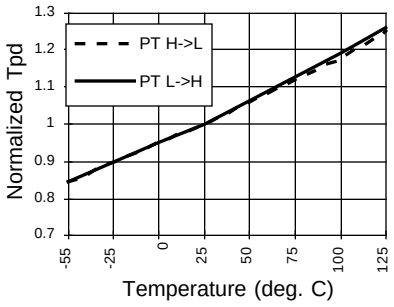
Normalized Tco vs Vcc



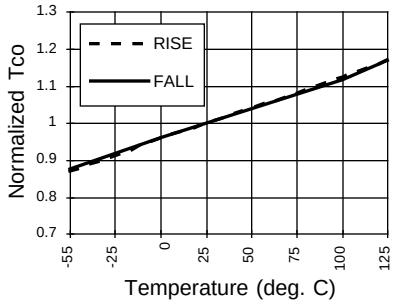
Normalized Tsu vs Vcc



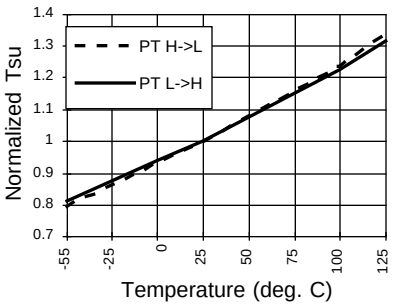
Normalized Tpd vs Temp



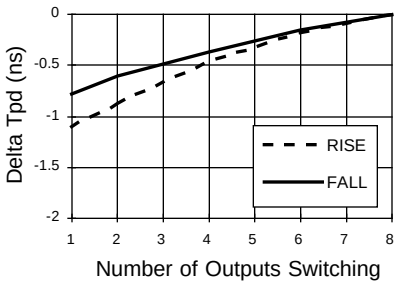
Normalized Tco vs Temp



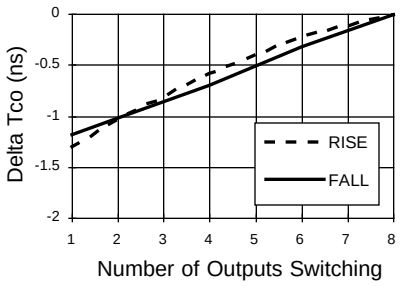
Normalized Tsu vs Temp



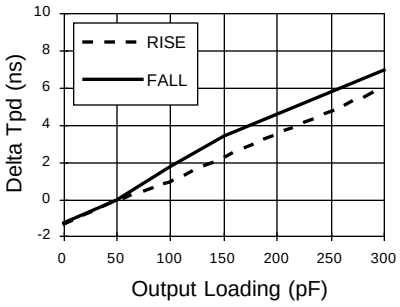
Delta Tpd vs # of Outputs Switching



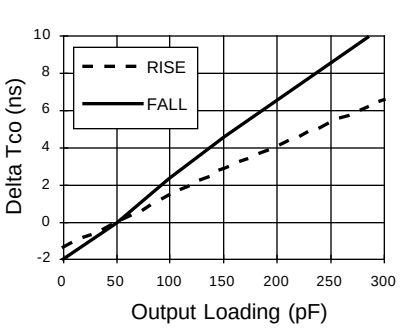
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

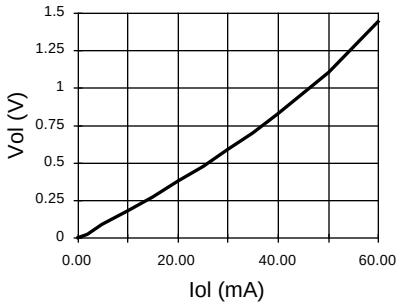


Delta Tco vs Output Loading

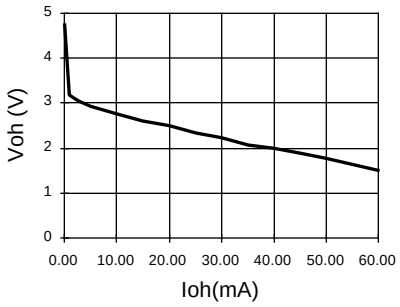


TYPICAL AC AND DC CHARACTERISTICS

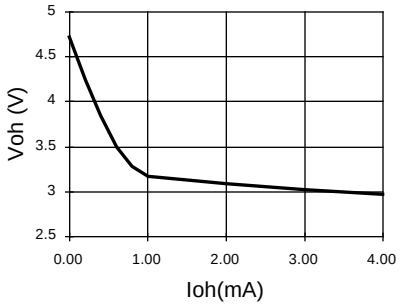
Vol vs Iol



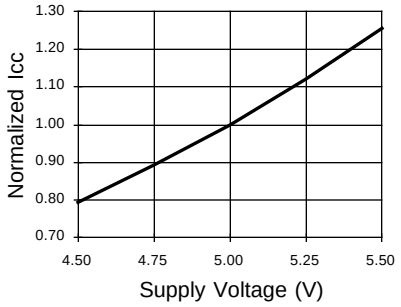
Voh vs Ioh



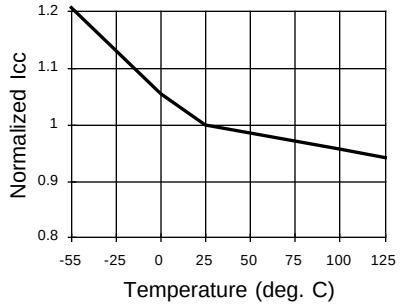
Voh vs Ioh



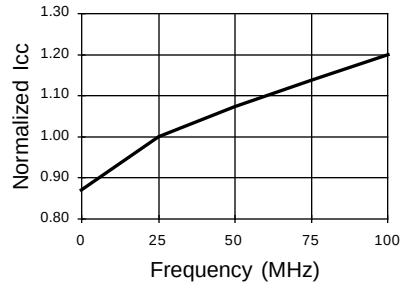
Normalized Icc vs Vcc



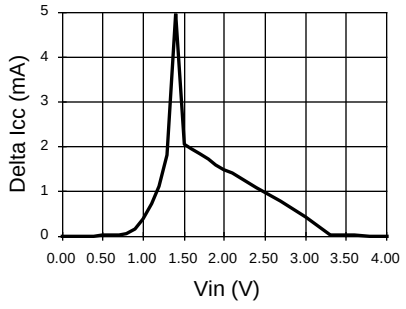
Normalized Icc vs Temp



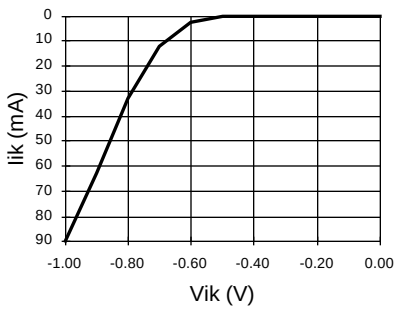
Normalized Icc vs Freq. (DPP & ITD > 10MHz)



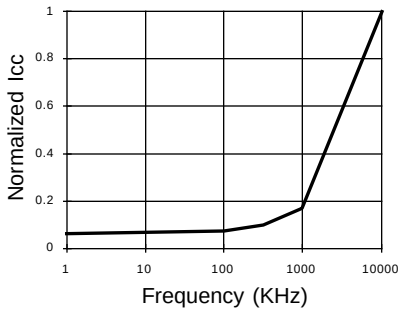
Delta Icc vs Vin (1 input)



Input Clamp (Vik)



Normalized Icc vs Freq. (ITD)



GAL16V8

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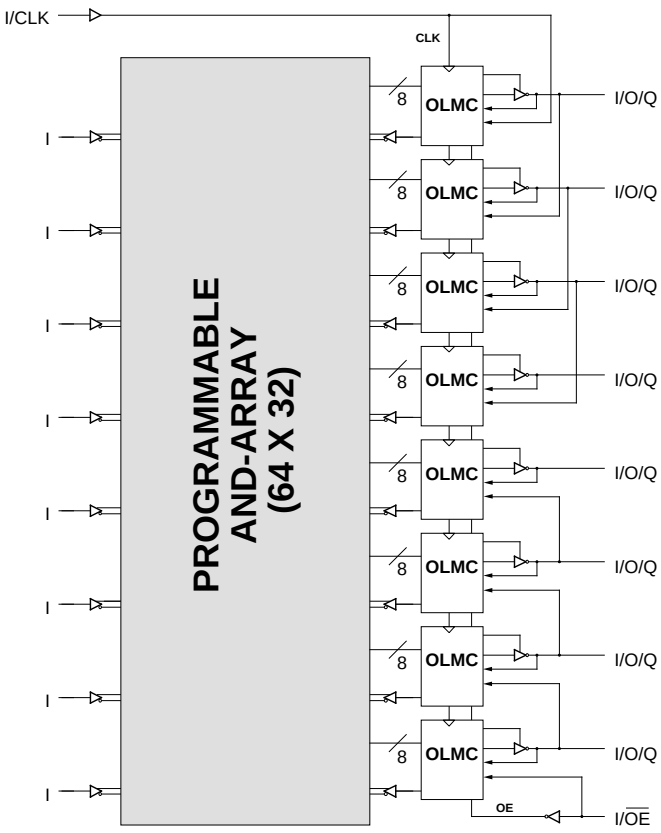
FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 5 ns Maximum Propagation Delay**
  - **— Fmax = 166 MHz**
  - **— 4 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - **— 75mA Typ Icc on Low Power Device**
  - **— 45mA Typ Icc on Quarter Power Device**
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

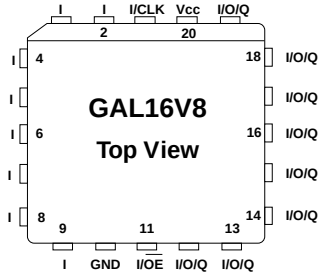
The GAL16V8C, at 5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E^2) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (**<**100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL16V8 are the PAL architectures listed in the table of the macrocell description section. GAL16V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

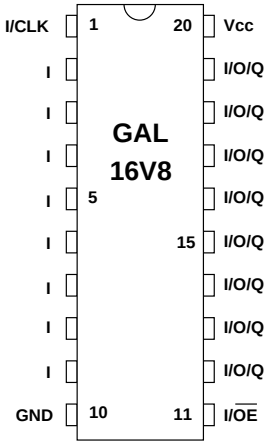
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

PIN CONFIGURATION

PLCC



DIP



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL16V8 ORDERING INFORMATION

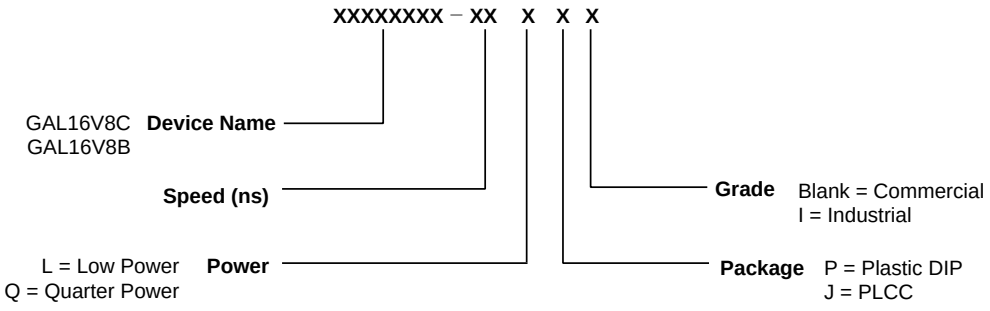
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
5	3	4	115	GAL16V8C-5LP	20-Pin Plastic DIP
			115	GAL16V8C-5LJ	20-Lead PLCC
7.5	7	5	115	GAL16V8C-7LP	20-Pin Plastic DIP
			115	GAL16V8C-7LJ	20-Lead PLCC
			115	GAL16V8B-7LP	20-Pin Plastic DIP
			115	GAL16V8B-7LJ	20-Lead PLCC
10	10	7	115	GAL16V8B-10LP	20-Pin Plastic DIP
			115	GAL16V8B-10LJ	20-Lead PLCC
15	12	10	55	GAL16V8B-15QP	20-Pin Plastic DIP
			55	GAL16V8B-15QJ	20-Lead PLCC
			90	GAL16V8B-15LP	20-Pin Plastic DIP
			90	GAL16V8B-15LJ	20-Lead PLCC
25	15	12	55	GAL16V8B-25QP	20-Pin Plastic DIP
			55	GAL16V8B-25QJ	20-Lead PLCC
			90	GAL16V8B-25LP	20-Pin Plastic DIP
			90	GAL16V8B-25LJ	20-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	7	5	130	GAL16V8C-7LPI	20-Pin Plastic DIP
			130	GAL16V8C-7LJI	20-Lead PLCC
10	10	7	130	GAL16V8B-10LPI	20-Pin Plastic DIP
			130	GAL16V8B-10LJI	20-Lead PLCC
15	12	10	130	GAL16V8B-15LPI	20-Pin Plastic DIP
			130	GAL16V8B-15LJI	20-Lead PLCC
20	13	11	65	GAL16V8B-20QPI	20-Pin Plastic DIP
			65	GAL16V8B-20QJI	20-Lead PLCC
25	15	12	65	GAL16V8B-25QPI	20-Pin Plastic DIP
			65	GAL16V8B-25QJI	20-Lead PLCC
			130	GAL16V8B-25LPI	20-Pin Plastic DIP
			130	GAL16V8B-25LJI	20-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes are illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL16V8 . The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL16V8 can emulate. It also shows the OLMC mode under which the GAL16V8 emulates the PAL architecture.

PAL Architectures Emulated by GAL16V8	GAL16V8 Global OLMC Mode
16R8	**Registered**
16R6	**Registered**
16R4	**Registered**
16RP8	**Registered**
16RP6	**Registered**
16RP4	**Registered**
16L8	**Complex**
16H8	**Complex**
16P8	**Complex**
10L8	**Simple**
12L6	**Simple**
14L4	**Simple**
16L2	**Simple**
10H8	**Simple**
12H6	**Simple**
14H4	**Simple**
16H2	**Simple**
10P8	**Simple**
12P6	**Simple**
14P4	**Simple**
16P2	**Simple**

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL16V8A
PLDesigner	P16V8R[2]	P16V8C[2]	P16V8C[2]	P16V8A
TANGO-PLD	G16V8R	G16V8C	G16V8AS[3]	G16V8

1) Used with **Configuration** keyword.
2) Prior to Version 2.0 support.
3) Supported on Version 1.20 or later.

REGISTERED MODE

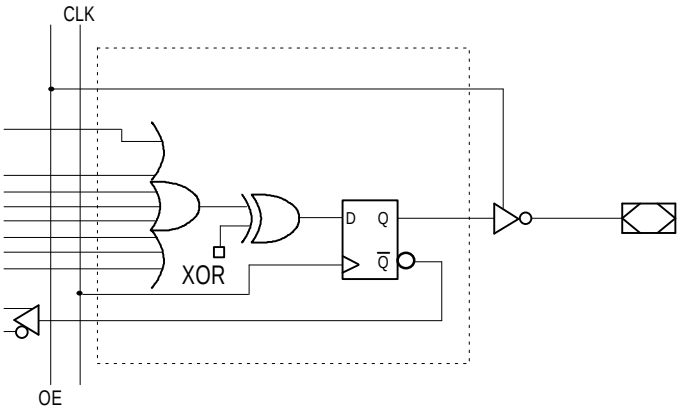
In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

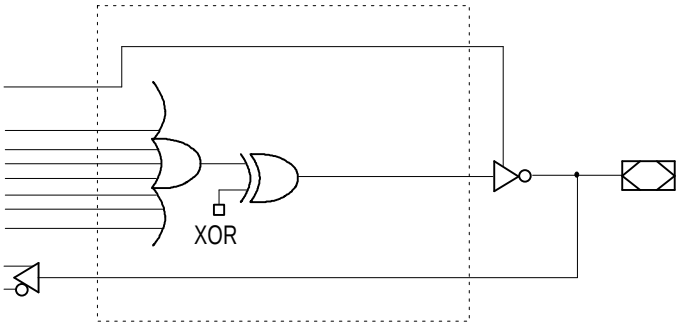
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 11 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$.



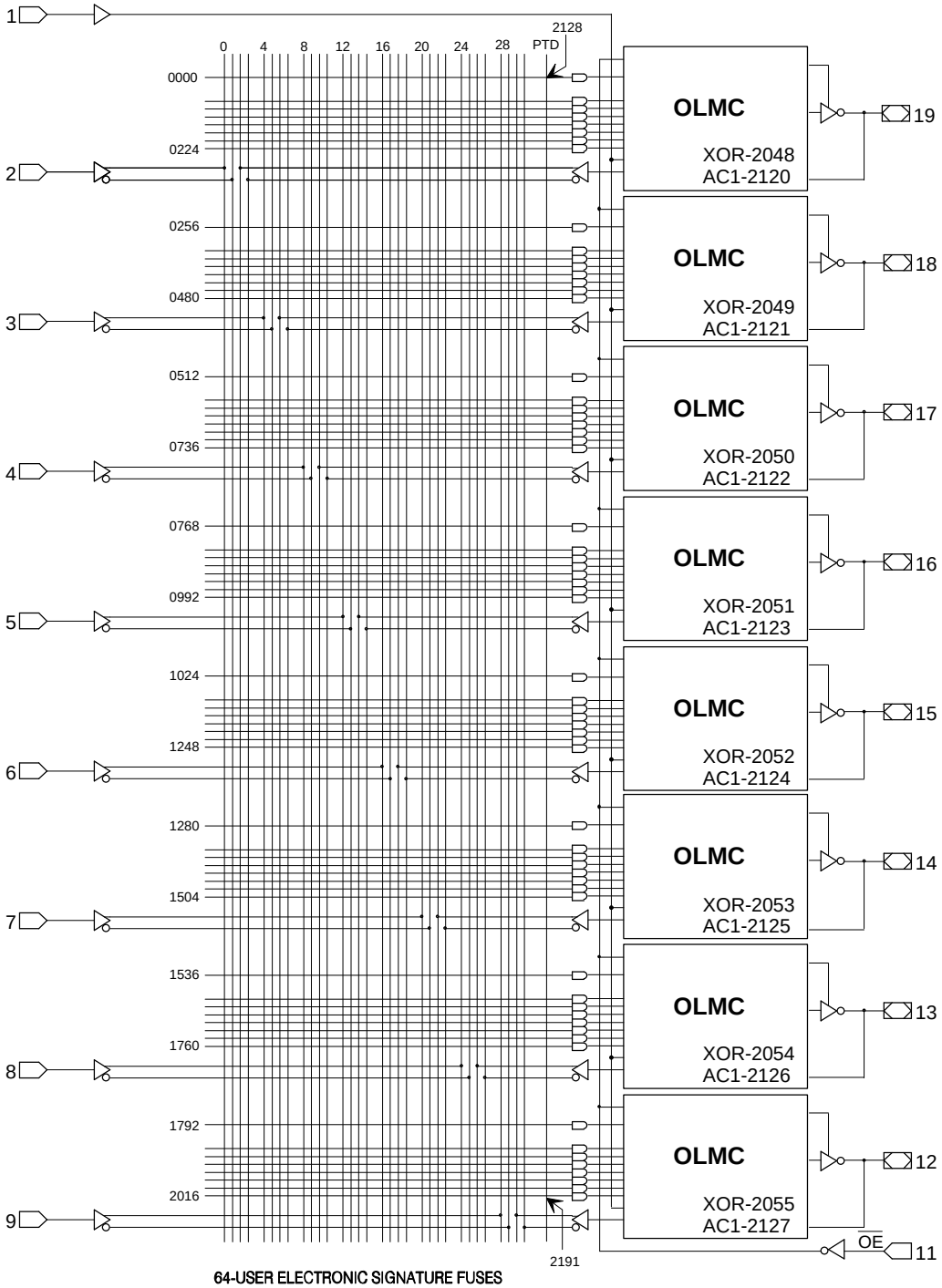
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

DIP & PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...			.... 2118, 2119
Byte 7	Byte 6	.... Byte 1	Byte 0

M S B L S B

SYN-2192
AC0-2193

COMPLEX MODE

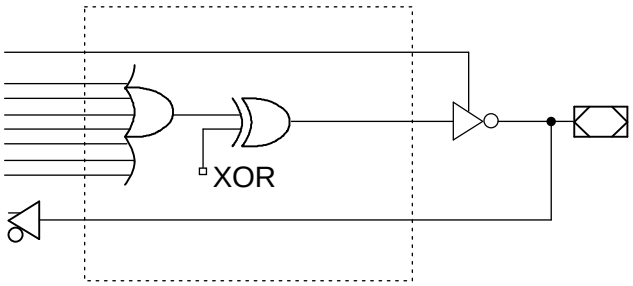
In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 12 & 19) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

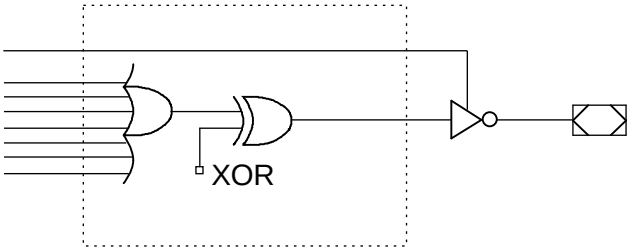
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 11 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 13 through Pin 18 are configured to this function.



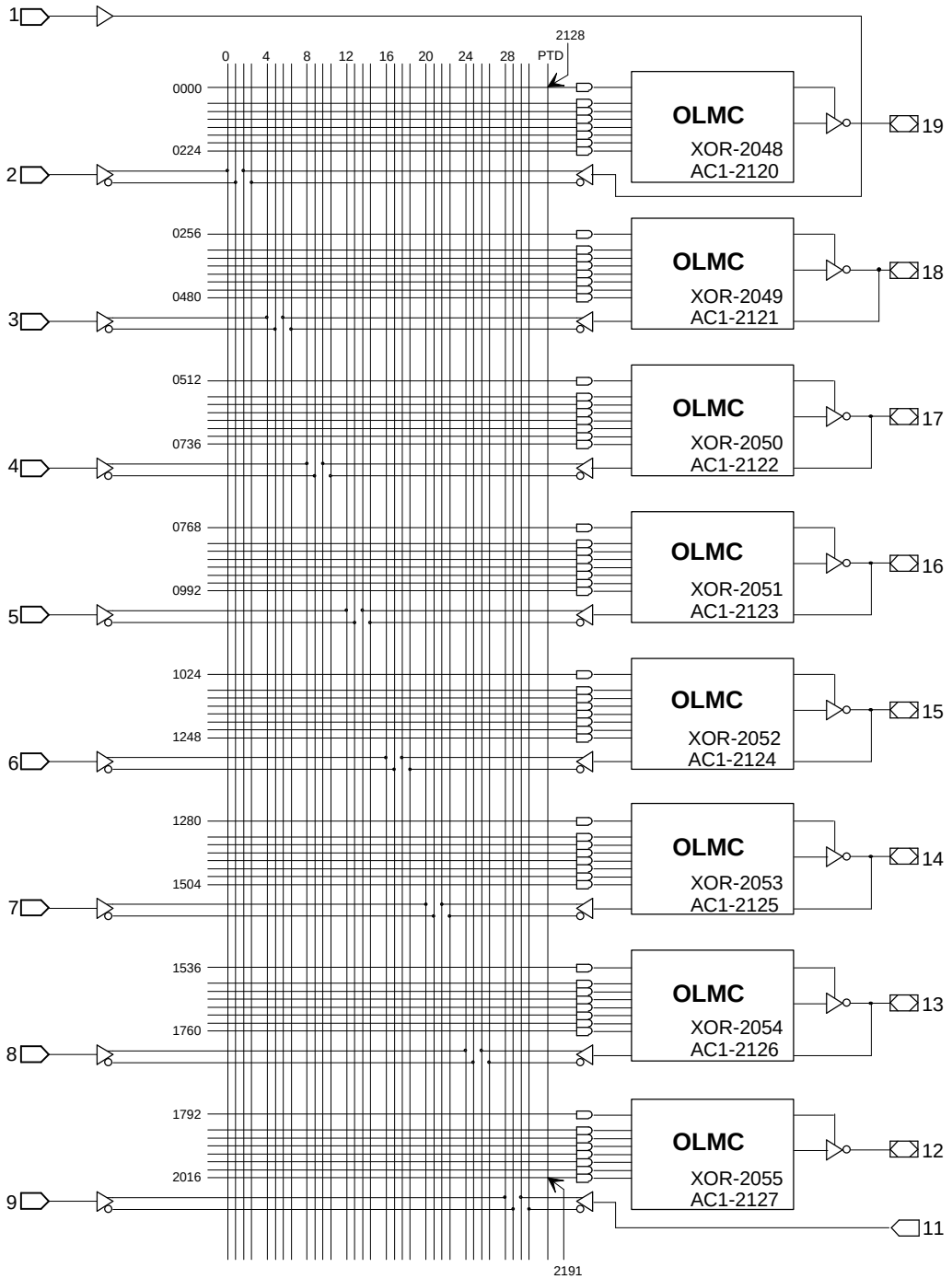
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 12 and Pin 19 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

DIP & PLCC Package Pinouts



SIMPLE MODE

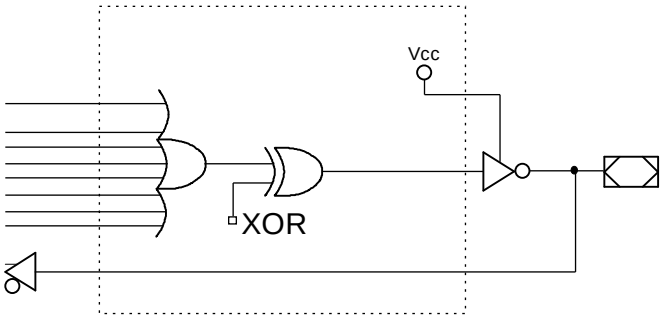
In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

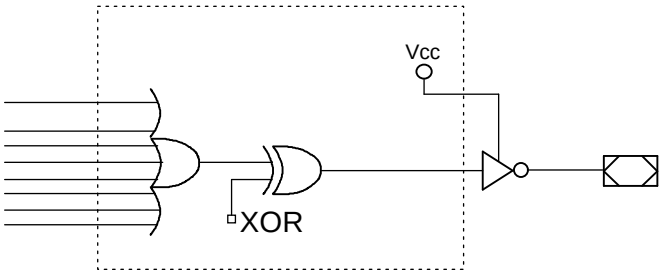
Pins 1 and 11 are always available as data inputs into the AND array. The center two macrocells (pins 15 & 16) cannot be used as input or I/O pins, and are only available as dedicated outputs.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



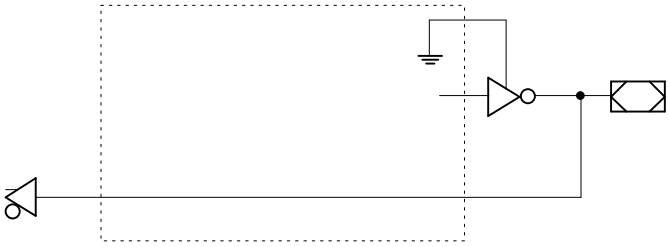
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 15 & 16 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 15 & 16 are permanently configured to this function.



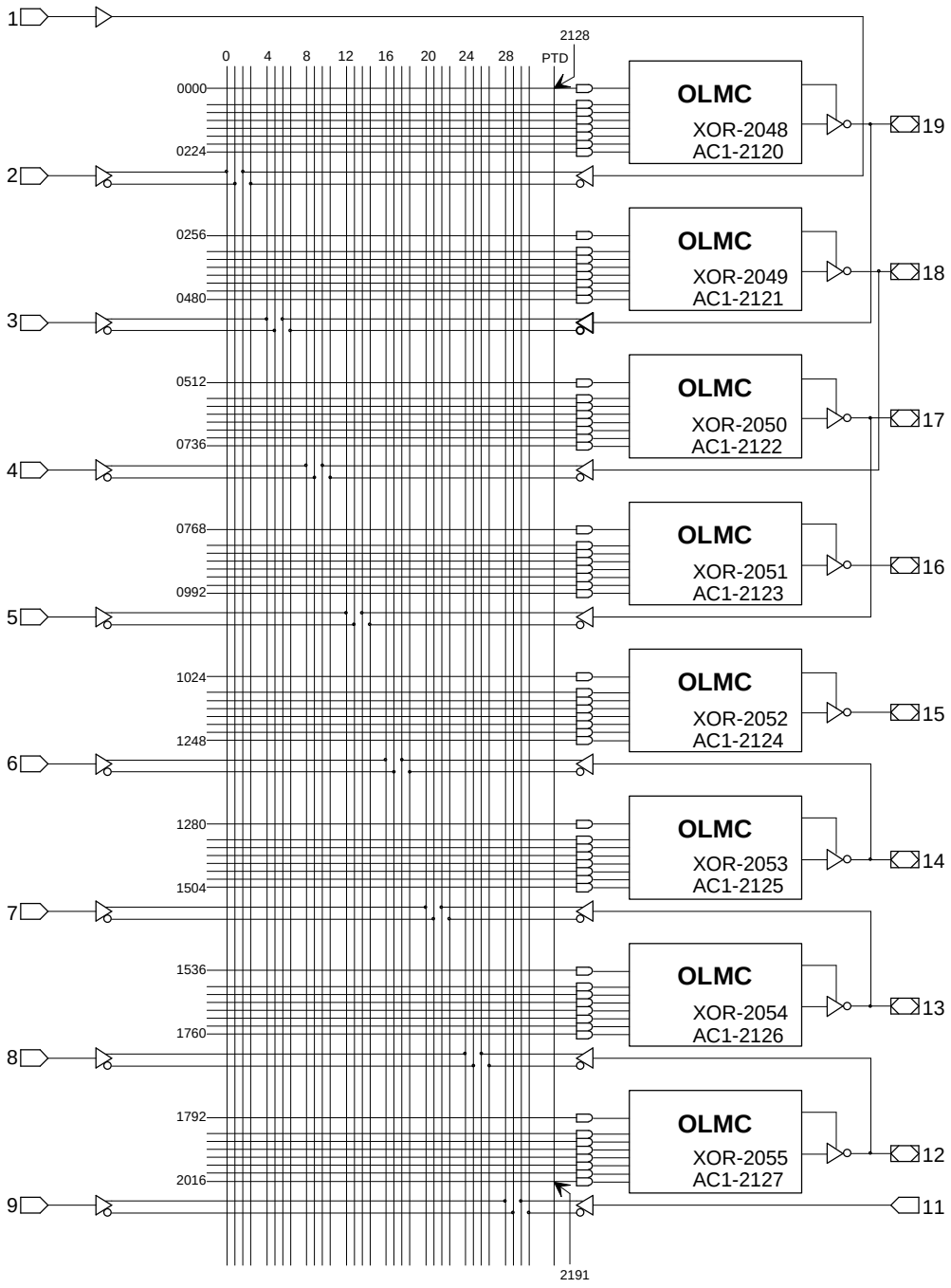
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 15 & 16 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

DIP & PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...	.... 2118, 2119
Byte 7 | Byte 6	.... Byte 1 | Byte 0

MSB LSB

SYN-2192
AC0-2193

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... –40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -5/-7	—	75	115	mA

INDUSTRIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -7	—	75	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION		COM -5 MIN.	COM -5 MAX.	COM -7 MIN.	COM -7 MAX.	IND -7 MIN.	IND -7 MAX.	UNITS
tpd	A	Input or I/O to Comb. Output	8 outputs switching	1	5	3	7.5	1	7.5	ns
			1 output switching	—	—	—	7	—	—	ns
tco	A	Clock to Output Delay		1	4	2	5	1	5	ns
tcf[2]	—	Clock to Feedback Delay		—	3	—	3	—	3	ns
tsu	—	Setup Time, Input or Feedback before Clock↑		3	—	7	—	7	—	ns
th	—	Hold Time, Input or Feedback after Clock↑		0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)		142.8	—	83.3	—	83.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)		166	—	100	—	100	—	MHz
	A	Maximum Clock Frequency with No Feedback		166	—	100	—	100	—	MHz
twh	—	Clock Pulse Duration, High		3	—	5	—	5	—	ns
twl	—	Clock Pulse Duration, Low		3	—	5	—	5	—	ns
ten	B	Input or I/O to Output Enabled		1	6	3	9	1	9	ns
	B	$\overline{OE}$ to Output Enabled		1	6	2	6	1	6	ns
tdis	C	Input or I/O to Output Disabled		1	5	2	9	1	9	ns
	C	$\overline{OE}$ to Output Disabled		1	5	1.5	6	1	6	ns

1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Descriptions section.
3) Refer to fmax Descriptions section. Characterized initially and after any design or process changes that may affect these parameters.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... –40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	24	mA
I_{OH}	High Level Output Current			—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C		–30	—	–150	mA
COMMERCIAL							
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -7/-10	—	75	115	mA
			L -15/-25	—	75	90	mA
			Q -15/-25	—	45	55	mA
INDUSTRIAL							
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -10/-15/-25	—	75	130	mA
			Q -20/-25	—	45	65	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM.	TEST COND[1].	DESCRIPTION		COM -7 MIN.	COM -7 MAX.	COM / IND -10 MIN.	COM / IND -10 MAX.	COM / IND -15 MIN.	COM / IND -15 MAX.	IND -20 MIN.	IND -20 MAX.	COM / IND -25 MIN.	COM / IND -25 MAX.	UNITS
tpd	A	Input or I/O to	8 outputs switching	3	7.5	3	10	3	15	3	20	3	25	ns
		Comb. Output	1 output switching	—	7	—	—	—	—	—	—	—	—	ns
tco	A	Clock to Output Delay		2	5	2	7	2	10	2	11	2	12	ns
tcf[2]	—	Clock to Feedback Delay		—	3	—	6	—	8	—	9	—	10	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑		7	—	10	—	12	—	13	—	15	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑		0	—	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)		83.3	—	58.8	—	45.5	—	41.6	—	37	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)		100	—	62.5	—	50	—	45.4	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback		100	—	62.5	—	62.5	—	50	—	41.6	—	MHz
twh	—	Clock Pulse Duration, High		5	—	8	—	8	—	10	—	12	—	ns
twl	—	Clock Pulse Duration, Low		5	—	8	—	8	—	10	—	12	—	ns
ten	B	Input or I/O to Output Enabled		3	9	3	10	—	15	—	20	—	25	ns
	B	$\overline{OE}$ to Output Enabled		2	6	2	10	—	15	—	18	—	20	ns
tdis	C	Input or I/O to Output Disabled		2	9	2	10	—	15	—	20	—	25	ns
	C	$\overline{OE}$ to Output Disabled		1.5	6	1.5	10	—	15	—	18	—	20	ns

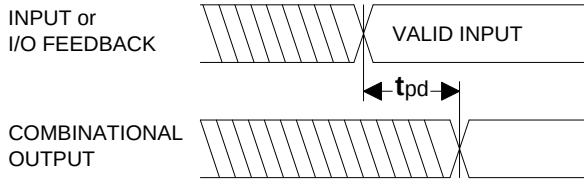
1) Refer to Switching Test Conditions section.
2) Calculated from fmax with internal feedback. Refer to fmax Descriptions section.
3) Refer to fmax Descriptions section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

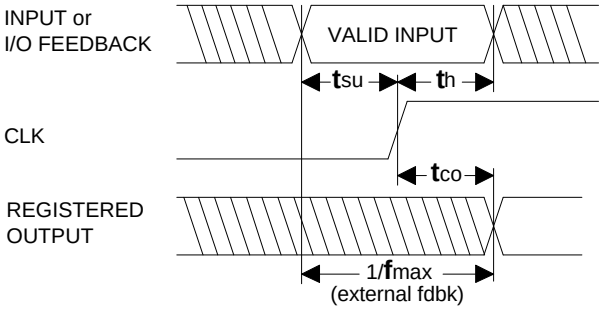
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

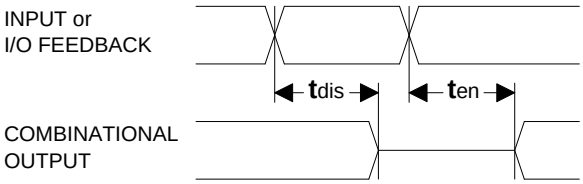
SWITCHING WAVEFORMS



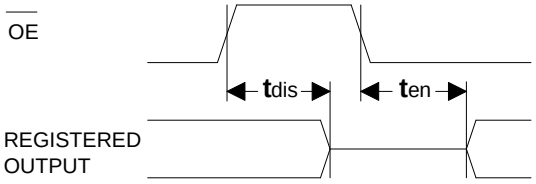
Combinatorial Output



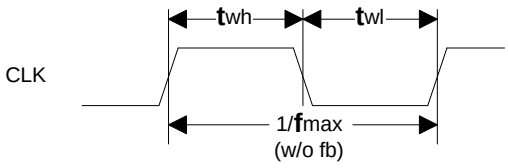
Registered Output



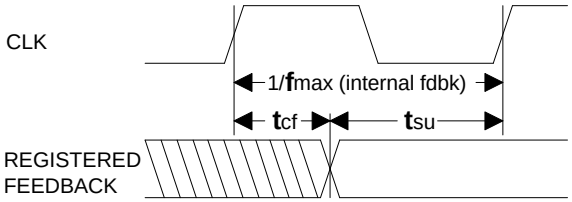
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

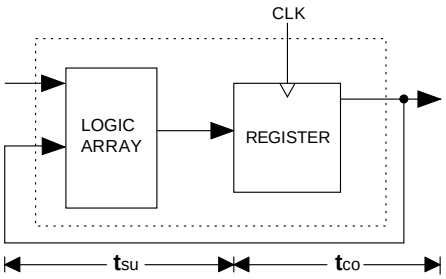


Clock Width



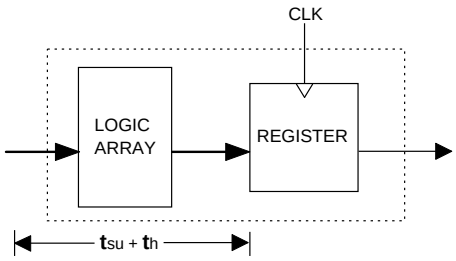
fmax with Feedback

fmax DESCRIPTIONS



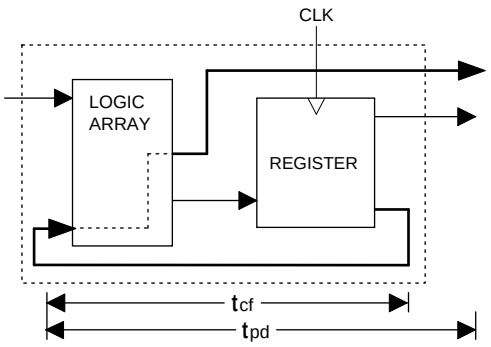
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



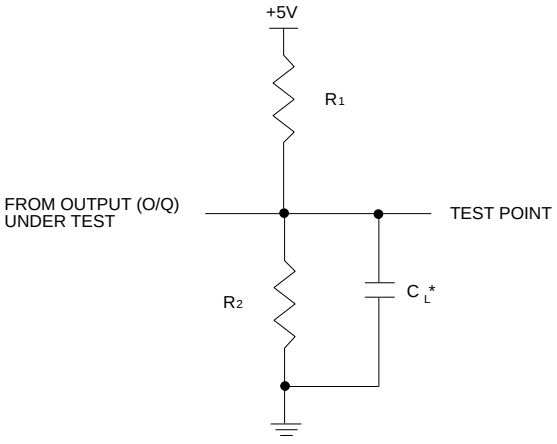
fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

SWITCHING TEST CONDITIONS

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	GAL16V8B	2 – 3ns 10% – 90%
	GAL16V8C	1.5ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See Figure

3-state levels are measured 0.5V from steady-state active level.



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL16V8B Output Load Conditions (see figure)

Test Condition		R1	R2	CL
A		200Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF

GAL16V8C Output Load Conditions (see figure)

Test Condition		R1	R2	CL
A		200Ω	200Ω	50pF
B	Active High	∞	200Ω	50pF
	Active Low	200Ω	200Ω	50pF
C	Active High	∞	200Ω	5pF
	Active Low	200Ω	200Ω	5pF

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL16V8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

SECURITY CELL

A security cell is provided in the GAL16V8 devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL16V8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias minimizes the potential of latch-up caused by negative input undershoots. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups in order to eliminate latch-up due to output overshoots.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

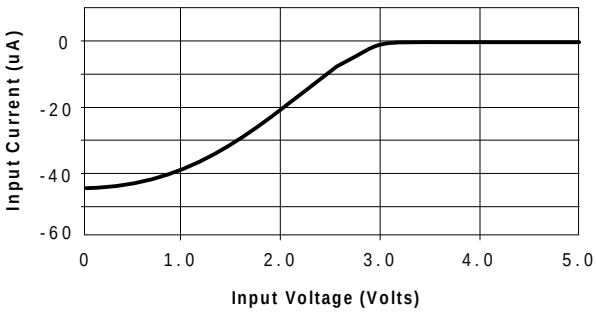
GAL16V8 devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

INPUT BUFFERS

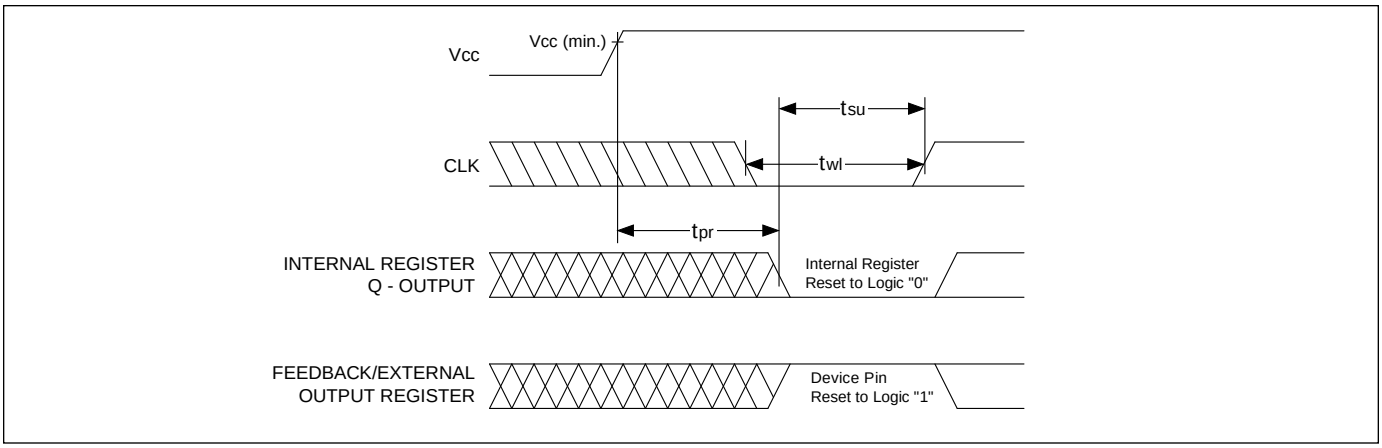
GAL16V8 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL16V8 input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or Ground. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Pull-up Characteristic

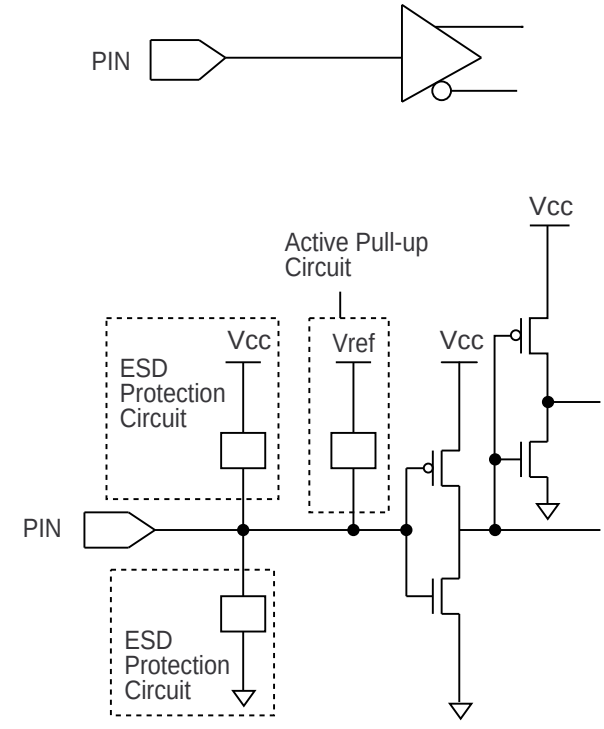


POWER-UP RESET



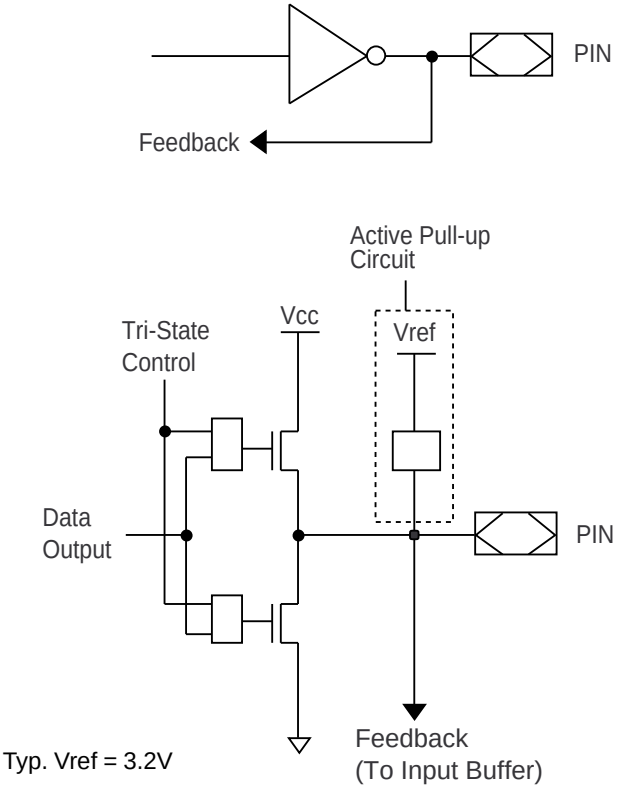
Circuitry within the GAL16V8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the device. First, the V_{CC} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typ. Vref = 3.2V

Typical Input

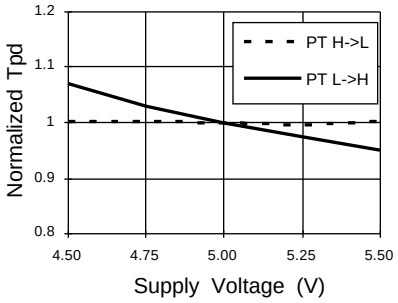


Typ. Vref = 3.2V

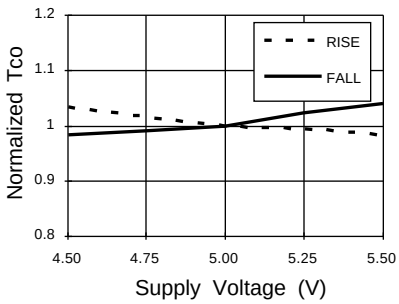
Typical Output

GAL 16V8C-5/-7: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

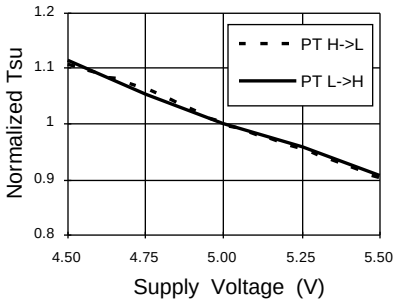
Normalized Tpd vs Vcc



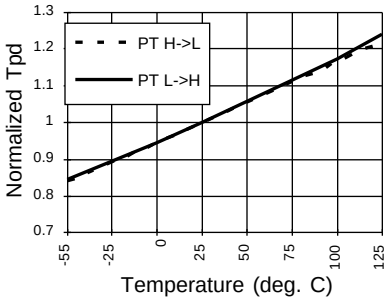
Normalized Tco vs Vcc



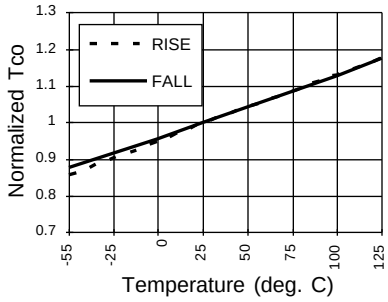
Normalized Tsu vs Vcc



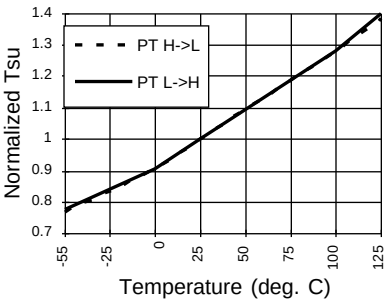
Normalized Tpd vs Temp



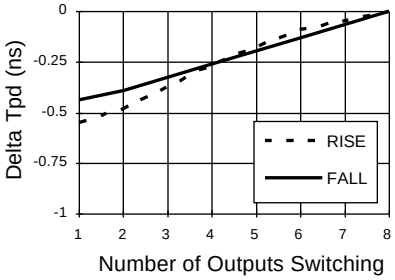
Normalized Tco vs Temp



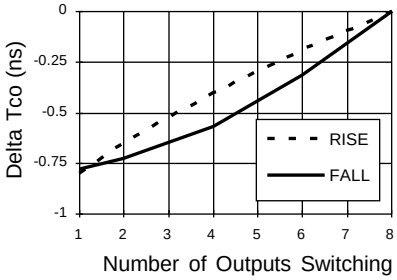
Normalized Tsu vs Temp



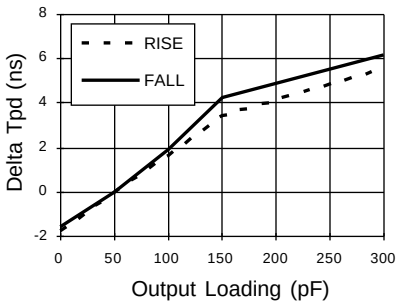
Delta Tpd vs # of Outputs Switching



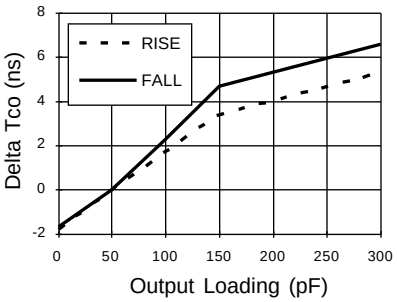
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

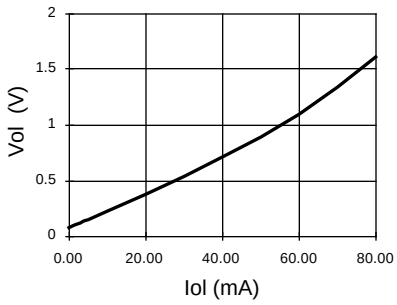


Delta Tco vs Output Loading

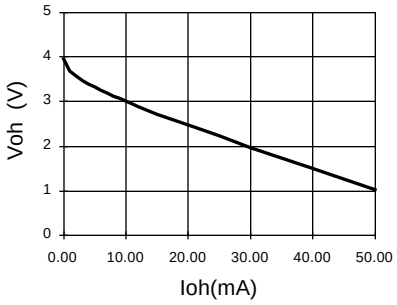


GAL 16V8C-5/-7: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

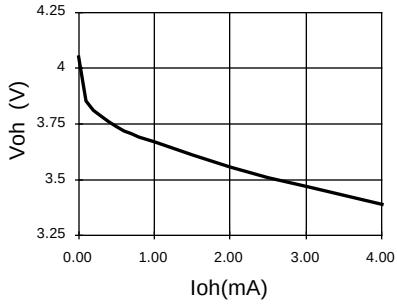
Vol vs Iol



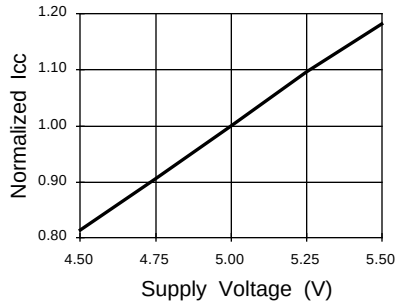
Voh vs Ioh



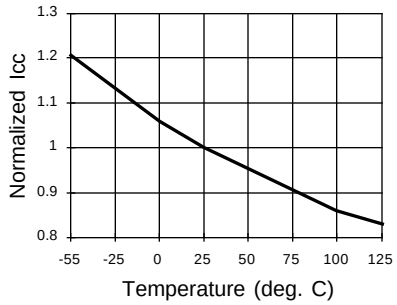
Voh vs Ioh



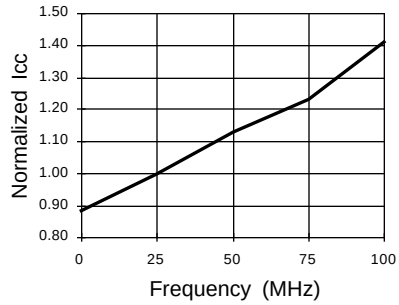
Normalized Icc vs Vcc



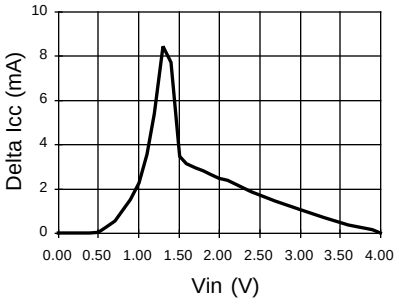
Normalized Icc vs Temp



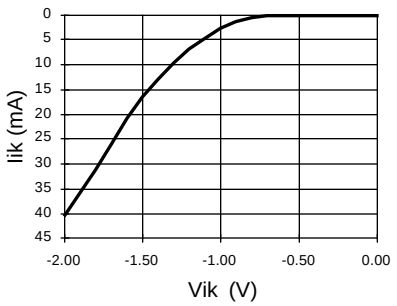
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

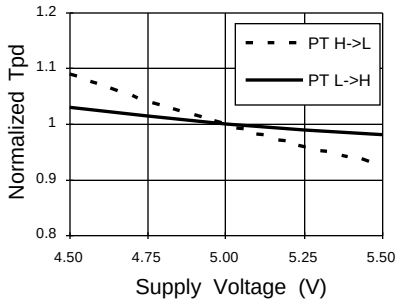


Input Clamp (Vik)

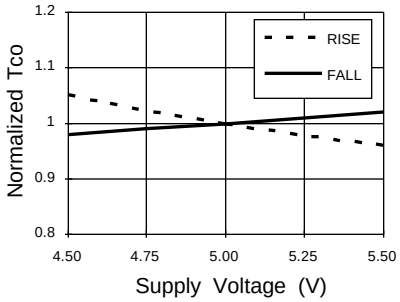


GAL 16V8B-7/-10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

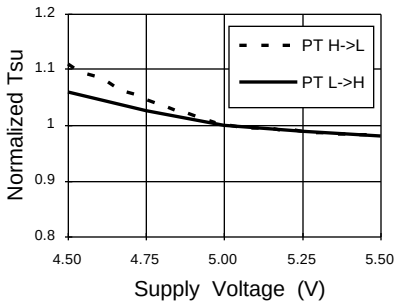
Normalized Tpd vs Vcc



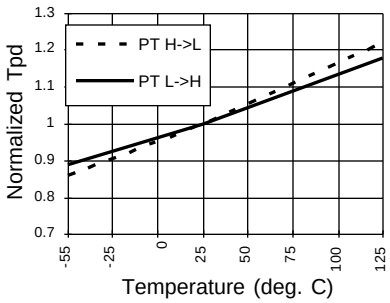
Normalized Tco vs Vcc



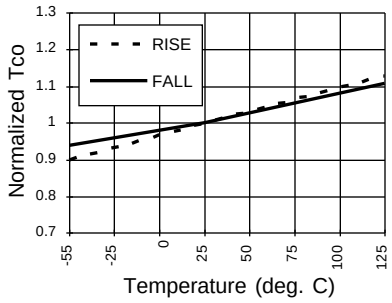
Normalized Tsu vs Vcc



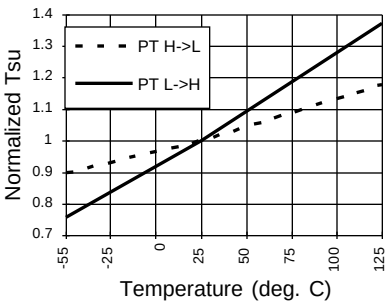
Normalized Tpd vs Temp



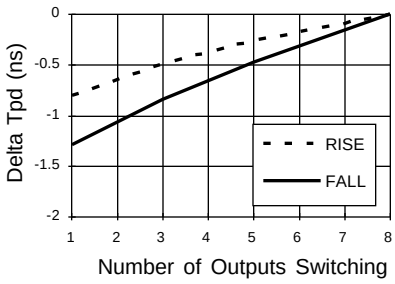
Normalized Tco vs Temp



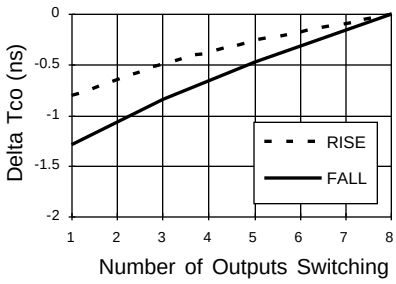
Normalized Tsu vs Temp



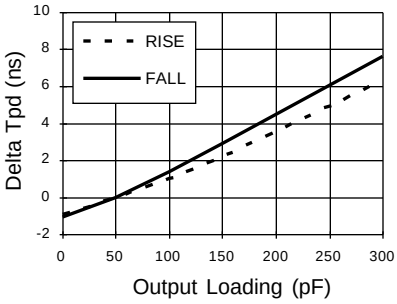
Delta Tpd vs # of Outputs Switching



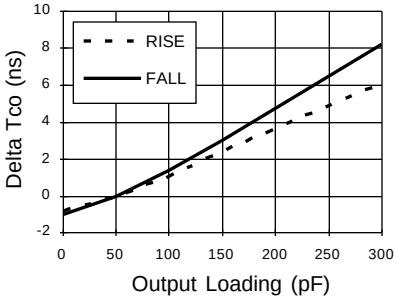
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

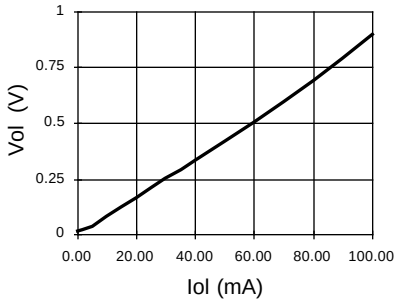


Delta Tco vs Output Loading

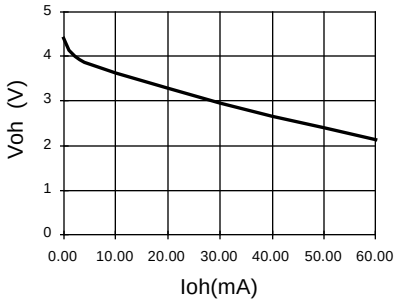


GAL 16V8B-7/-10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

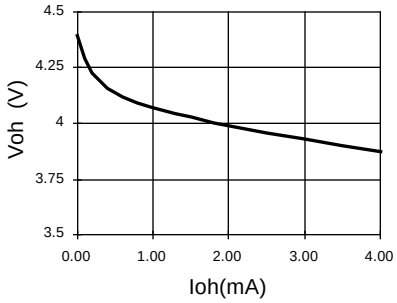
Vol vs Iol



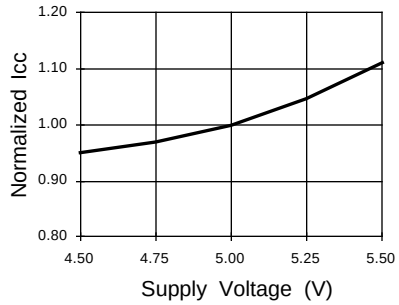
Voh vs Ioh



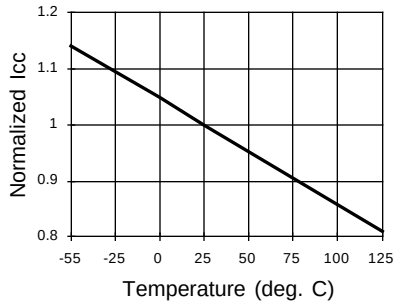
Voh vs Ioh



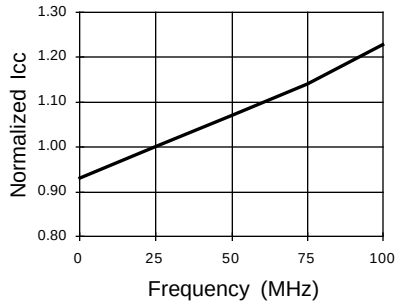
Normalized Icc vs Vcc



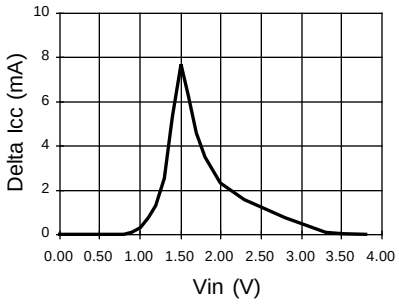
Normalized Icc vs Temp



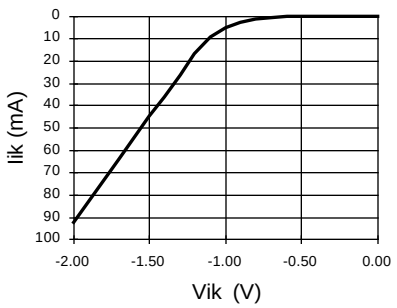
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

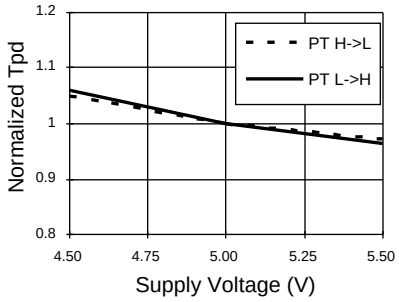


Input Clamp (Vik)

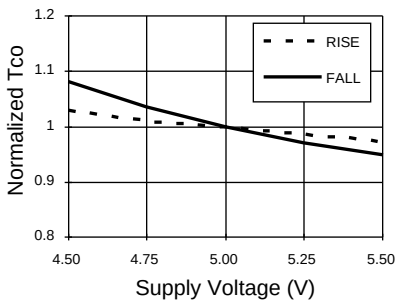


GAL 16V8B-15/-25: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

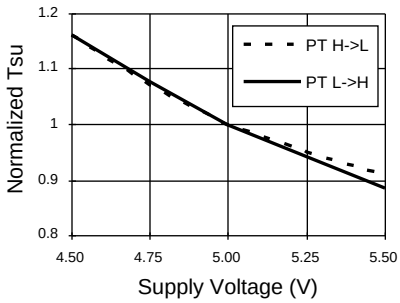
Normalized Tpd vs Vcc



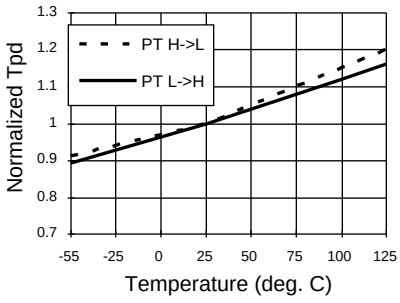
Normalized Tco vs Vcc



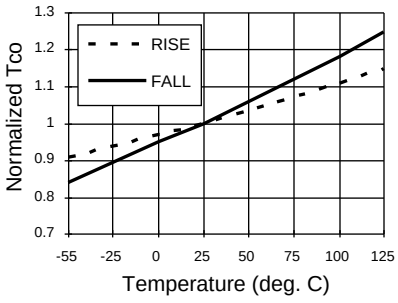
Normalized Tsu vs Vcc



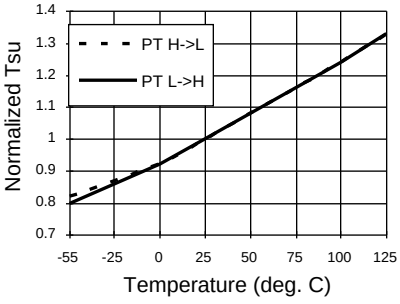
Normalized Tpd vs Temp



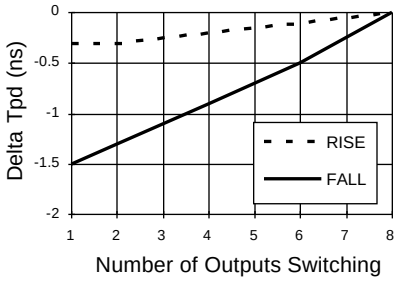
Normalized Tco vs Temp



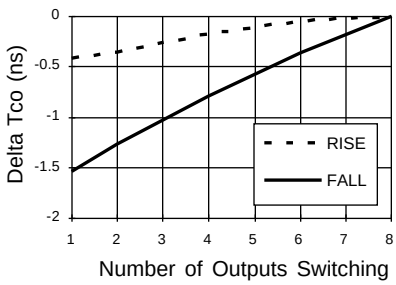
Normalized Tsu vs Temp



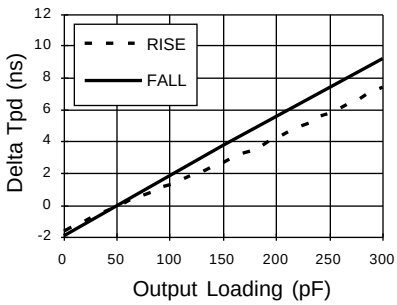
Delta Tpd vs # of Outputs Switching



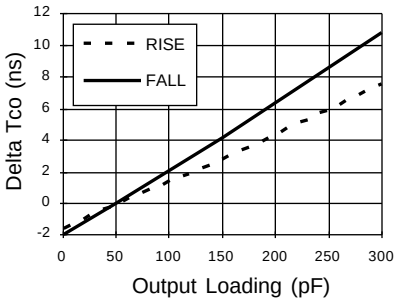
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

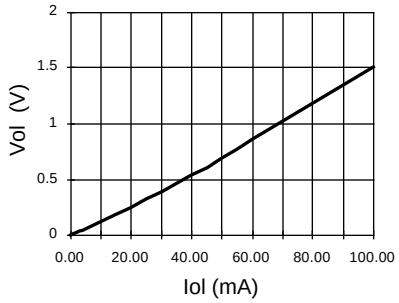


Delta Tco vs Output Loading

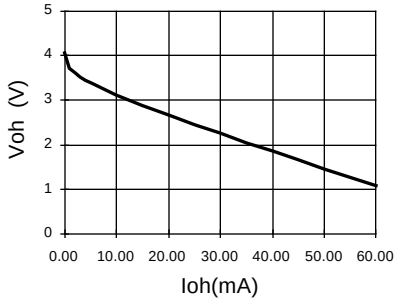


GAL 16V8B-15/-25: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

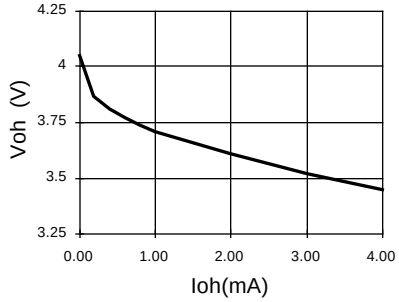
Vol vs Iol



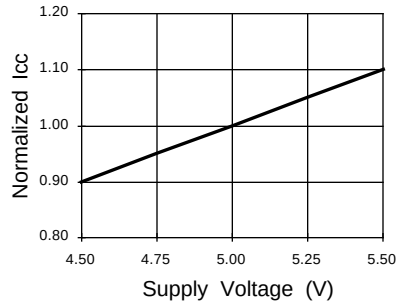
Voh vs Ioh



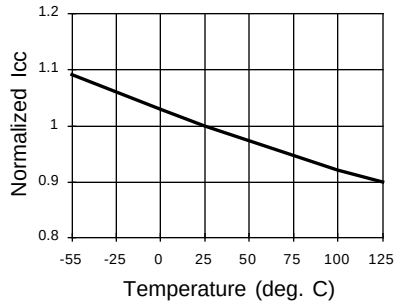
Voh vs Ioh



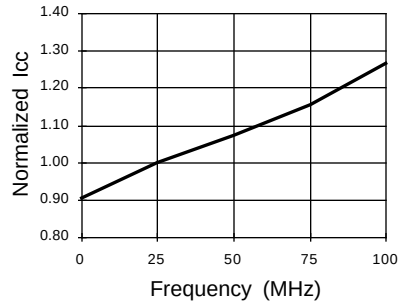
Normalized Icc vs Vcc



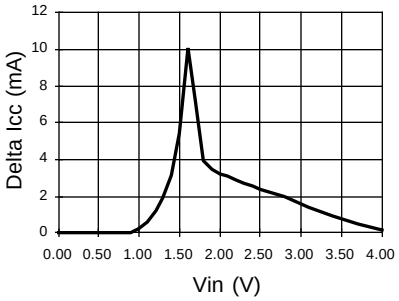
Normalized Icc vs Temp



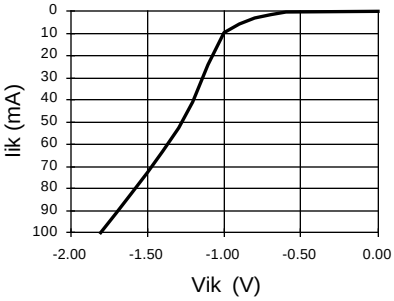
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



GAL16VP8

High-Speed E²CMOS PLD Generic Array Logic™

FEATURES

- **HIGH DRIVE E²CMOS® GAL® DEVICE**
  - **— TTL Compatible 64 mA Output Drive**
  - **— 15 ns Maximum Propagation Delay**
  - **— Fmax = 80 MHz**
  - **— 10 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **ENHANCED INPUT AND OUTPUT FEATURES**
  - **— Schmitt Trigger Inputs**
  - **— Programmable Open-Drain or Totem-Pole Outputs**
  - **— Active Pull-Ups on All Inputs and I/O pins**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Architecturally Compatible with Standard GAL16V8**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— Ideal for Bus Control & Bus Arbitration Logic**
  - **— Bus Address Decode Logic**
  - **— Memory Address, Data and Control Circuits**
  - **— DMA Control**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

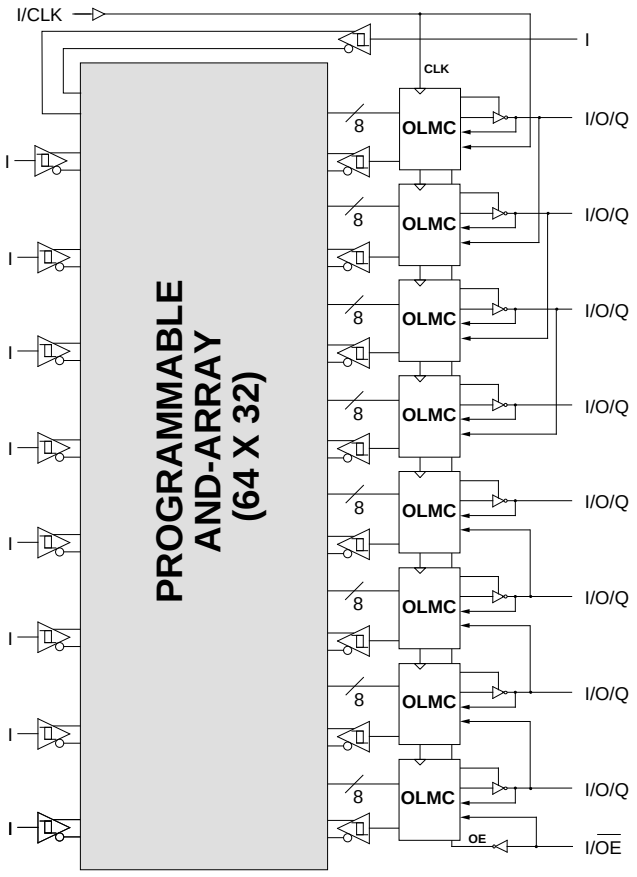
DESCRIPTION

The GAL16VP8, with 64 mA drive capability and 15 ns maximum propagation delay time is ideal for Bus and Memory control applications. The GAL16VP8 is manufactured using Lattice Semiconductor's advanced E²CMOS process which combines CMOS with Electrically Erasable (E²) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

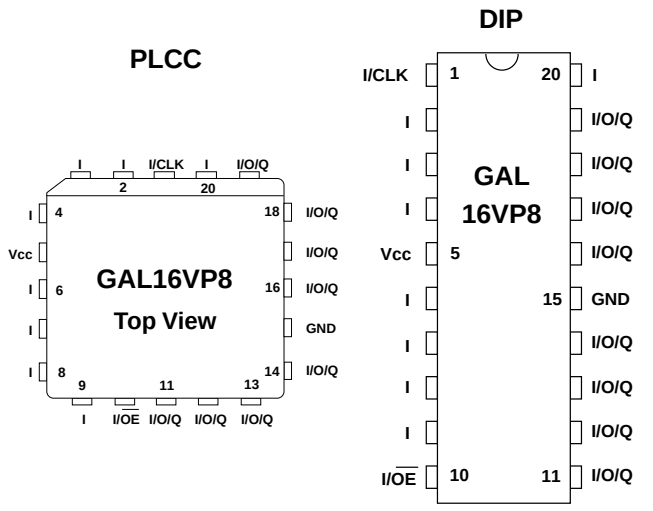
System bus and memory interfaces require control logic before driving the bus or memory interface signals. The GAL16VP8 combines the familiar GAL16V8 architecture with bus drivers as its outputs. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The 64mA output drive eliminates the need for additional devices to provide bus driving capability.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



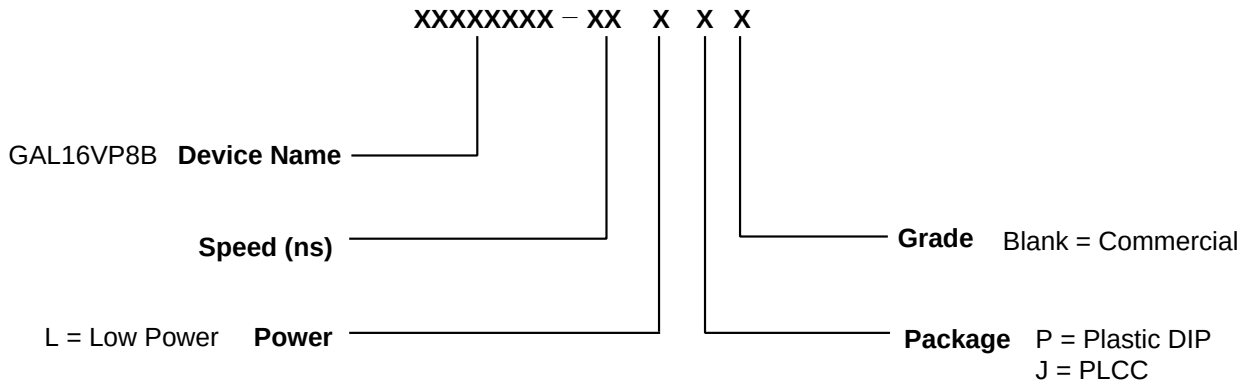
LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL16VP8 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	8	10	115	GAL16VP8B-15LP	20-Pin Plastic DIP
			115	GAL16VP8B-15LJ	20-Lead PLCC
25	10	15	115	GAL16VP8B-25LP	20-Pin Plastic DIP
			115	GAL16VP8B-25LJ	20-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 and AC2 bit of each of the macrocells controls the input/output and totem-pole/open-drain configuration. These two global and 24 individual architecture bits define all possible configurations in a GAL16VP8. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. Most compilers also have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.
In **registered mode** pin 1 and pin 10 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 10 become dedicated inputs and use the feedback paths of pin19 and pin 11 respectively. Because of this feedback path usage, pin19 and pin 11 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 14 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

In addition to the architecture configurations, the logic compiler software also supports configuration of either totem-pole or open-drain outputs. The actual architecture bit configuration, again, is transparent to the user with the default configuration being the standard totem-pole output.

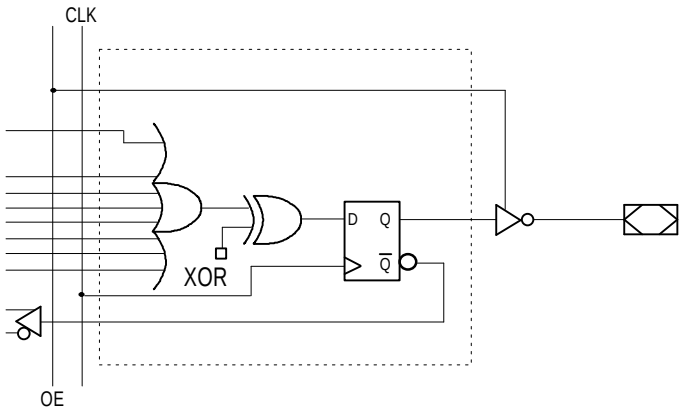
REGISTERED MODE

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

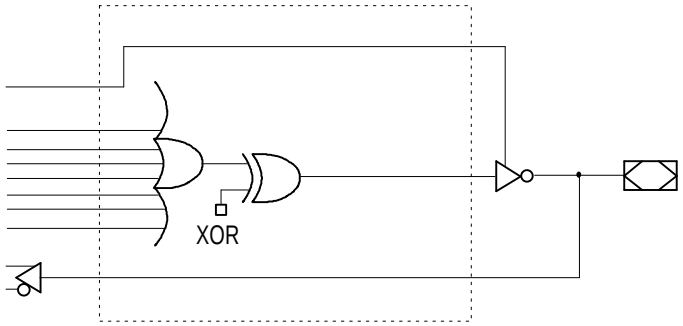
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pin 1 controls common CLK for the registered outputs.
- Pin 10 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 10 are permanently configured as CLK & $\overline{OE}$.



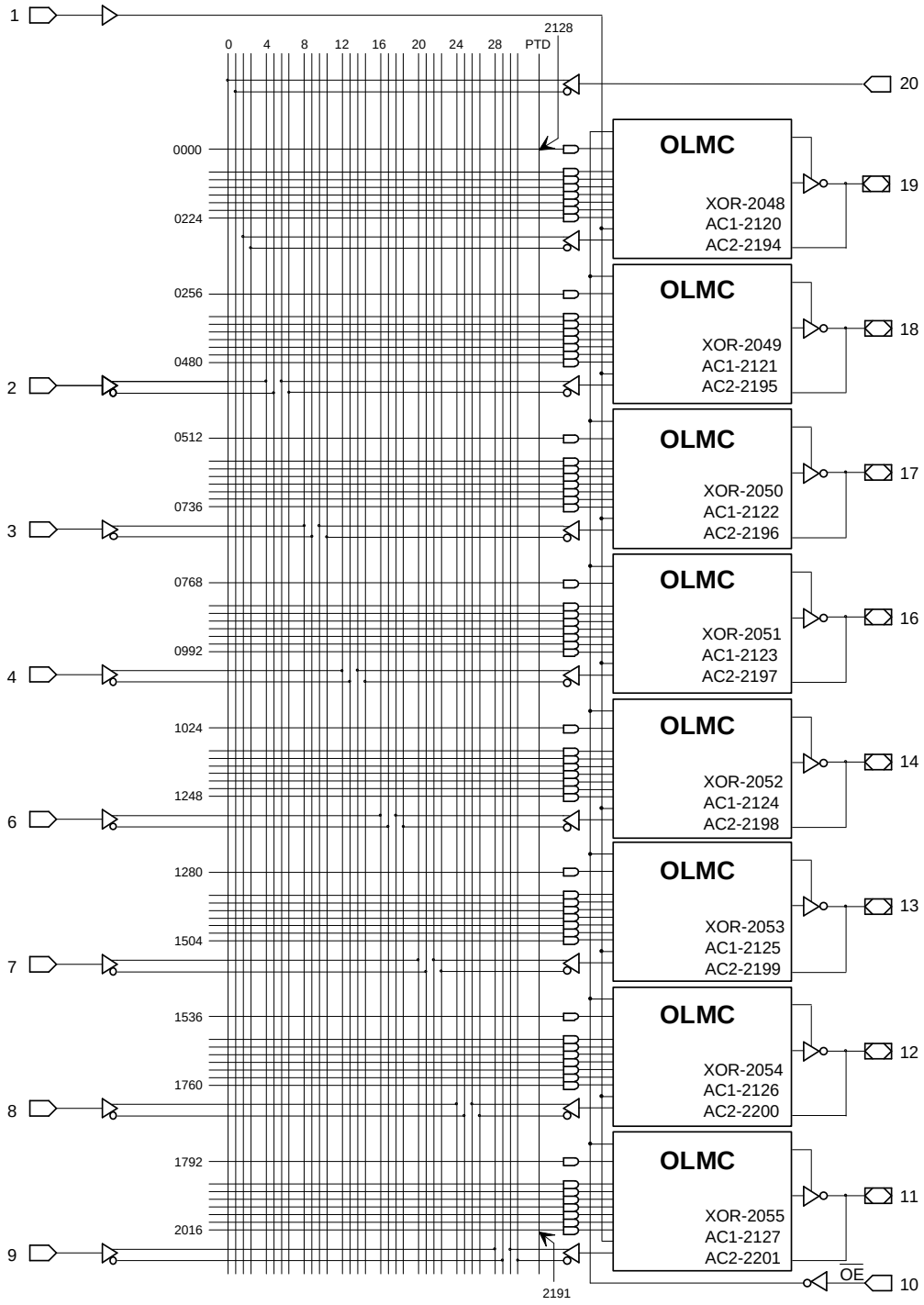
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pin 1 & Pin 10 are permanently configured as CLK & $\overline{OE}$.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

DIP and PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2055, ...	.... 2118, 2119
Byte7 | Byte6	.... Byte1 | Byte0

MSB LSB

SYN-2192
AC0-2193

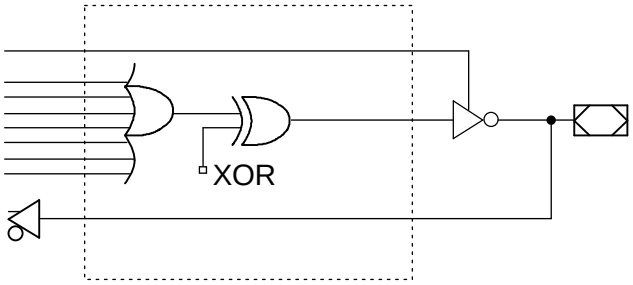
COMPLEX MODE

In the Complex mode, macrocells are configured as output only or I/O functions.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 11 & 19) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

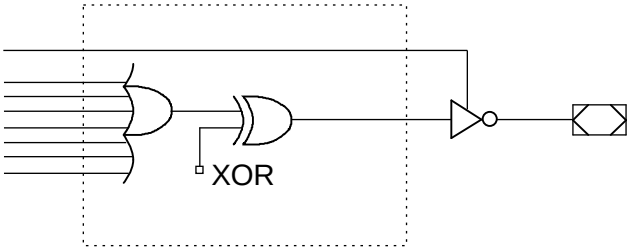
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 10 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pin 12 through Pin 18 are configured to this function.



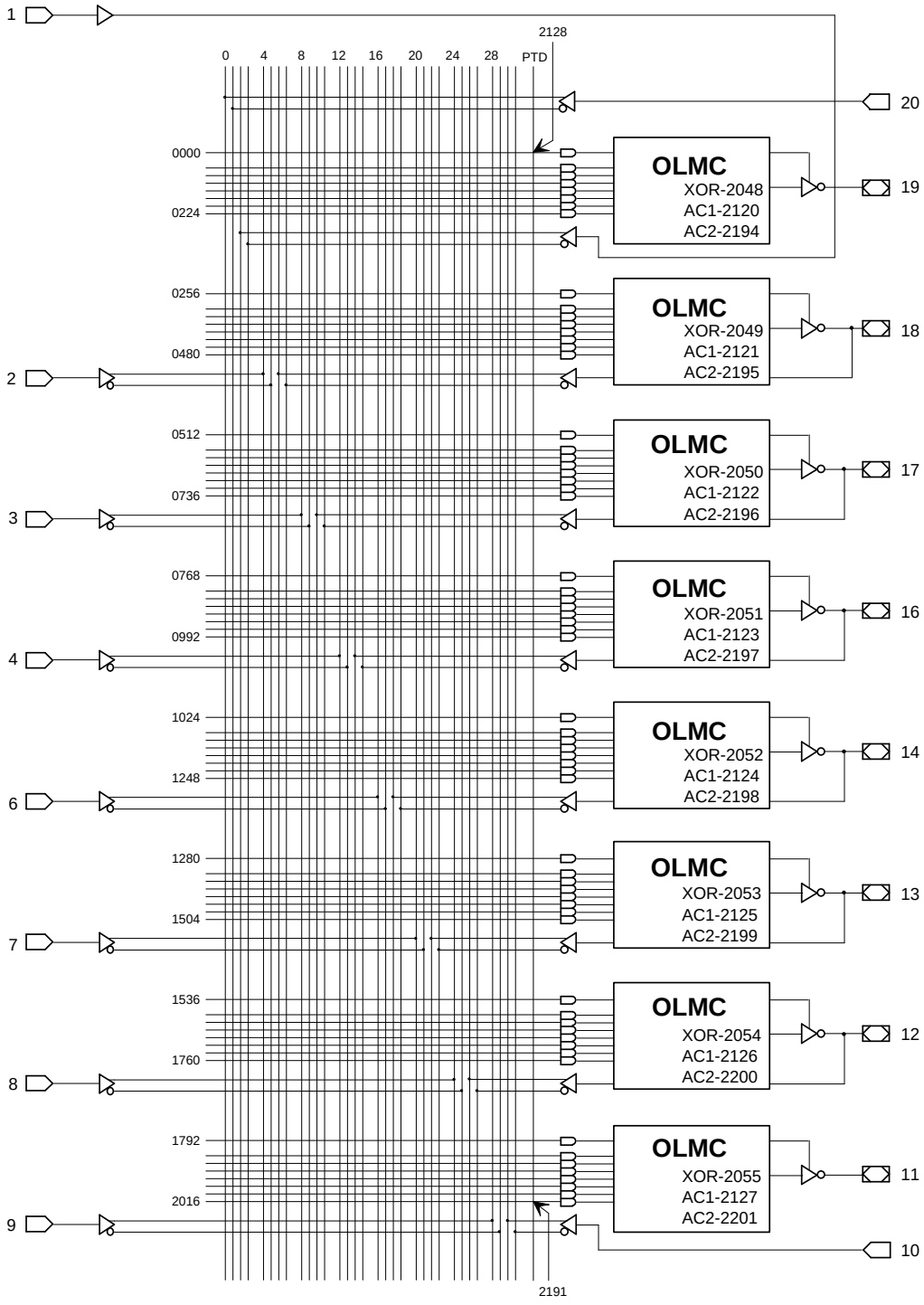
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pin 11 and Pin 19 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

DIP and PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2055, ...	.... 2118, 2119
Byte7 | Byte6	.... Byte1 | Byte0

MSB LSB

SYN-2192
AC0-2193

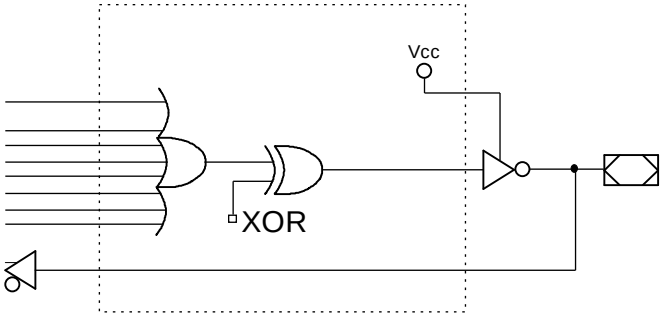
SIMPLE MODE

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

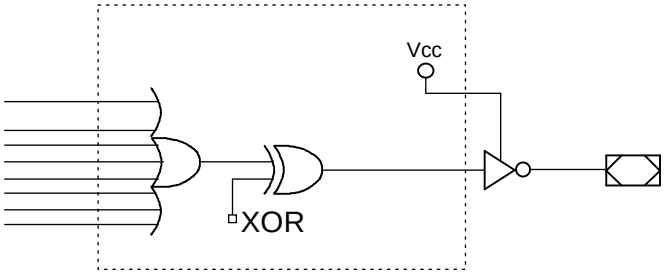
Pins 1 and 10 are always available as data inputs into the AND array. The center two macrocells (pins 14 & 16) cannot be used in the input configuration.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



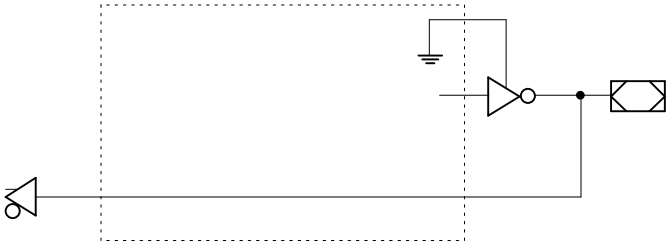
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- All OLMC **except** pins 14 & 16 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pins 14 & 16 are permanently configured to this function.



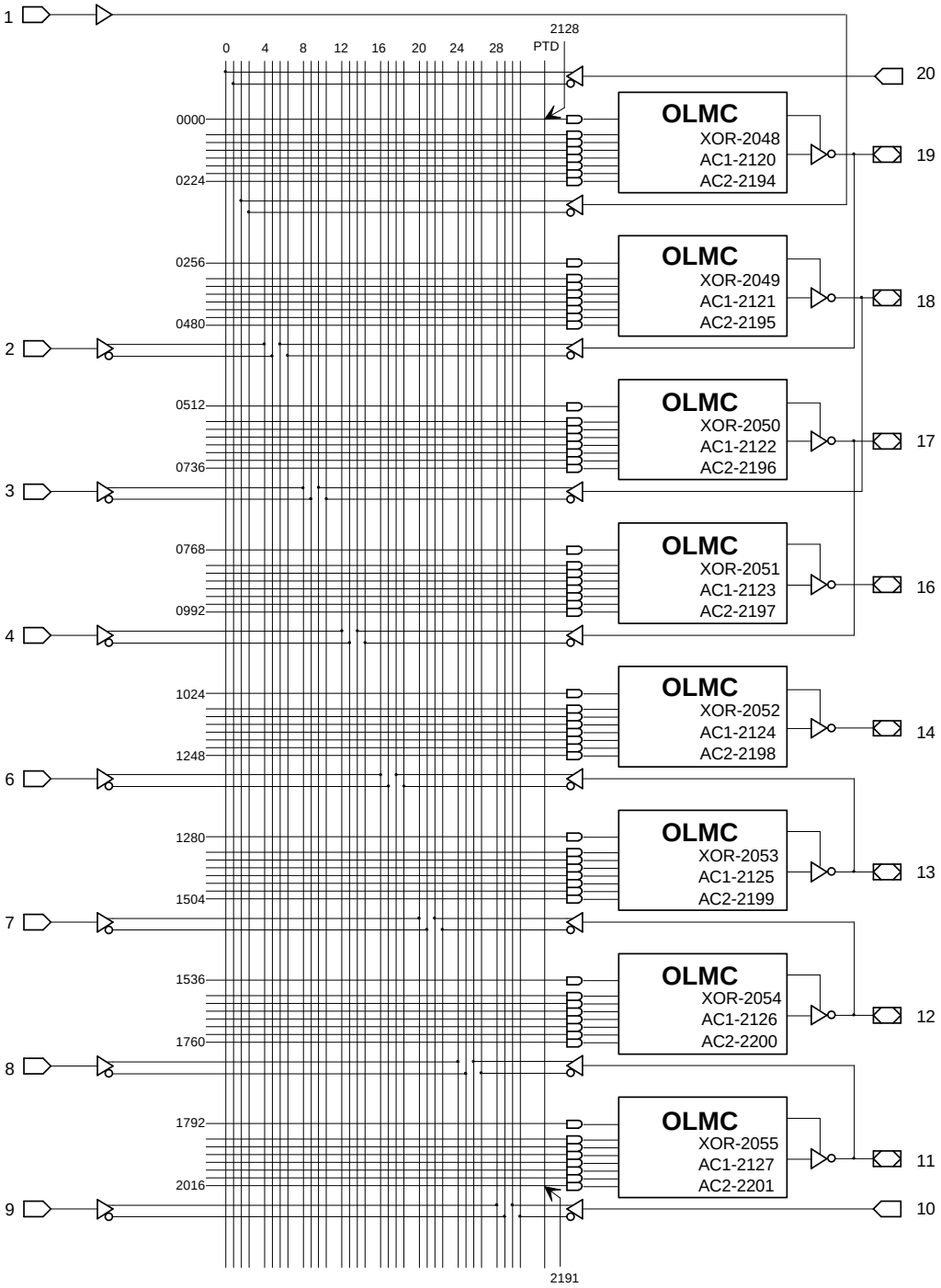
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- All OLMC **except** pins 14 & 16 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

DIP and PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2055, ...		.... 2118, 2119
Byte7	Byte6	.... Byte1 Byte0

MSB LSB

SYN-2192
AC0-2193

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[4]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
V_{I}[1]	Input Clamp Voltage	Vcc = Min. I_{IN} = –32mA	—		–1.2	V
I_{IL}[2]	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	64	mA
I_{OH}	High Level Output Current		—	—	–32	mA
I_{OS}[3]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–60	—	–400	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -15/-25	—	90	115	mA

1) Guaranteed but not 100% tested.
2) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
3) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
4) Typical values are at Vcc = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -15		COM -25		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinational Output	3	15	3	25	ns
tco	A	Clock to Output Delay	2	10	2	15	ns
tcf[2]	—	Clock to Feedback Delay	—	4.5	—	10	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	8	—	10	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	55.5	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	80	—	50	—	MHz
	A	Maximum Clock Frequency with No Feedback	80	—	50	—	MHz
twh	—	Clock Pulse Duration, High	6	—	10	—	ns
twl	—	Clock Pulse Duration, Low	6	—	10	—	ns
ten	B	Input or I/O to Output Enabled	—	15	—	20	ns
	B	$\overline{OE}$ to Output Enabled	—	12	—	15	ns
tdis	C	Input or I/O to Output Disabled	—	15	—	20	ns
	C	$\overline{OE}$ to Output Disabled	—	12	—	15	ns

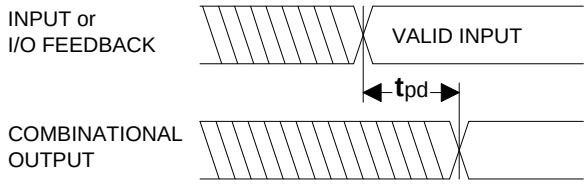
1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Specification section.
3) Refer to fmax Specification section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

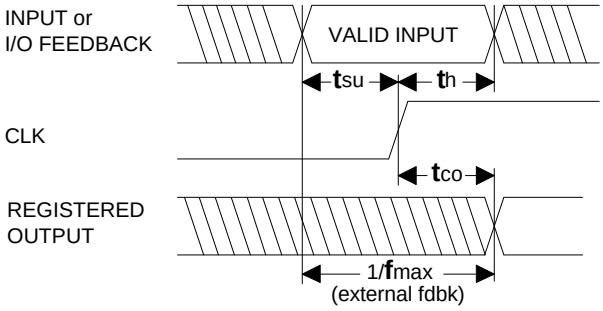
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	15	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

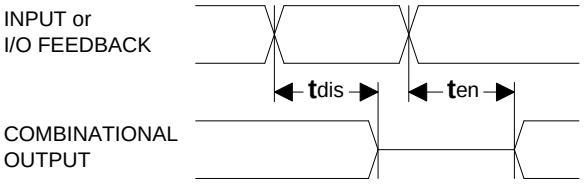
SWITCHING WAVEFORMS



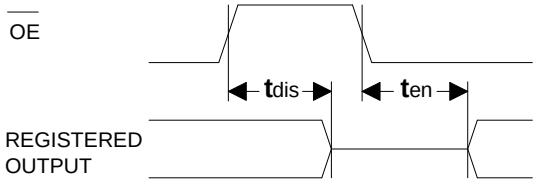
Combinatorial Output



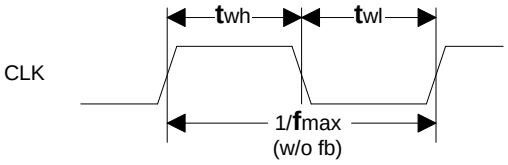
Registered Output



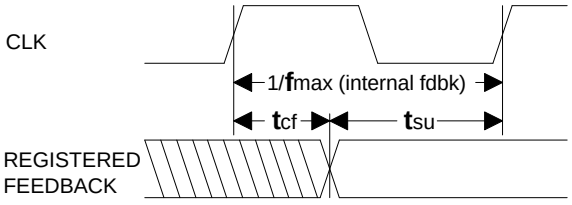
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

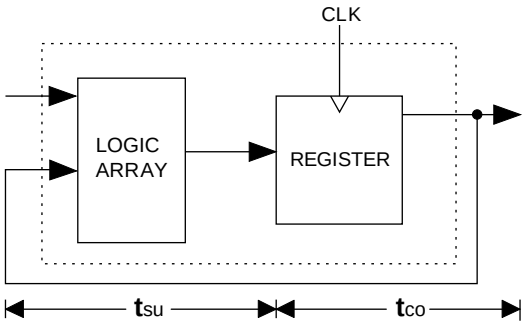


Clock Width



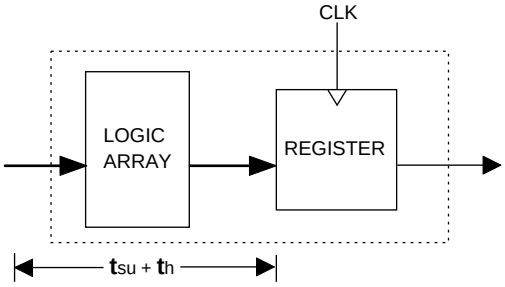
fmax with Feedback

fmax DESCRIPTIONS



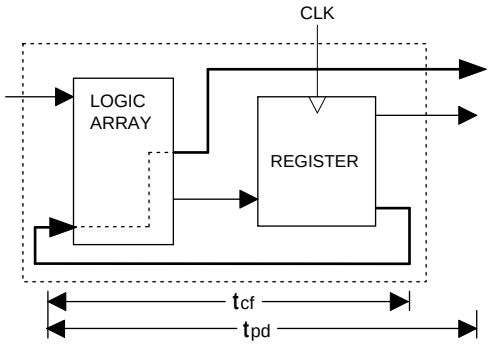
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

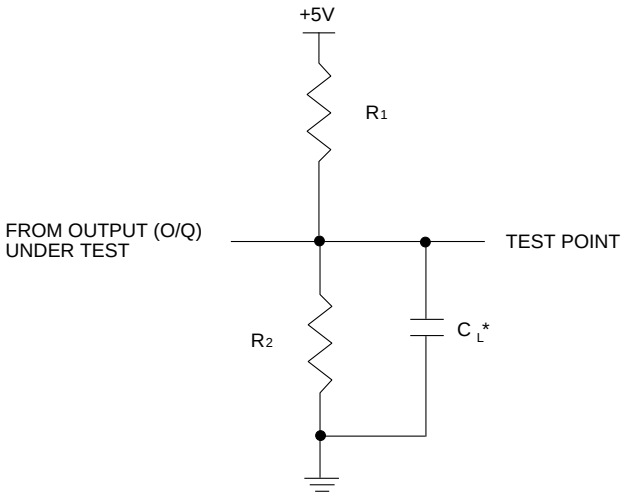
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R1	R2	CL
A		500Ω	500Ω	50pF
B	Active High	∞	500Ω	50pF
	Active Low	500Ω	500Ω	50pF
C	Active High	∞	500Ω	5pF
	Active Low	500Ω	500Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL16VP8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

SECURITY CELL

The security cell is provided on all GAL16VP8 devices to prevent unauthorized copying of the array patterns. Once programmed, the circuitry enabling array is disabled, preventing further programming or verification of the array. The cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. Signature data is always available to the user.

LATCH-UP PROTECTION

GAL16VP8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

BULK ERASE MODE

During a programming cycle, a clear function performs a bulk erase of the array and the architecture word. In addition, the electronic signature word and the security cell are erased. This mode resets a previously configured device back to its original state, which is all JEDEC ones.

SCHMITT TRIGGER INPUTS

One of the enhancements of the GAL16VP8 for bus interface logic implementation is input hysteresis. The threshold of the positive going edge is 1.5V, while the threshold of the negative going edge is 1.3V. This provides a typical hysteresis of 200mV between positive and negative transitions of the inputs.

HIGH DRIVE OUTPUTS

All eight outputs of the GAL16VP8 are capable of driving 64 mA loads when driving low and 32 mA loads when driving high. Near symmetrical high and low output drive capability provides small skews between high-to-low and low-to-high output transitions.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

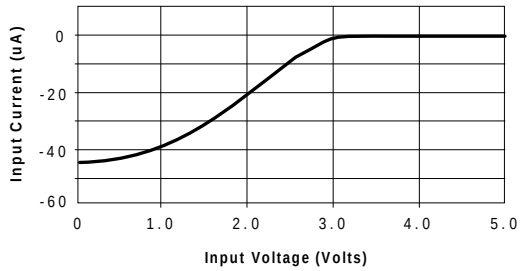
The GAL16VP8 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing.
If necessary, approved GAL programmers capable of executing test vectors can perform output register preload automatically.

INPUT BUFFERS

GAL16VP8 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

GAL16VP8 input buffers have active pull-ups within their input structure. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

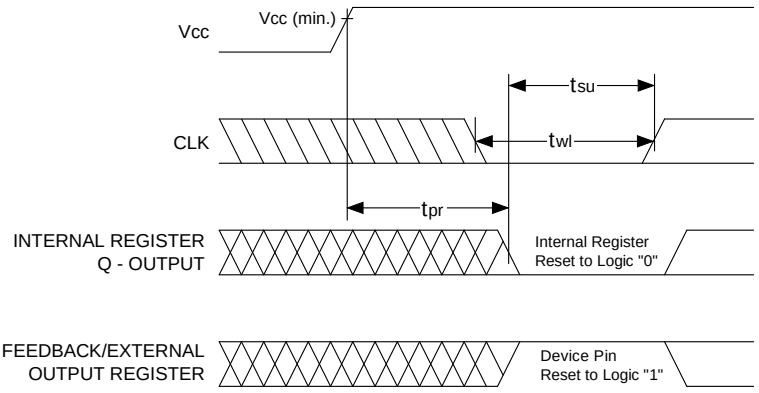
Typical Input Pull-up Characteristic



PROGRAMMABLE OPEN-DRAIN OUTPUTS

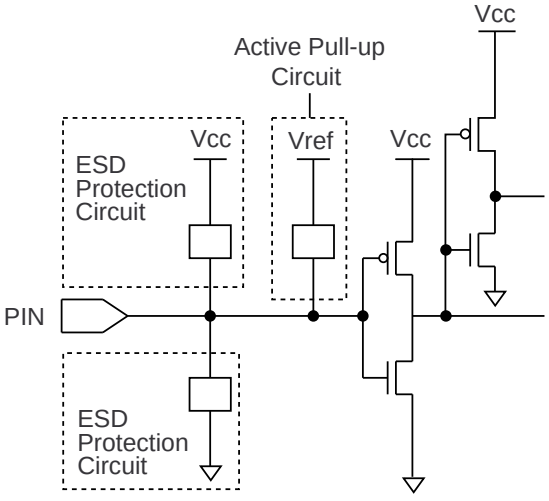
In addition to the standard GAL16V8 type configuration, the outputs of the GAL16VP8 are individually programmable either as a standard totempole output or an open-drain output. The totempole output drives the specified V_{OH} and V_{OL} levels whereas the open-drain output drives only the specified V_{OL}. The V_{OH} level on the open-drain ouput depends on the external loading and pull-up. This output configuration is controlled by the AC2 fuse. When AC2 cell is erased (JEDEC "1") the output is configured as a totempole output and when AC2 cell is programmed (JEDEC "0") the output is configured as an open-drain. The default configuration when the device is in bulk erased state is totempole configuration. The AC2 fuses associated with each of the outputs is included in all of the logic diagrams.

POWER-UP RESET



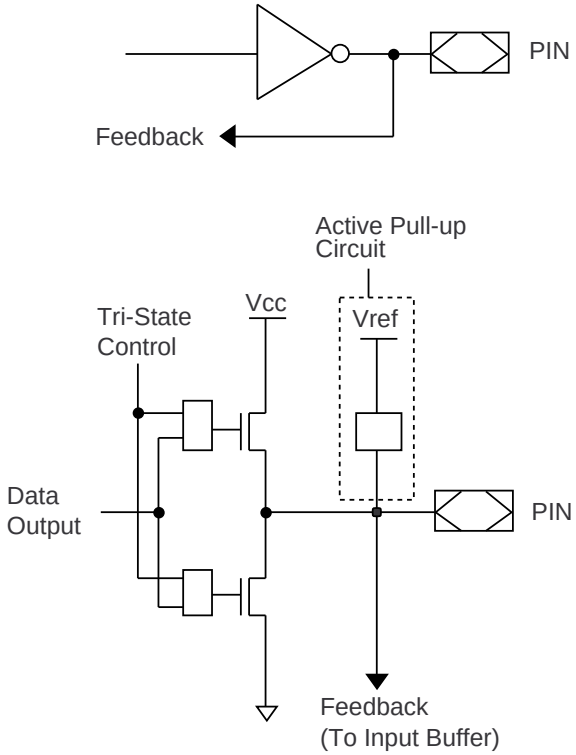
Circuitry within the GAL16VP8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL16VP8. First, the V_{CC} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Vref = 3.1V

Typical Input

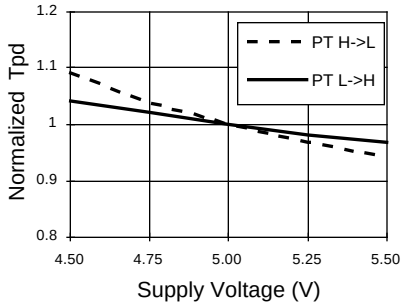


Vref = 3.1V

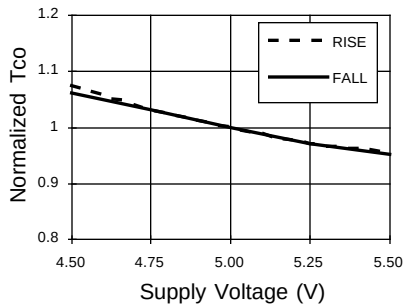
Typical Output

TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

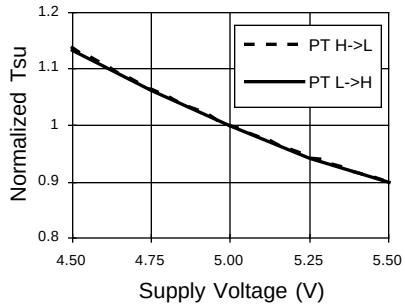
Normalized Tpd vs Vcc



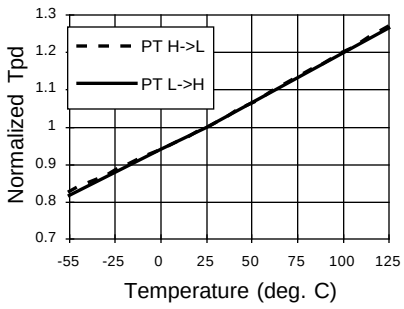
Normalized Tco vs Vcc



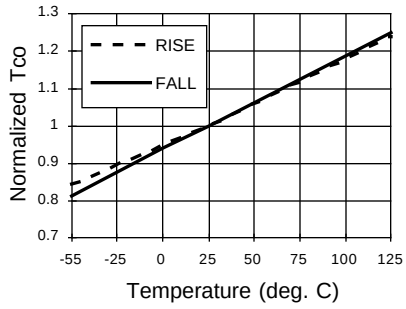
Normalized Tsu vs Vcc



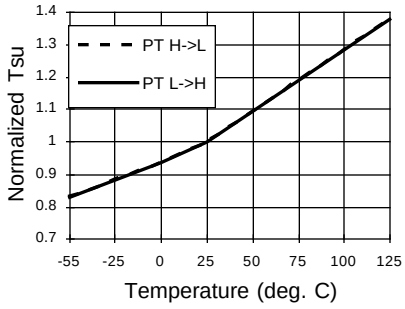
Normalized Tpd vs Temp



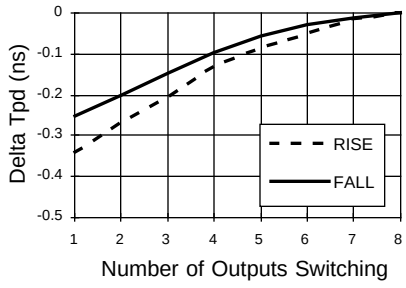
Normalized Tco vs Temp



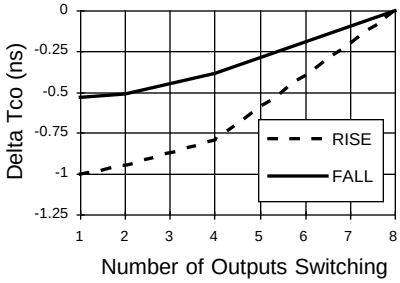
Normalized Tsu vs Temp



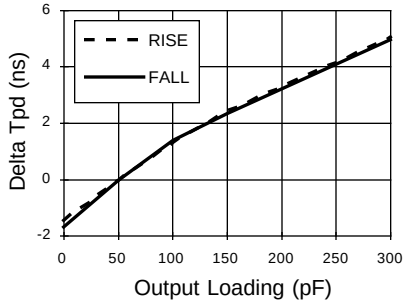
Delta Tpd vs # of Outputs Switching



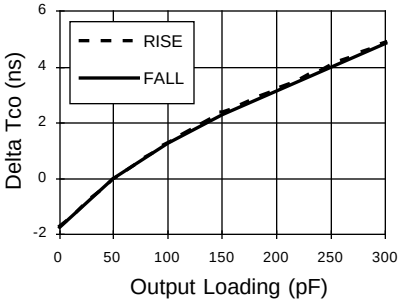
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

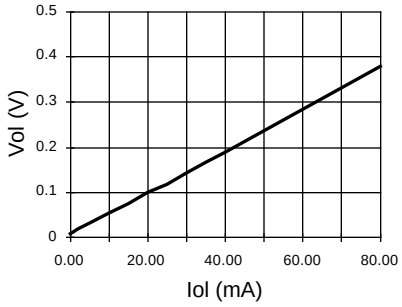


Delta Tco vs Output Loading

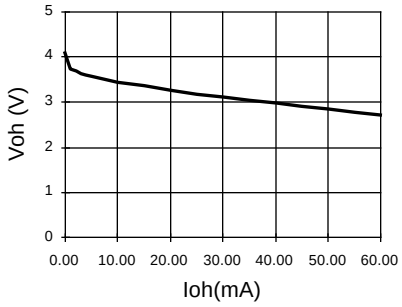


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

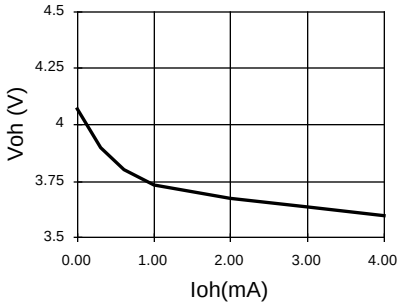
Vol vs Iol



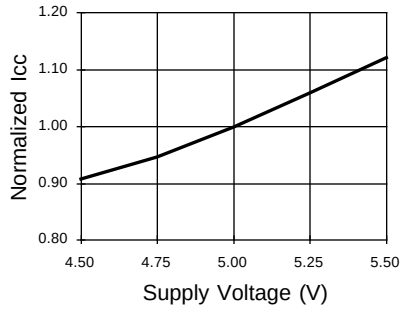
Voh vs Ioh



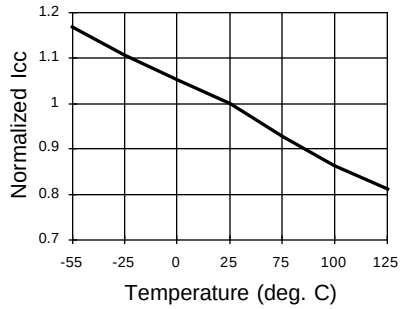
Voh vs Ioh



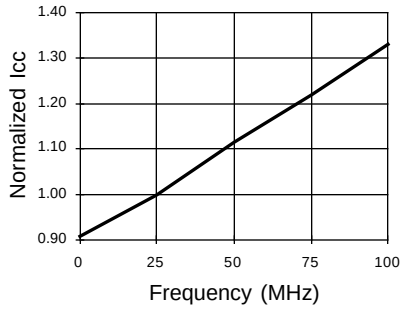
Normalized Icc vs Vcc



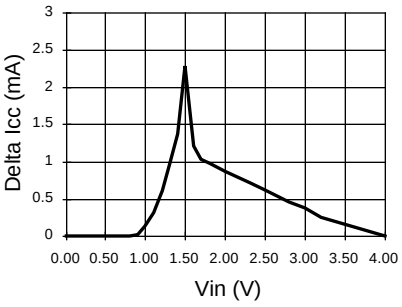
Normalized Icc vs Temp



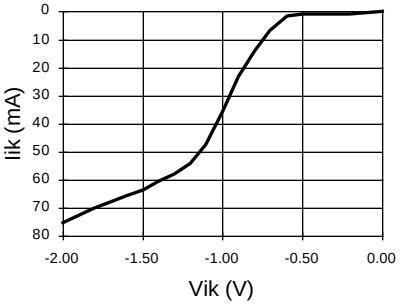
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



GAL18V10

High Performance E²CMOS PLD
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 7.5 ns Maximum Propagation Delay**
  - **— Fmax = 111 MHz**
  - **— 5.5 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 16 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **LOW POWER CMOS**
  - **— 75 mA Typical Icc**
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Uses Standard 22V10 Macrocell Architecture**
  - **— Maximum Flexibility for Complex Logic Designs**
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

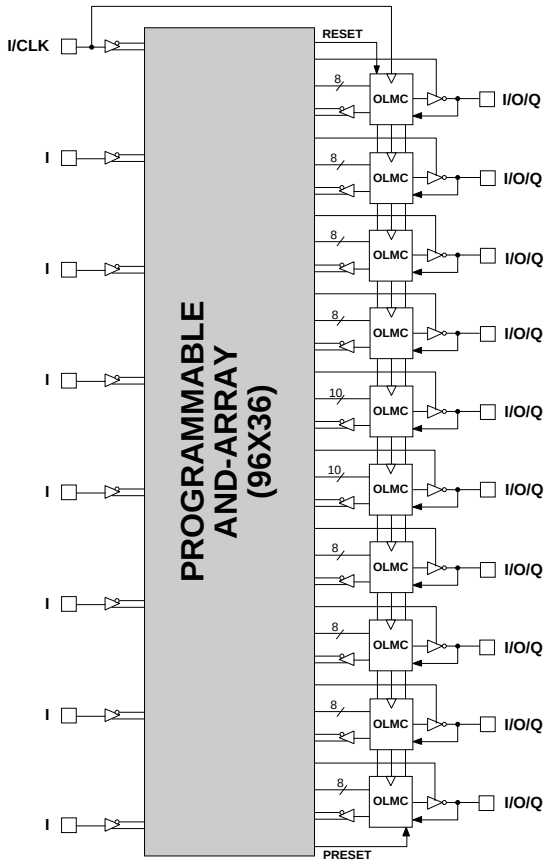
DESCRIPTION

The GAL18V10, at 7.5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide a very flexible 20-pin PLD. CMOS circuitry allows the GAL18V10 to consume much less power when compared to its bipolar counterparts. The E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

By building on the popular 22V10 architecture, the GAL18V10 eliminates the learning curve usually associated with using a new device architecture. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL18V10 OLMC is fully compatible with the OLMC in standard bipolar and CMOS 22V10 devices.

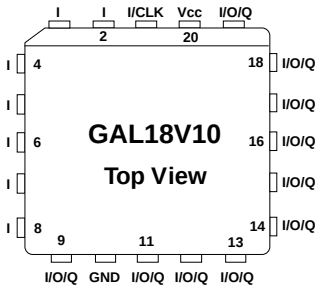
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM

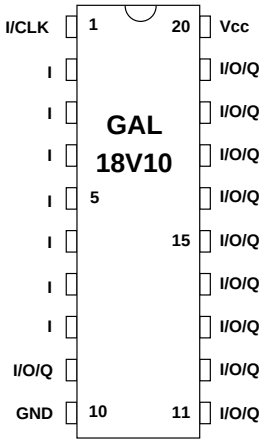


PIN CONFIGURATION

PLCC



DIP



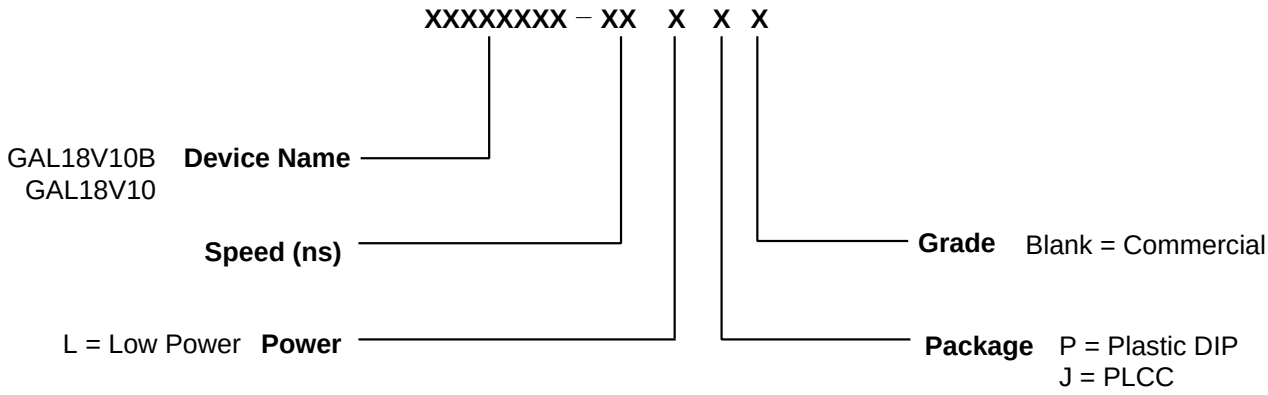
LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL18V10 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	6	5.5	115	GAL18V10B-7LP	20-Pin Plastic DIP
			115	GAL18V10B-7LJ	20-Lead PLCC
10	7	7	115	GAL18V10B-10LP	20-Pin Plastic DIP
			115	GAL18V10B-10LJ	20-Lead PLCC
15	8	10	115	GAL18V10B-15LP	20-Pin Plastic DIP
			115	GAL18V10B-15LJ	20-Lead PLCC
			115	GAL18V10-15LP	20-Pin Plastic DIP
			115	GAL18V10-15LJ	20-Lead PLCC
20	12	12	115	GAL18V10B-20LP	20-Pin Plastic DIP
			115	GAL18V10B-20LJ	20-Lead PLCC
			115	GAL18V10-20LP	20-Pin Plastic DIP
			115	GAL18V10-20LJ	20-Lead PLCC

PART NUMBER DESCRIPTION



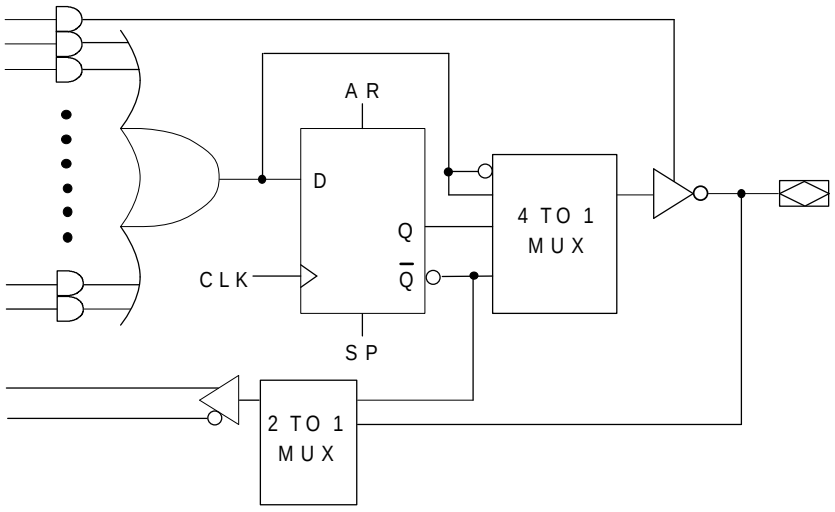
OUTPUT LOGIC MACROCELL (OLMC)

The GAL18V10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to ten product terms (pins 14 and 15), and the other eight OLMCs have eight product terms each. In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL18V10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registered outputs to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL18V10 OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL18V10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the the following page.

REGISTERED

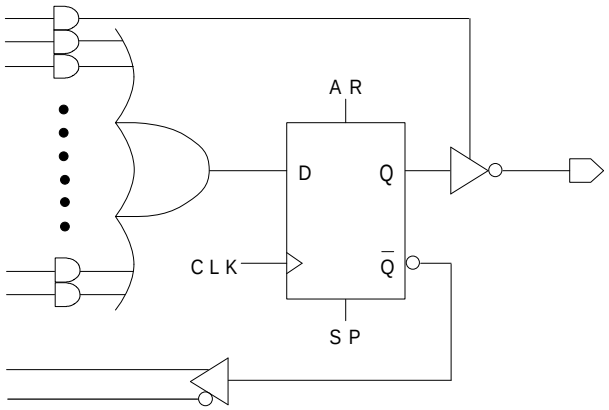
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

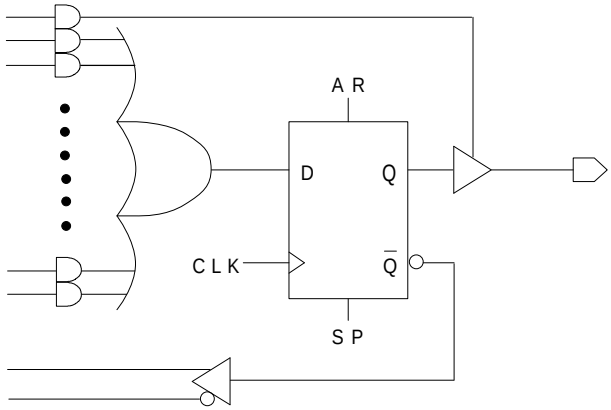
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE



ACTIVE LOW

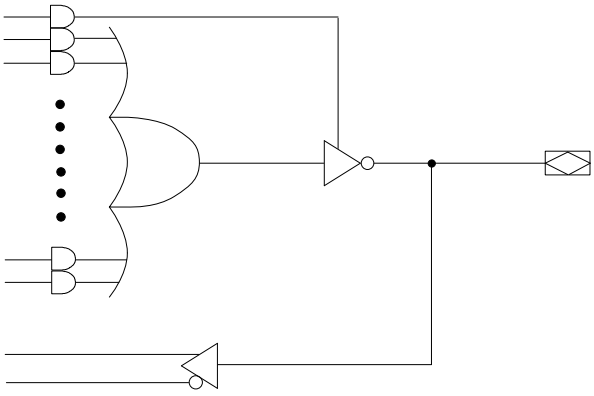
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

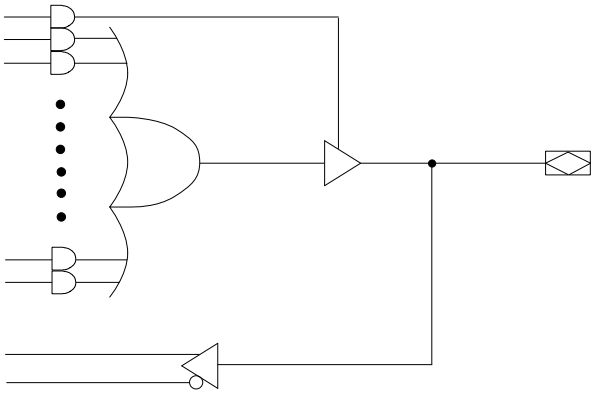
$S_0 = 1$
$S_1 = 0$

COMBINATORIAL MODE



ACTIVE LOW

$S_0 = 0$
$S_1 = 1$

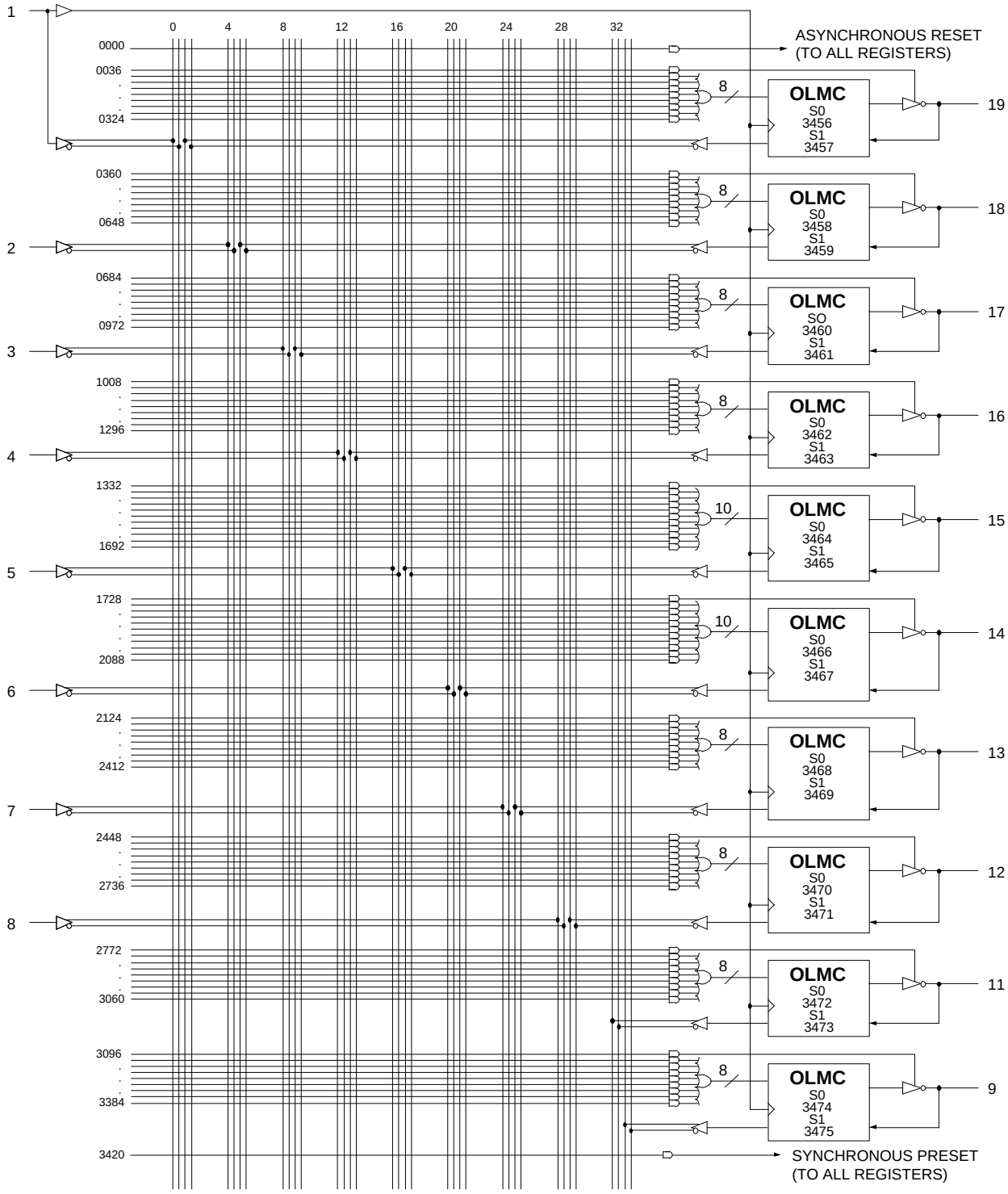


ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

GAL18V10 LOGIC DIAGRAM / JEDEC FUSE MAP

DIP and PLCC Package Pinouts



3476, 3477 ...	Electronic Signature						... 3538, 3539
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0

MSB LSB

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–130	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -7/-10/-15/-20	—	75	115	mA

1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM.	TEST COND.[1]	DESCRIPTION	COM -7		COM -10		COM -15		COM -20		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Comb. Output	—	7.5	—	10	—	15	—	20	ns
tco	A	Clock to Output Delay	—	5.5	—	7	—	10	—	12	ns
tcf[2]	—	Clock to Feedback Delay	—	3.5	—	3.5	—	7	—	10	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑	5.5	—	6	—	8	—	12	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	90.9	—	76.9	—	55.5	—	41.6	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	111	—	105	—	66.7	—	45.4	—	MHz
	A	Maximum Clock Frequency with No Feedback	111	—	105	—	66.7	—	62.5	—	MHz
twh	—	Clock Pulse Duration, High	4	—	4	—	6	—	8	—	ns
twl	—	Clock Pulse Duration, Low	4	—	4	—	6	—	8	—	ns
ten	B	Input or I/O to Output Enabled	—	8	—	10	—	15	—	20	ns
tdis	C	Input or I/O to Output Disabled	—	8	—	9	—	15	—	20	ns
tar	A	Input or I/O to Asynch. Reset of Reg.	—	13	—	13	—	20	—	20	ns
tarw	—	Asynch. Reset Pulse Duration	8	—	8	—	10	—	15	—	ns
tarr	—	Asynch. Reset to Clk↑ Recovery Time	8	—	8	—	10	—	15	—	ns
tspr	—	Synch. Preset to Clk↑ Recovery Time	10	—	10	—	10	—	12	—	ns

1) Refer to Switching Test Conditions section.
2) Calculated from fmax with internal feedback. Refer to fmax Description section.
3) Refer to fmax Description section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–50	—	–135	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -15/-20	—	75	115	mA

1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	COM -15 MIN.	COM -15 MAX.	COM -20 MIN.	COM -20 MAX.	UNITS
tpd	A	Input or I/O to Combinatorial Output	—	15	—	20	ns
tco	A	Clock to Output Delay	—	10	—	12	ns
tcf[2]	—	Clock to Feedback Delay	—	7	—	10	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	12	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu +tco)	50	—	41.6	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	58.8	—	45.4	—	MHz
	A	Maximum Clock Frequency with No Feedback	62.5	—	62.5	—	MHz
twh	—	Clock Pulse Duration, High	8	—	8	—	ns
twl	—	Clock Pulse Duration, Low	8	—	8	—	ns
ten	B	Input or I/O to Output Enabled	—	15	—	20	ns
tdis	C	Input or I/O to Output Disabled	—	15	—	20	ns
tar	A	Input or I/O to Asynchronous Reset of Register	—	20	—	20	ns
tarw	—	Asynchronous Reset Pulse Duration	10	—	15	—	ns
tarr	—	Asynchronous Reset to Clock Recovery Time	15	—	15	—	ns
tspr	—	Synchronous Preset to Clock Recovery Time	10	—	12	—	ns

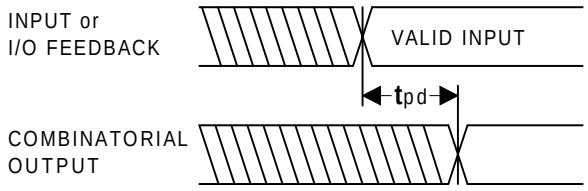
1) Refer to Switching Test Conditions section.
2) Calculated from fmax with internal feedback. Refer to fmax Description section.
3) Refer to fmax Description section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

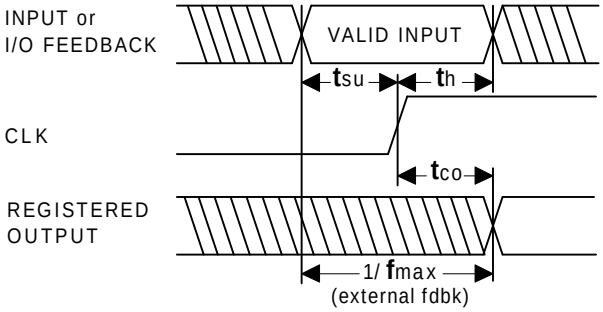
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

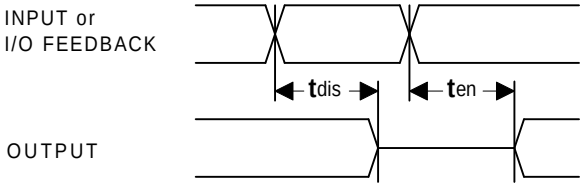
SWITCHING WAVEFORMS



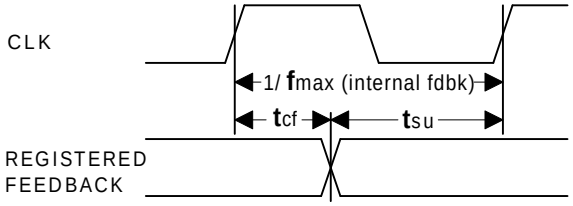
Combinatorial Output



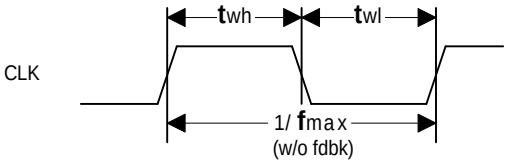
Registered Output



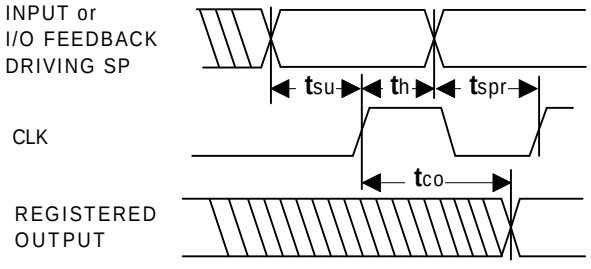
Input or I/O to Output Enable/Disable



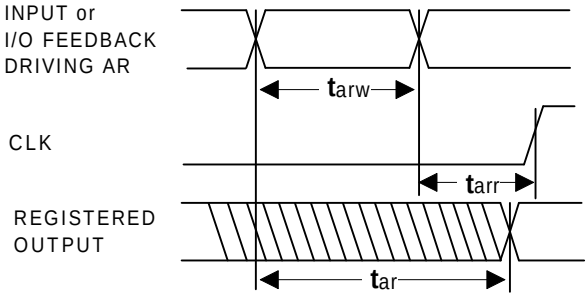
fmax with Feedback



Clock Width

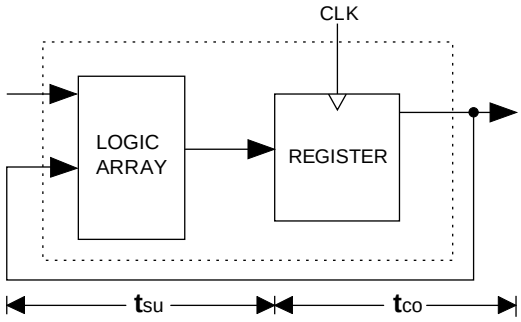


Synchronous Preset



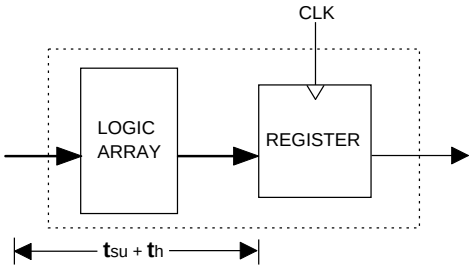
Asynchronous Reset

fmax DESCRIPTIONS



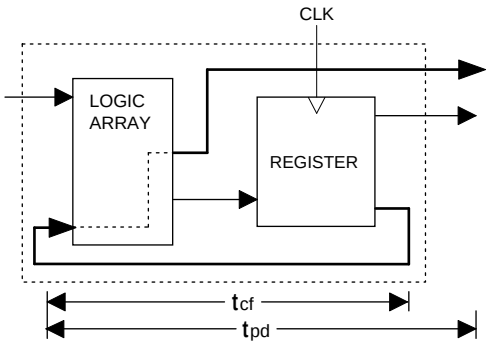
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

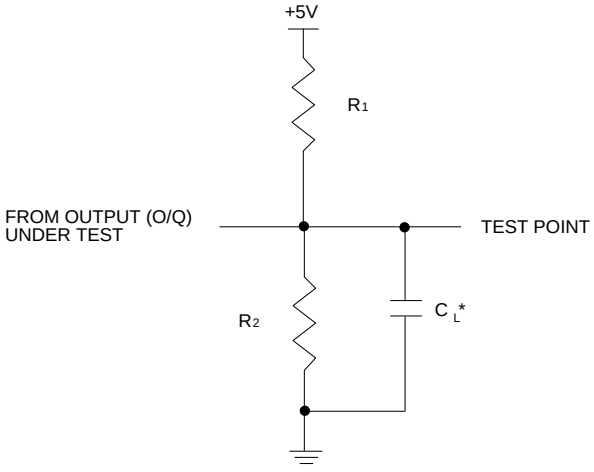
SWITCHING TEST CONDITIONS

Input Pulse Levels		GND to 3.0V
Input Rise and	-7/-10	2ns 10% – 90%
Fall Times	-15/-20	3ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL18V10 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

SECURITY CELL

A security cell is provided in every GAL18V10 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL18V10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

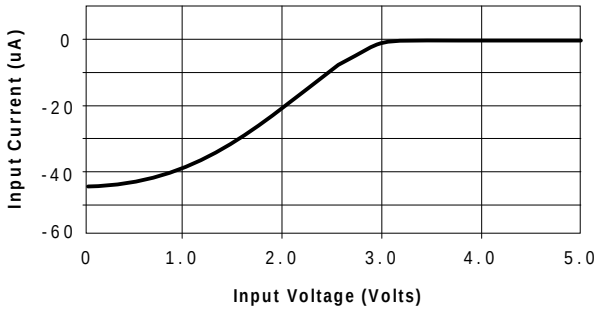
The GAL18V10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

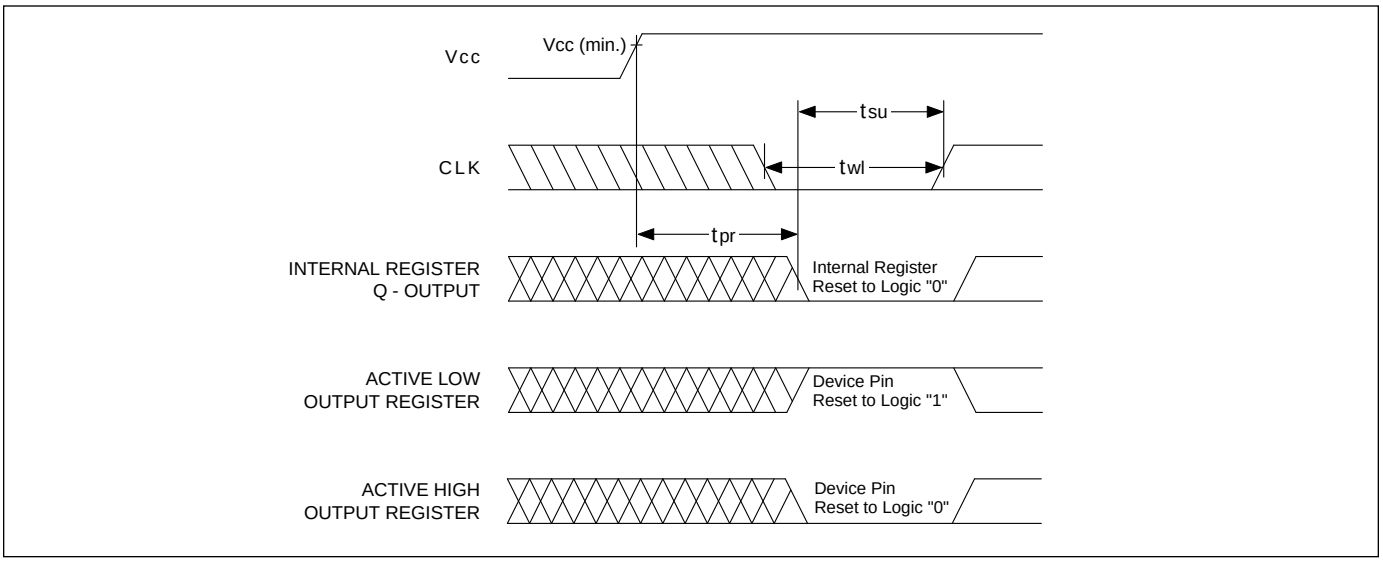
GAL18V10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device.

Typical Input Current

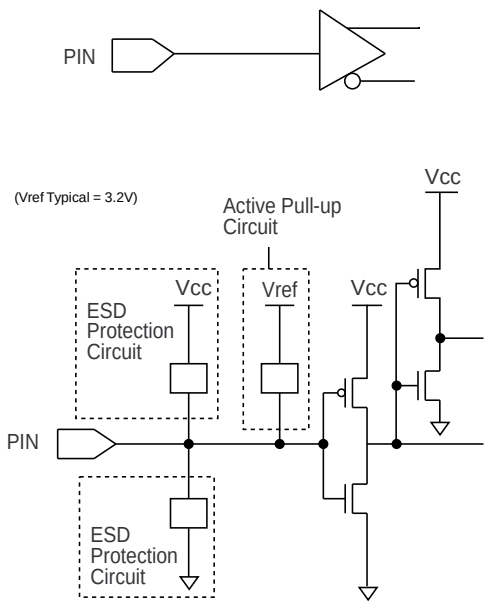


POWER-UP RESET

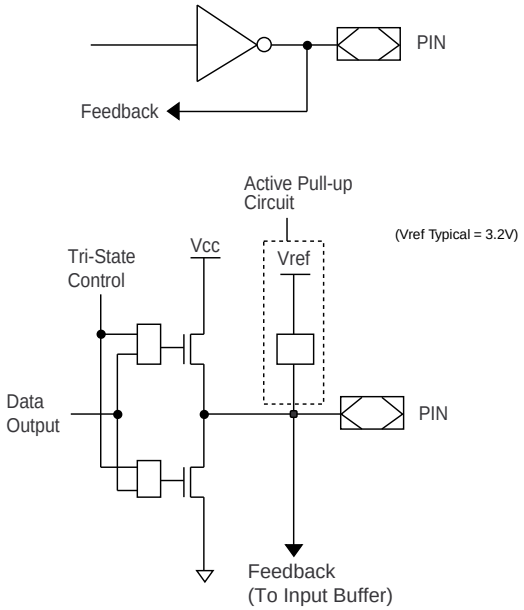


Circuitry within the GAL18V10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the device. First, the V_{CC} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



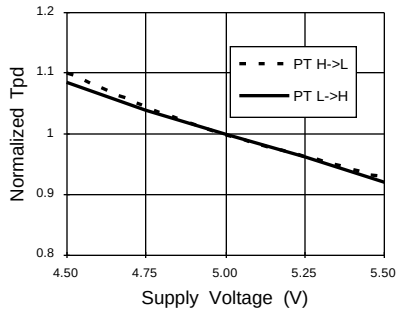
Typical Input



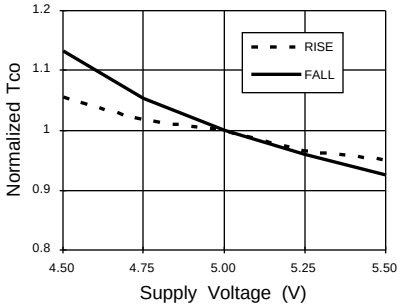
Typical Output

GAL18V10B: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

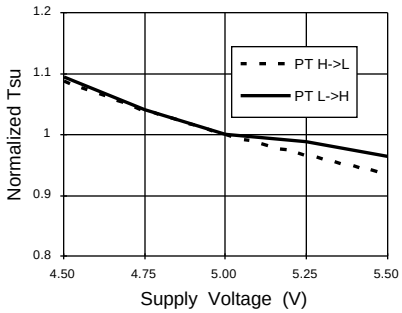
Normalized Tpd vs Vcc



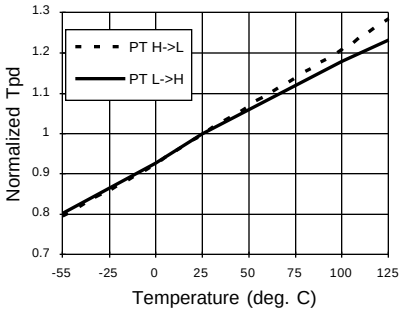
Normalized Tco vs Vcc



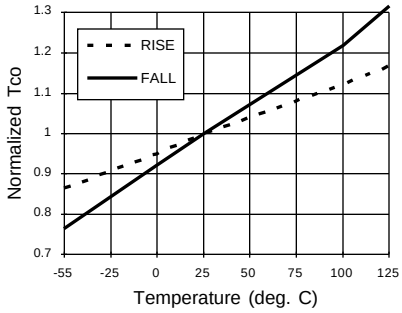
Normalized Tsu vs Vcc



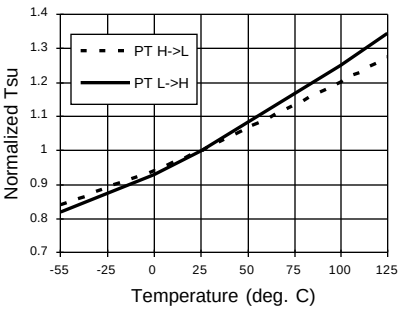
Normalized Tpd vs Temp



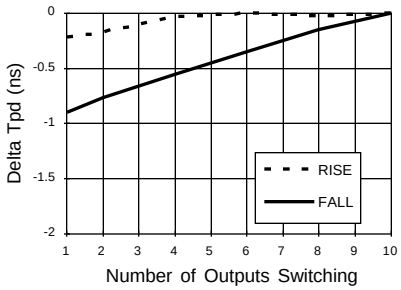
Normalized Tco vs Temp



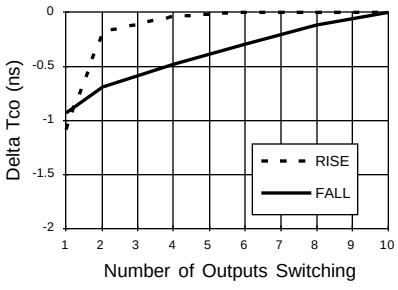
Normalized Tsu vs Temp



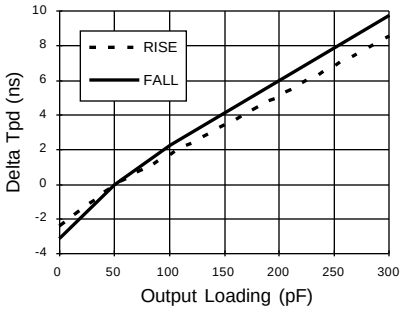
Delta Tpd vs # of Outputs Switching



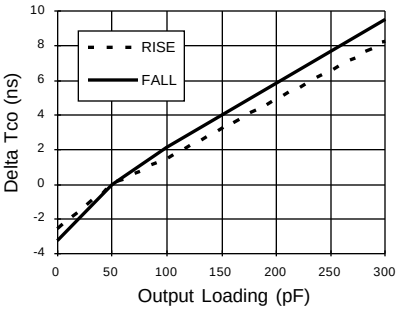
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

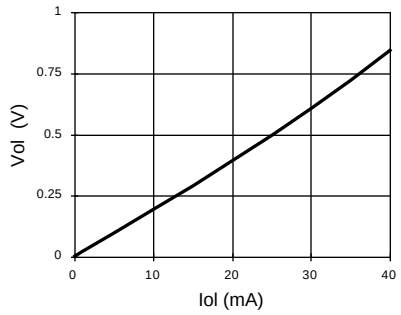


Delta Tco vs Output Loading

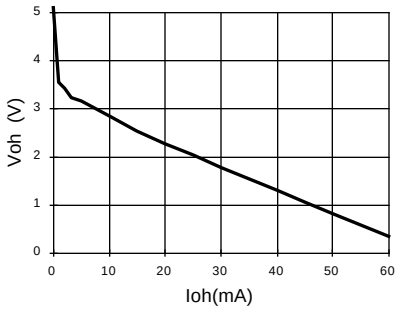


GAL18V10B: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

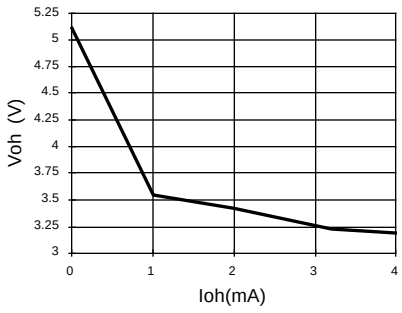
Vol vs Iol



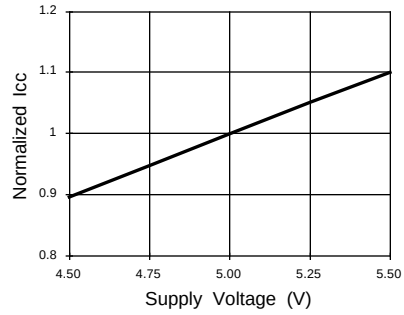
Voh vs Ioh



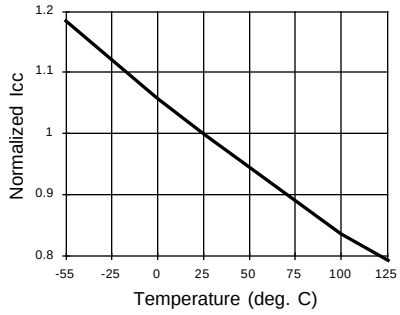
Voh vs Ioh



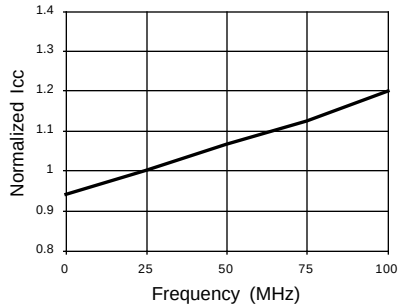
Normalized Icc vs Vcc



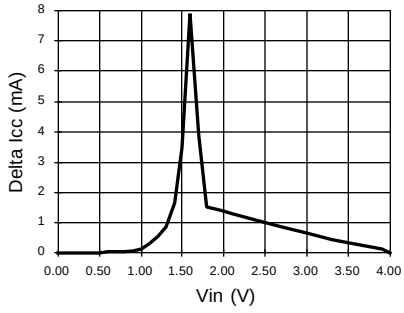
Normalized Icc vs Temp



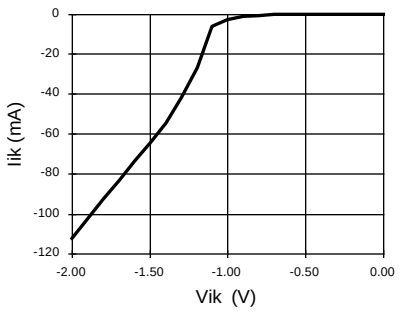
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

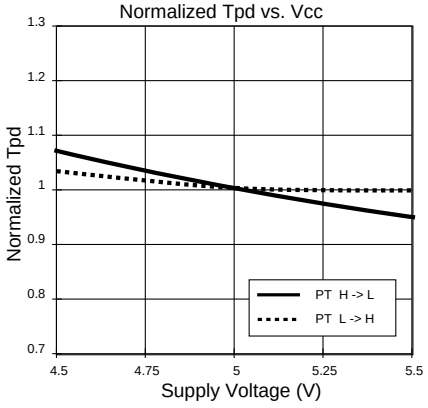


Input Clamp (Vik)

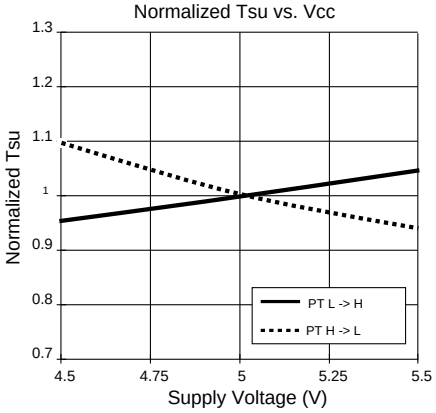


GAL18V10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

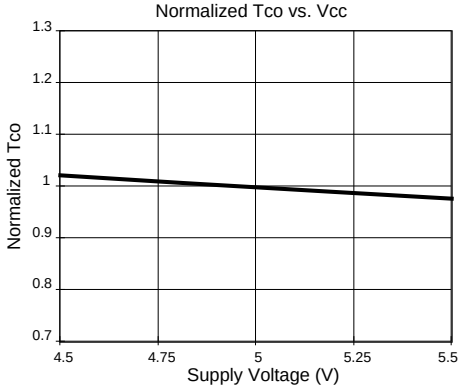
Normalized Tpd vs. Vcc



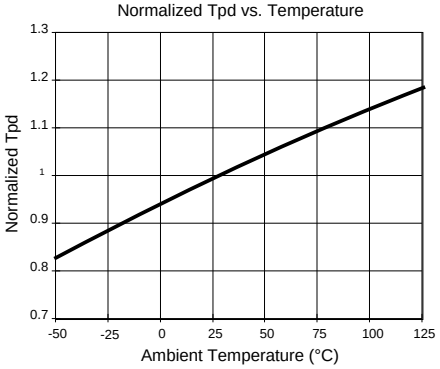
Normalized Tsu vs. Vcc



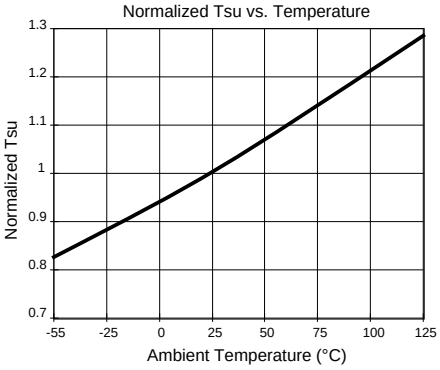
Normalized Tco vs. Vcc



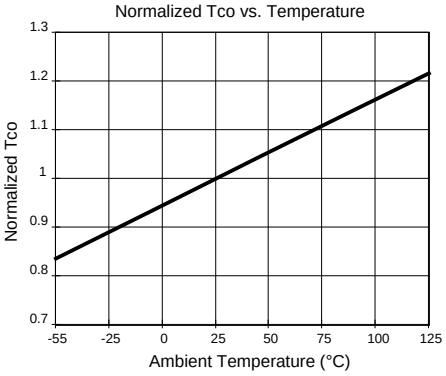
Normalized Tpd vs. Temperature



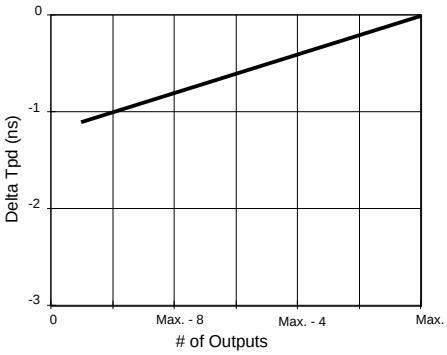
Normalized Tsu vs. Temperature



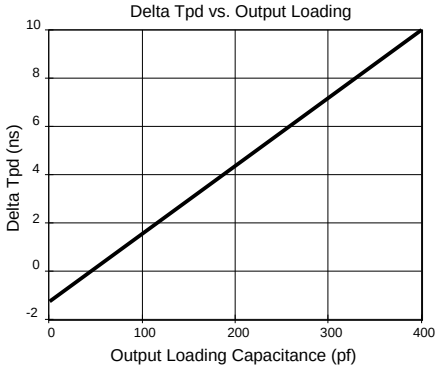
Normalized Tco vs. Temperature



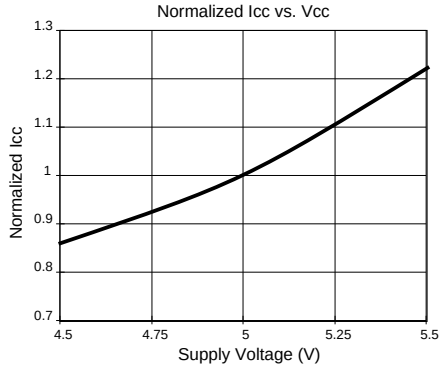
Delta Tpd vs. # of Outputs Switching



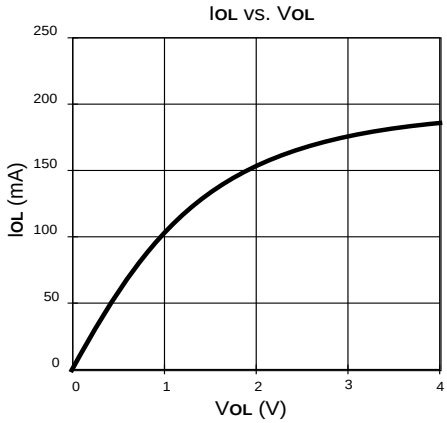
Delta Tpd vs. Output Loading



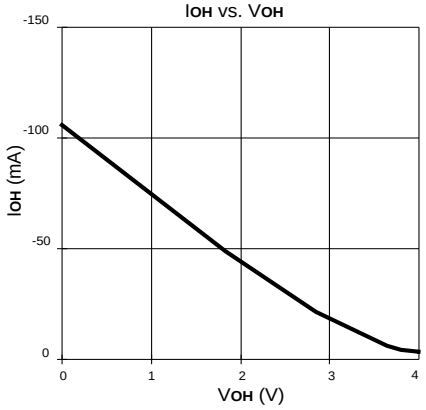
Normalized Icc vs. Vcc



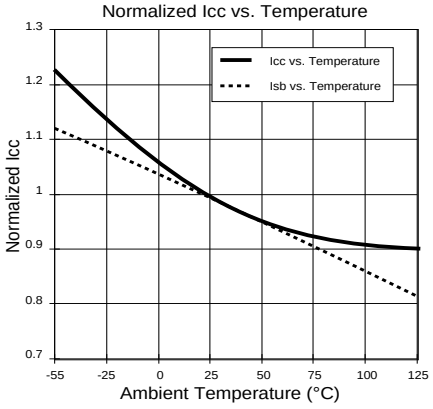
I_{OL} vs. V_{OL}



I_{OH} vs. V_{OH}



Normalized Icc vs. Temperature



GAL20RA10

High-Speed Asynchronous E²CMOS PLD
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 7.5 ns Maximum Propagation Delay**
  - **— Fmax = 83.3 MHz**
  - **— 9 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 8 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - **— 75mA Typical I_{CC}**
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100 ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Independent Programmable Clocks**
  - **— Independent Asynchronous Reset and Preset**
  - **— Registered or Combinatorial with Polarity**
  - **— Full Function and Parametric Compatibility with PAL20RA10**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— State Machine Control**
  - **— Standard Logic Consolidation**
  - **— Multiple Clock Logic Designs**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

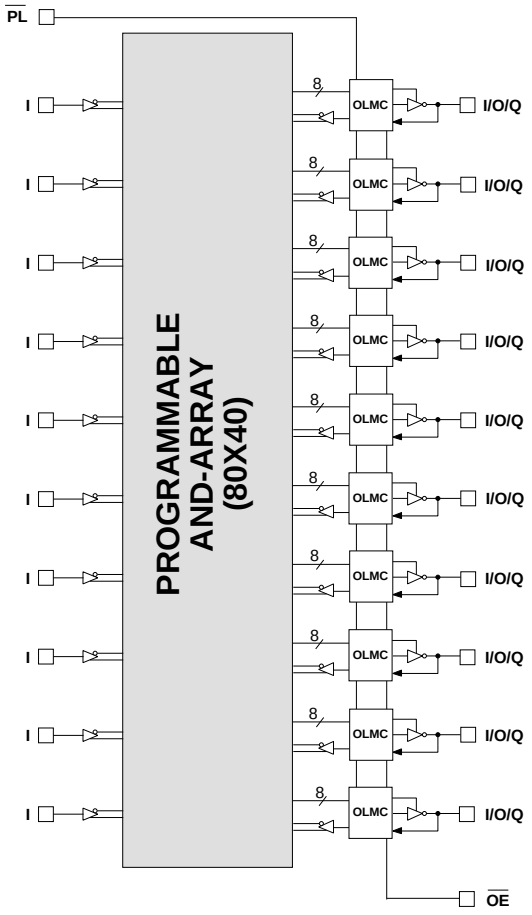
DESCRIPTION

The GAL20RA10 combines a high performance CMOS process with electrically erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. Lattice Semiconductor's E²CMOS circuitry achieves power levels as low as 75mA typical I_{CC} which represents a substantial savings in power when compared to bipolar counterparts. E² technology offers high speed (<100ms) erase times providing the ability to reprogram, reconfigure or test the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20RA10 is a direct parametric compatible CMOS replacement for the PAL20RA10 device.

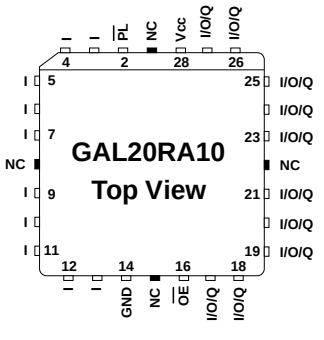
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacturing. Therefore, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM

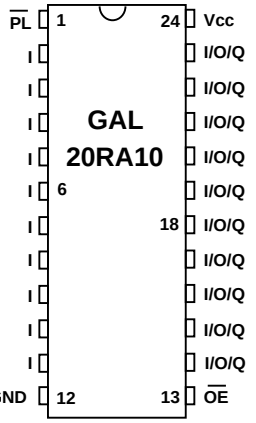


PIN CONFIGURATION

PLCC



DIP



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL20RA10 ORDERING INFORMATION

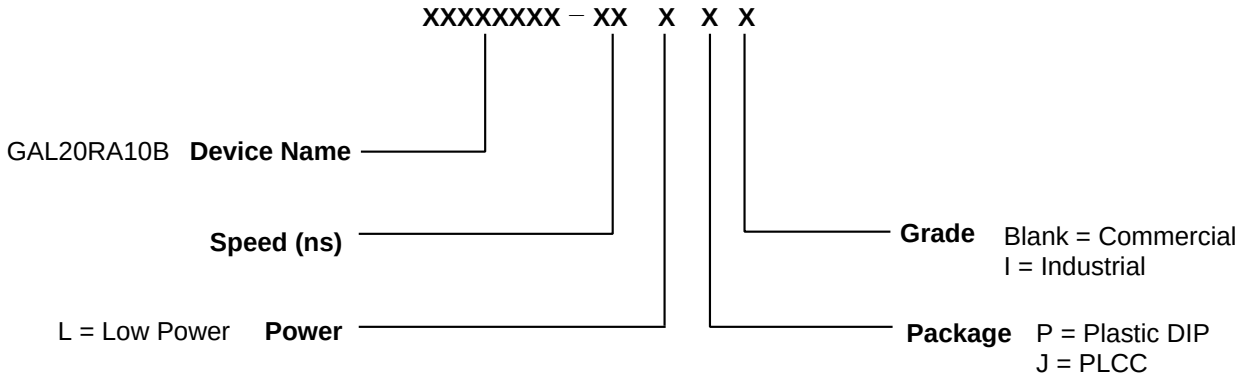
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	3	9	100	GAL20RA10B-7LJ	28-Lead PLCC
10	4	11	100	GAL20RA10B-10LP	24-Pin Plastic DIP
			100	GAL20RA10B-10LJ	28-Lead PLCC
15	7	15	100	GAL20RA10B-15LP	24-Pin Plastic DIP
			100	GAL20RA10B-15LJ	28-Lead PLCC
20	10	20	100	GAL20RA10B-20LP	24-Pin Plastic DIP
			100	GAL20RA10B-20LJ	28-Lead PLCC
30	20	30	100	GAL20RA10B-30LP	24-Pin Plastic DIP
			100	GAL20RA10B-30LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
20	10	20	120	GAL20RA10B-20LPI	24-Pin Plastic DIP
			120	GAL20RA10B-20LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The GAL20RA10 OLMC consists of 10 D flip-flops with individual asynchronous programmable reset, preset and clock product terms. The sum of four product terms and an Exclusive-OR provide a programmable polarity D-input to each flip-flop. An output enable term combined with the dedicated output enable pin provides tri-state control of each output. Each OLMC has a flip-flop bypass, allowing any combination of registered or combinatorial outputs.

The GAL20RA10 has 10 dedicated input pins and 10 programmable I/O pins, which can be either inputs, outputs, or dynamic I/O. Each pin has a unique path to the logic array. All macrocells have the same type and number of data and control product terms, allowing the user to exchange I/O pin assignments without restriction.

INDEPENDENT PROGRAMMABLE CLOCKS

An independent clock control product term is provided for each GAL20RA10 macrocell. Data is clocked into the flip-flop on the active edge of the clock product term. The use of individual clock control product terms allow up to ten separate clocks. These clocks can be derived from any pin or combination of pins and/or feedback from other flip-flops. Multiple clock sources allow a number of asynchronous register functions to be combined into a single GAL20RA10. This allows the designer to combine discrete logic functions into a single device.

PROGRAMMABLE POLARITY

The polarity of the D-input to each macrocell flip-flop is individually programmable to be active high or low. This is accomplished with a programmable Exclusive-OR gate on the D-input of each flip-flop. The polarity of the pin is active low when XOR bit is programmed (or zero) and is active high when XOR bit is erased (or one). Because of the inverted output buffer, the XOR gate output node is opposite polarity from the pin. It should be noted that the programmable polarity only affects the data latched into the flip-flop on the active edge of the clock product term. The reset, preset and preload will alter the state of the flip-flop independent of the state of programmable polarity bit. The ability to program the active polarity of the D-inputs can be used to reduce the total number of product terms used, by allowing the DeMorganization of the logic functions. This logic reduction is accomplished by the logic compiler, and does not require the designer to define the polarity.

OUTPUT ENABLE

The output of each GAL20RA10 macrocell is controlled by the “AND’ing” of an independent output enable product term and a common active low output enable pin (pin 13 on DIP package / pin 16 on PLCC package). The output is enabled while the output enable product term is active and the output enable pin is low. This output control structure allows several output enable alternatives.

ASYNCHRONOUS RESET AND PRESET

Each GAL20RA10 macrocell has an independent asynchronous reset and preset control product term. The reset and preset product terms are level sensitive, and will hold the flip-flop in the reset or preset state while the product term is active independent of the clock or D-inputs. It should be noted that the reset and preset term alter the state of the flip-flop whose output is inverted by the output buffer. A reset of the flip-flop will result in the output pin becoming a logic high and a preset will result in a logic low.

RESET	PRESET	FUNCTION
0	0	Registered function of data product term
1	0	Reset register to "0" (device pin = "1")
0	1	Preset register to "1" (device pin = "0")
1	1	Register-bypass (combinatorial output)

COMBINATORIAL CONTROL

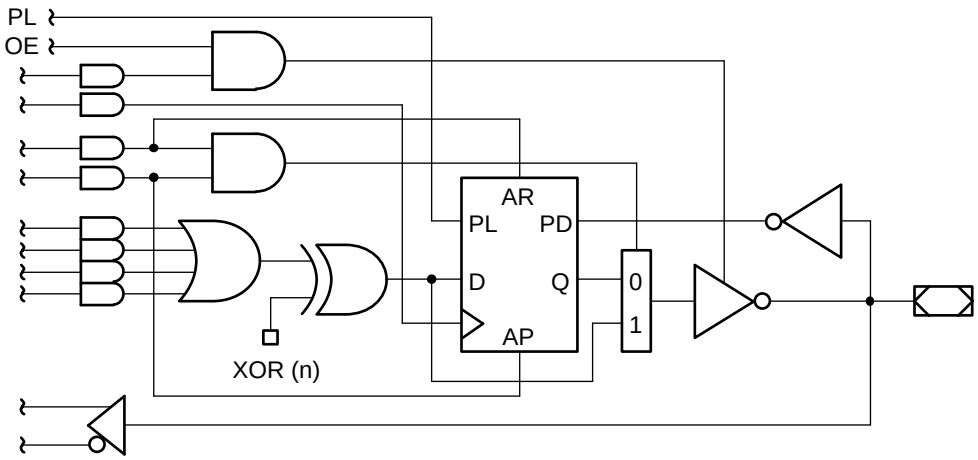
The register in each GAL20RA10 macrocell may be bypassed by asserting both the reset and preset product terms. While both product terms are active the flip-flop is bypassed and the D- input is presented directly to the inverting output buffer. This provides the designer the ability to dynamically configure any macrocell as a combinatorial output, or to fix the macrocell as combinatorial only by forcing both reset and preset product terms active. Some logic compilers will configure macrocells as registered or combinatorial based on the logic equations, others require the designer to force the reset and preset product terms active for combinatorial macrocells.

PARALLEL FLIP-FLOP PRELOAD

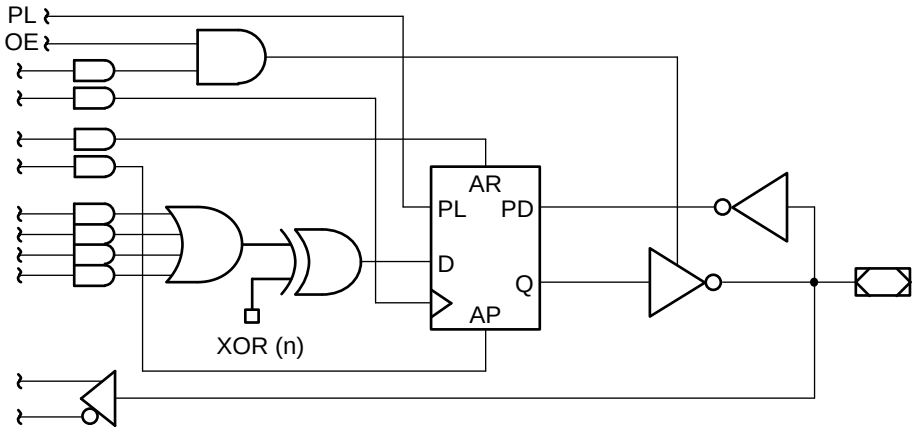
The flip-flops of a GAL20RA10 can be reset or preset from the I/O pins by applying a logic low to the preload pin (pin 1 on DIP package / pin 2 on PLCC package) and applying the desired logic level to each I/O pin. The I/O pins must remain valid for the preload setup and hold time. All 10 flip-flops are reset or preset during preload, independent of all other OLMC inputs.

A logic low on an I/O pin during preload will preset the flip-flop, a logic high will reset the flip-flop. The output of any flip-flop to be preloaded must be disabled. Enabling the output during preload will maintain the current logic state. It should be noted that the preload alters the state of the flip-flop whose output is inverted by the output buffer. A reset of the flip-flop will result in the output pin becoming a logic high and a preset will result in a logic low. Note that the common output enable pin will disable all 10 outputs of the GAL20RA10 when held high.

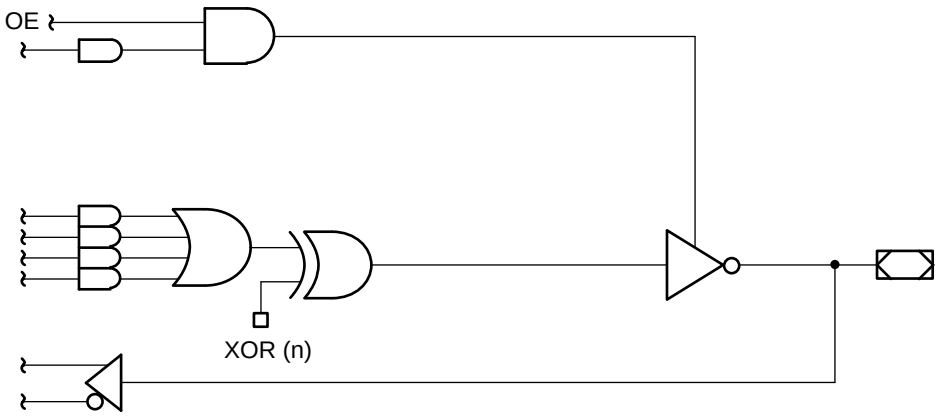
OUTPUT LOGIC MACROCELL DIAGRAM



OUTPUT LOGIC MACROCELL CONFIGURATION (REGISTERED with POLARITY)

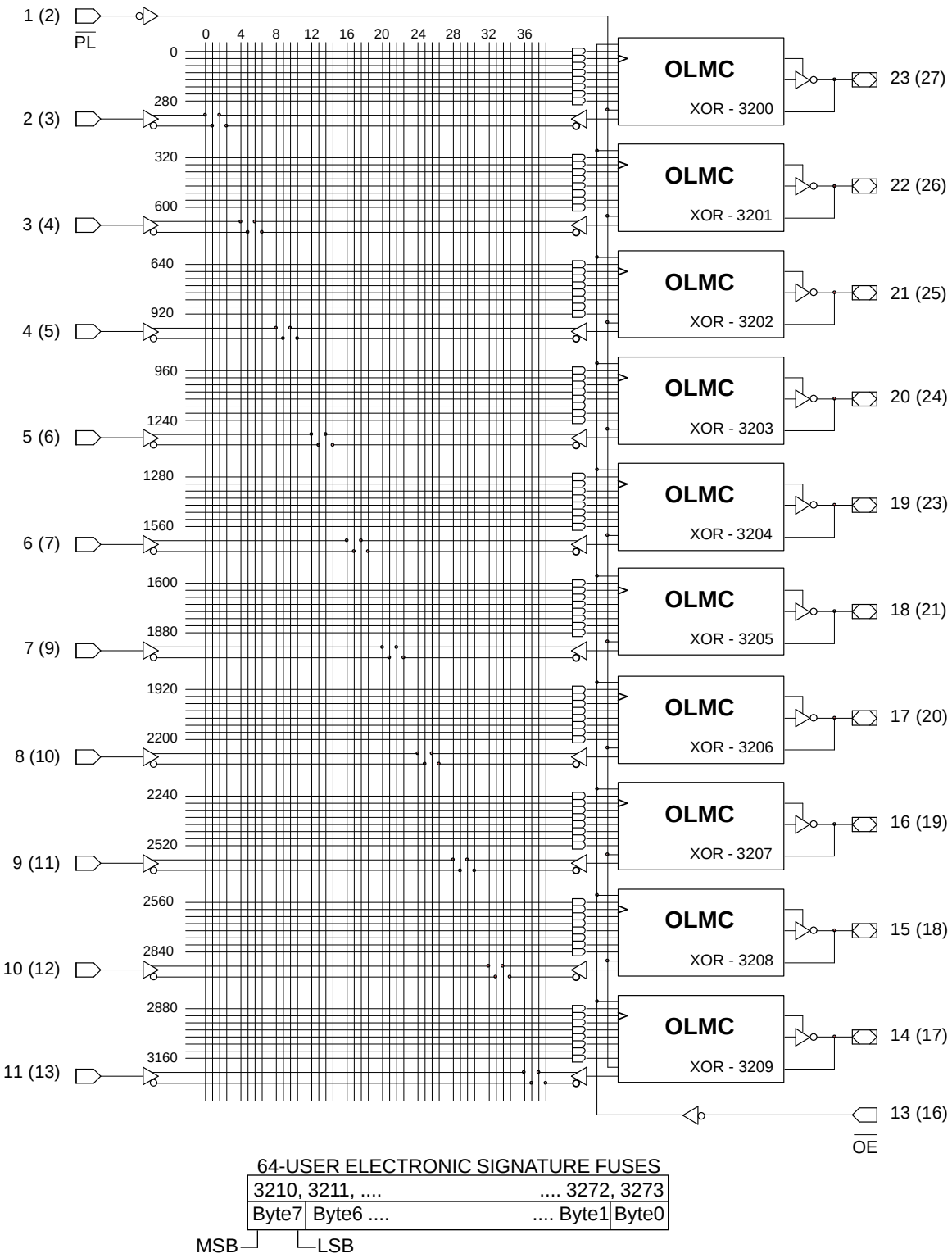


OUTPUT LOGIC MACROCELL CONFIGURATION (COMBINATORIAL with POLARITY)



GAL20RA10 LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1.Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... -40 to +85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	-50	—	-135	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -7/-10/-15/-20/-30	—	75	100	mA

INDUSTRIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -20	—	75	120	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM.	TEST COND[1].	DESCRIPTION	COM -7 MIN.	COM -7 MAX.	COM -10 MIN.	COM -10 MAX.	COM -15 MIN.	COM -15 MAX.	COM / IND -20 MIN.	COM / IND -20 MAX.	COM -30 MIN.	COM -30 MAX.	UNITS
tpd	A	Input or I/O to Combinatorial Output	2	7.5	2	10	—	15	—	20	—	30	ns
tco	A	Clock to Output Delay	2	9	2	11	—	15	—	20	—	30	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑	3	—	4	—	7	—	10	—	20	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	2	—	3	—	3	—	3	—	10	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	83.3	—	66.7	—	45.0	—	33.3	—	20.0	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	71.4	—	50.0	—	41.7	—	25.0	—	MHz
twh	—	Clock Pulse Duration, High	6	—	7	—	10	—	12	—	20	—	ns
twl	—	Clock Pulse Duration, Low	6	—	7	—	10	—	12	—	20	—	ns
ten/tdis	B,C	I or I/O to Output Enabled / Disabled	—	7.5	—	10	—	15	—	20	—	30	ns
ten/tdis	B,C	$\overline{OE}$ to Output Enabled / Disabled	—	5	—	9	—	12	—	15	—	20	ns
tar/tap	A	Input or I/O to Async. Reset / Preset	—	9	—	11	—	15	—	20	—	30	ns
tarw/tapw	—	Async. Reset / Preset Pulse Duration	6	—	10	—	15	—	20	—	20	—	ns
tarr/tapr	—	Async. Reset / Preset Recovery Time	7	—	7	—	10	—	12	—	20	—	ns
twp	—	Preload Pulse Duration	8	—	10	—	15	—	20	—	30	—	ns
tsp	—	Preload Setup Time	5	—	7	—	10	—	15	—	25	—	ns
thp	—	Preload Hold Time	5	—	7	—	10	—	15	—	25	—	ns

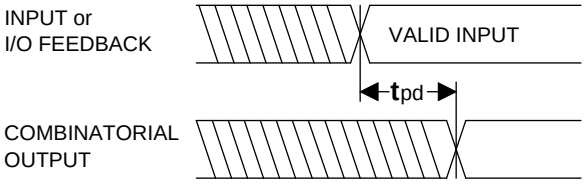
1) Refer to Switching Test Conditions section.
2) Refer to fmax Descriptions section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

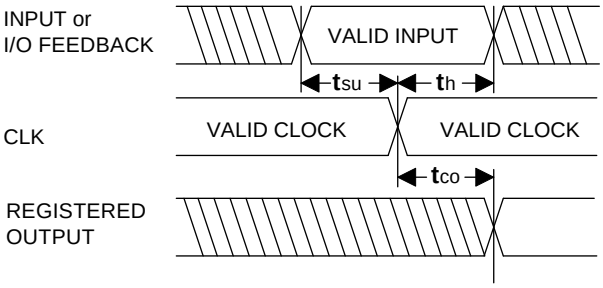
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

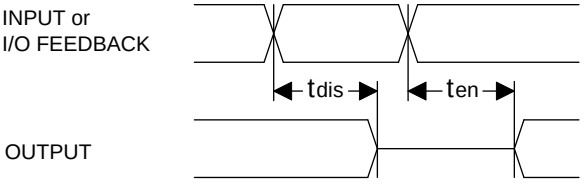
SWITCHING WAVEFORMS



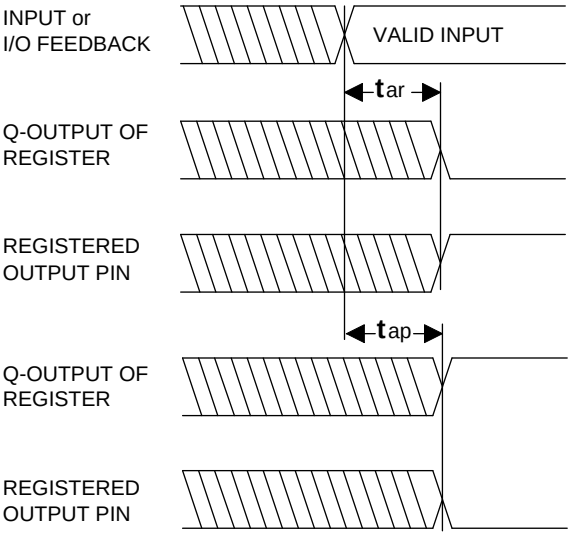
Combinatorial Output



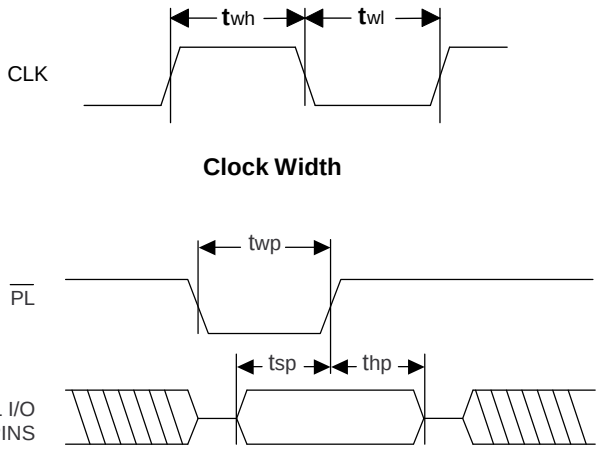
Registered Output



Input or I/O to Output Enable/Disable

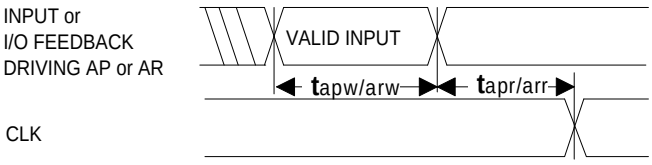


Asynchronous Reset and Preset

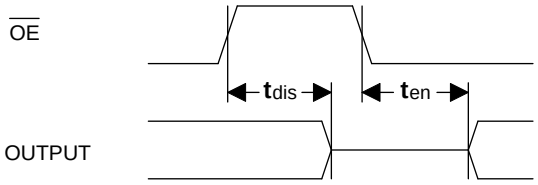


Clock Width

Parallel Preload

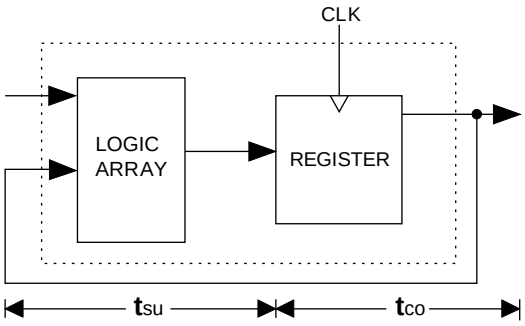


Asynchronous Reset and Preset Recovery



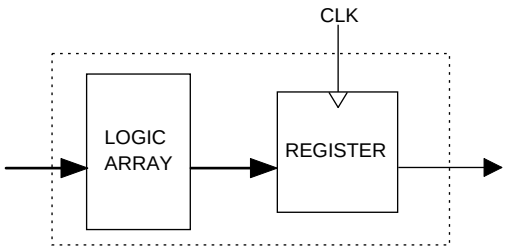
$\overline{OE}$ to Enable / Disable

fmax DESCRIPTIONS



fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.

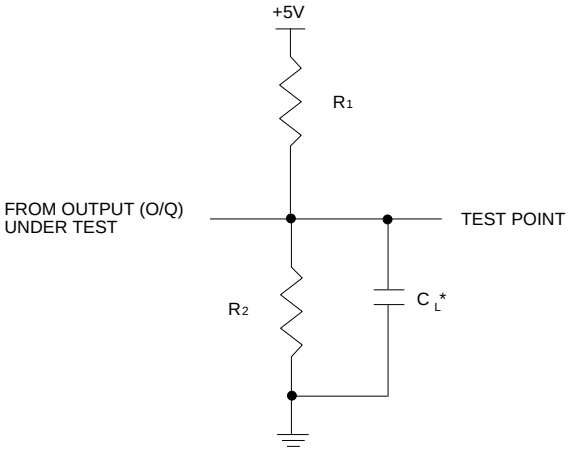
SWITCHING TEST CONDITIONS

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	-7/-10	2ns 10% – 90%
	-15/-20/-30	3ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		470Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	470Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	470Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL20RA10 device. It contains 64 bits of reprogrammable memory that contains user defined data. Some uses include user ID codes, revision numbers, pattern identification or inventory control codes. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature bits if programmed to any value other then zero(0) will alter the checksum of the device.

SECURITY CELL

A security cell is provided in every GAL20RA10 device as a deterrent to unauthorized copying of the device pattern. Once programmed, this cell prevents further read access of the device pattern information. This cell can be only be reset by reprogramming the device. The original pattern can never be examined once this cell is programmed. The Electronic Signature is always available regardless of the security cell state.

LATCH-UP PROTECTION

GAL20RA10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

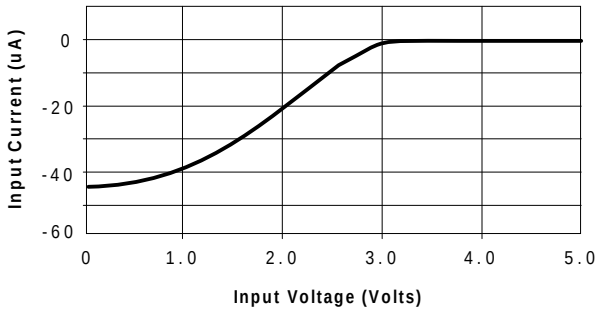
GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

INPUT BUFFERS

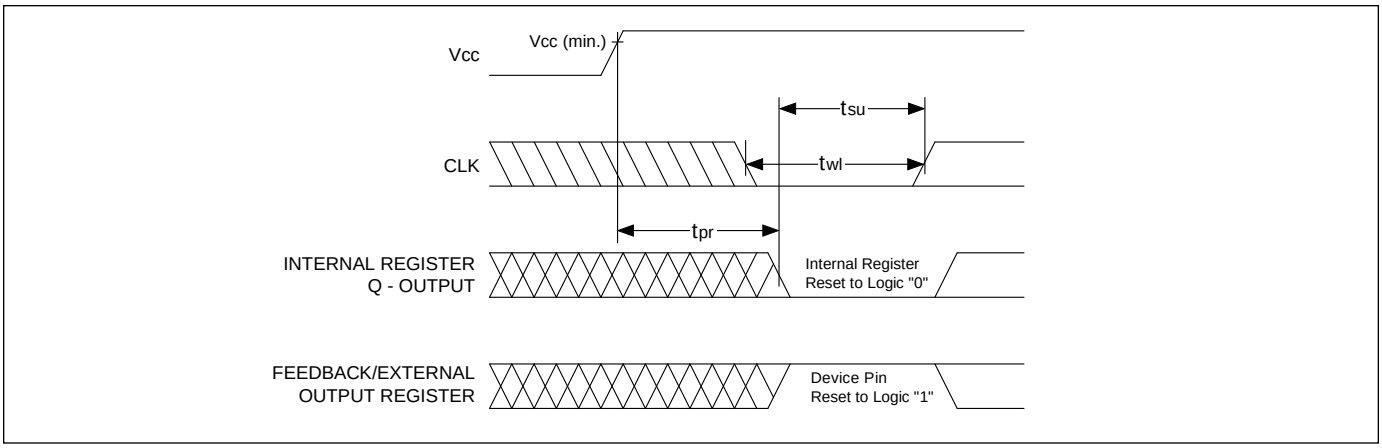
GAL20RA10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance and present a much lighter load to the driving logic than traditional bipolar devices.

GAL20RA10 input buffers have active pull-ups within their input structure. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce Icc for the device.

Typical Input Pull-up Characteristic

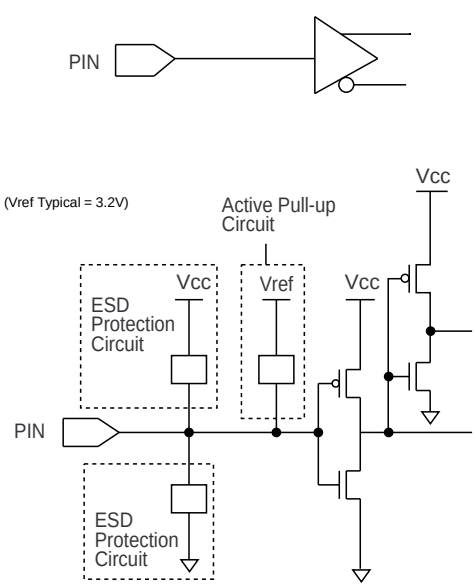


POWER-UP RESET

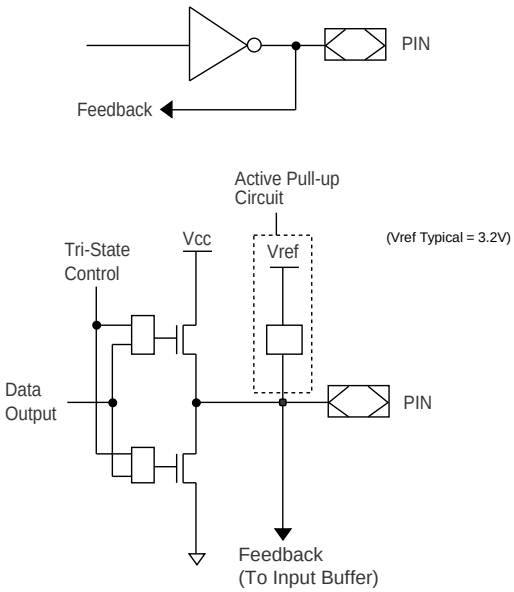


Circuitry within the GAL20RA10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will be high on power-up, because of the inverting buffer on the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown to the right. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20RA10. First, the Vcc rise must be monotonic. Second, the clock input must be at a static TTL level as shown in the diagram during power up. The registers will reset within a maximum of 1µs. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



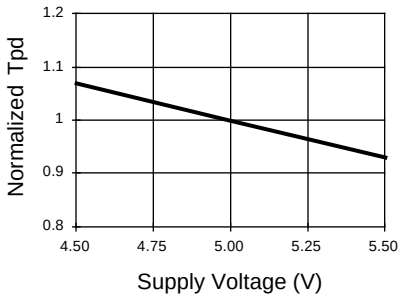
Typical Input



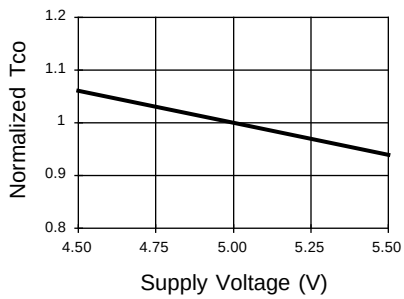
Typical Output

GAL20RA10B-7/-10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

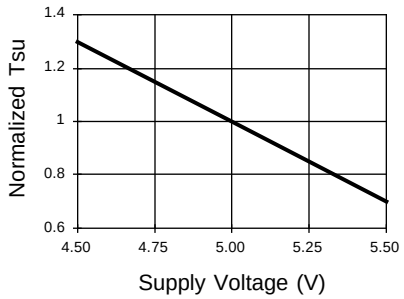
Normalized Tpd vs Vcc



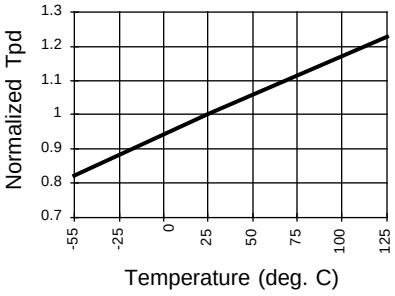
Normalized Tco vs Vcc



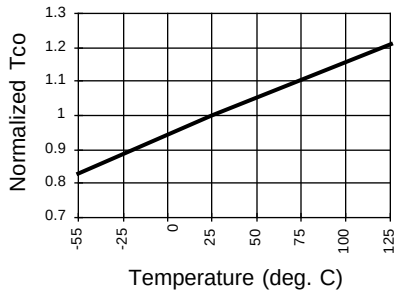
Normalized Tsu vs Vcc



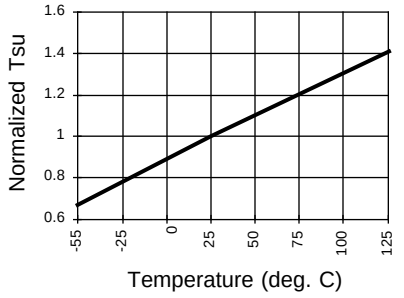
Normalized Tpd vs Temp



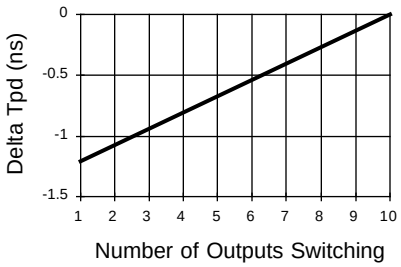
Normalized Tco vs Temp



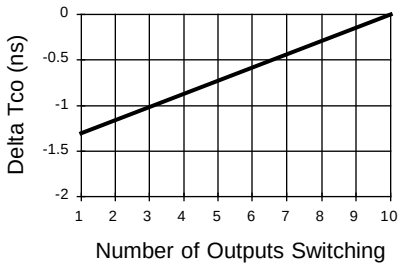
Normalized Tsu vs Temp



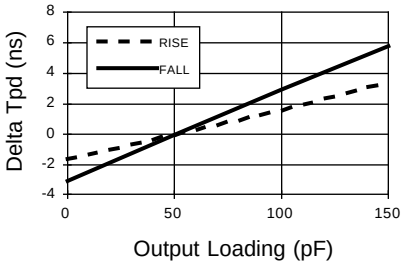
Delta Tpd vs # of Outputs Switching



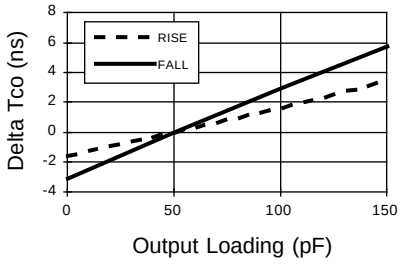
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

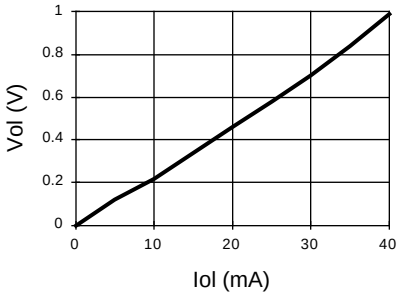


Delta Tco vs Output Loading

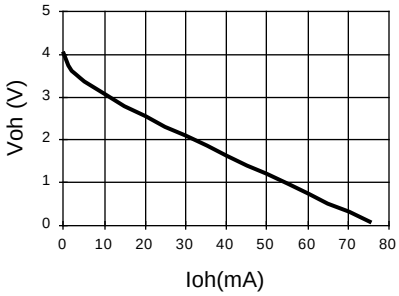


GAL20RA10B-7/-10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

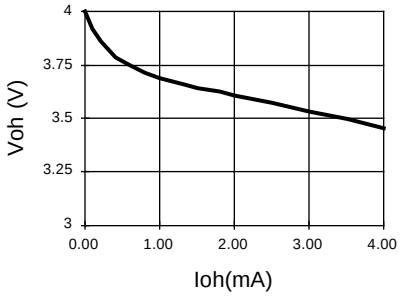
Vol vs Iol



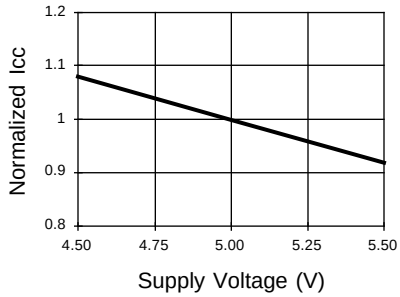
Voh vs Ioh



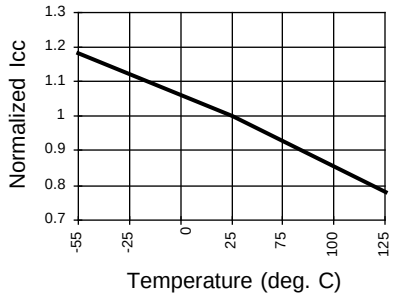
Voh vs Ioh



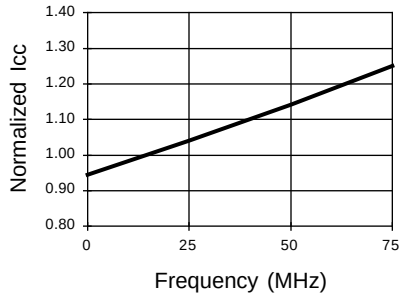
Normalized Icc vs Vcc



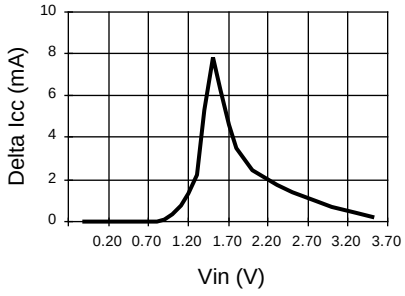
Normalized Icc vs Temp



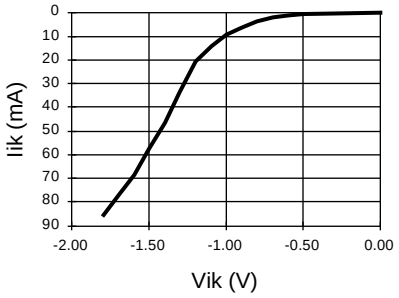
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

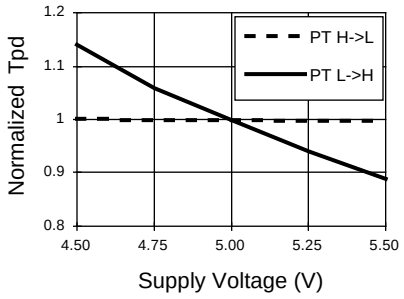


Input Clamp (Vik)

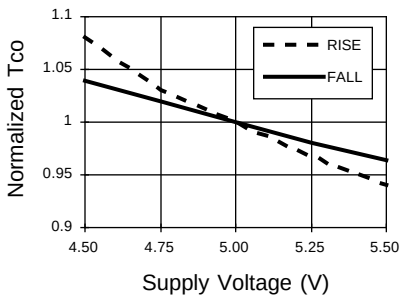


GAL20RA10B-15/-20/-30: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

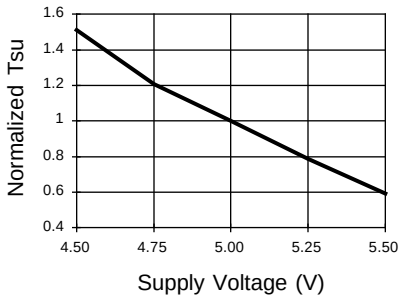
Normalized Tpd vs Vcc



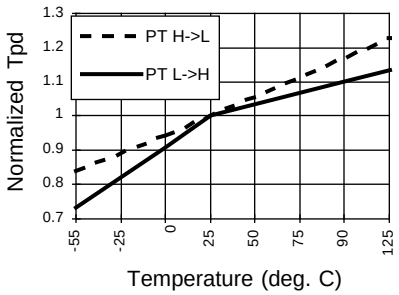
Normalized Tco vs Vcc



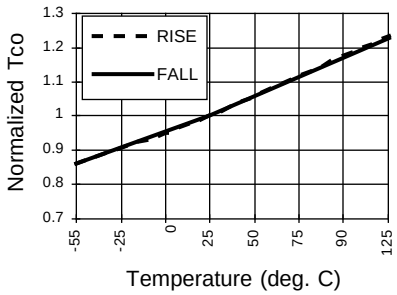
Normalized Tsu vs Vcc



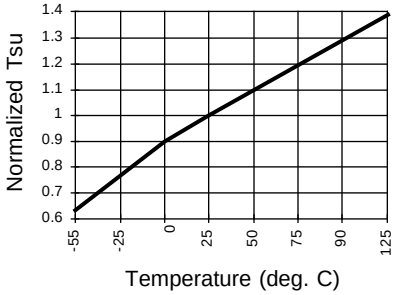
Normalized Tpd vs Temp



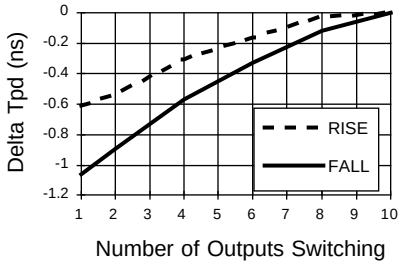
Normalized Tco vs Temp



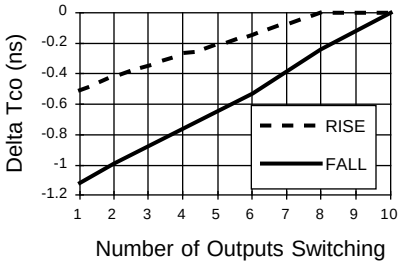
Normalized Tsu vs Temp



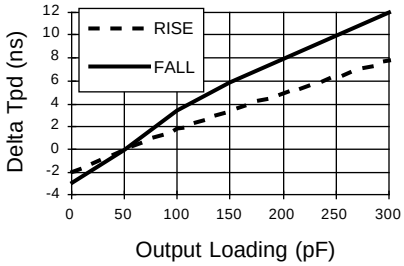
Delta Tpd vs # of Outputs Switching



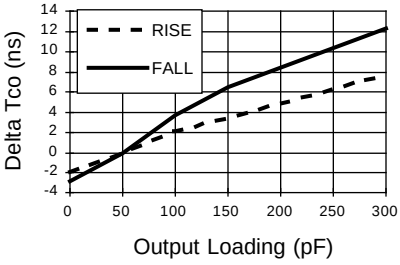
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

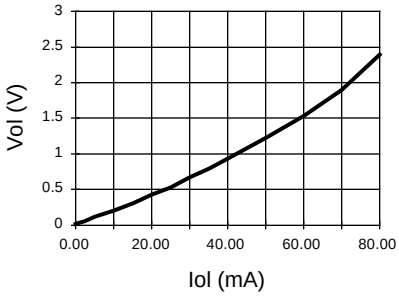


Delta Tco vs Output Loading

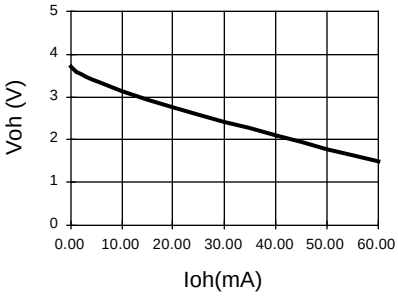


GAL20RA10B-15/-20/-30: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

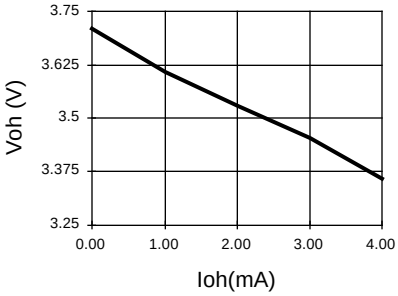
Vol vs Iol



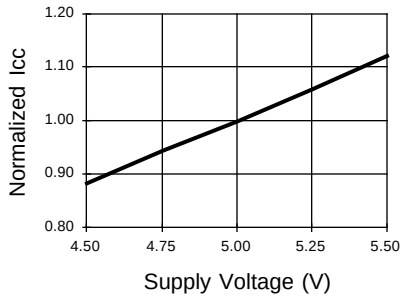
Voh vs Ioh



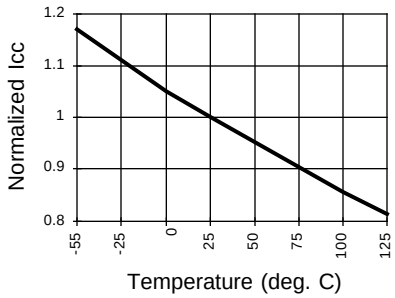
Voh vs Ioh



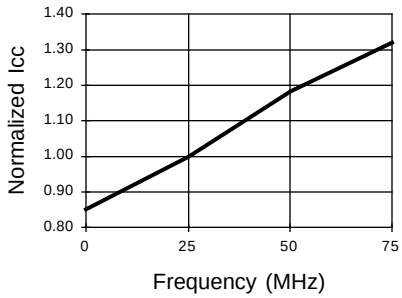
Normalized Icc vs Vcc



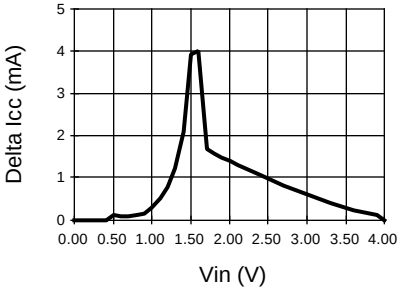
Normalized Icc vs Temp



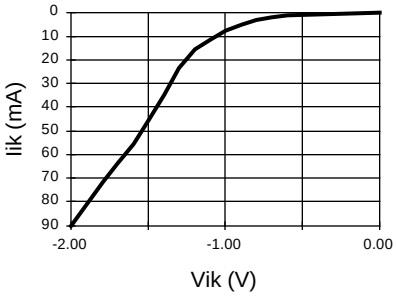
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



GAL20LV8

Low Voltage E²CMOS PLD Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 3.5 ns Maximum Propagation Delay**
  - **— Fmax = 250 MHz**
  - **— 2.5 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
  - **— TTL-Compatible Balanced 8mA Output Drive**
- **3.3V LOW VOLTAGE 20V8 ARCHITECTURE**
  - **— JEDEC-Compatible 3.3V Interface Standard**
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— Glue Logic for 3.3V Systems**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

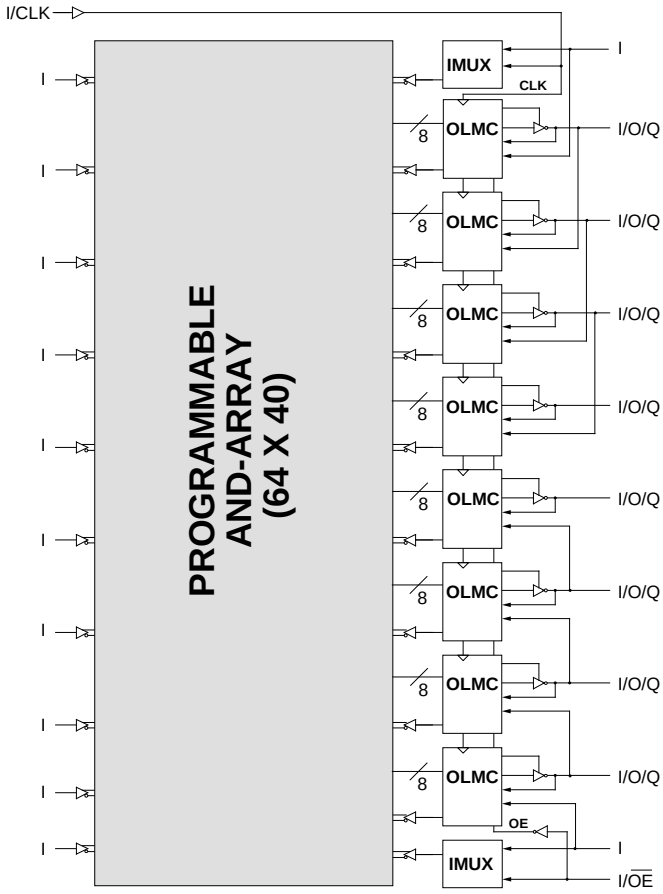
DESCRIPTION

The GAL20LV8D, at 3.5 ns maximum propagation delay time, provides the highest speed performance available in the PLD market. The GAL20LV8D is manufactured using Lattice Semiconductor's advanced 3.3V E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL20LV8D are the PAL architectures listed in the table of the macrocell description section. GAL20LV8D devices are capable of emulating any of these PAL architectures with full function/fuse map compatibility.

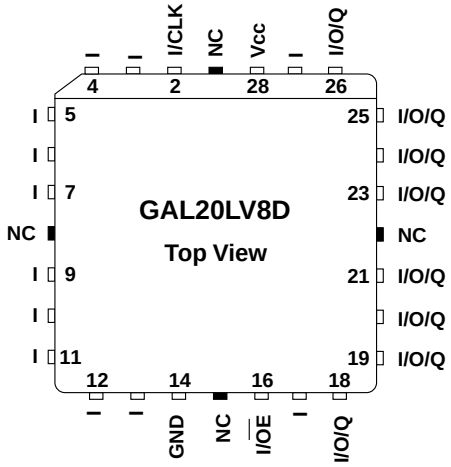
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

PLCC



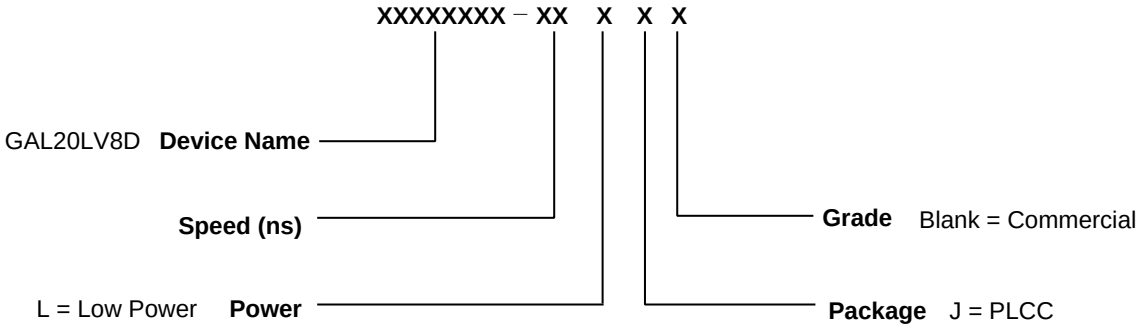
LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL20LV8 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
3.5	3	2.5	70	GAL20LV8D-3LJ	28-Lead PLCC
5	4	3	70	GAL20LV8D-5LJ	28-Lead PLCC
7.5	5	5	70	GAL20LV8D-7LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL20LV8D . The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL20LV8D can emulate. It also shows the OLMC mode under which the devices emulate the PAL architecture.

PAL Architectures Emulated by GAL20LV8D	GAL20LV8D Global OLMC Mode
20R8	**Registered**
20R6	**Registered**
20R4	**Registered**
20RP8	**Registered**
20RP6	**Registered**
20RP4	**Registered**
20L8	**Complex**
20H8	**Complex**
20P8	**Complex**
14L8	**Simple**
16L6	**Simple**
18L4	**Simple**
20L2	**Simple**
14H8	**Simple**
16H6	**Simple**
18H4	**Simple**
20H2	**Simple**
14P8	**Simple**
16P6	**Simple**
18P4	**Simple**
20P2	**Simple**

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 2 and pin 16 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 2 and pin 16 become dedicated inputs and use the feedback paths of pin 26 and pin 18 respectively. Because of this feedback path usage, pin 26 and pin 18 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 21 and 23) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOG/iC	GAL20V8_R	GAL20V8_C7	GAL20V8_C8	GAL20V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL20V8A
PLDesigner	P20V8R[2]	P20V8C[2]	P20V8C[2]	P20V8A
TANGO-PLD	G20V8R	G20V8C	G20V8AS[3]	G20V8

1) Used with **Configuration** keyword.
2) Prior to Version 2.0 support.
3) Supported on Version 1.20 or later.

REGISTERED MODE

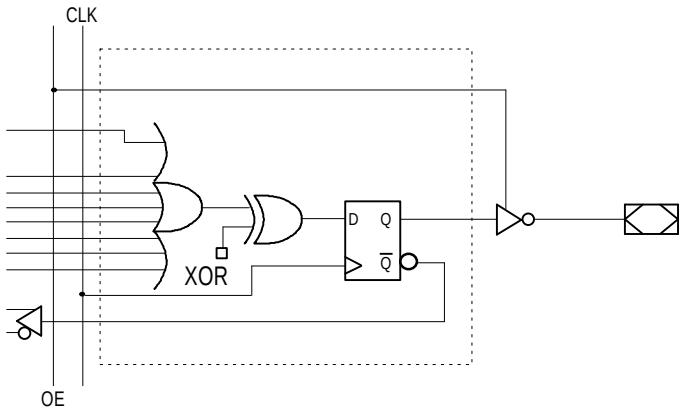
In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 20R8 and 20RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

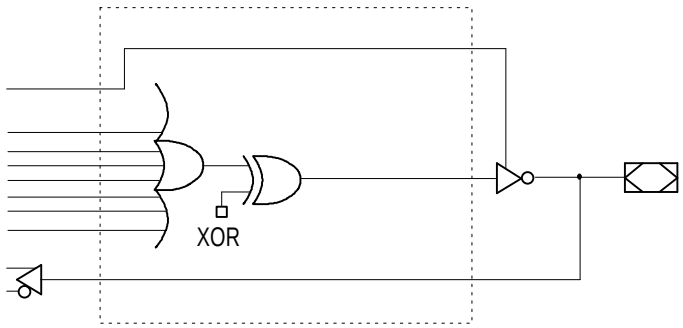
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 2 controls common CLK for the registered outputs.
- Pin 16 controls common $\overline{OE}$ for the registered outputs.
- Pin 2 & Pin 16 are permanently configured as CLK & $\overline{OE}$.



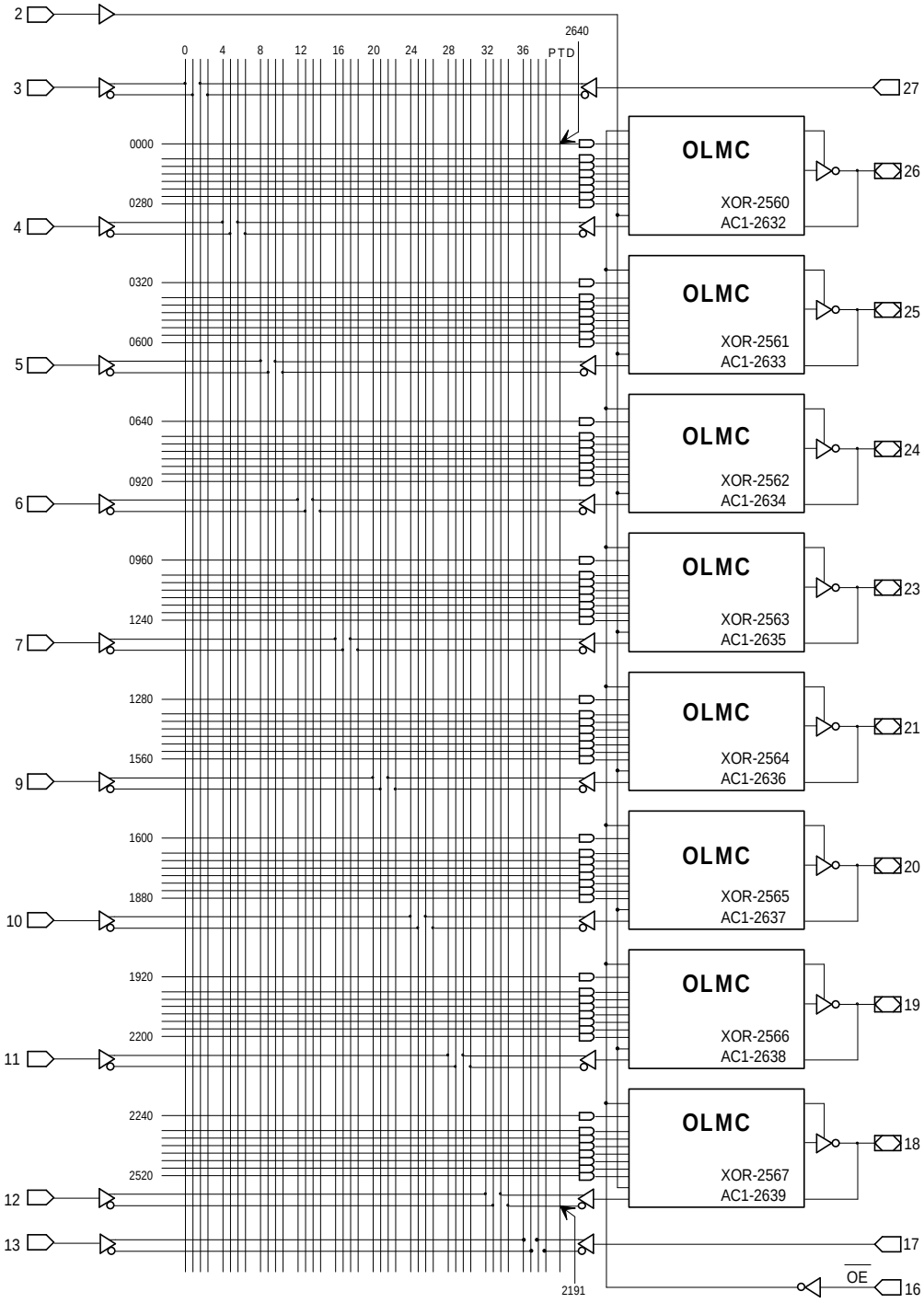
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 2 & Pin 16 are permanently configured as CLK & $\overline{OE}$.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

PLCC Package Pinout



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte7 | Byte6	.... Byte1 | Byte0

MSB LSB

SYN-2704
AC0-2705

COMPLEX MODE

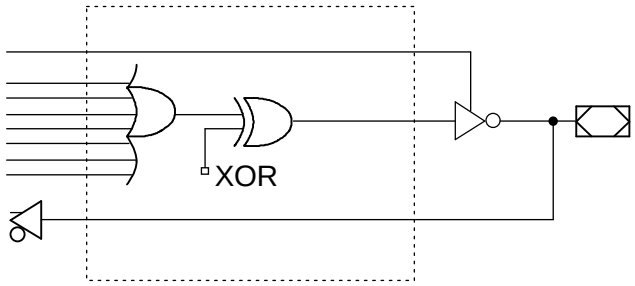
In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 20L8 and 20P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 18 & 26) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

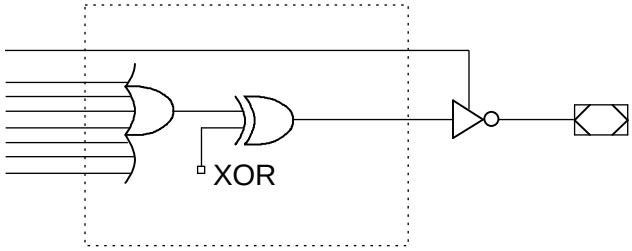
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 2 and 16 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 19 through Pin 25 are configured to this function.



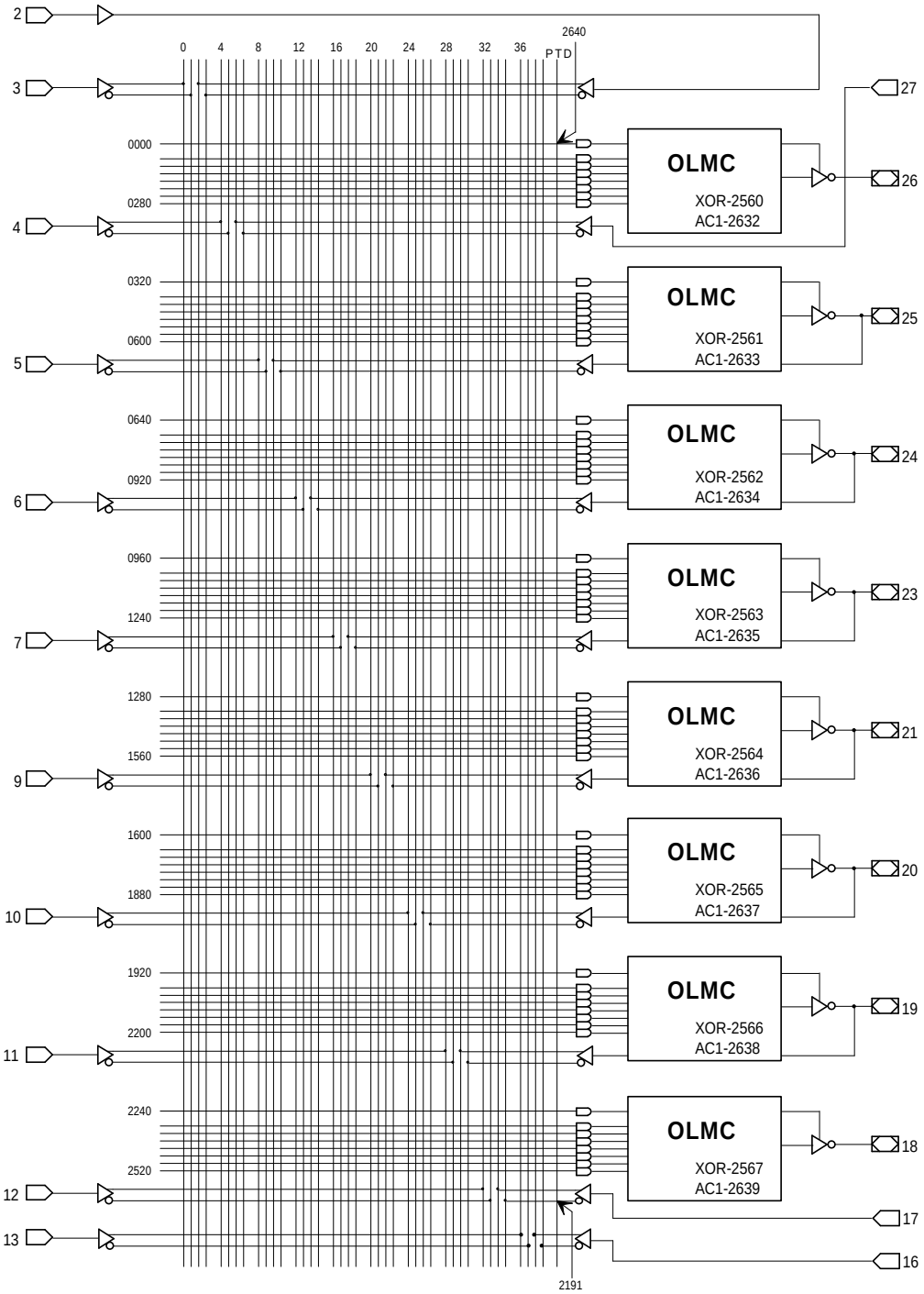
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 18 and Pin 26 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

PLCC Package Pinout



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte7 | Byte6	.... Byte1 | Byte0

MSB — LSB

SYN-2704
AC0-2705

SIMPLE MODE

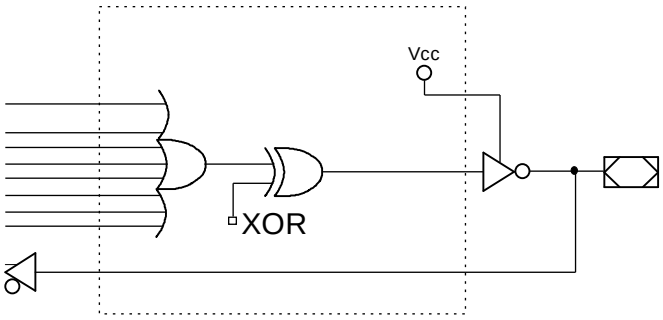
In the Simple mode, pins are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 14L8 and 16P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

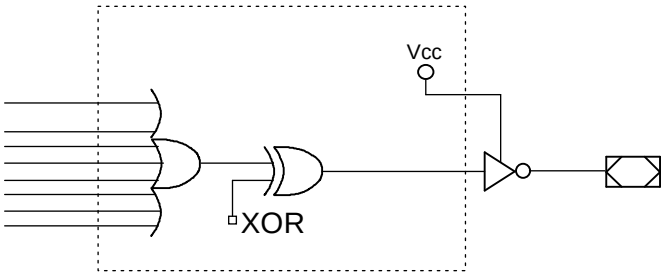
Pins 2 and 16 are always available as data inputs into the AND array. The "center" two macrocells (pins 21 & 23) cannot be used in the input configuration.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



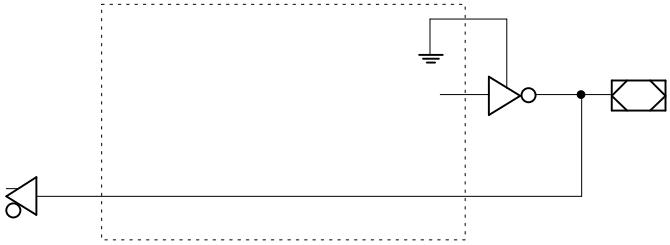
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 21 & 23 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 21 & 23 are permanently configured to this function.



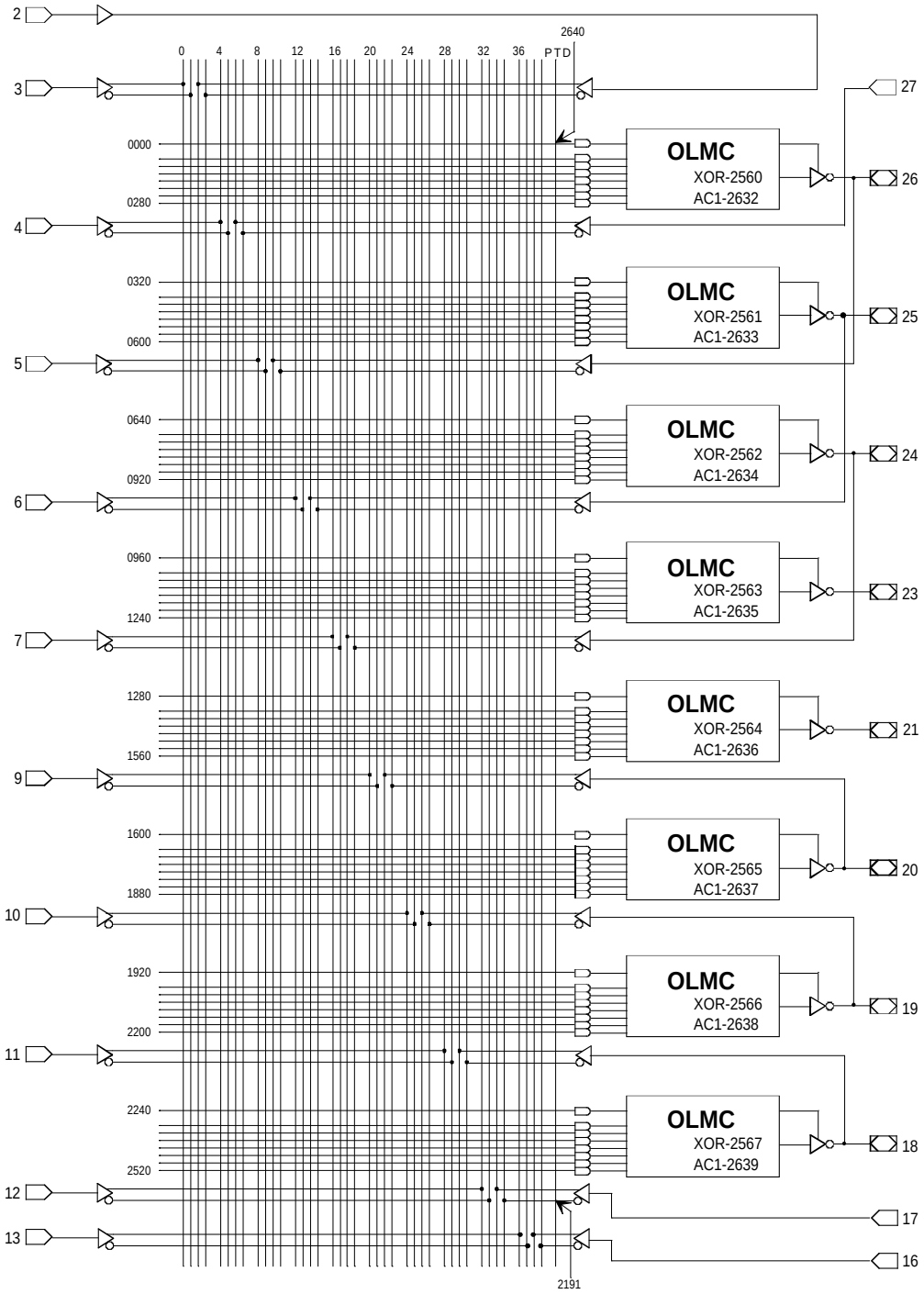
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 21 & 23 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

PLCC Package Pinout



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte7 | Byte6	.... Byte1 | Byte0

MSB — LSB

SYN-2704
AC0-2705

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +4.6V
Input voltage applied ..... –0.5 to +4.6V
Off-state output voltage applied ..... –0.5 to +4.6V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.3	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+0.5	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$Vcc\text{-}0.2V \le V_{IN} \le V_{CC}$	—	—	10	µA
		$Vcc \le V_{IN} \le$ 4.6V	—	—	20	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.4	V
		I_{OL} = 500µA Vin = V_{IL} or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -100µA Vin = V_{IL} or V_{IH}	Vcc-0.2V	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	–8	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = 0.5V T_A= 25°C	–15	—	–80	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0V V_{IH} = 3.0V Unused Inputs at V_{IL} f_{toggle} = 1MHz Outputs Open	—	45	70	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 3.3V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -3		COM -5		COM -7		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd[2]	A	Input or I/O to Combinational Output	1	3.5	1	5	1	7.5	ns
tco[2]	A	Clock to Output Delay	1	2.5	1	3	1	5	ns
tcf[3]	—	Clock to Feedback Delay	—	2	—	2	—	3	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	3	—	4	—	5	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
fmax[4]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	180	—	142.8	—	100	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	200	—	166	—	125	—	MHz
	A	Maximum Clock Frequency with No Feedback	250	—	166	—	125	—	MHz
twh[4]	—	Clock Pulse Duration, High	2	—	3	—	4	—	ns
twl[4]	—	Clock Pulse Duration, Low	2	—	3	—	4	—	ns
ten	B	Input or I/O to Output Enabled	—	4.5	—	6	—	7.5	ns
	B	$\overline{OE}$ to Output Enabled	—	3.5	—	5	—	6.5	ns
tdis	C	Input or I/O to Output Disabled	—	4.5	—	6	—	7.5	ns
	C	$\overline{OE}$ to Output Disabled	—	3.5	—	5	—	6.5	ns

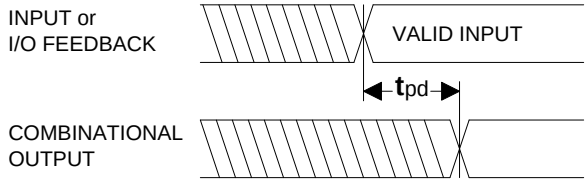
1) Refer to Switching Test Conditions section.
2) Minimum values for tpd and tco are not 100% tested but established by characterization.
3) Calculated from fmax with internal feedback. Refer to fmax Descriptions section.
4) Refer to fmax Descriptions section. Guaranteed by characterization.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

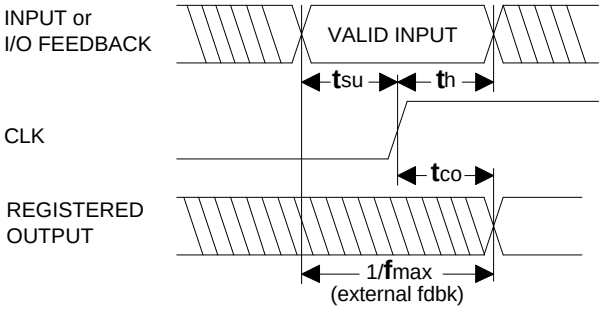
SYMBOL	PARAMETER	TYPICAL*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	5	pF	V_{CC} = 3.3V, V_I = 0V
$C_{I/O}$	I/O Capacitance	5	pF	V_{CC} = 3.3V, $V_{I/O}$ = 0V

*Guaranteed but not 100% tested.

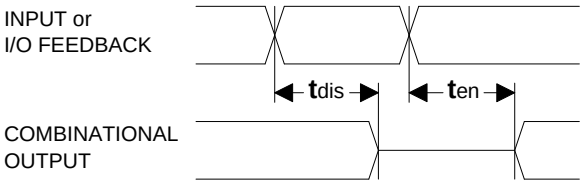
SWITCHING WAVEFORMS



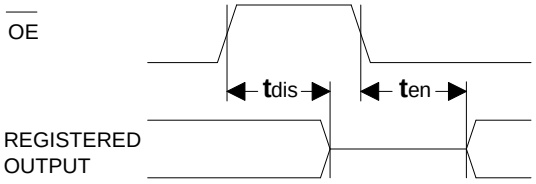
Combinatorial Output



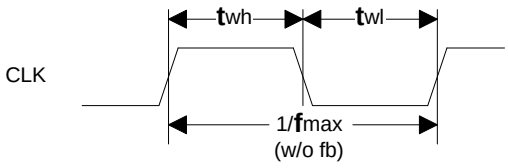
Registered Output



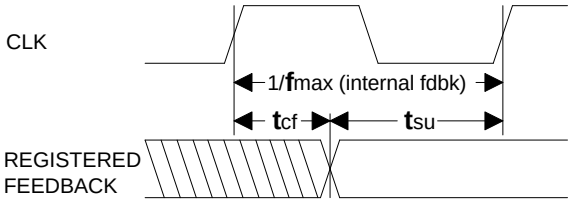
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

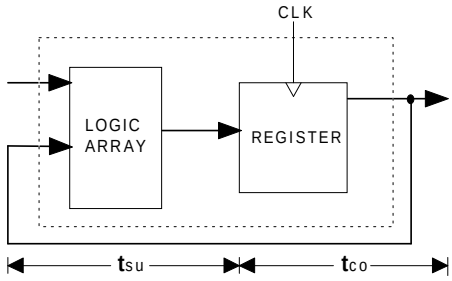


Clock Width



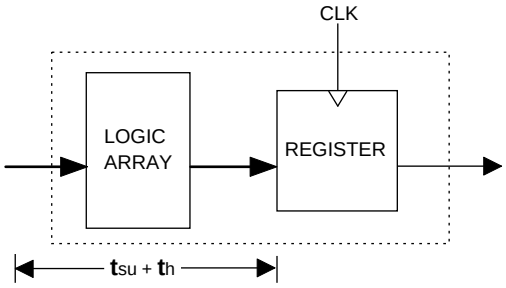
fmax with Feedback

fmax DESCRIPTIONS



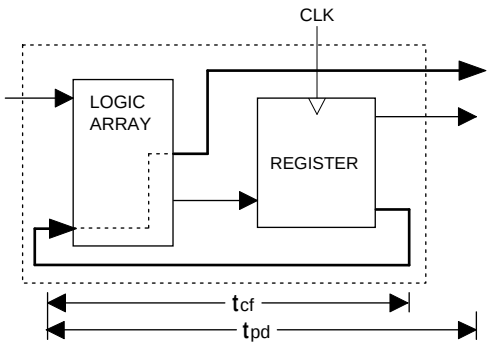
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

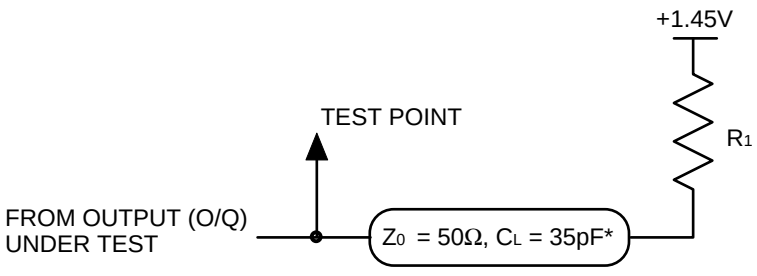
Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	1.5ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Output Load Conditions (see figure)

Test Condition		R_1	C_L
A		50Ω	35pF
B	High Z to Active High at 1.9V	50Ω	35pF
	High Z to Active Low at 1.0V	50Ω	35pF
C	Active High to High Z at 1.9V	50Ω	35pF
	Active Low to High Z at 1.0V	50Ω	35pF



*C_L includes test fixture and probe capacitance.

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL20LV8D device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

SECURITY CELL

A security cell is provided in the GAL20LV8D devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL20LV8D devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias minimizes the potential of latch-up caused by negative input undershoots.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

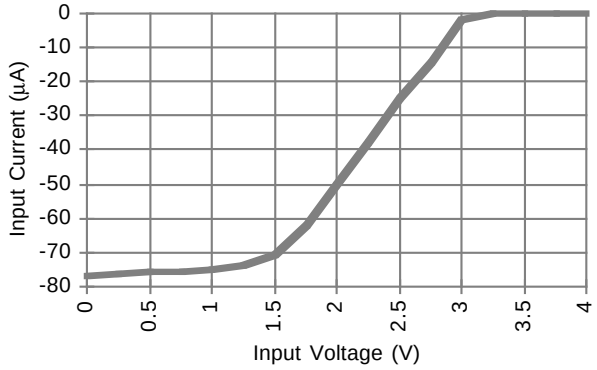
GAL20LV8D devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

INPUT BUFFERS

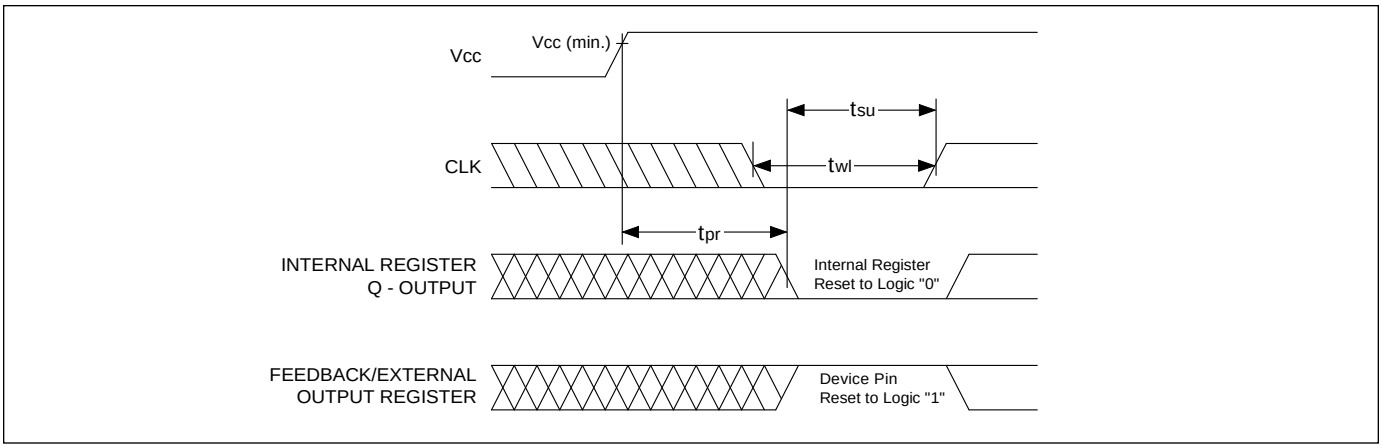
GAL20LV8D devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL20LV8D input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or Ground. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Pull-up Characteristic

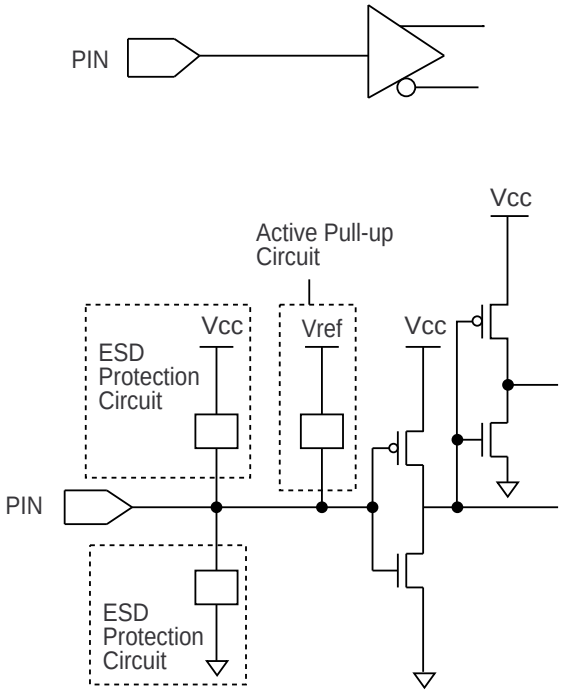


POWER-UP RESET



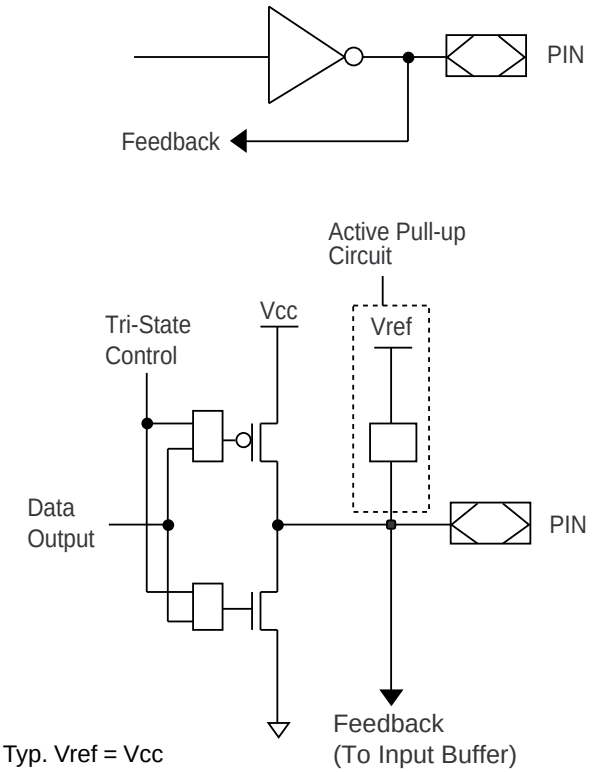
Circuitry within the GAL20LV8D provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr}, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the device. First, the V_{CC} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typ. Vref = Vcc

Typical Input

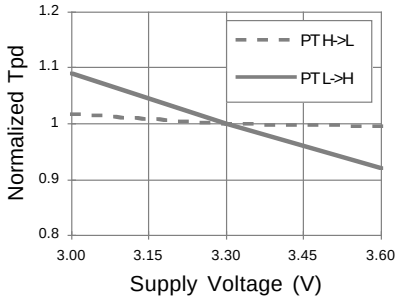


Typ. Vref = Vcc

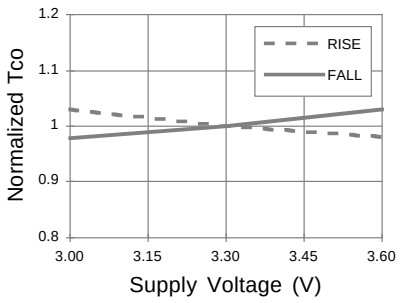
Typical Output

TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

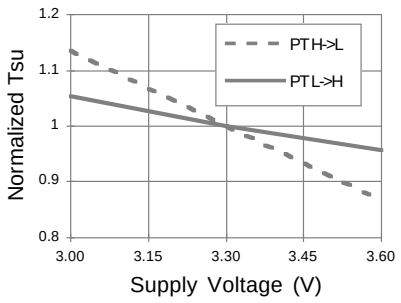
Normalized Tpd vs Vcc



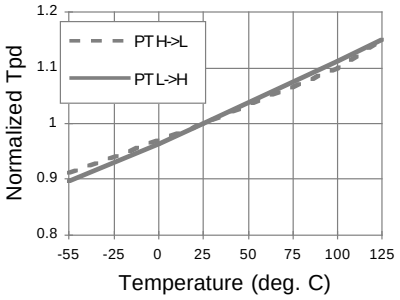
Normalized Tco vs Vcc



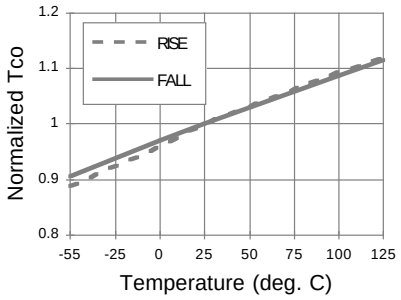
Normalized Tsu vs Vcc



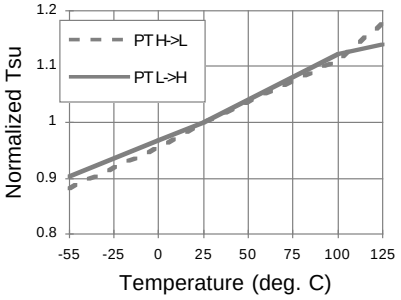
Normalized Tpd vs Temp



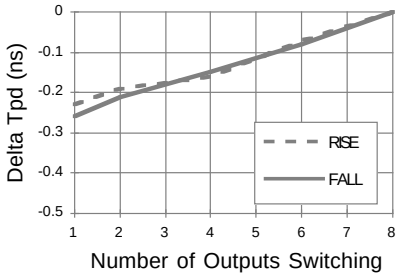
Normalized Tco vs Temp



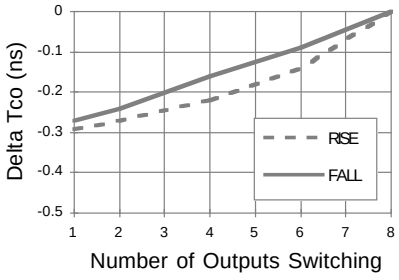
Normalized Tsu vs Temp



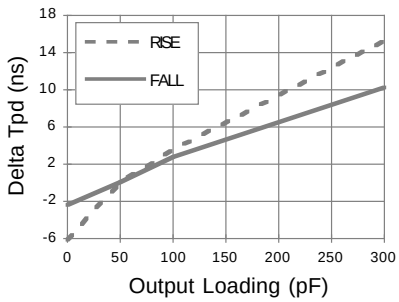
Delta Tpd vs # of Outputs Switching



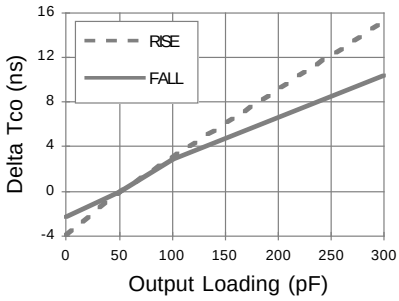
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

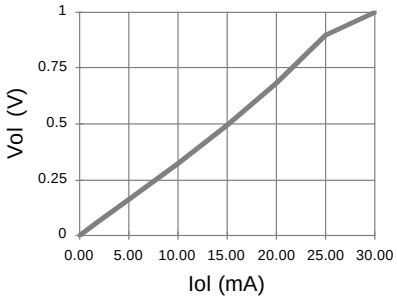


Delta Tco vs Output Loading

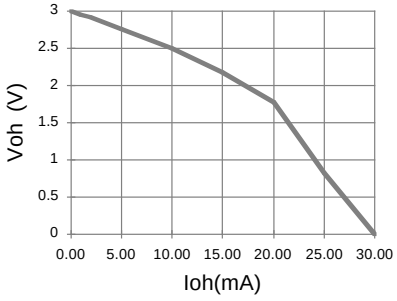


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

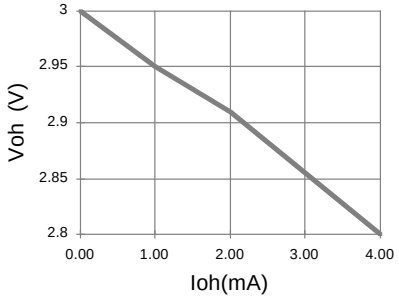
Vol vs Iol



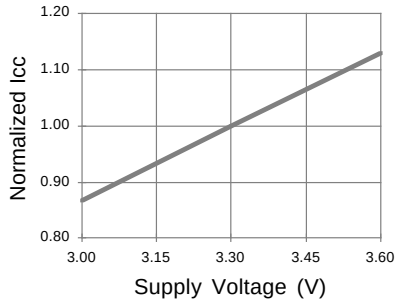
Voh vs Ioh



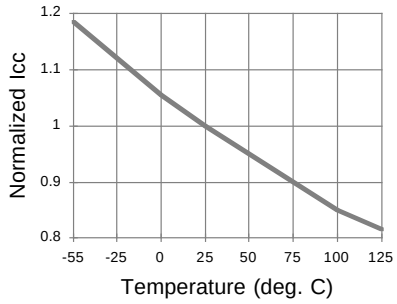
Voh vs Ioh



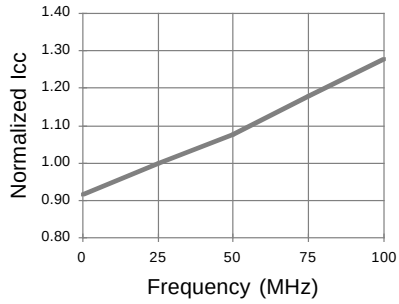
Normalized Icc vs Vcc



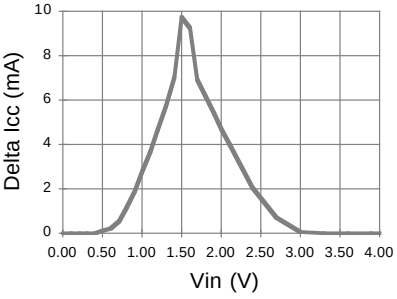
Normalized Icc vs Temp



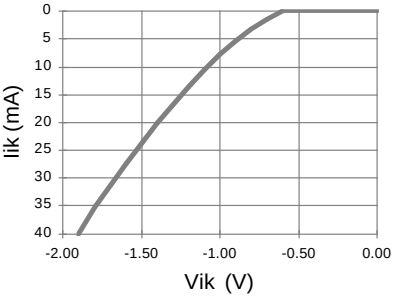
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



GAL20LV8ZD

Low Voltage, Zero Power E²CMOS PLD
Generic Array Logic™

FEATURES

- **3.3V LOW VOLTAGE, ZERO POWER OPERATION**
  - **— JEDEC Compatible 3.3V Interface Standard**
  - **— Interfaces with Standard 5V TTL Devices**
  - **— 50μA Typical Standby Current (100μA Max.)**
  - **— 45mA Typical Active Current (55mA Max.)**
  - **— Dedicated Power-down Pin**
- **HIGH PERFORMANCE E²CMOS TECHNOLOGY**
  - **— TTL Compatible Balanced 8 mA Output Drive**
  - **— 15 ns Maximum Propagation Delay**
  - **— Fmax = 62.5 MHz**
  - **— 10 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— Glue Logic for 3.3V Systems**
  - **— Ideal for Mixed 3.3V and 5V Systems**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

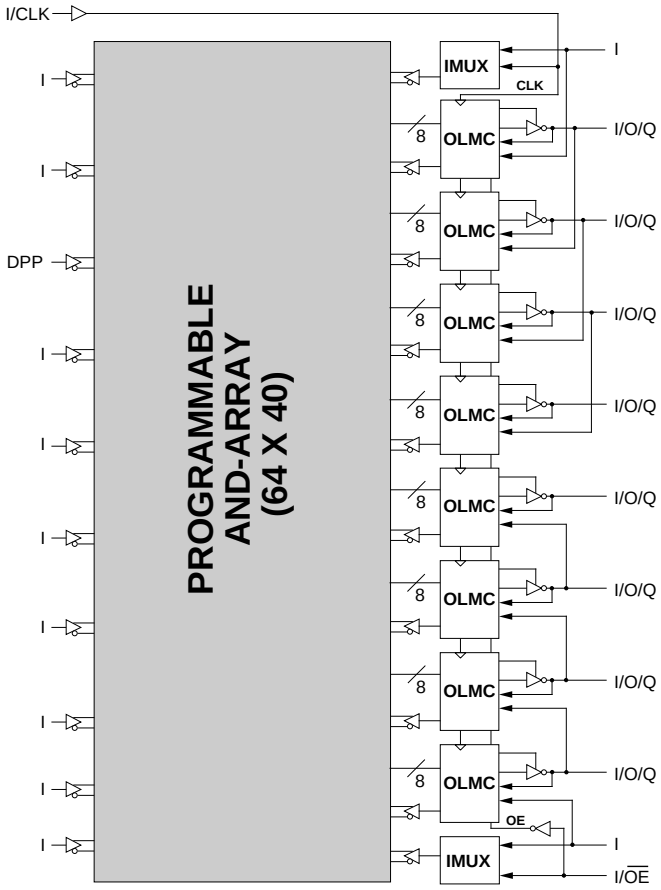
DESCRIPTION

The GAL20LV8ZD, at 100 μA standby current and 15ns propagation delay provides the highest speed low-voltage PLD available in the market. The GAL20LV8ZD is manufactured using Lattice Semiconductor's advanced 3.3V E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology.

The GAL20LV8ZD utilizes a dedicated power-down pin (DPP) to put the device into standby mode. It has 19 inputs available to the AND array and is capable of interfacing with both 3.3V and standard 5V devices.

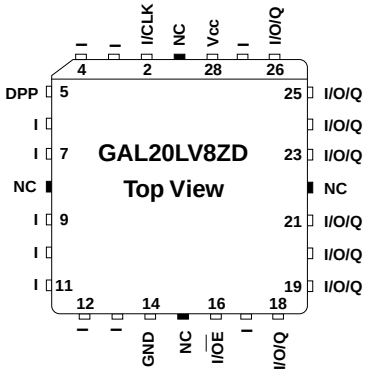
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

PLCC



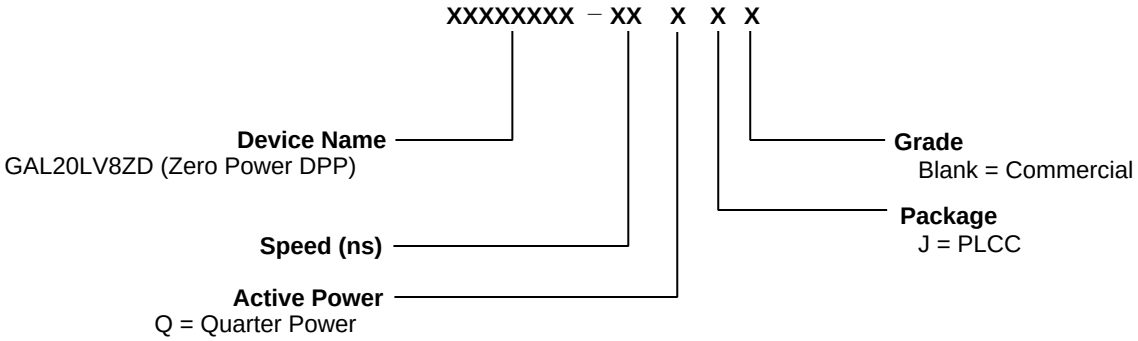
LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL20LV8ZD ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Isb (μA)	Ordering #	Package
15	12	10	55	100	GAL20LV8ZD-15QJ	28-Lead PLCC
25	15	15	55	100	GAL20LV8ZD-25QJ	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL20LV8ZD. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. Most compilers also have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 2 and pin 16 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 2 and pin 16 become dedicated inputs and use the feedback paths of pin 26 and pin 18 respectively. Because of this feedback path usage, pin 26 and pin 18 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 21 and 23) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

When using the standard GAL20V8 JEDEC fuse pattern generated by the logic compilers for the GAL20LV8ZD, special attention must be given to pin 5 (DPP) to make sure that it is not used as one of the functional inputs.

REGISTERED MODE

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

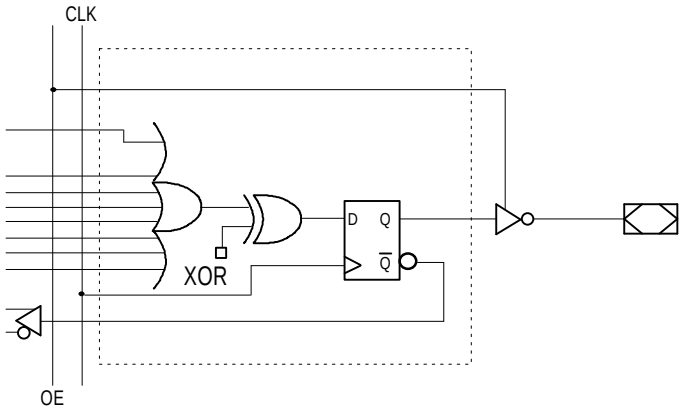
Architecture configurations available in this mode are similar to the common 20R8 and 20RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

Registered outputs have eight product terms per output. I/O's have seven product terms per output.

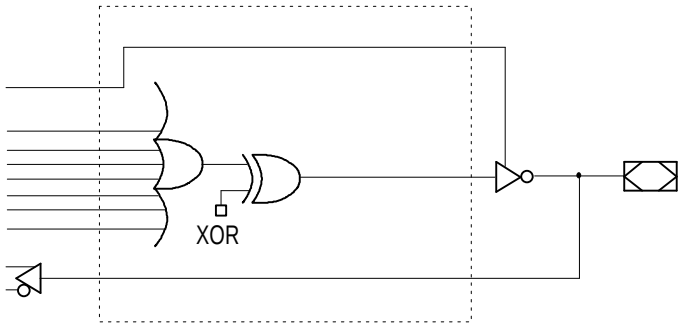
Pin 5 is used as dedicated power-down pin on GAL20LV8ZD. It cannot be used as functional input.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 2 controls common CLK for the registered outputs.
- Pin 16 controls common $\overline{OE}$ for the registered outputs.
- Pin 2 & Pin 16 are permanently configured as CLK & $\overline{OE}$.



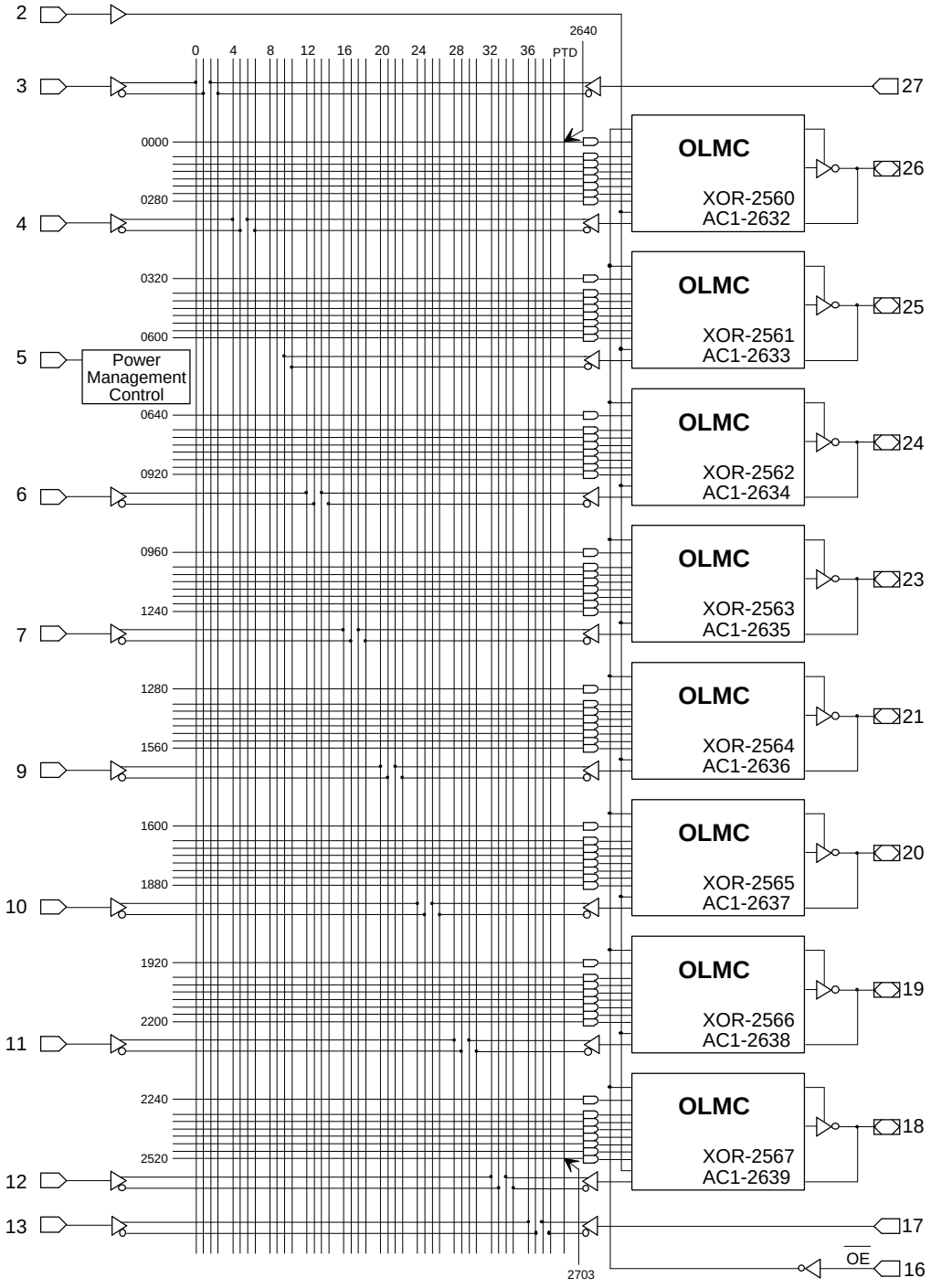
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 2 & Pin 16 are permanently configured as CLK & $\overline{OE}$.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

PLCC Package Pinout



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte7 | Byte6	.... Byte1 | Byte0

MSB LSB

SYN-2704
AC0-2705

COMPLEX MODE

In the Complex mode, macrocells are configured as output only or I/O functions.

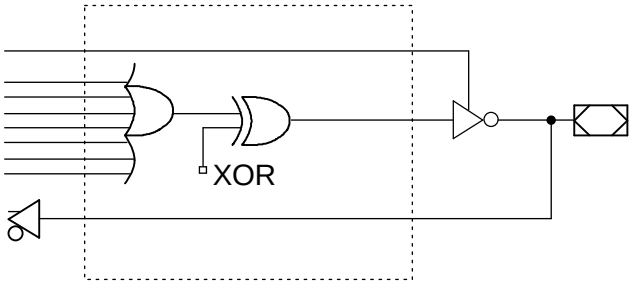
Architecture configurations available in this mode are similar to the common 20L8 and 20P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 18 & 26) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 2 and 16 are always available as data inputs into the AND array.

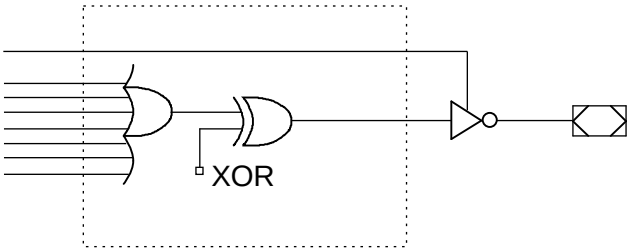
Pin 5 is used as dedicated power-down pin on GAL20LV8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 19 through Pin 25 are configured to this function.



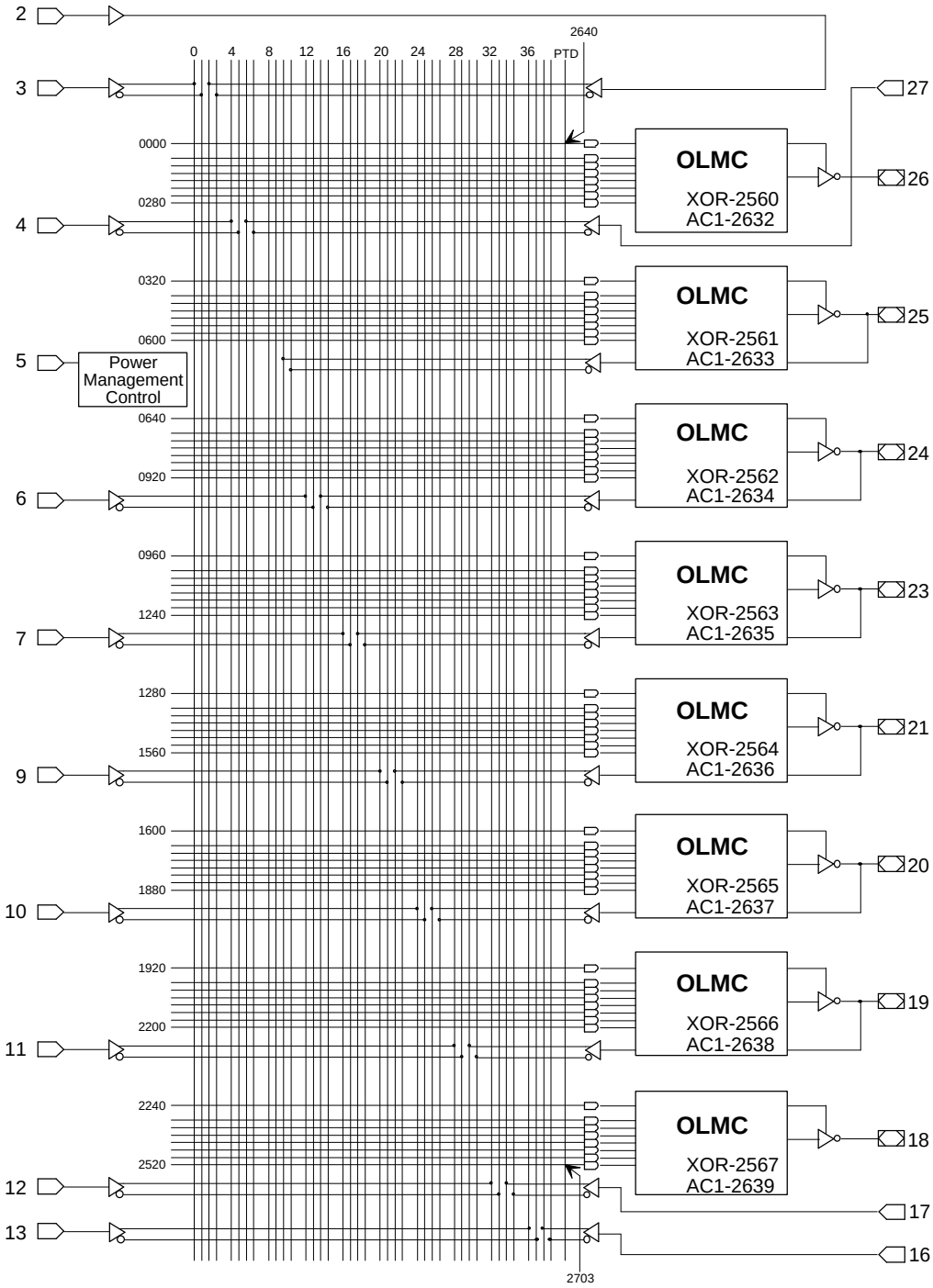
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 18 and Pin 26 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

PLCC Package Pinout



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...		.... 2630, 2631
Byte7	Byte6	.... Byte1 Byte0

MSB LSB

SYN-2704
AC0-2705

SIMPLE MODE

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

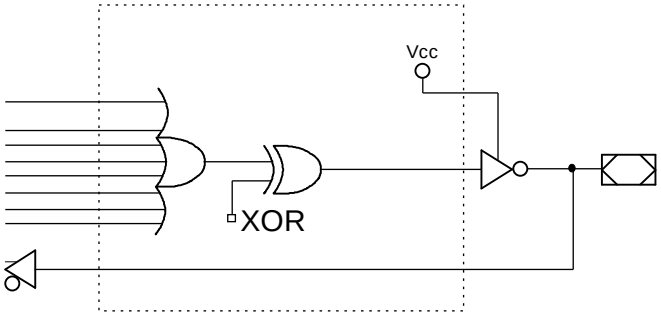
Architecture configurations available in this mode are similar to the common 14L8 and 16P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

Pins 2 and 16 are always available as data inputs into the AND array. The center two macrocells (pins 21 & 23) cannot be used in the input configuration.

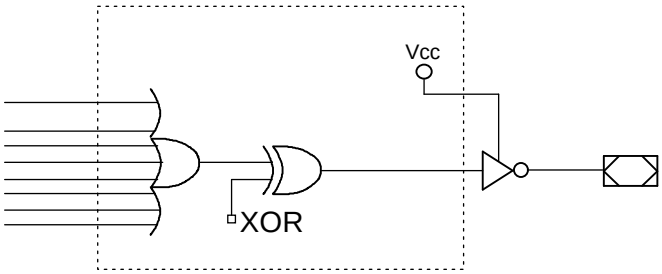
Pin 5 is used as dedicated power-down pin on GAL20LV8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



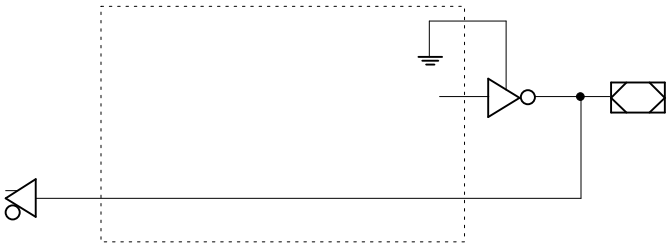
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 21 & 23 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 21 & 23 are permanently configured to this function.



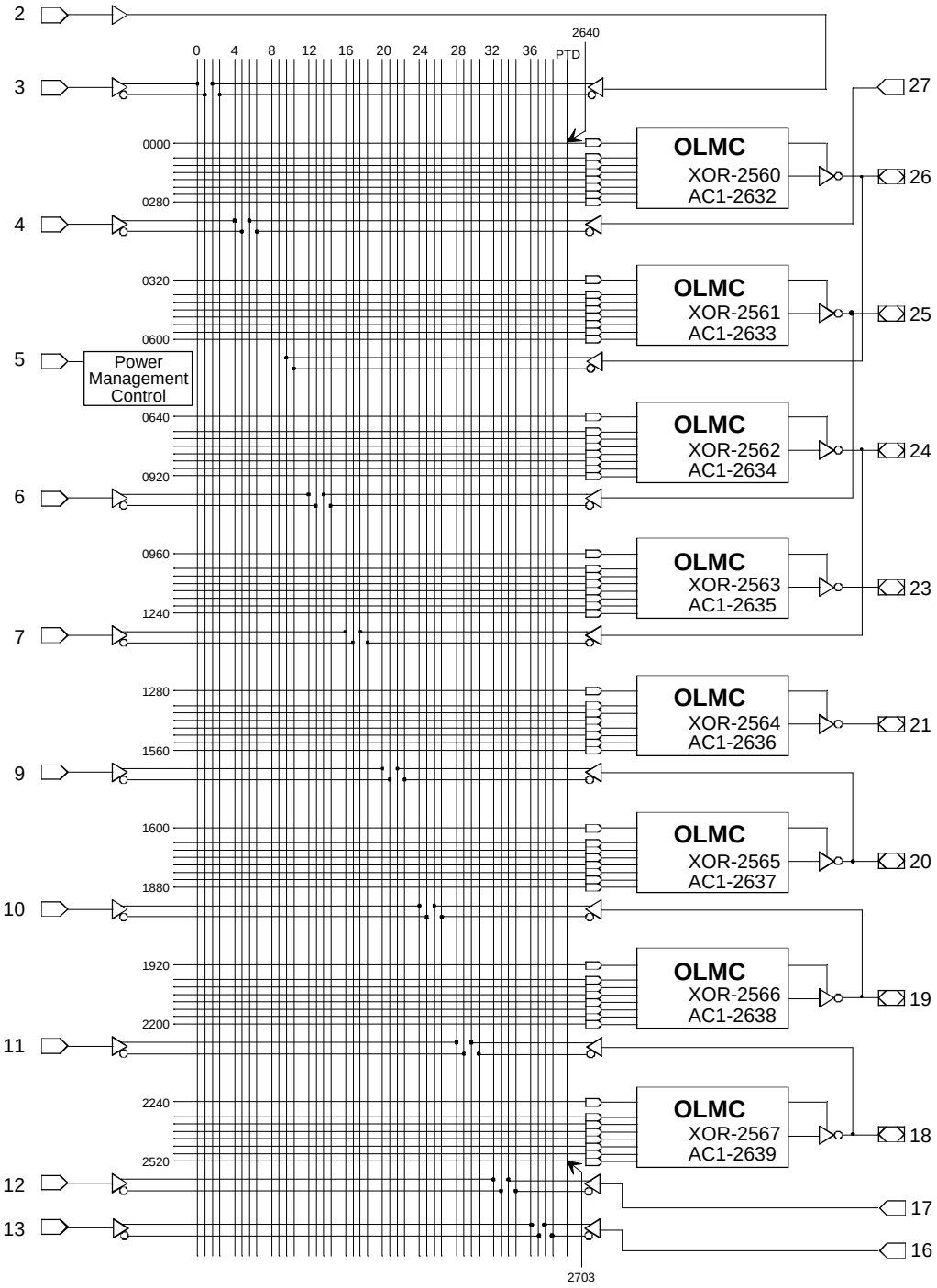
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 21 & 23 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte7 | Byte6	.... Byte1 | Byte0

MSB — LSB

SYN-2704
AC0-2705

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +5.6V

Input voltage applied ..... -0.5 to +5.6V
Off-state output voltage applied ..... -0.5 to +5.6V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	5.25	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CC}\text{-}0.2)V \le V_{IN} \le V_{CC}$	—	—	10	µA
		$V_{CC} \le V_{IN} \le 5.25V$	—	—	1	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. $V_{in} = V_{IL}$ or V_{IH}	—	—	0.5	V
		I_{OL} = 0.5 mA $V_{in} = V_{IL}$ or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} = MAX. $V_{in} = V_{IL}$ or V_{IH}	2.4	—	—	V
		I_{OH} = -0.5 mA $V_{in} = V_{IL}$ or V_{IH}	Vcc-0.45	—	—	V
		I_{OH} = -100µA $V_{in} = V_{IL}$ or V_{IH}	Vcc-0.2	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-8	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = GND T_A = 25°C	-30	—	-130	mA

COMMERCIAL

I_{SB}	Stand-by Power Supply Current	V_{IL} = GND V_{IH} = Vcc Outputs Open	ZD -15/-25	—	50	100	µA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15 MHz Outputs Open	ZD -15/-25	—	45	55	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 3.3V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM	TEST COND.[1]	DESCRIPTION	COM -15 MIN.	COM -15 MAX.	COM -25 MIN.	COM -25 MAX.	UNITS
tpd	A	Input or I/O to Combinatorial Output	3	15	3	25	ns
tco	A	Clock to Output Delay	2	10	2	15	ns
tcf[2]	—	Clock to Feedback Delay	—	8	—	10	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑	12	—	15	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	45.5	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	50	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	62.5	—	41.6	—	MHz
twh	—	Clock Pulse Duration, High	8	—	12	—	ns
twl	—	Clock Pulse Duration, Low	8	—	12	—	ns
ten	B	Input or I/O to Output Enabled	—	17	—	25	ns
	B	OE↓ to Output Enabled	—	16	—	20	ns
tdis	C	Input or I/O to Output Disabled	—	18	—	25	ns
	C	OE↑ to Output Disabled	—	17	—	20	ns

1) Refer to Switching Test Conditions section.
2) Calculated from fmax with internal feedback. Refer to fmax Description section.
3) Refer to fmax Description section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TYPICAL*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 3.3V, V_I = 0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 3.3V, $V_{I/O}$ = 0V

*Guaranteed but not 100% tested.

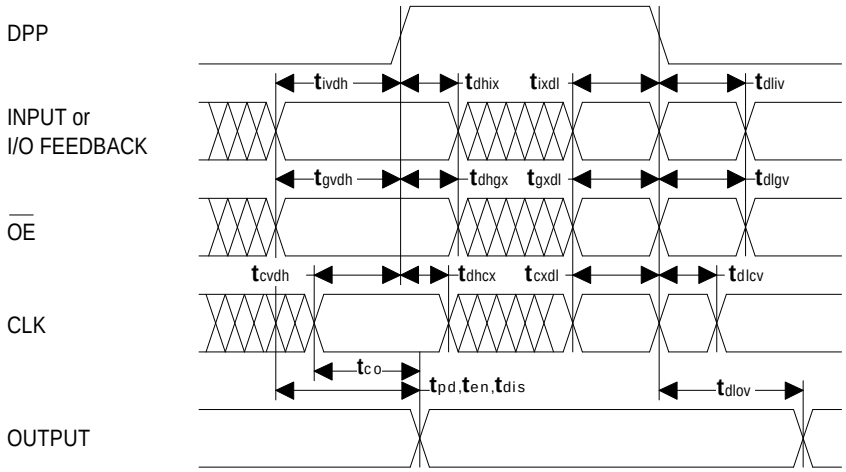
DEDICATED POWER-DOWN PIN SPECIFICATIONS

Over Recommended Operating Conditions

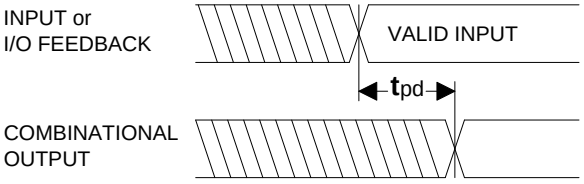
PARAMETER	TEST COND[1].	DESCRIPTION	COM -15		COM -25		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{whd}	—	DPP Pulse Duration High	40	—	40	—	ns
t_{wld}	—	DPP Pulse Duration Low	30	—	40	—	ns
ACTIVE TO STANDBY							
t_{ivdh}	—	Valid Input before DPP High	0	—	0	—	ns
t_{gvdh}	—	Valid OE before DPP High	0	—	0	—	ns
t_{cvdh}	—	Valid Clock before DPP High	0	—	0	—	ns
t_{dhix}	—	Input Don't Care after DPP High	—	15	—	25	ns
t_{dhgx}	—	$\overline{OE}$ Don't Care after DPP High	—	15	—	25	ns
t_{dhcx}	—	Clock Don't Care after DPP High	—	15	—	25	ns
STANDBY TO ACTIVE							
t_{ixdl}	—	Input Don't Care before DPP Low	—	0	—	0	ns
t_{gxdl}	—	$\overline{OE}$ Don't Care before DPP Low	—	0	—	0	ns
t_{cxdl}	—	Clock Don't Care before DPP Low	—	0	—	0	ns
t_{dliv}	—	DPP Low to Valid Input	20	—	25	—	ns
t_{dlgv}	—	DPP Low to Valid OE	20	—	25	—	ns
t_{dlcv}	—	DPP Low to Valid Clock	30	—	35	—	ns
t_{dlov}	A	DPP Low to Valid Output	5	45	5	45	ns

1) Refer to **Switching Test Conditions** section.

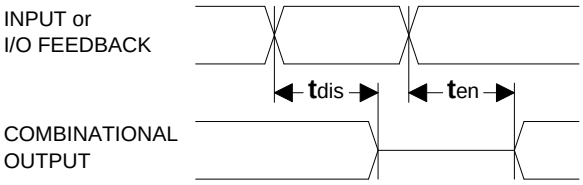
DEDICATED POWER-DOWN PIN (DPP) TIMING WAVEFORMS



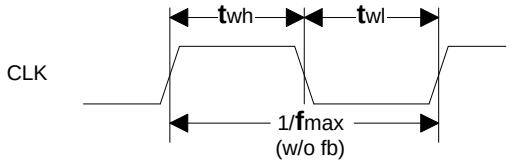
SWITCHING WAVEFORMS



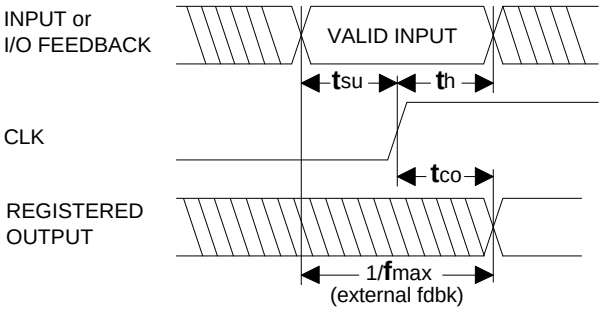
Combinatorial Output



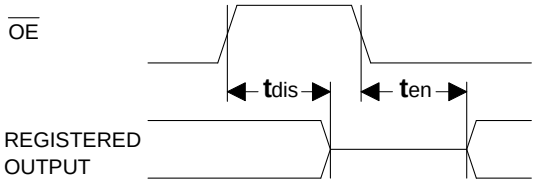
Input or I/O to Output Enable/Disable



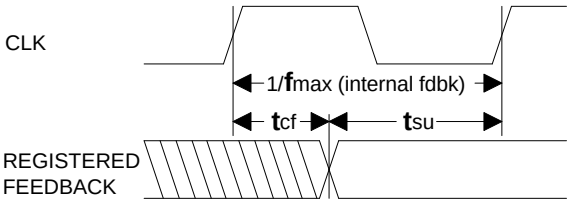
Clock Width



Registered Output

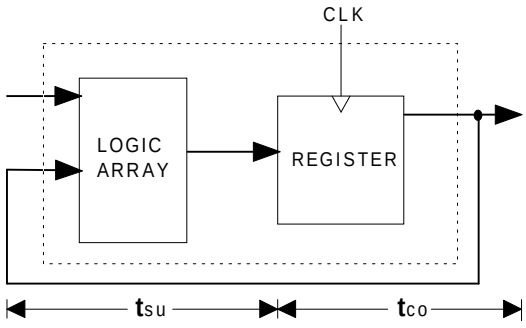


$\overline{OE}$ to Output Enable/Disable



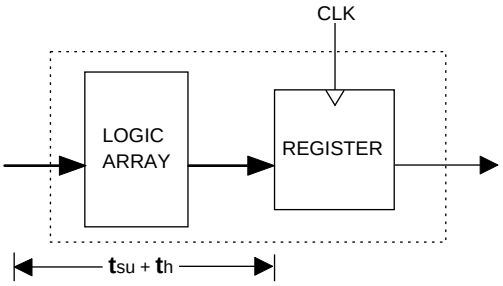
fmax with Feedback

fmax SPECIFICATIONS



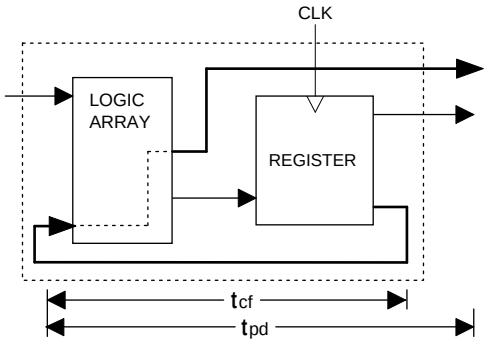
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

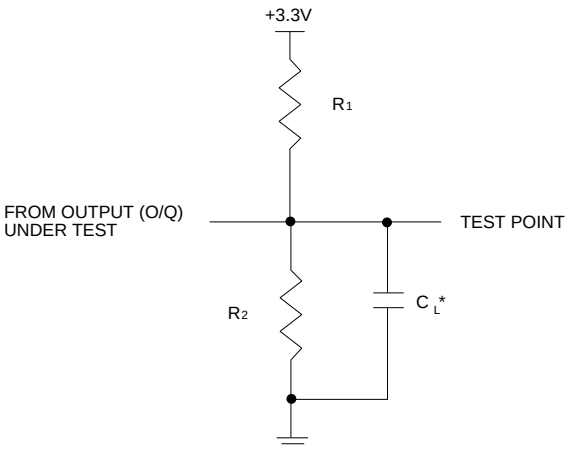
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	2ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level. 3-state to active transitions are measured at (Voh - 0.5) V and (Vol + 0.5) V.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		270Ω	220Ω	35pF
B	Active High	270Ω	220Ω	35pF
	Active Low	270Ω	220Ω	35pF
C	Active High	270Ω	220Ω	5pF
	Active Low	270Ω	220Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL20LV8ZD device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter checksum.

SECURITY CELL

A security cell is provided in the GAL20LV8ZD devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The electronic signature data is always available to the user, regardless of the state of this security cell.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

The GAL20LV8ZD devices includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

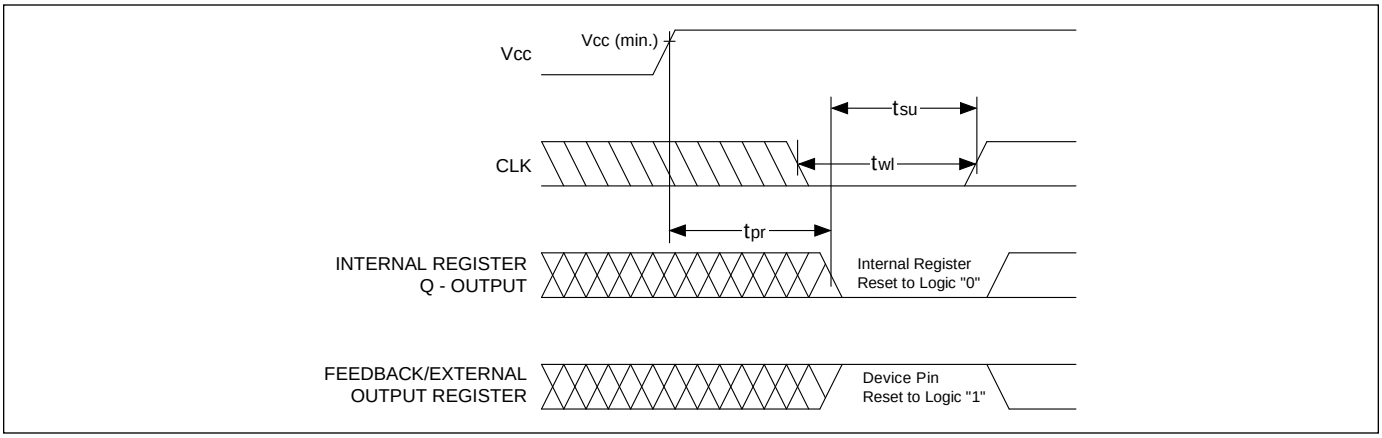
INPUT BUFFERS

GAL20LV8ZD devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

DEDICATED POWER-DOWN PIN (DPP)

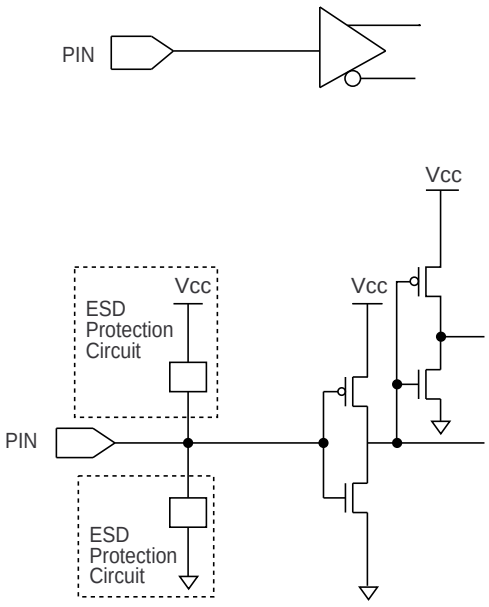
The GAL20LV8ZD uses pin 5 as the dedicated power-down signal to put the device in to the power-down state. DPP is an active high signal where a logic high driven on this signal puts the device into power-down state. Input pin 5 cannot be used as a logic function input on this device.

POWER-UP RESET

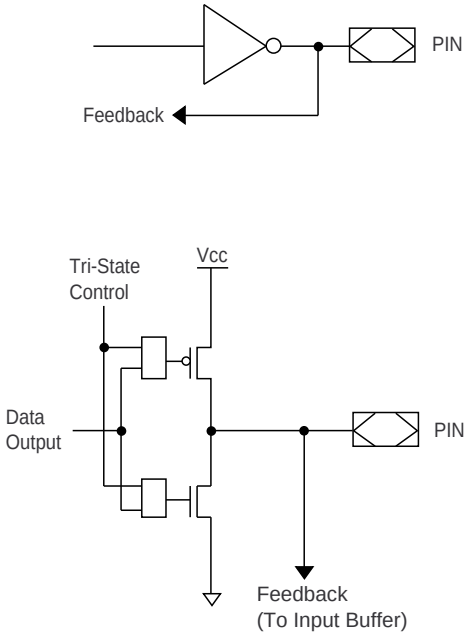


Circuitry within the GAL20LV8ZD provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr}, 10µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20LV8ZD. First, the V_{CC} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



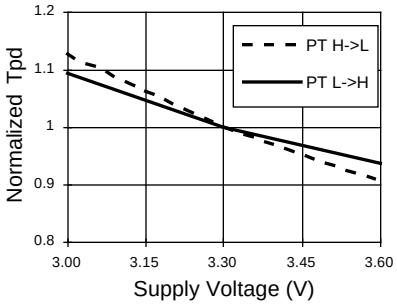
Typical Input



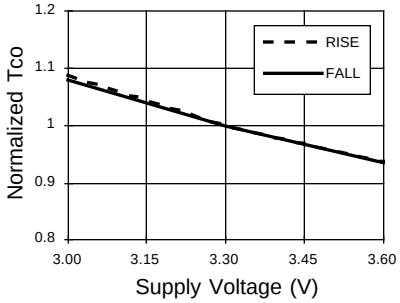
Typical Output

TYPICAL AC AND DC CHARACTERISTICS

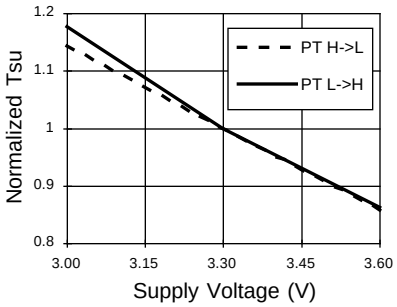
Normalized Tpd vs Vcc



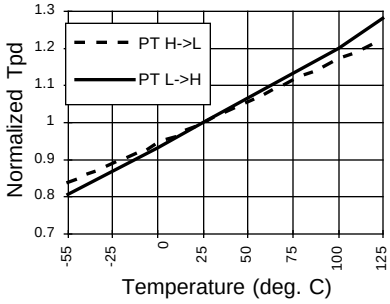
Normalized Tco vs Vcc



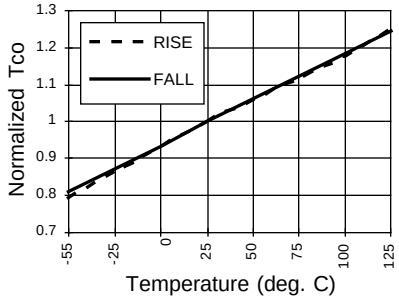
Normalized Tsu vs Vcc



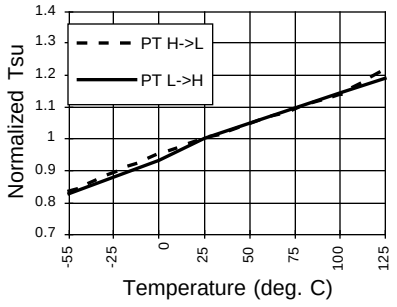
Normalized Tpd vs Temp



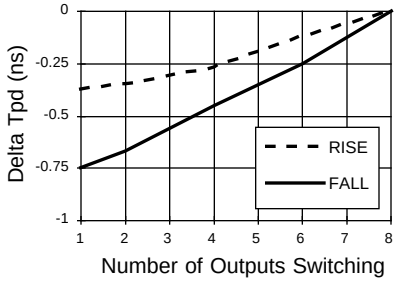
Normalized Tco vs Temp



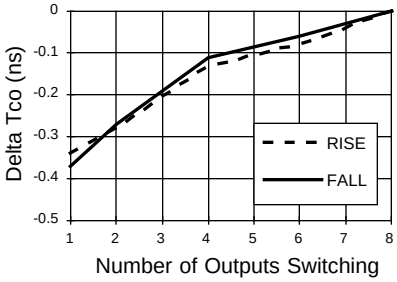
Normalized Tsu vs Temp



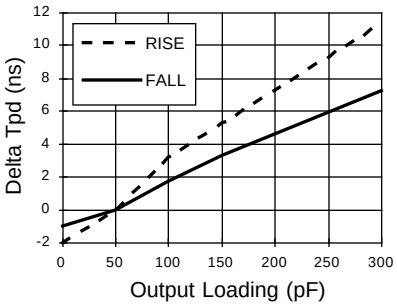
Delta Tpd vs # of Outputs Switching



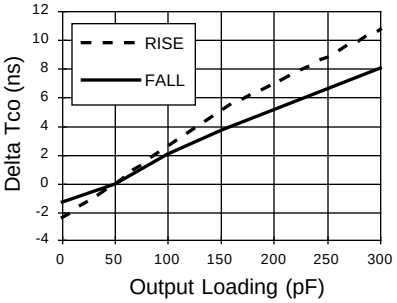
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

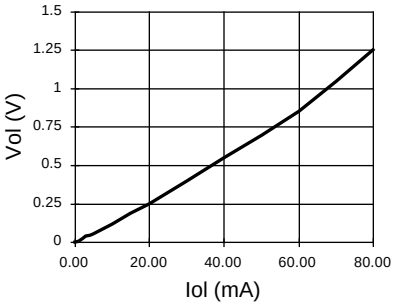


Delta Tco vs Output Loading

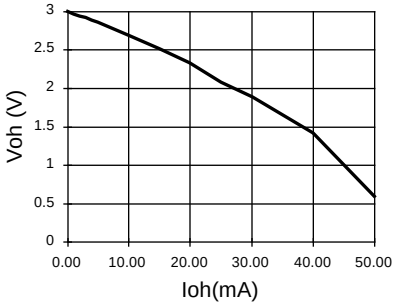


TYPICAL AC AND DC CHARACTERISTICS

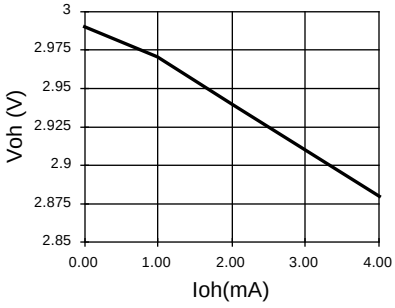
Vol vs Iol



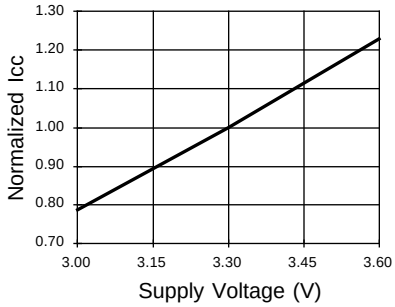
Voh vs Ioh



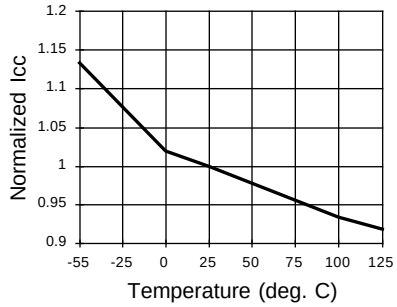
Voh vs Ioh



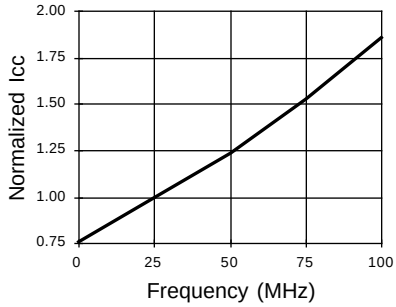
Normalized Icc vs Vcc



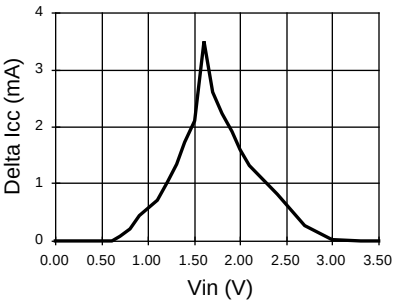
Normalized Icc vs Temp



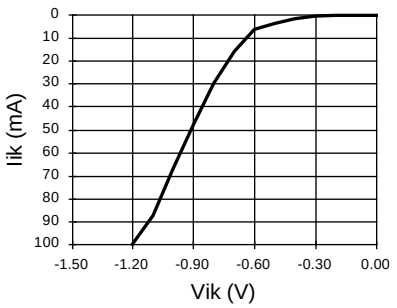
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



GAL20V8Z
GAL20V8ZD

Zero Power E²CMOS PLD

FEATURES

- **ZERO POWER E²CMOS TECHNOLOGY**
  - **— 100μA Standby Current**
  - **— Input Transition Detection on GAL20V8Z**
  - **— Dedicated Power-down Pin on GAL20V8ZD**
  - **— Input and Output Latching During Power Down**
- **HIGH PERFORMANCE E²CMOS TECHNOLOGY**
  - **— 12 ns Maximum Propagation Delay**
  - **— Fmax = 83.3 MHz**
  - **— 8 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 16 mA Output Drive**
  - **— UltraMOS® Advanced CMOS Technology**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Architecturally Similar to Standard GAL20V8**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— Battery Powered Systems**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

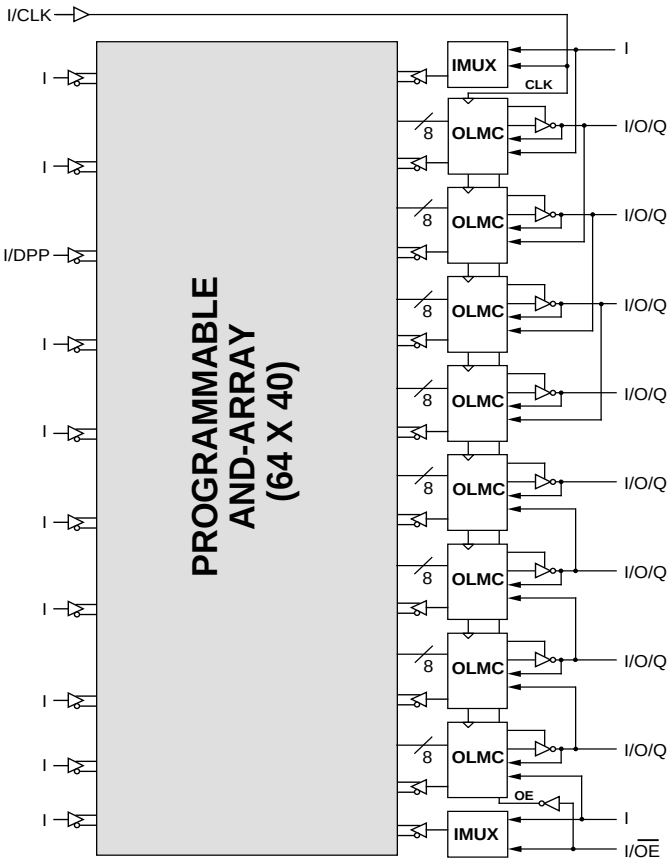
DESCRIPTION

The GAL20V8Z and GAL20V8ZD, at 100 μA standby current and 12ns propagation delay provides the highest speed and lowest power combination PLD available in the market. The GAL20V8Z/ZD is manufactured using Lattice Semiconductor's advanced zero power E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology.

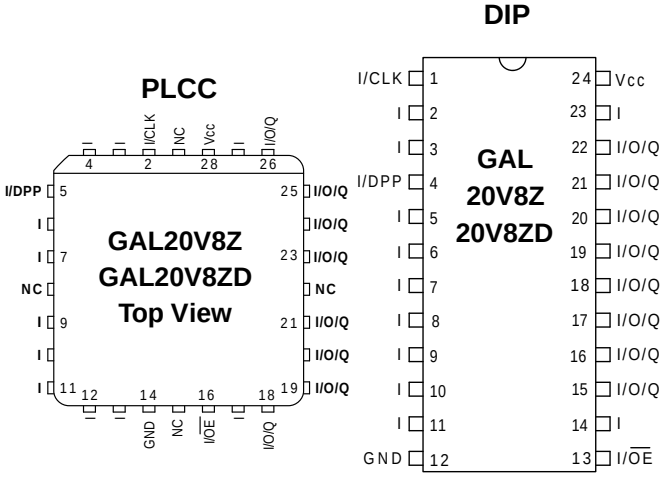
The GAL20V8Z uses Input Transition Detection (ITD) to put the device in standby mode and is capable of emulating the full functionality of the standard GAL20V8. The GAL20V8ZD utilizes a dedicated power-down pin (DPP) to put the device in standby mode. It has 19 inputs available to the AND array.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL 20V8Z/ZD ORDERING INFORMATION

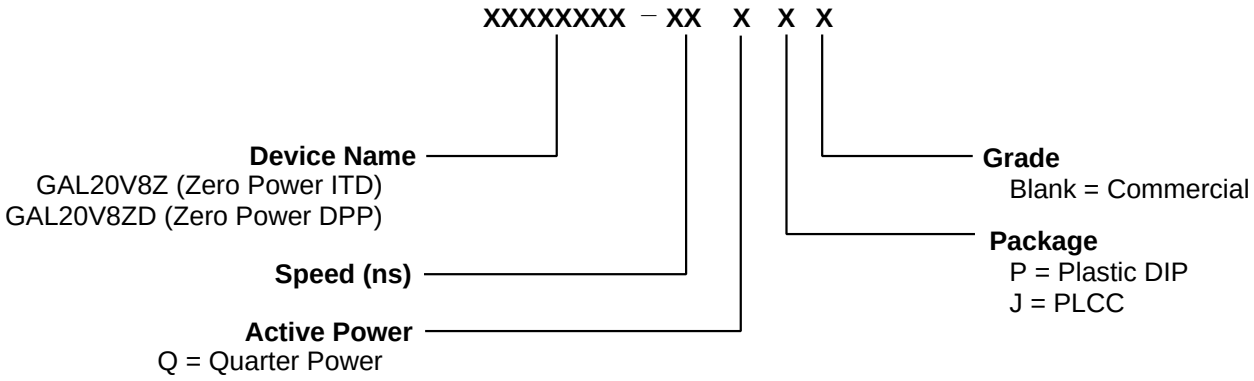
GAL20V8Z: Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	ISB (μA)	Ordering #	Package
12	10	8	55	100	GAL20V8Z-12QP	24-Pin Plastic DIP
			55	100	GAL20V8Z-12QJ	28-Lead PLCC
15	15	10	55	100	GAL20V8Z-15QP	24-Pin Plastic DIP
			55	100	GAL20V8Z-15QJ	28-Lead PLCC

GAL20V8ZD: Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	ISB (μA)	Ordering #	Package
12	10	8	55	100	GAL20V8ZD-12QP	24-Pin Plastic DIP
			55	100	GAL20V8ZD-12QJ	28-Lead PLCC
15	15	10	55	100	GAL20V8ZD-15QP	24-Pin Plastic DIP
			55	100	GAL20V8ZD-15QJ	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL20V8Z/ZD. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. Most compilers also have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1(2) and pin 13(16) are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1(2) and pin 13(16) become dedicated inputs and use the feedback paths of pin 22(26) and pin 15(18) respectively. Because of this feedback path usage, pin 22(26) and pin 15(18) do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 18(21) and 19(23)) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

When using the standard GAL20V8 JEDEC fuse pattern generated by the logic compilers for the GAL20V8ZD, special attention must be given to pin 4(5) (DPP) to make sure that it is not used as one of the functional inputs.

REGISTERED MODE

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

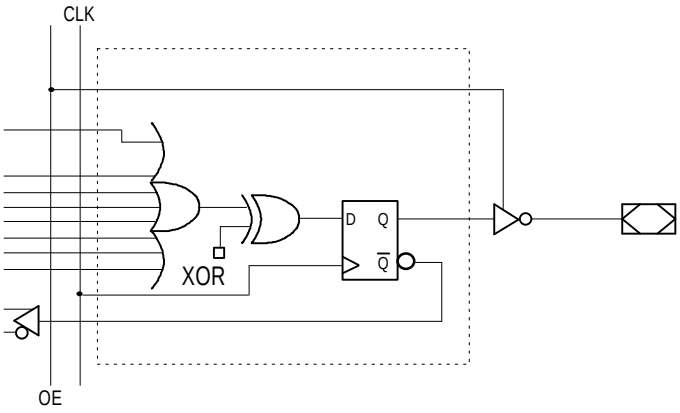
Architecture configurations available in this mode are similar to the common 20R8 and 20RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

Registered outputs have eight product terms per output. I/O's have seven product terms per output.

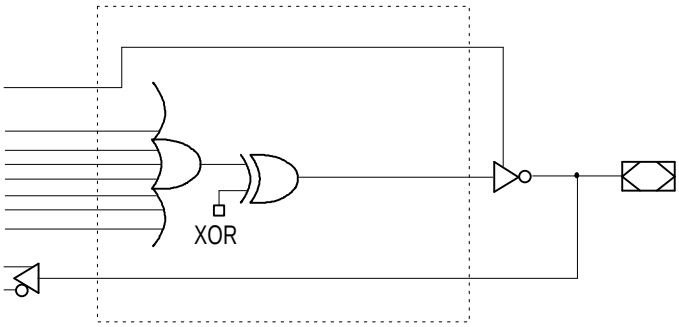
Pin 4(5) is used as dedicated power-down pin on GAL20V8ZD. It cannot be used as functional input.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1(2) controls common CLK for the registered outputs.
- Pin 13(16) controls common $\overline{OE}$ for the registered outputs.
- Pin 1(2) & Pin 13(16) are permanently configured as CLK & $\overline{OE}$.



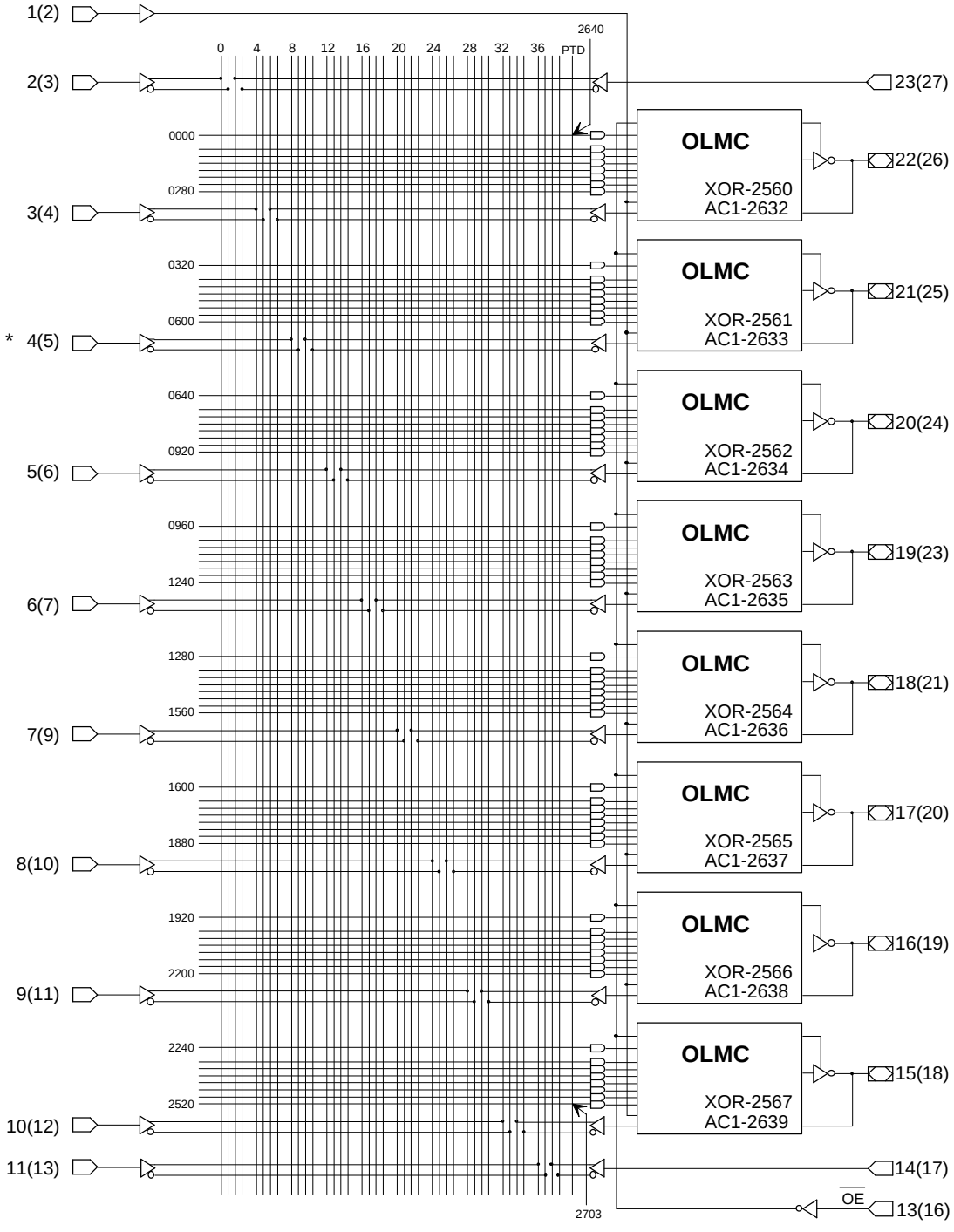
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1(2) & Pin 13(16) are permanently configured as CLK & $\overline{OE}$.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...			.... 2630, 2631
Byte7	Byte6	.... Byte1	Byte0

MSB LSB

SYN-2704
AC0-2705

* Note: Input not available on GAL20V8ZD

COMPLEX MODE

In the Complex mode, macrocells are configured as output only or I/O functions.

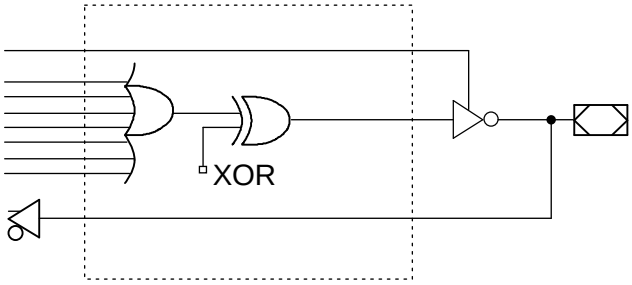
Architecture configurations available in this mode are similar to the common 20L8 and 20P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 15(18) & 22(26)) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1(2) and 13(16) are always available as data inputs into the AND array.

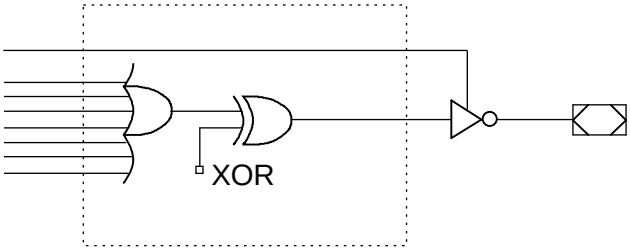
Pin 4(5) is used as dedicated power-down pin on GAL20V8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 16(19) through Pin 21(25) are configured to this function.



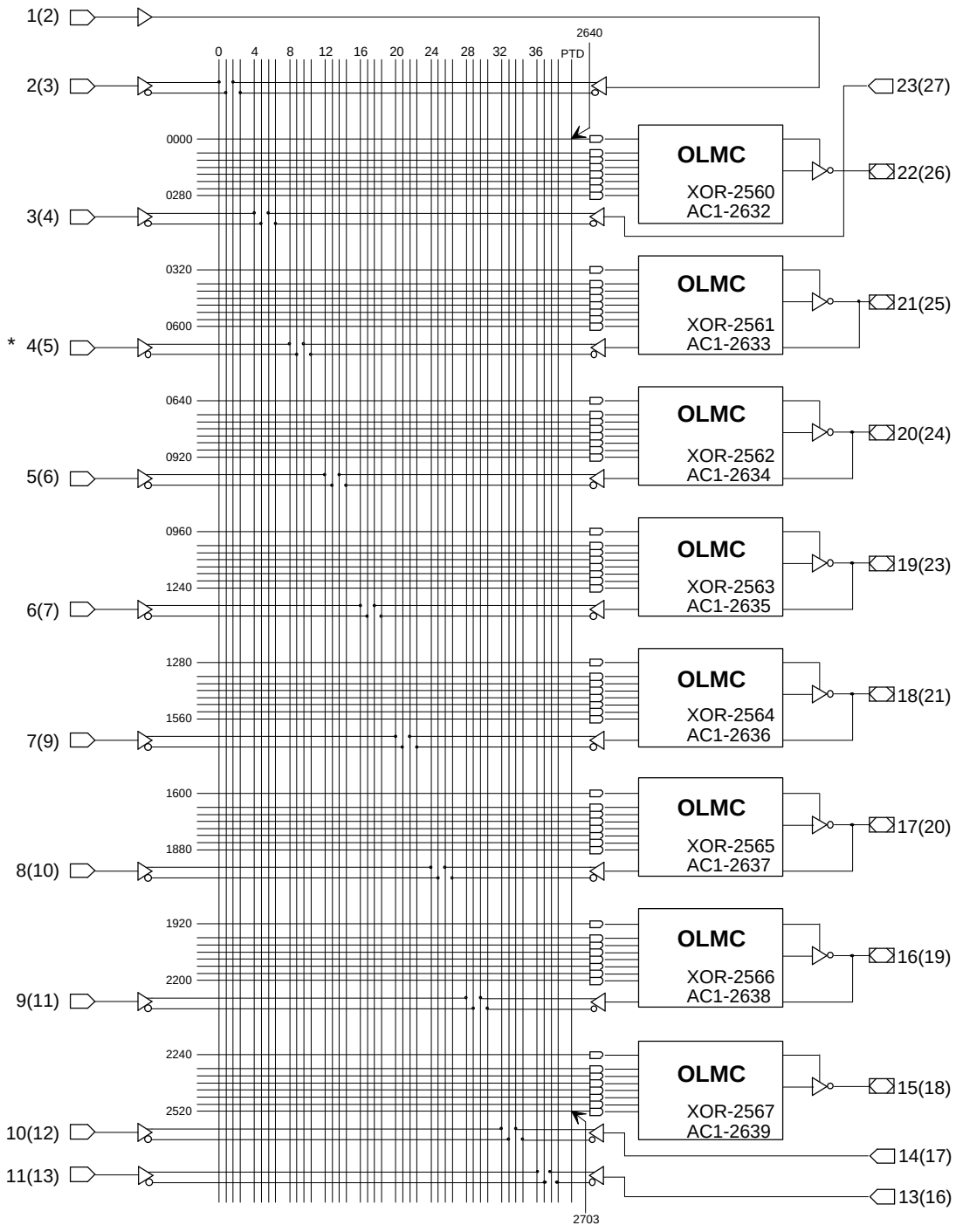
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 15(18) and Pin 22(26) are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...		.... 2630, 2631	
Byte7	Byte6	.... Byte1	Byte0

MSB LSB

SYN-2704
AC0-2705

* Note: Input not available on GAL20V8ZD

SIMPLE MODE

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

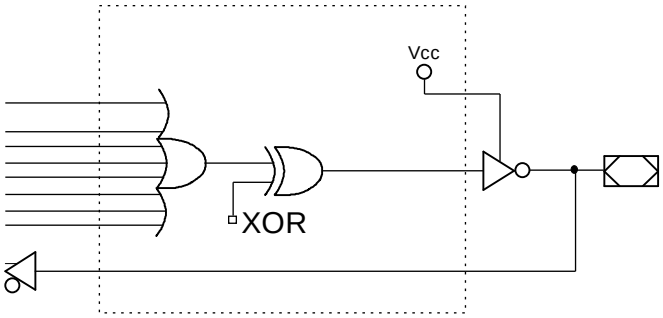
Architecture configurations available in this mode are similar to the common 14L8 and 16P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

Pins 1(2) and 13(16) are always available as data inputs into the AND array. The center two macrocells (pins 18(21) & 19(23)) cannot be used in the input configuration.

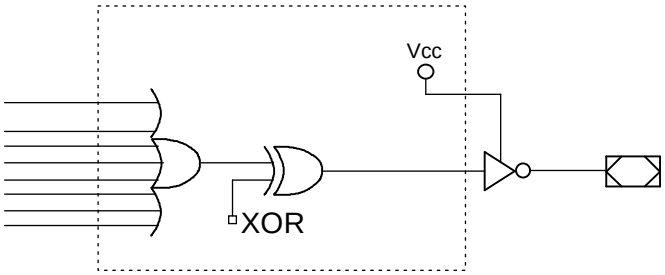
Pin 4(5) is used as dedicated power-down pin on GAL20V8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



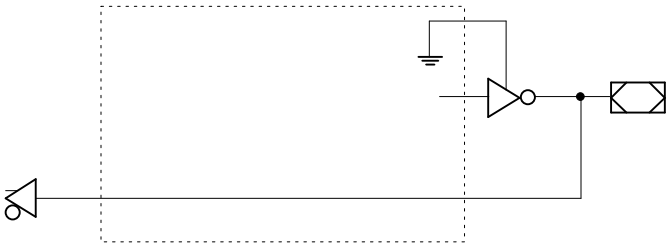
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 18(21) & 19(23) can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 18(21) & 19(23) are permanently configured to this function.



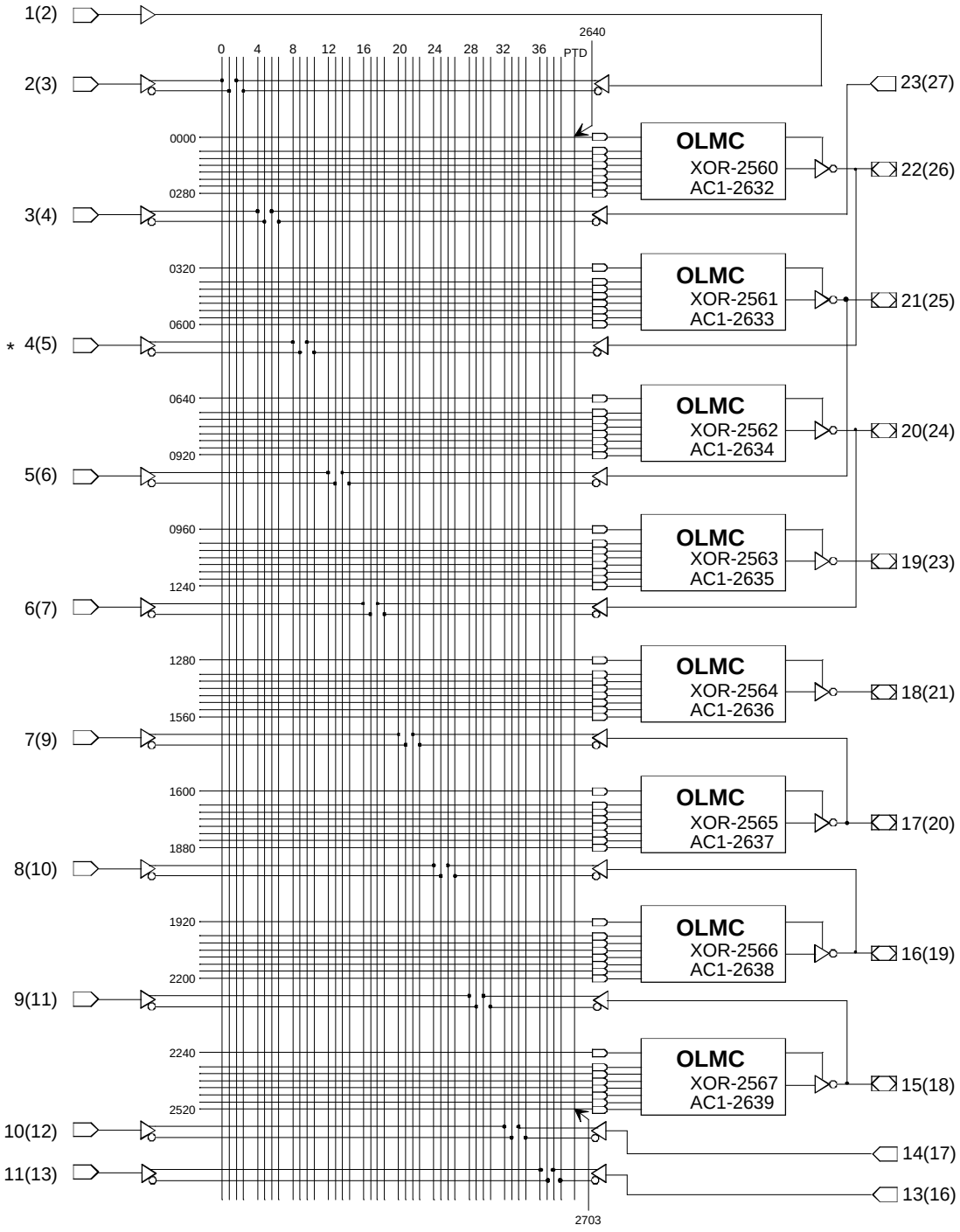
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 18(21) & 19(23) can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte7 | Byte6	.... Byte1 | Byte0

MSB — LSB

SYN-2704
AC0-2705

* Note: Input not available on GAL20V8ZD

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -100 µA Vin = V_{IL} or V_{IH}	Vcc-1	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA

COMMERCIAL

I_{SB}	Stand-by Power Supply Current	V_{IL} = GND V_{IH} = Vcc Outputs Open	Z-12/-15 ZD-12/-15	—	50	100	µA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15 MHz Outputs Open	Z-12/-15 ZD-12/-15	—	—	55	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

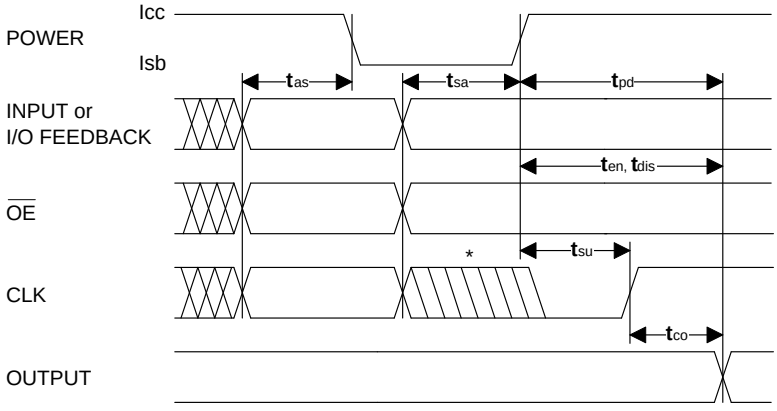
AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -12 MIN.	COM -12 MAX.	COM -15 MIN.	COM -15 MAX.	UNITS
tpd	A	Input or I/O to Combinational Output	3	12	3	15	ns
tco	A	Clock to Output Delay	2	8	2	10	ns
tcf[2]	—	Clock to Feedback Delay	—	6	—	7	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	15	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	55	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	62.5	—	45.5	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	MHz
twh	—	Clock Pulse Duration, High	6	—	8	—	ns
twl	—	Clock Pulse Duration, Low	6	—	8	—	ns
ten	B	Input or I/O to Output Enabled	—	12	—	15	ns
	B	$\overline{OE}$ to Output Enabled	—	12	—	15	ns
tdis	C	Input or I/O to Output Disabled	—	15	—	15	ns
	C	$\overline{OE}$ to Output Disabled	—	12	—	15	ns
tas	—	Last Active Input to Standby	60	140	50	150	ns
tsa[4]	—	Standby to Active Output	6	13	5	15	ns

1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Specification section.
3) Refer to fmax Specification section.
4) Add **t**sa to **t**pd, **t**su, **t**en and **t**dis when the device is coming out of standby state.

STANDBY POWER TIMING WAVEFORMS



* Note: Rising clock edges are allowed during **t**sa but outputs are not guaranteed.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -12		COM -15		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinational Output	3	12	3	15	ns
tco	A	Clock to Output Delay	2	8	2	10	ns
tcf[2]	—	Clock to Feedback Delay	—	6	—	7	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	15	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	55	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	62.5	—	45.5	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	MHz
twh	—	Clock Pulse Duration, High	6	—	8	—	ns
twl	—	Clock Pulse Duration, Low	6	—	8	—	ns
ten	B	Input or I/O to Output Enabled	—	12	—	15	ns
	B	$\overline{OE}$ to Output Enabled	—	12	—	15	ns
tdis	C	Input or I/O to Output Disabled	—	15	—	15	ns
	C	$\overline{OE}$ to Output Disabled	—	12	—	15	ns

1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Specification section.
3) Refer to fmax Specification section.

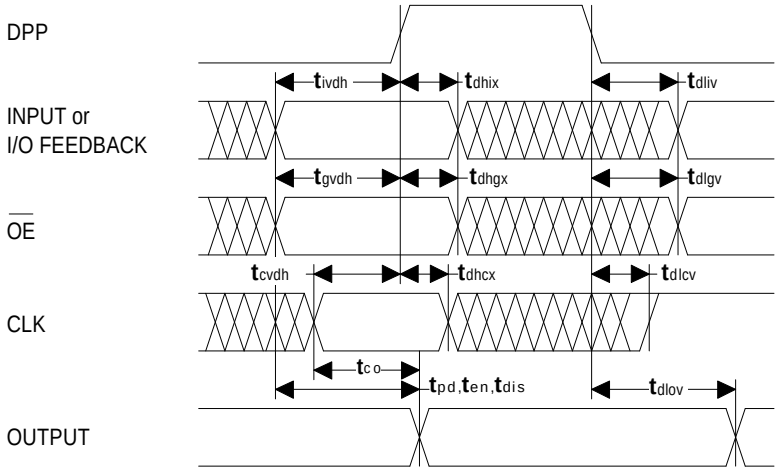
DEDICATED POWER-DOWN PIN SPECIFICATIONS

Over Recommended Operating Conditions

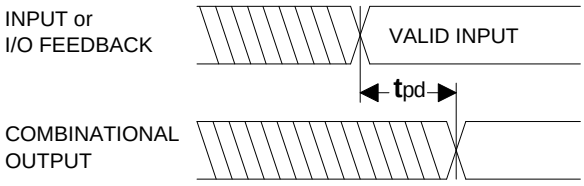
PARAMETER	TEST COND[1].	DESCRIPTION	COM -12		COM -15		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{whd}	—	DPP Pulse Duration High	12	—	15	—	ns
t_{wld}	—	DPP Pulse Duration Low	25	—	30	—	ns
ACTIVE TO STANDBY							
t_{ivdh}	—	Valid Input before DPP High	5	—	8	—	ns
t_{gvdh}	—	Valid OE before DPP High	0	—	0	—	ns
t_{cvdh}	—	Valid Clock Before DPP High	0	—	0	—	ns
t_{dhix}	—	Input Don't Care after DPP High	—	2	—	5	ns
t_{dhgx}	—	$\overline{OE}$ Don't Care after DPP High	—	6	—	9	ns
t_{dhcx}	—	Clock Don't Care after DPP High	—	8	—	11	ns
STANDBY TO ACTIVE							
t_{dliv}	—	DPP Low to Valid Input	12	—	15	—	ns
t_{dlgv}	—	DPP Low to Valid $\overline{OE}$	16	—	20	—	ns
t_{dlcv}	—	DPP Low to Valid Clock	18	—	20	—	ns
t_{dlov}	A	DPP Low to Valid Output	5	24	5	30	ns

1) Refer to Switching Test Conditions section.

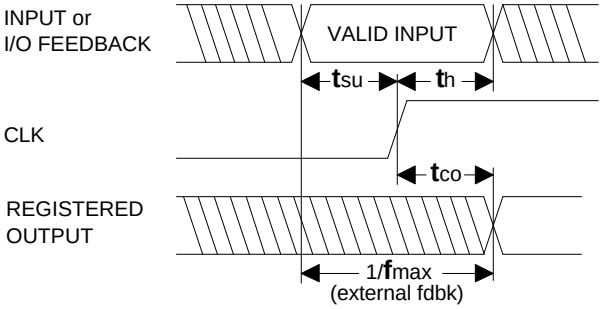
DEDICATED POWER-DOWN PIN (DPP) TIMING WAVEFORMS



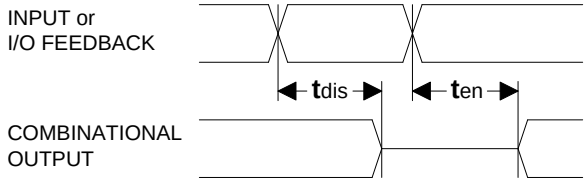
SWITCHING WAVEFORMS



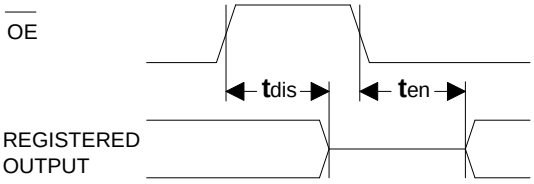
Combinatorial Output



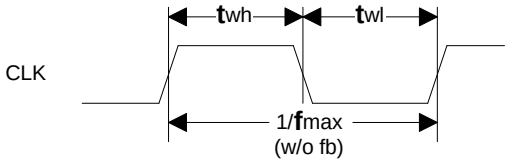
Registered Output



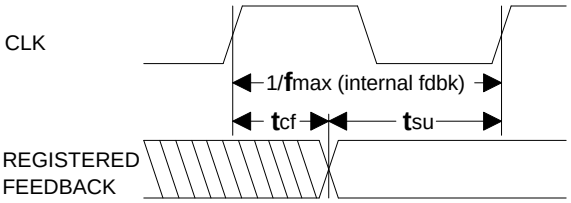
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

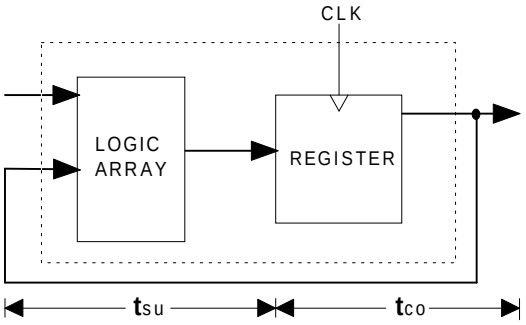


Clock Width



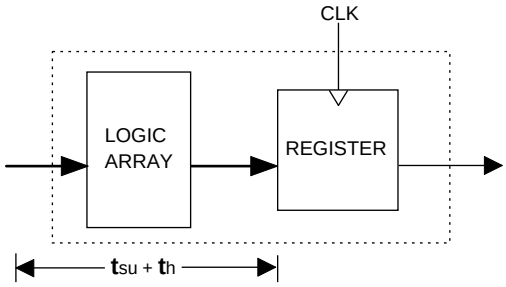
f_{max} with Feedback

fmax SPECIFICATIONS



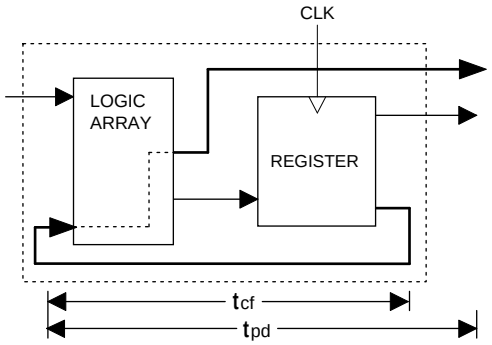
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

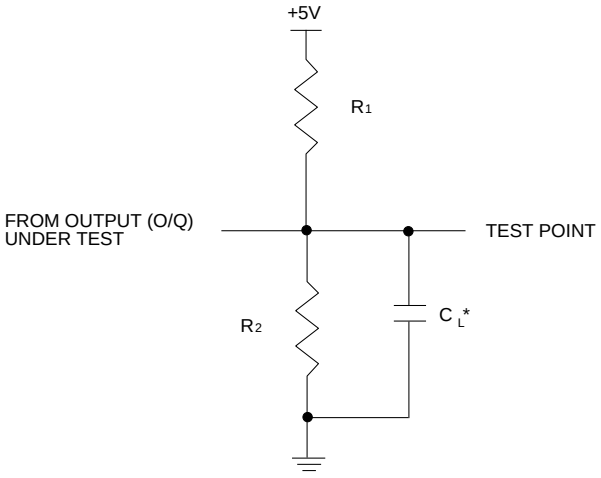
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL20V8Z/ZD device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter checksum.

SECURITY CELL

A security cell is provided in the GAL20V8Z/ZD devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The electronic signature data is always available to the user, regardless of the state of this security cell.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the GAL Development Tools Section of the Data Book). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle

INPUT TRANSITION DETECTION (ITD)

The GAL20V8Z relies on its internal input detection circuitry to put the device in power down mode. If there is no input transition for the specified period of time, the device will go into the power down state. Any valid input transition will put the device back into active state. The first rising clock transition from power-down state only acts as a wake up signal into the device and will not clock the data input through to the output (refer to standby power timing waveform for more detail). Any input pulse widths greater than 5ns at input voltage level of 1.5V will be detected as input transition. The device will not detect any input pulse widths less than 1ns measured at input voltage level of 1.5V as input transition.

DEDICATED POWER-DOWN PIN (DPP)

The GAL20V8ZD uses pin 4 (pin 5 on PLCC) as the dedicated power-down signal to put the device in power-down state. DPP is an active high signal where logic high driven on this signal puts the device into power-down state. Input pin 4 (5) cannot be used as a functional input on this device.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

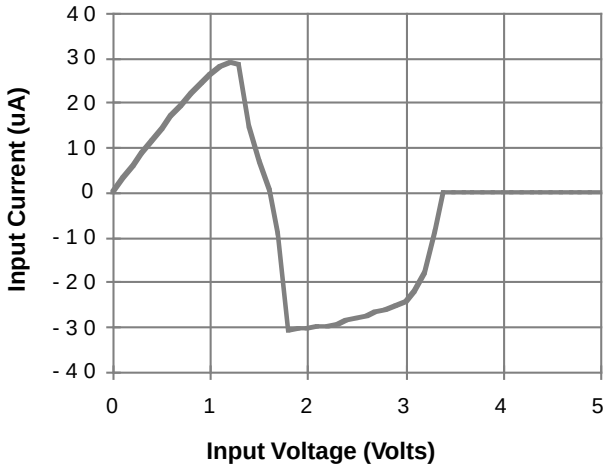
The GAL20V8Z/ZD devices includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

INPUT BUFFERS

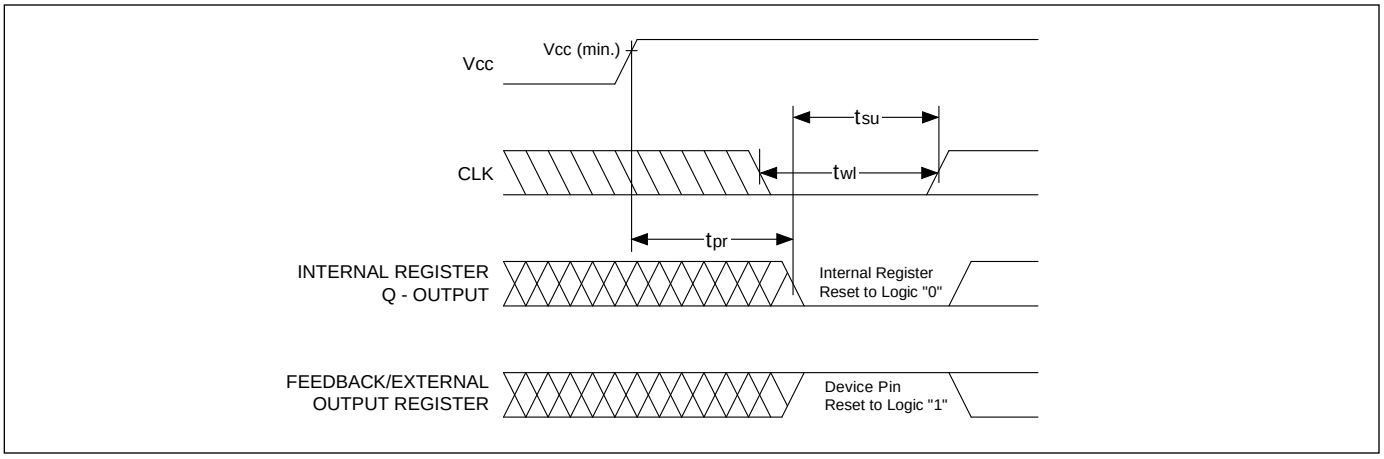
GAL20V8Z/ZD devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL20V8Z/ZD input buffers have latches within the buffers. As a result, when the device goes into standby mode the inputs will be latched to its values prior to standby. In order to overcome the input latches, they will have to be driven by an external source. Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Characteristic

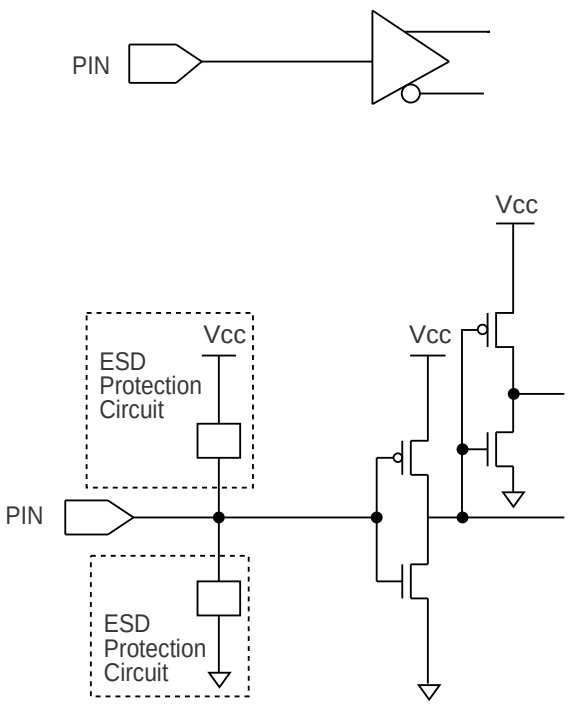


POWER-UP RESET

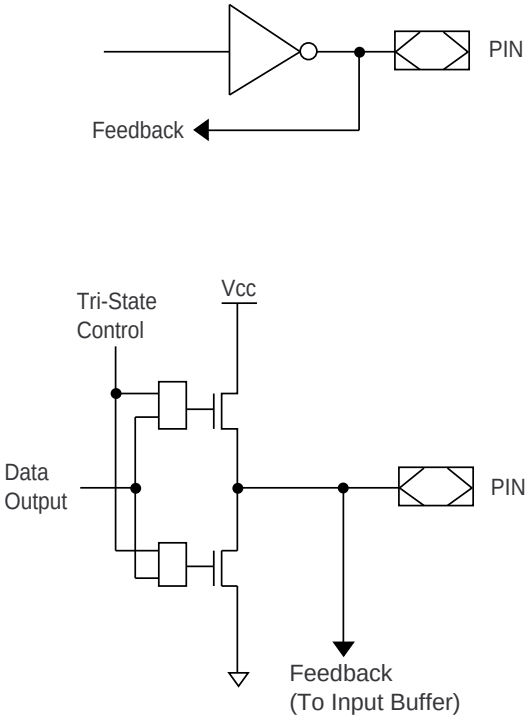


Circuitry within the GAL20V8Z/ZD provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20V8Z/ZD. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



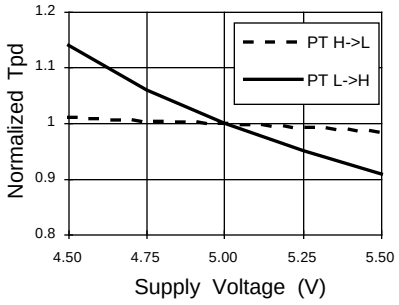
Typical Input



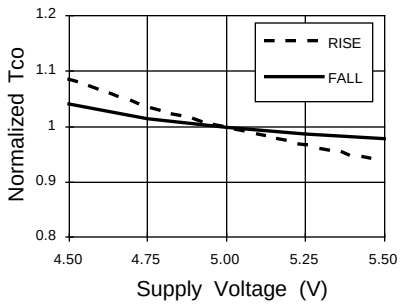
Typical Output

TYPICAL AC AND DC CHARACTERISTICS

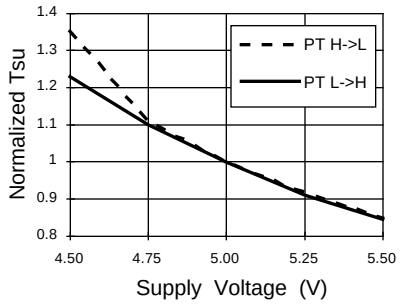
Normalized Tpd vs Vcc



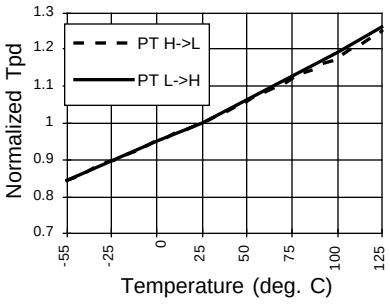
Normalized Tco vs Vcc



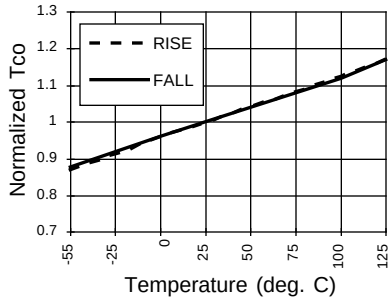
Normalized Tsu vs Vcc



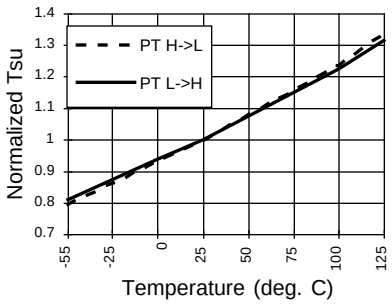
Normalized Tpd vs Temp



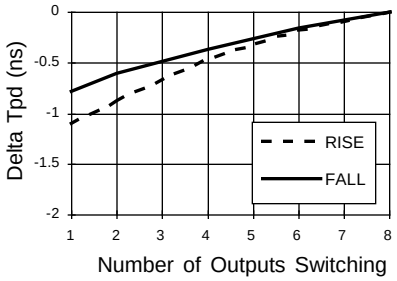
Normalized Tco vs Temp



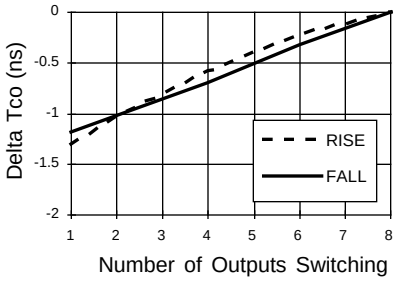
Normalized Tsu vs Temp



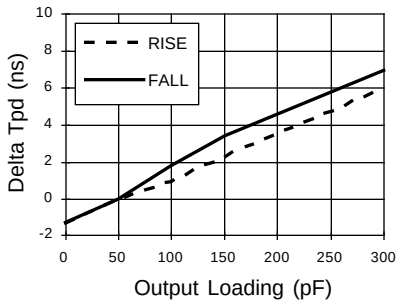
Delta Tpd vs # of Outputs Switching



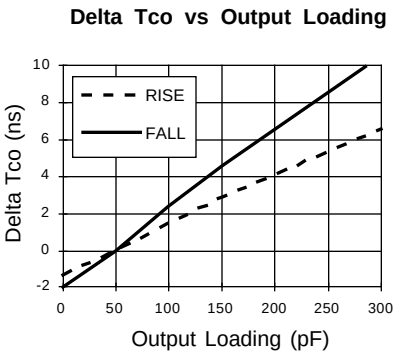
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

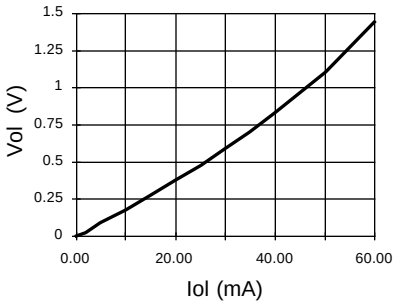


Delta Tco vs Output Loading

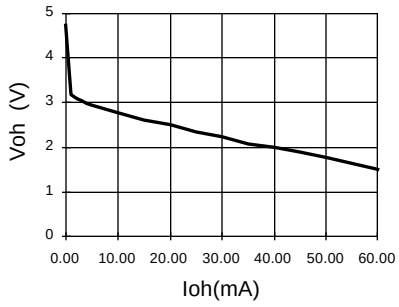


TYPICAL AC AND DC CHARACTERISTICS

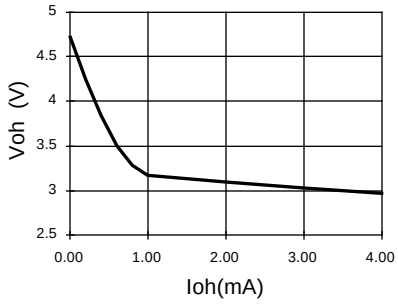
Vol vs Iol



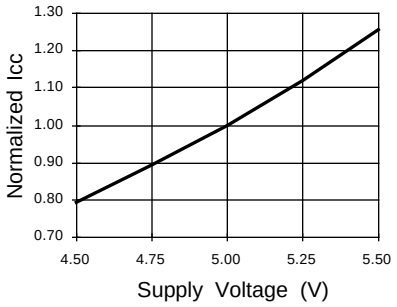
Voh vs Ioh



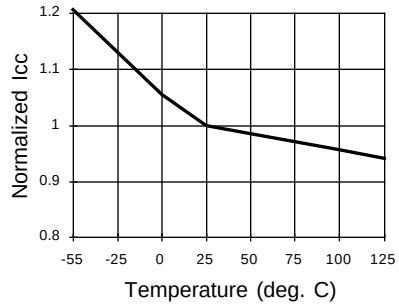
Voh vs Ioh



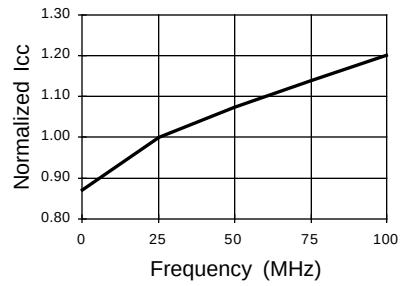
Normalized Icc vs Vcc



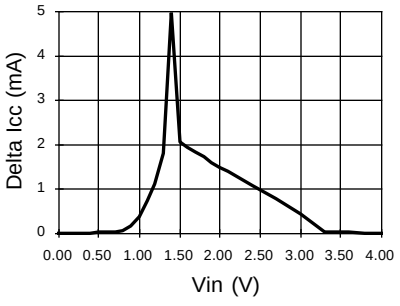
Normalized Icc vs Temp



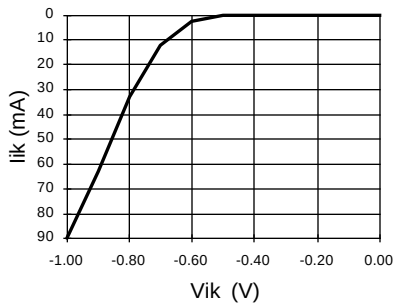
Normalized Icc vs Freq. (DPP & ITD > 10MHz)



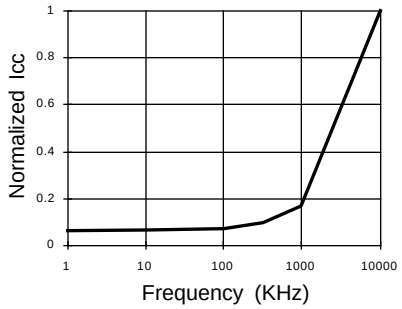
Delta Icc vs Vin (1 input)



Input Clamp (Vik)



Normalized Icc vs Freq. (ITD)



GAL20V8

High Performance E²CMOS PLD
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 5 ns Maximum Propagation Delay**
  - **— Fmax = 166 MHz**
  - **— 4 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - **— 75mA Typ Icc on Low Power Device**
  - **— 45mA Typ Icc on Quarter Power Device**
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Also Emulates 24-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

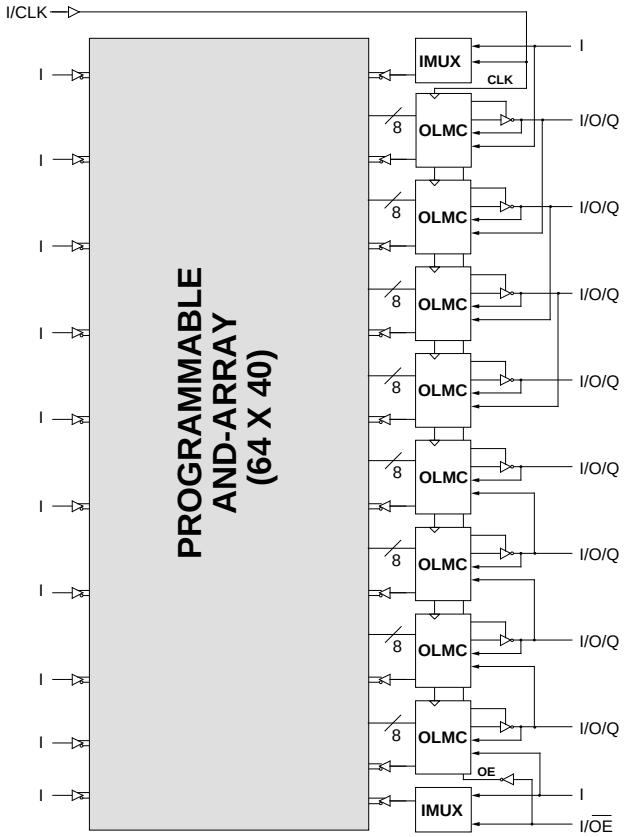
DESCRIPTION

The GAL20V8C, at 5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

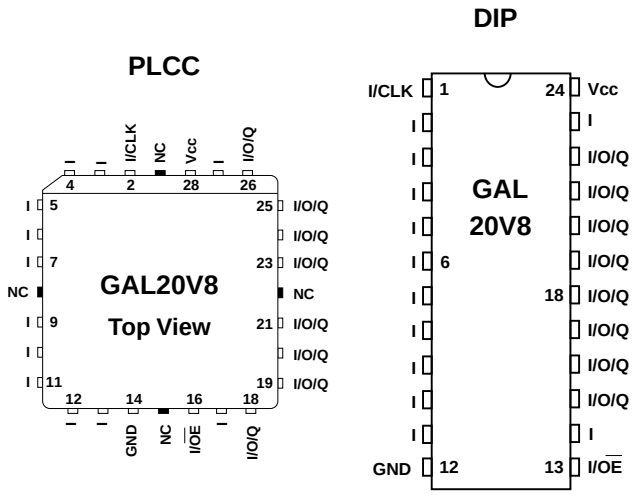
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL20V8 are the PAL architectures listed in the table of the macrocell description section. GAL20V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL20V8 ORDERING INFORMATION

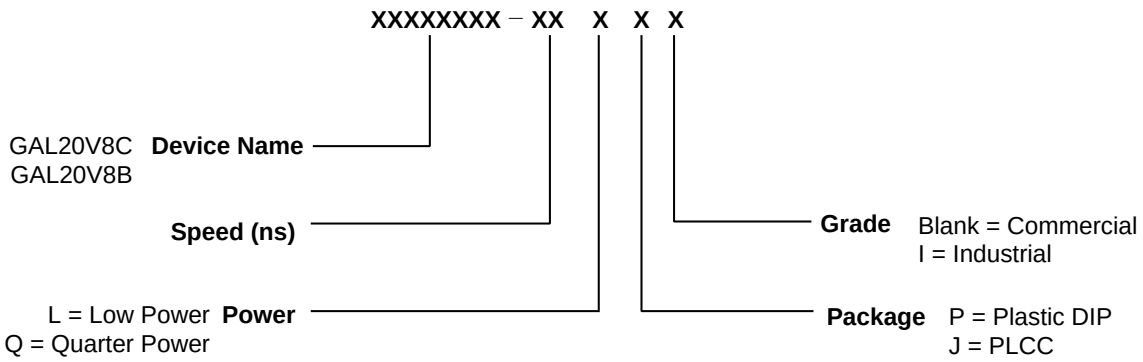
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
5	3	4	115	GAL20V8C-5LJ	28-Lead PLCC
7.5	7	5	115	GAL20V8C-7LJ	28-Lead PLCC
			115	GAL20V8B-7LP	24-Pin Plastic DIP
			115	GAL20V8B-7LJ	28-Lead PLCC
10	10	7	115	GAL20V8C-10LJ	28-Lead PLCC
			115	GAL20V8B-10LP	24-Pin Plastic DIP
			115	GAL20V8B-10LJ	28-Lead PLCC
15	12	10	55	GAL20V8B-15QP	24-Pin Plastic DIP
			55	GAL20V8B-15QJ	28-Lead PLCC
			90	GAL20V8B-15LP	24-Pin Plastic DIP
			90	GAL20V8B-15LJ	28-Lead PLCC
25	15	12	55	GAL20V8B-25QP	24-Pin Plastic DIP
			55	GAL20V8B-25QJ	28-Lead PLCC
			90	GAL20V8B-25LP	24-Pin Plastic DIP
			90	GAL20V8B-25LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	10	7	130	GAL20V8C-10LJI	28-Lead PLCC
			130	GAL20V8B-10LPI	24-Pin Plastic DIP
			130	GAL20V8B-10LJI	28-Lead PLCC
15	12	10	130	GAL20V8B-15LPI	24-Pin Plastic DIP
			130	GAL20V8B-15LJI	28-Lead PLCC
20	13	11	65	GAL20V8B-20QPI	24-Pin Plastic DIP
			65	GAL20V8B-20QJI	28-Lead PLCC
25	15	12	65	GAL20V8B-25QPI	24-Pin Plastic DIP
			65	GAL20V8B-25QJI	28-Lead PLCC
			130	GAL20V8B-25LPI	24-Pin Plastic DIP
			130	GAL20V8B-25LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL20V8 . The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL20V8 can emulate. It also shows the OLMC mode under which the devices emulate the PAL architecture.

PAL Architectures Emulated by GAL20V8	GAL20V8 Global OLMC Mode
20R8	**Registered**
20R6	**Registered**
20R4	**Registered**
20RP8	**Registered**
20RP6	**Registered**
20RP4	**Registered**
20L8	**Complex**
20H8	**Complex**
20P8	**Complex**
14L8	**Simple**
16L6	**Simple**
18L4	**Simple**
20L2	**Simple**
14H8	**Simple**
16H6	**Simple**
18H4	**Simple**
20H2	**Simple**
14P8	**Simple**
16P6	**Simple**
18P4	**Simple**
20P2	**Simple**

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 13 (DIP pinout) are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 13 become dedicated inputs and use the feedback paths of pin 22 and pin 15 respectively. Because of this feedback path usage, pin 22 and pin 15 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 18 and 19) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOG/iC	GAL20V8_R	GAL20V8_C7	GAL20V8_C8	GAL20V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL20V8A
PLDesigner	P20V8R[2]	P20V8C[2]	P20V8C[2]	P20V8A
TANGO-PLD	G20V8R	G20V8C	G20V8AS[3]	G20V8

1) Used with **Configuration** keyword.
2) Prior to Version 2.0 support.
3) Supported on Version 1.20 or later.

REGISTERED MODE

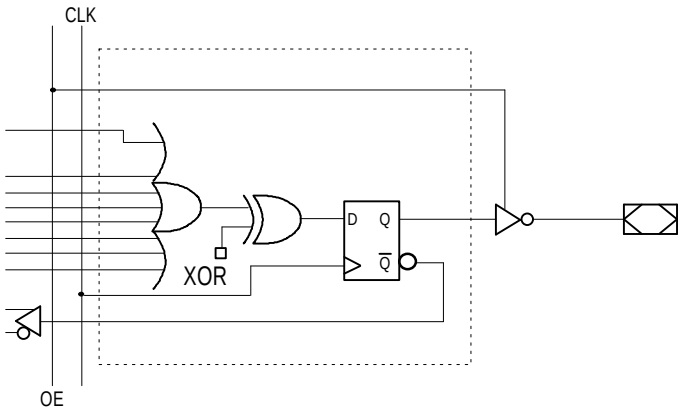
In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 20R8 and 20RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

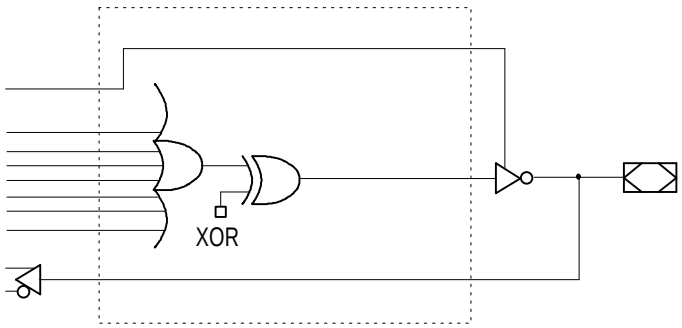
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 13 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 13 are permanently configured as CLK & $\overline{OE}$.



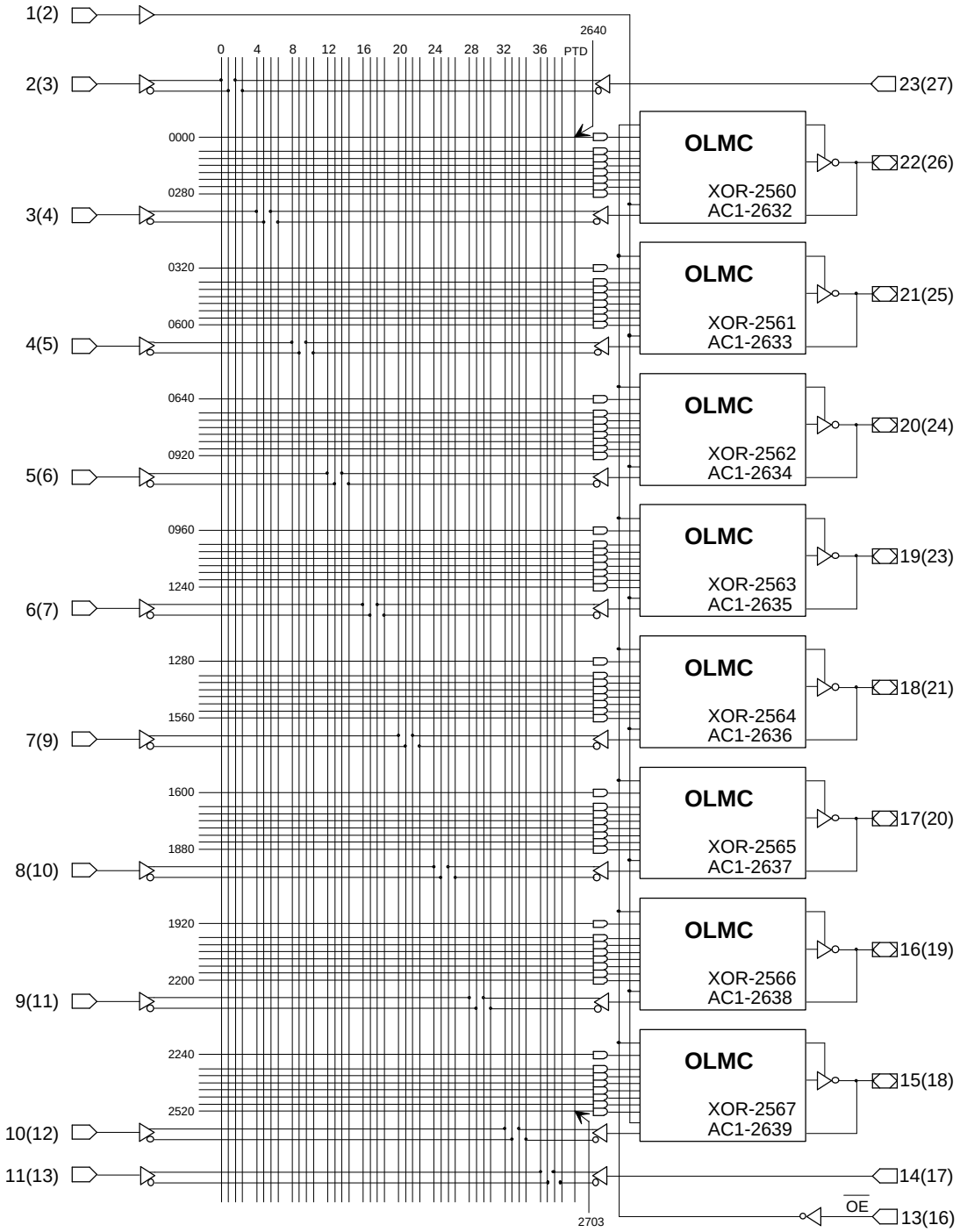
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 13 are permanently configured as CLK & $\overline{OE}$.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte 7 | Byte 6	.... Byte 1 | Byte 0

MSB LSB

SYN-2704
AC0-2705

COMPLEX MODE

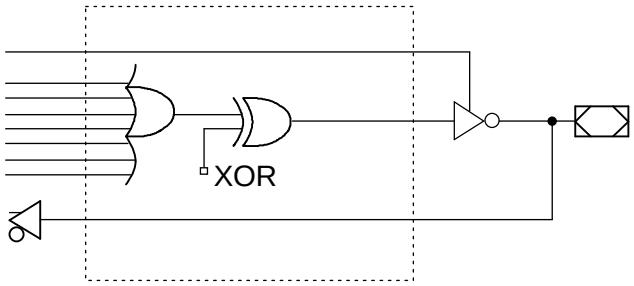
In the Complex mode, macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 20L8 and 20P8 devices with programmable polarity in each macrocell.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 15 & 22) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

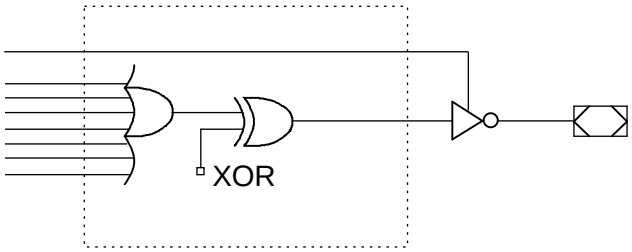
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 13 are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 16 through Pin 21 are configured to this function.



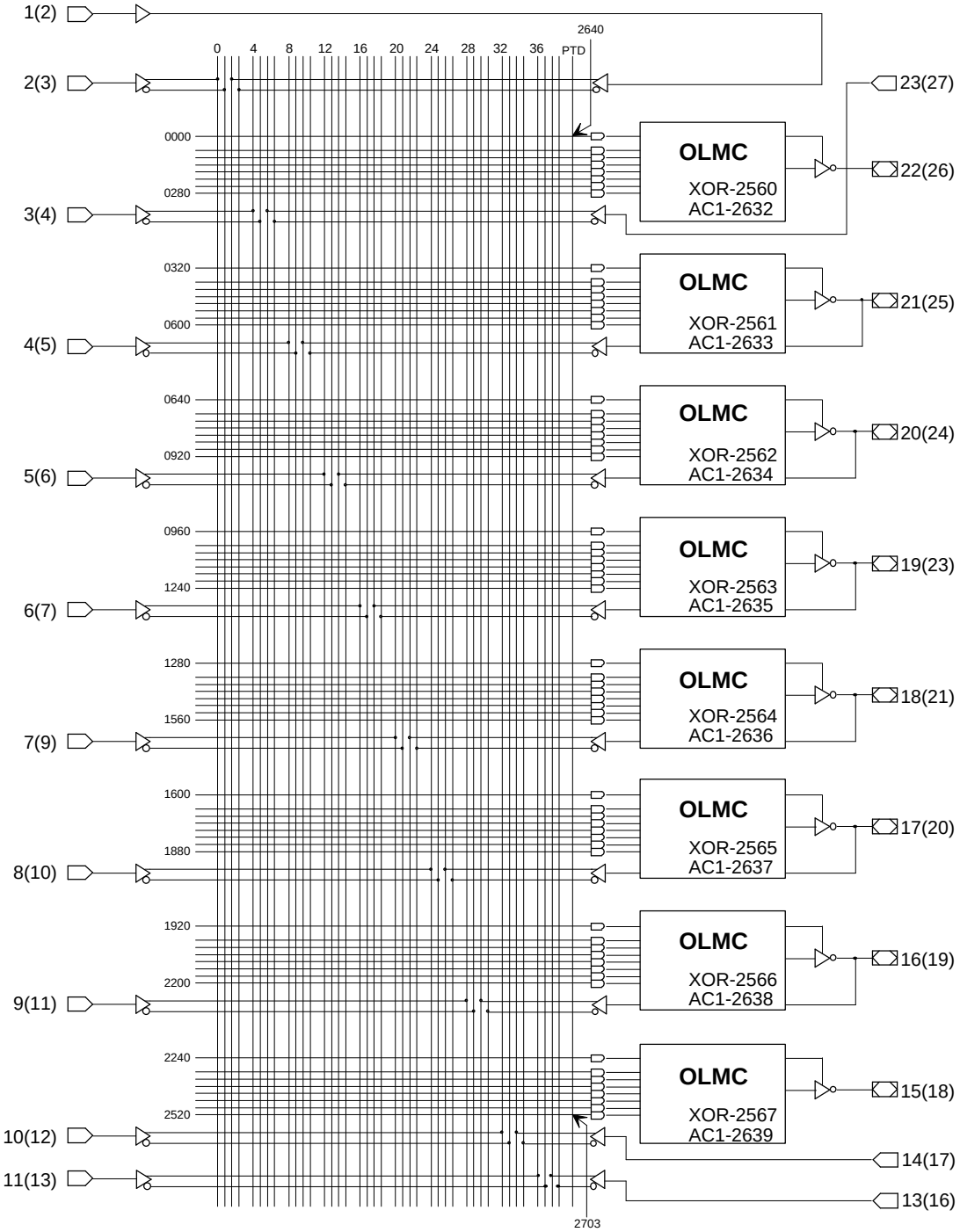
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1.
- Pin 15 and Pin 22 are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte 7 | Byte 6	.... Byte 1 | Byte 0

MSB LSB

SYN-2704
AC0-2705

SIMPLE MODE

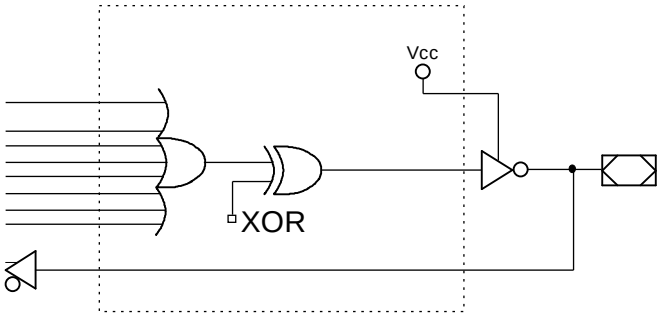
In the Simple mode, pins are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 14L8 and 16P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

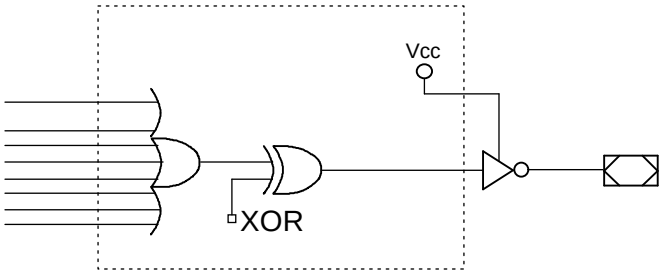
Pins 1 and 13 are always available as data inputs into the AND array. The "center" two macrocells (pins 18 & 19) cannot be used in the input configuration.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



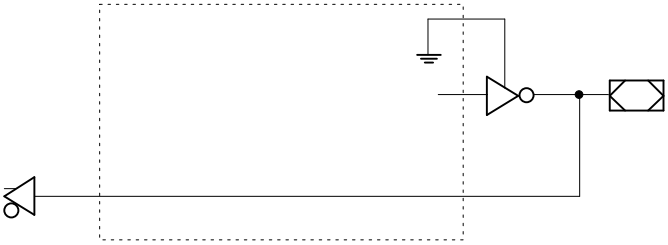
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 18 & 19 can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 18 & 19 are permanently configured to this function.



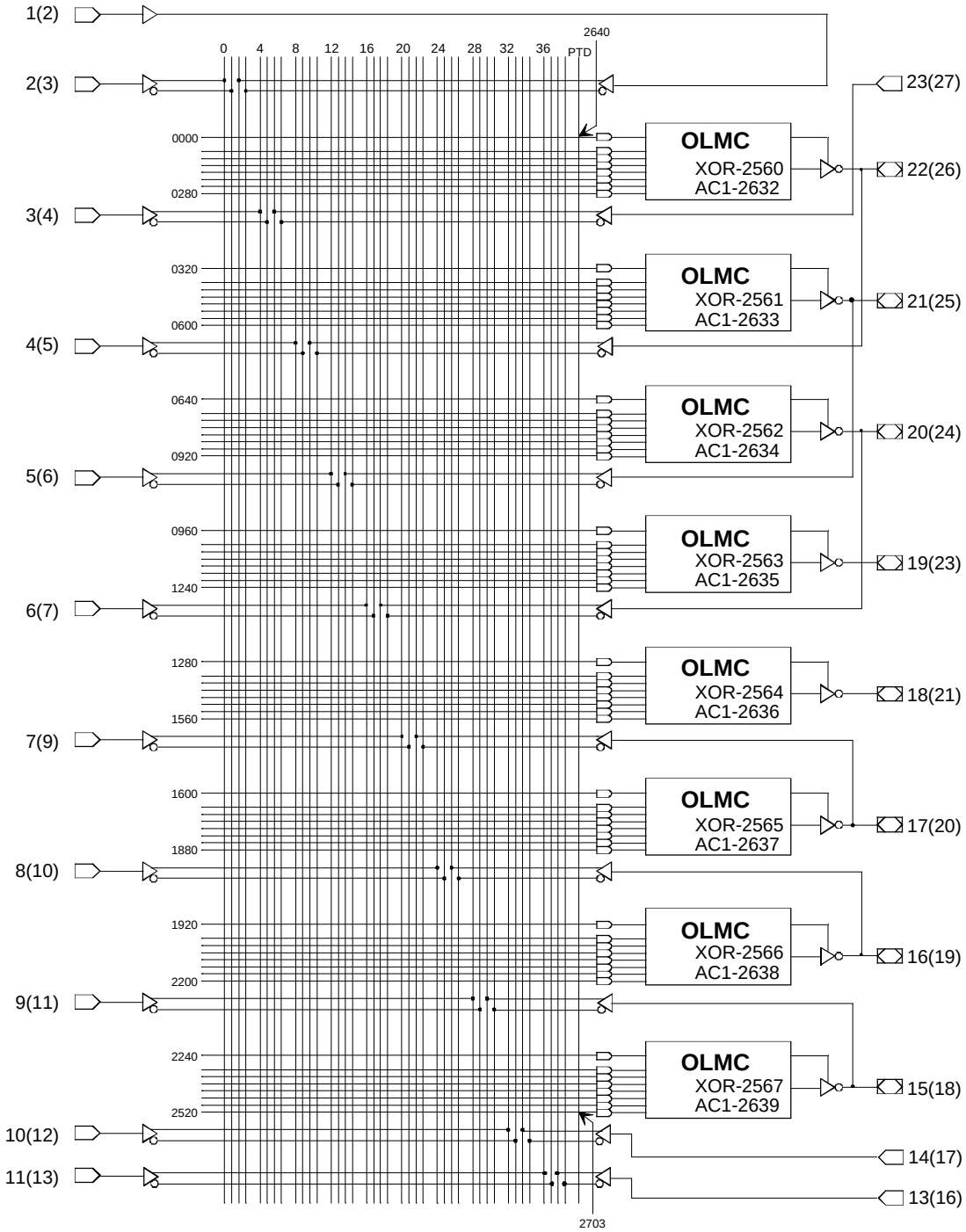
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 18 & 19 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...			.... 2630, 2631
Byte 7	Byte 6	.... Byte 1	Byte 0

MSB LSB

SYN-2704
AC0-2705

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... –40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -5/-7/-10	—	75	115	mA

INDUSTRIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L-10	—	75	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION		COM -5 MIN.	COM -5 MAX.	COM -7 MIN.	COM -7 MAX.	COM/IND -10 MIN.	COM/IND -10 MAX.	UNITS
tpd	A	Input or I/O to Comb. Output	8 outputs switching	1	5	3	7.5	3	10	ns
			1 output switching	—	—	—	7	—	—	ns
tco	A	Clock to Output Delay		1	4	2	5	2	7	ns
tcf[2]	—	Clock to Feedback Delay		—	3	—	3	—	6	ns
tsu	—	Setup Time, Input or Feedback before Clock↑		3	—	7	—	10	—	ns
th	—	Hold Time, Input or Feedback after Clock↑		0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)		142.8	—	83.3	—	58.8	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)		166	—	100	—	62.5	—	MHz
	A	Maximum Clock Frequency with No Feedback		166	—	100	—	62.5	—	MHz
twh	—	Clock Pulse Duration, High		3	—	5	—	8	—	ns
twl	—	Clock Pulse Duration, Low		3	—	5	—	8	—	ns
ten	B	Input or I/O to Output Enabled		1	6	3	9	3	10	ns
	B	$\overline{OE}$ to Output Enabled		1	6	2	6	2	10	ns
tdis	C	Input or I/O to Output Disabled		1	5	2	9	2	10	ns
	C	$\overline{OE}$ to Output Disabled		1	5	1.5	6	1.5	10	ns

1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Descriptions section.
3) Refer to fmax Descriptions section. Characterized initially and after any design or process changes that may affect these parameters.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... –40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	24	mA
I_{OH}	High Level Output Current			—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C		–30	—	–150	mA
COMMERCIAL							
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	**L** -7/-10	—	75	115	mA
			L -15/-25	—	75	90	mA
			Q -15/-25	—	45	55	mA
INDUSTRIAL							
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	**L** -10/-15/-25	—	75	130	mA
			Q -20/-25	—	45	65	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM.	TEST COND[1].	DESCRIPTION		COM -7 MIN.	COM -7 MAX.	COM / IND -10 MIN.	COM / IND -10 MAX.	COM / IND -15 MIN.	COM / IND -15 MAX.	IND -20 MIN.	IND -20 MAX.	COM / IND -25 MIN.	COM / IND -25 MAX.	UNITS
tpd	A	Input or I/O to	8 outputs switching	3	7.5	3	10	3	15	3	20	3	25	ns
		Comb. Output	1 output switching	—	7	—	—	—	—	—	—	—	—	ns
tco	A	Clock to Output Delay		2	5	2	7	2	10	2	11	2	12	ns
tcf[2]	—	Clock to Feedback Delay		—	3	—	6	—	8	—	9	—	10	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑		7	—	10	—	12	—	13	—	15	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑		0	—	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)		83.3	—	58.8	—	45.5	—	41.6	—	37	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)		100	—	62.5	—	50	—	45.4	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback		100	—	62.5	—	62.5	—	50	—	41.7	—	MHz
twh	—	Clock Pulse Duration, High		5	—	8	—	8	—	10	—	12	—	ns
twl	—	Clock Pulse Duration, Low		5	—	8	—	8	—	10	—	12	—	ns
ten	B	Input or I/O to Output Enabled		3	9	3	10	—	15	—	20	—	25	ns
	B	$\overline{OE}$ to Output Enabled		2	6	2	10	—	15	—	18	—	20	ns
tdis	C	Input or I/O to Output Disabled		2	9	2	10	—	15	—	20	—	25	ns
	C	$\overline{OE}$ to Output Disabled		1.5	6	1.5	10	—	15	—	18	—	20	ns

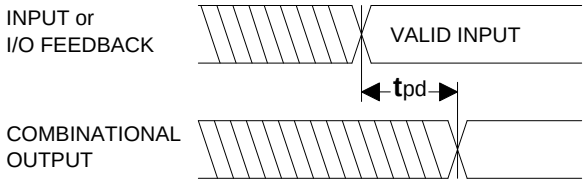
1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Descriptions section.
3) Refer to fmax Descriptions section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

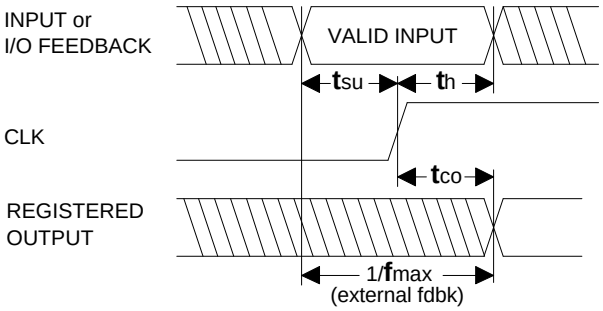
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

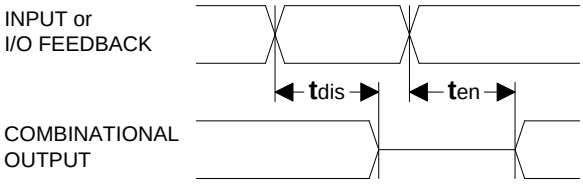
SWITCHING WAVEFORMS



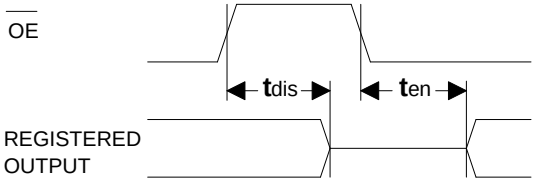
Combinatorial Output



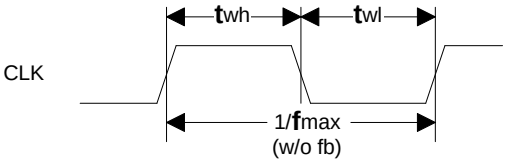
Registered Output



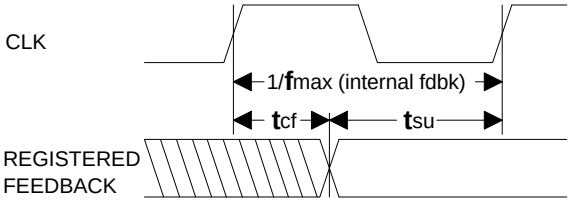
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

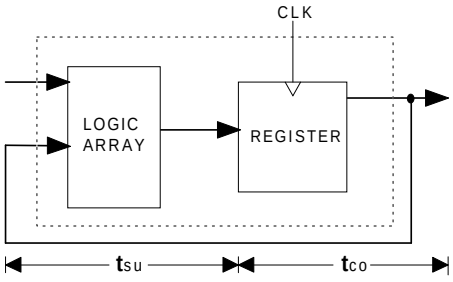


Clock Width



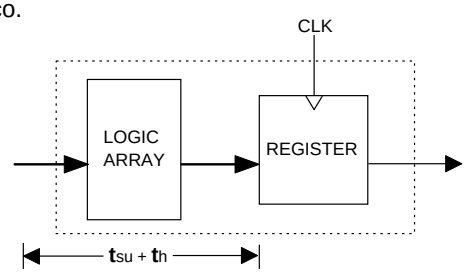
fmax with Feedback

fmax DESCRIPTIONS



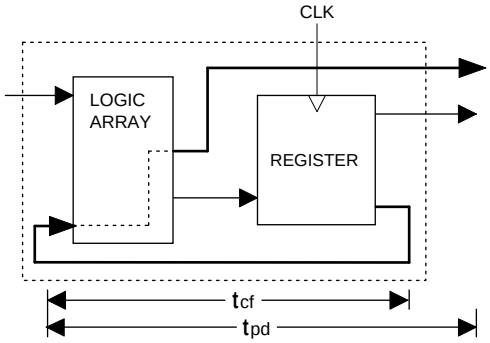
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



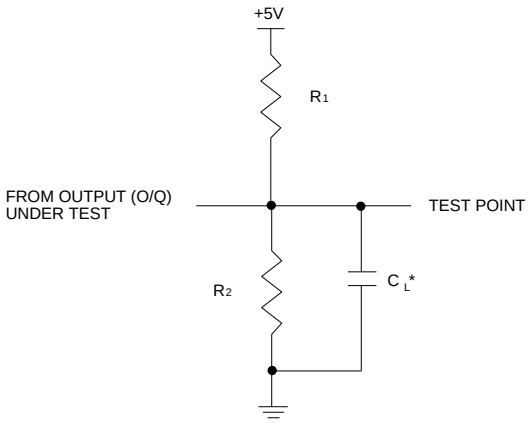
fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

SWITCHING TEST CONDITIONS

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	GAL20V8B	2 – 3ns 10% – 90%
	GAL20V8C	1.5ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See Figure

3-state levels are measured 0.5V from steady-state active level.



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL20V8B Output Load Conditions (see figure)

Test Condition		R1	R2	CL
A		200Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF

GAL20V8C Output Load Conditions (see figure)

Test Condition		R1	R2	CL
A		200Ω	200Ω	50pF
B	Active High	∞	200Ω	50pF
	Active Low	200Ω	200Ω	50pF
C	Active High	∞	200Ω	5pF
	Active Low	200Ω	200Ω	5pF

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL20V8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

SECURITY CELL

A security cell is provided in the GAL20V8 devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL20V8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias minimizes the potential of latch-up caused by negative input undershoots. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups in order to eliminate latch-up due to output overshoots.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

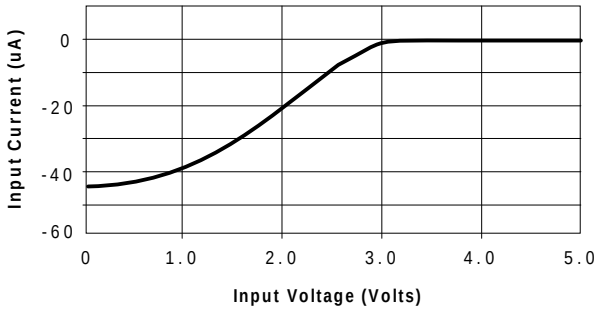
GAL20V8 devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

INPUT BUFFERS

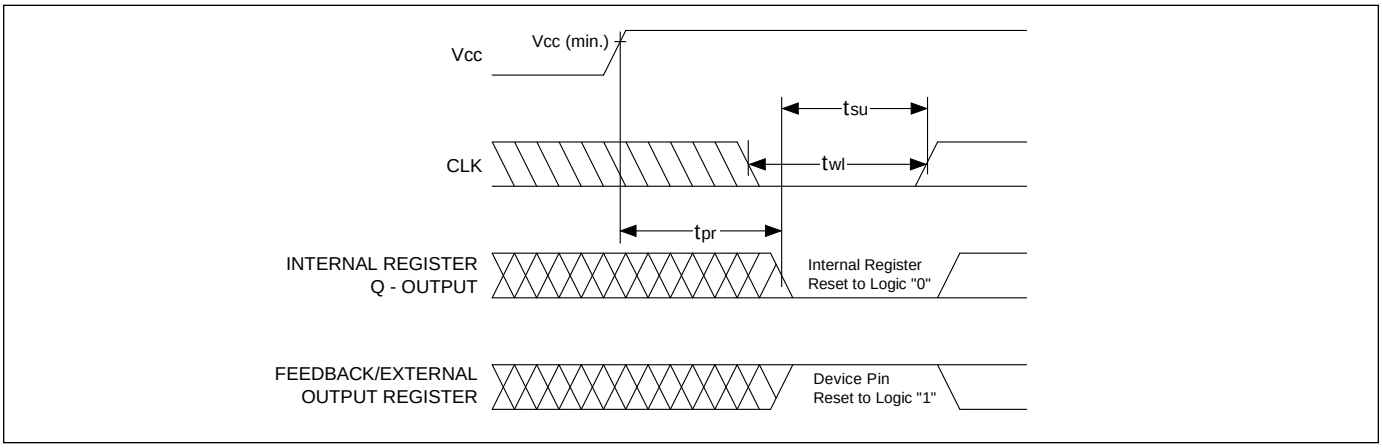
GAL20V8 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL20V8 input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or Ground. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Pull-up Characteristic

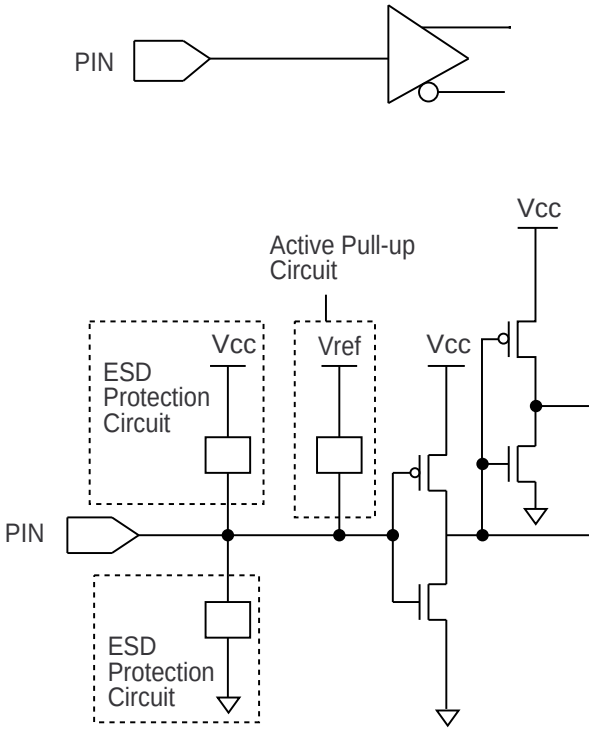


POWER-UP RESET



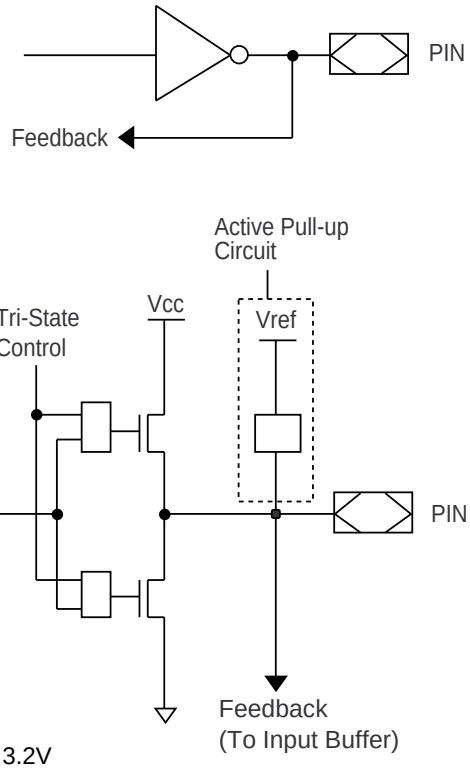
Circuitry within the GAL20V8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr}, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the device. First, the V_{CC} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typ. Vref = 3.2V

Typical Input

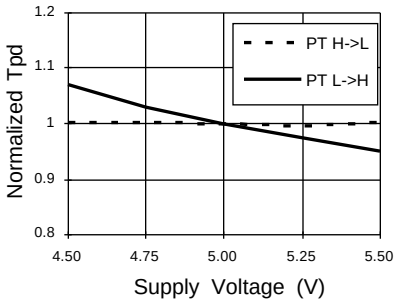


Typ. Vref = 3.2V

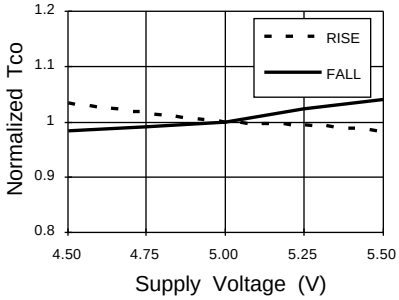
Typical Output

GAL 20V8C: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

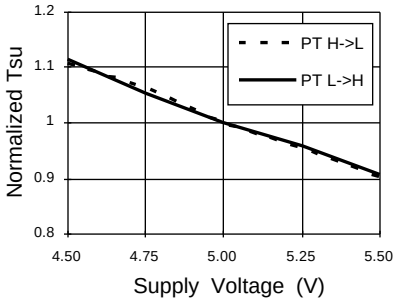
Normalized Tpd vs Vcc



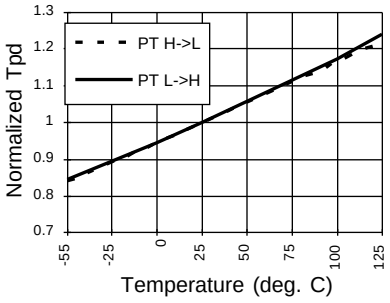
Normalized Tco vs Vcc



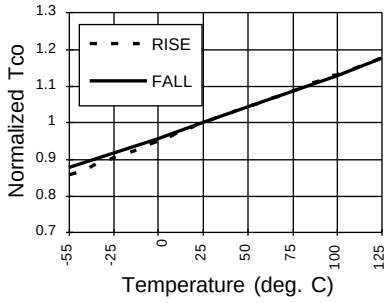
Normalized Tsu vs Vcc



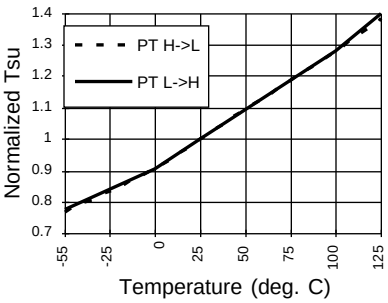
Normalized Tpd vs Temp



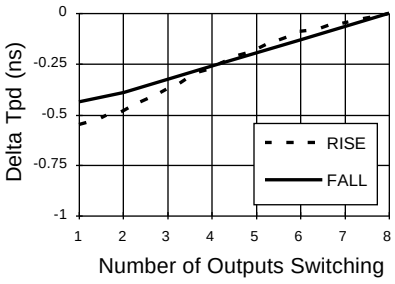
Normalized Tco vs Temp



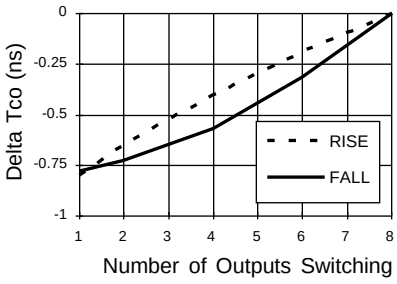
Normalized Tsu vs Temp



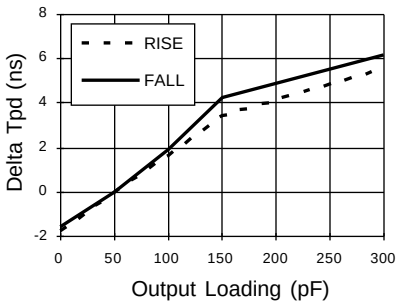
Delta Tpd vs # of Outputs Switching



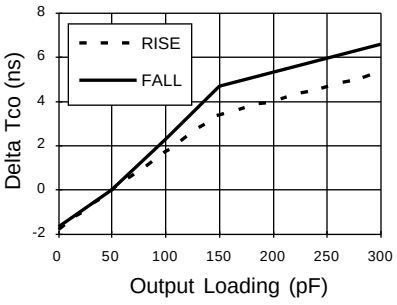
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

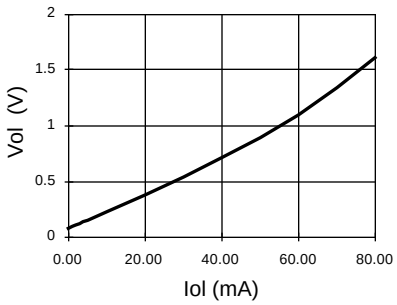


Delta Tco vs Output Loading

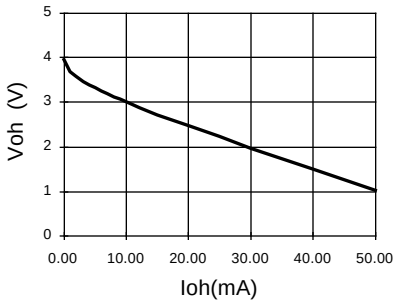


GAL 20V8C: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

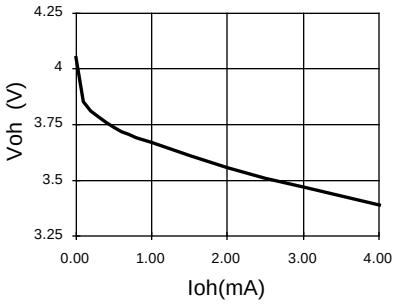
Vol vs Iol



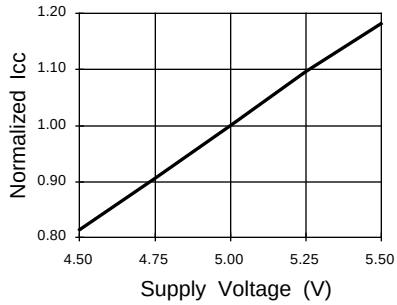
Voh vs Ioh



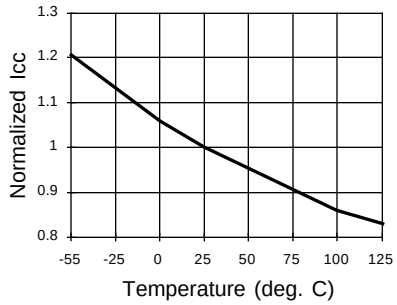
Voh vs Ioh



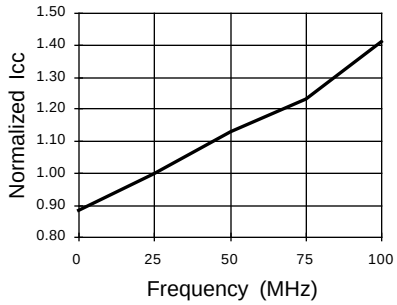
Normalized Icc vs Vcc



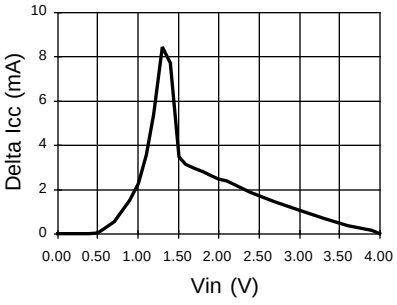
Normalized Icc vs Temp



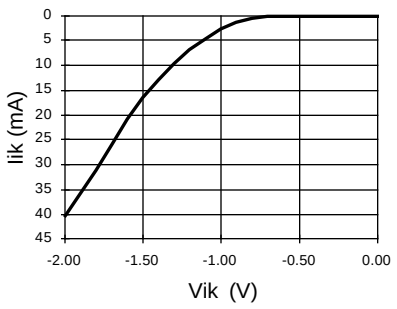
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

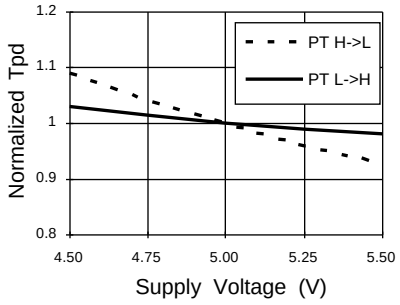


Input Clamp (Vik)

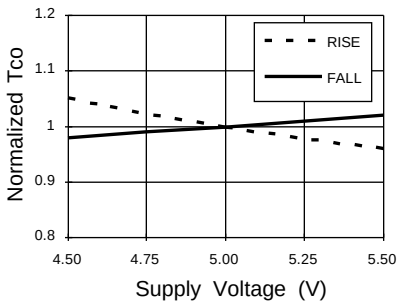


GAL 20V8B-7/-10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

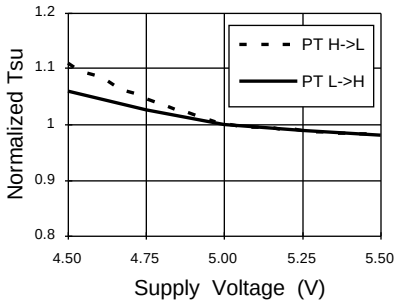
Normalized Tpd vs Vcc



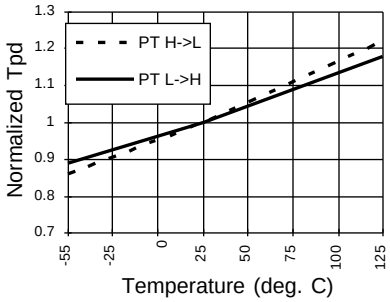
Normalized Tco vs Vcc



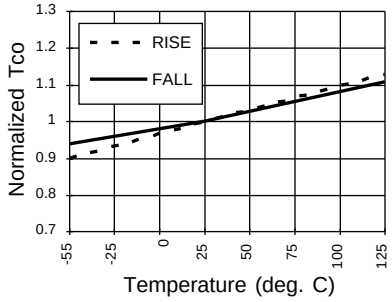
Normalized Tsu vs Vcc



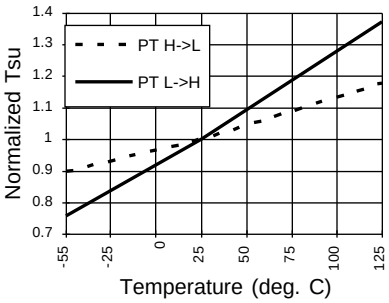
Normalized Tpd vs Temp



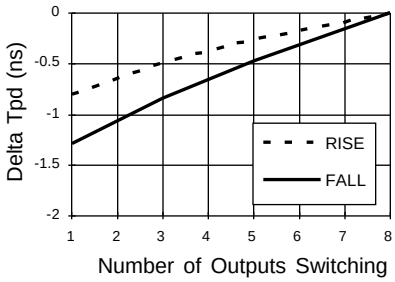
Normalized Tco vs Temp



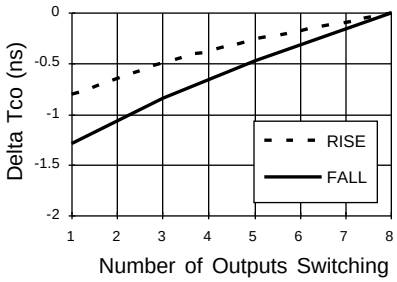
Normalized Tsu vs Temp



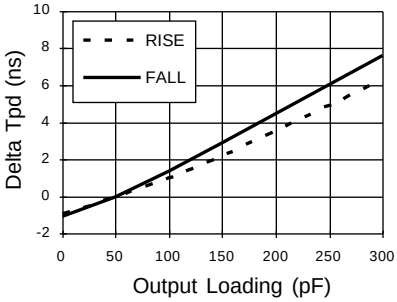
Delta Tpd vs # of Outputs Switching



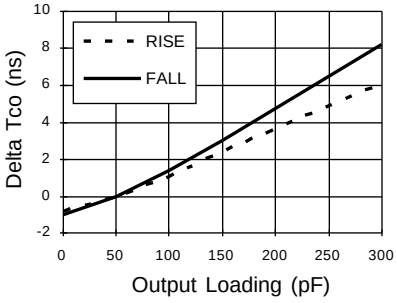
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

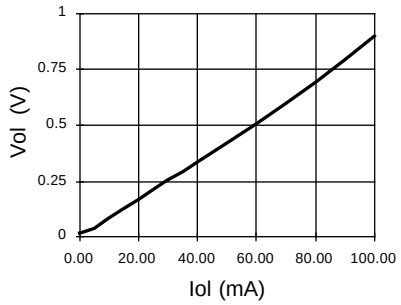


Delta Tco vs Output Loading

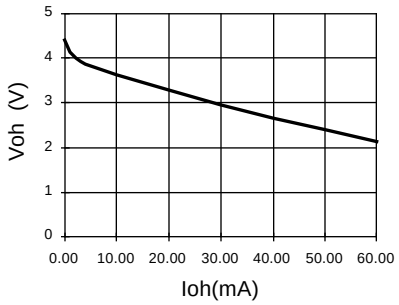


GAL 20V8B-7/-10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

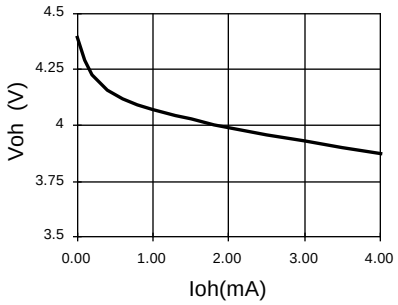
Vol vs Iol



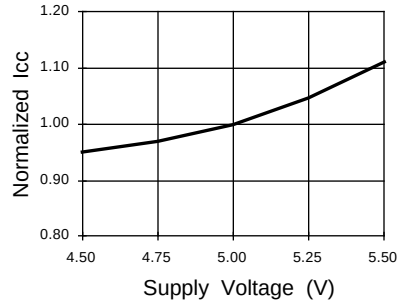
Voh vs Ioh



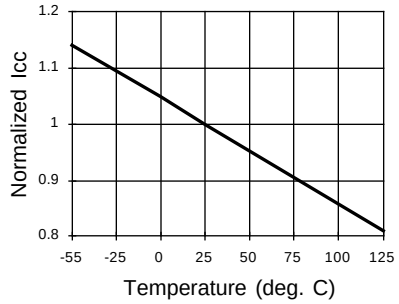
Voh vs Ioh



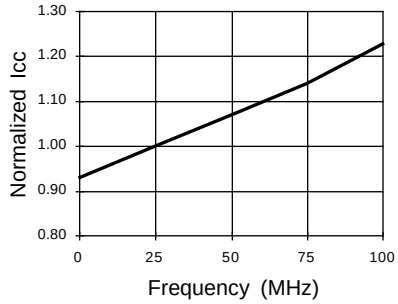
Normalized Icc vs Vcc



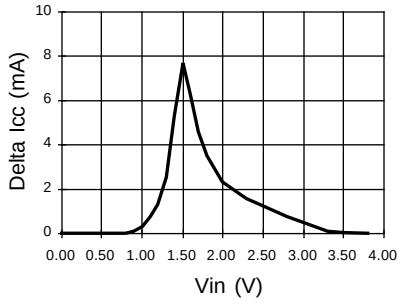
Normalized Icc vs Temp



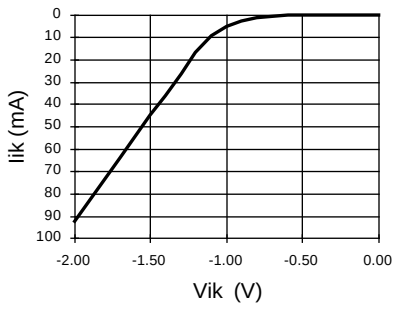
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

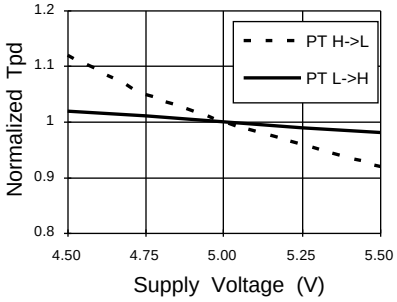


Input Clamp (Vik)

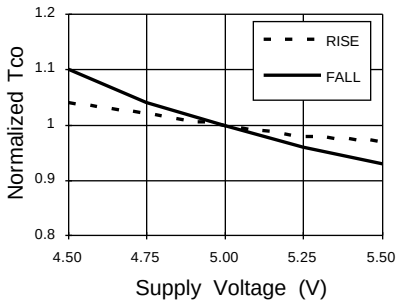


GAL 20V8B-15/-25: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

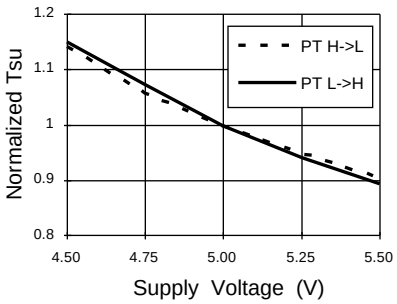
Normalized Tpd vs Vcc



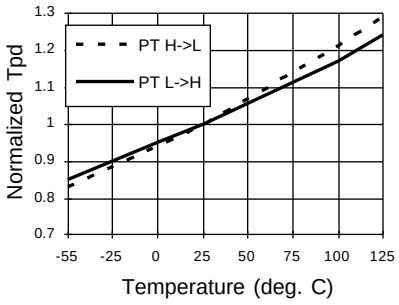
Normalized Tco vs Vcc



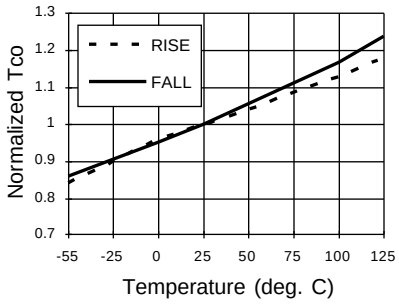
Normalized Tsu vs Vcc



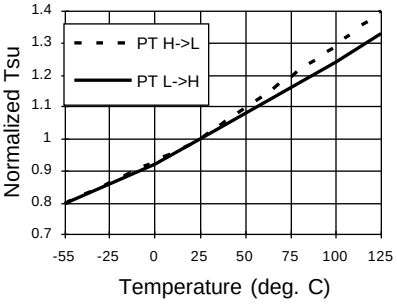
Normalized Tpd vs Temp



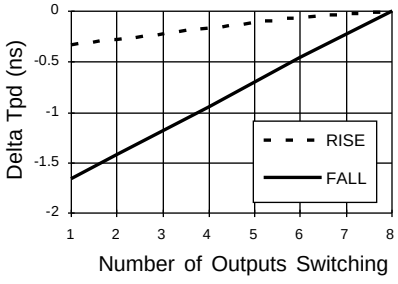
Normalized Tco vs Temp



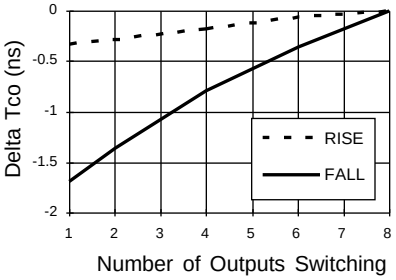
Normalized Tsu vs Temp



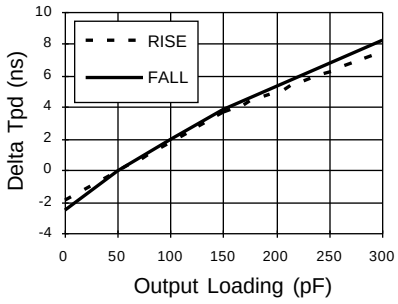
Delta Tpd vs # of Outputs Switching



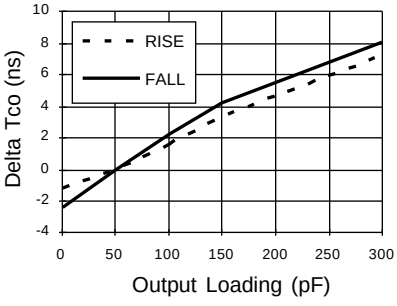
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

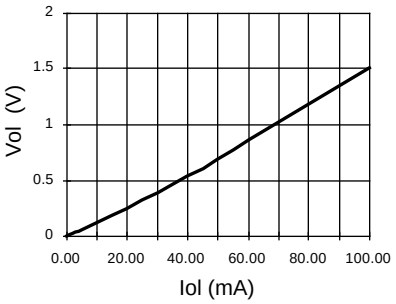


Delta Tco vs Output Loading

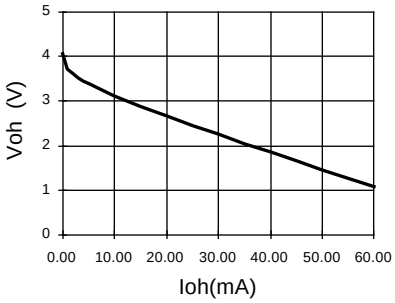


GAL 20V8B-15/-25: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

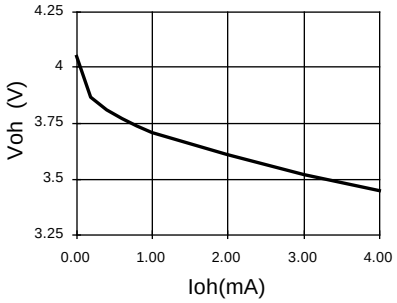
Vol vs Iol



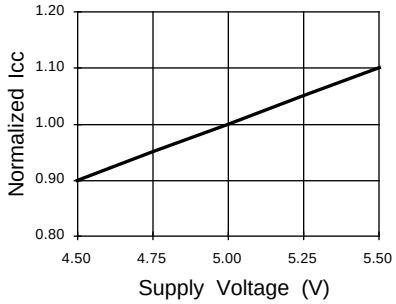
Voh vs Ioh



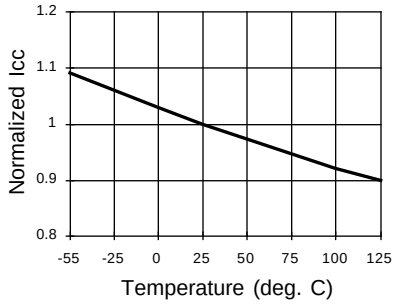
Voh vs Ioh



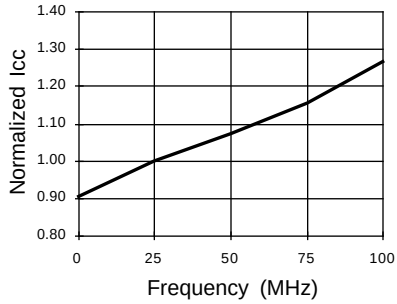
Normalized Icc vs Vcc



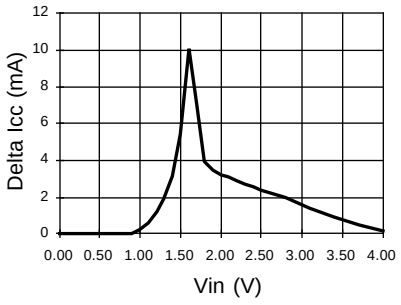
Normalized Icc vs Temp



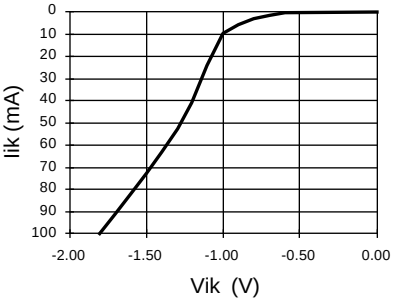
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



GAL20VP8

High-Speed E²CMOS PLD
Generic Array Logic™

FEATURES

- **HIGH DRIVE E²CMOS® GAL® DEVICE**
  - **— TTL Compatible 64 mA Output Drive**
  - **— 15 ns Maximum Propagation Delay**
  - **— Fmax = 80 MHz**
  - **— 10 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **ENHANCED INPUT AND OUTPUT FEATURES**
  - **— Schmitt Trigger Inputs**
  - **— Programmable Open-Drain or Totem-Pole Outputs**
  - **— Active Pull-Ups on All Inputs and I/O pins**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Architecturally Compatible with Standard GAL20V8**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— Ideal for Bus Control & Bus Arbitration Logic**
  - **— Bus Address Decode Logic**
  - **— Memory Address, Data and Control Circuits**
  - **— DMA Control**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

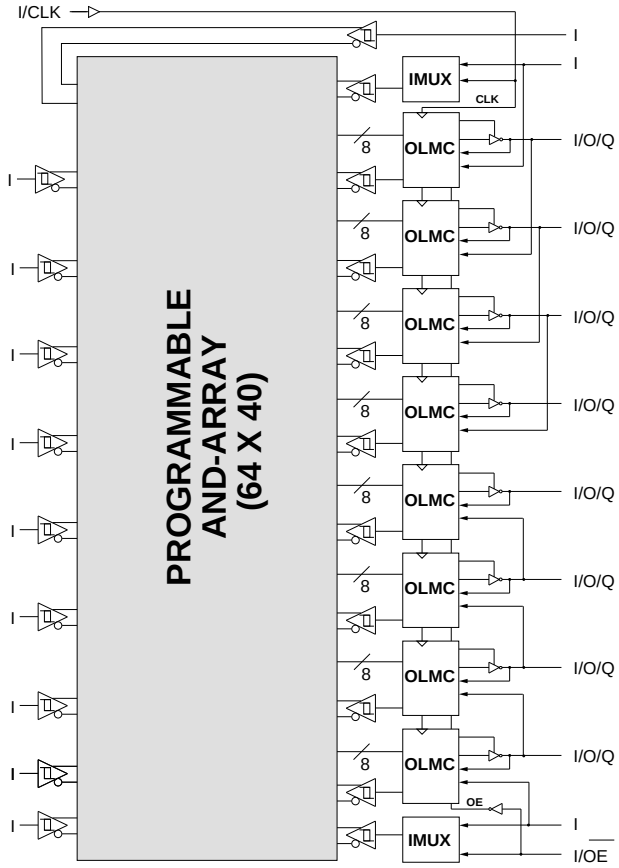
DESCRIPTION

The GAL20VP8, with 64 mA drive capability and 15 ns maximum propagation delay time is ideal for Bus and Memory control applications. The GAL20VP8 is manufactured using Lattice Semiconductor's advanced E²CMOS process which combines CMOS with Electrically Erasable (E²) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

System bus and memory interfaces require control logic before driving the bus or memory interface signals. The GAL20VP8 combines the familiar GAL20V8 architecture with bus drivers as its outputs. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The 64mA output drive eliminates the need for additional devices to provide bus-driving capability.

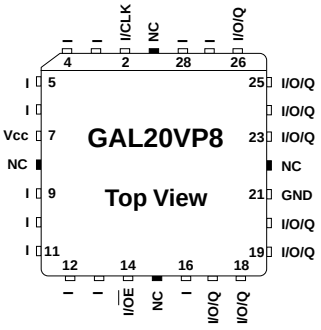
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM

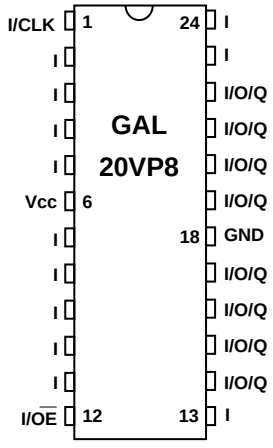


PIN CONFIGURATION

PLCC



DIP



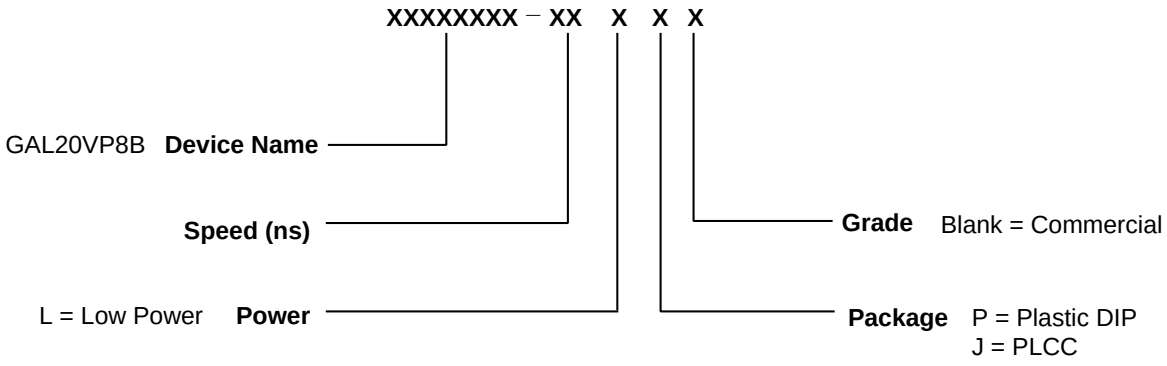
LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL20VP8 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	8	10	115	GAL20VP8B-15LP	24-Pin Plastic DIP
			115	GAL20VP8B-15LJ	28-Lead PLCC
25	10	15	115	GAL20VP8B-25LP	24-Pin Plastic DIP
			115	GAL20VP8B-25LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 and AC2 bit of each of the macrocells controls the input/output and totem-pole/open-drain configuration. These two global and 24 individual architecture bits define all possible configurations in a GAL20VP8. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

COMPILER SUPPORT FOR OLMC

Software compilers support the three different global OLMC modes as different device types. Most compilers also have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1(2) and pin 12(14) are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1(2) and pin 12(14) become dedicated inputs and use the feedback paths of pin 22(26) and pin 14(17) respectively. Because of this feedback path usage, pin 22(26) and pin 14(17) do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 17(20) and 19(23)) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

In addition to the architecture configurations, the logic compiler software also supports configuration of either totem-pole or open-drain outputs. The actual architecture bit configuration, again, is transparent to the user with the default configuration being the standard totem-pole output.

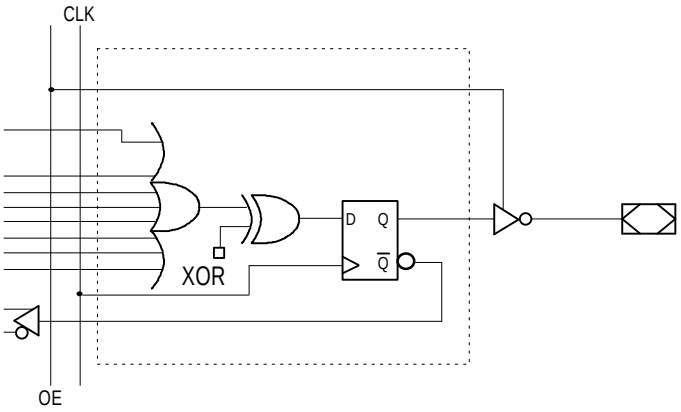
REGISTERED MODE

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

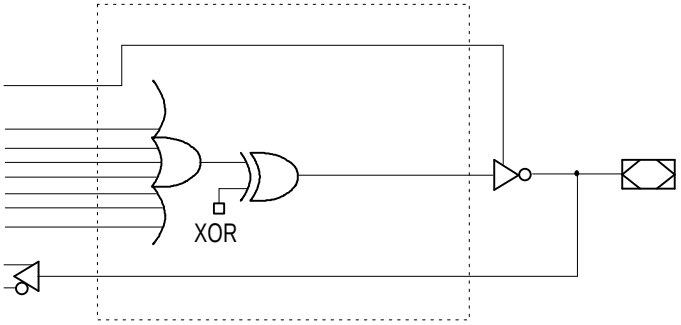
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pin 1(2) controls common CLK for the registered outputs.
- Pin 12(14) controls common $\overline{OE}$ for the registered outputs.
- Pin 1(2) & Pin 12(14) are permanently configured as CLK & $\overline{OE}$.



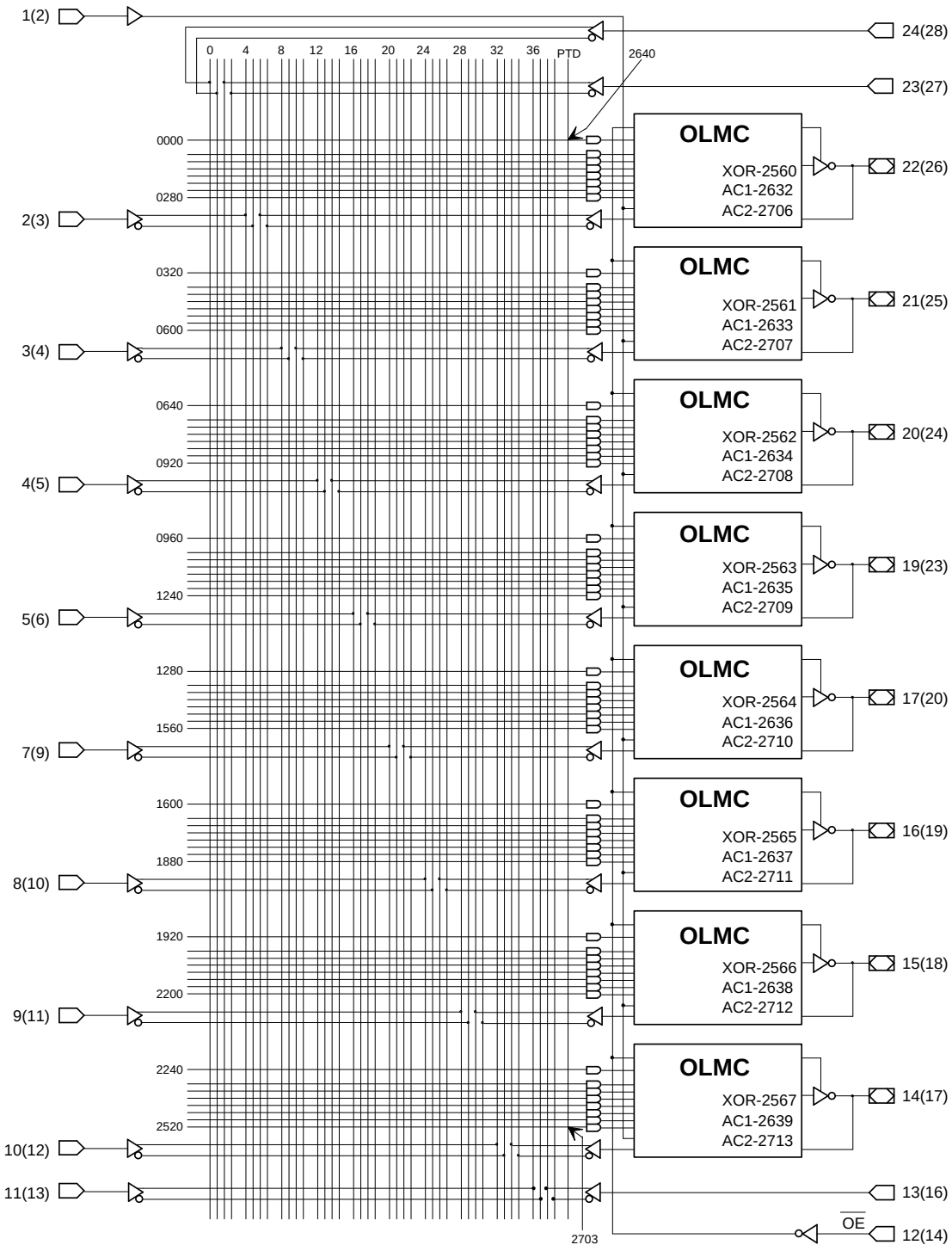
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pin 1(2) & Pin 12(14) are permanently configured as CLK & $\overline{OE}$.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

REGISTERED MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte7 Byte6	.... Byte1 Byte0

MSB LSB

SYN-2704
AC0-2705

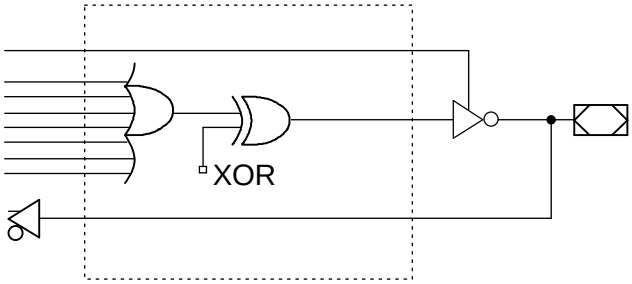
COMPLEX MODE

In the Complex mode, macrocells are configured as output only or I/O functions.

Up to six I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 14(17) & 22(26)) do not have input capability. Designs requiring eight I/O's can be implemented in the Registered mode.

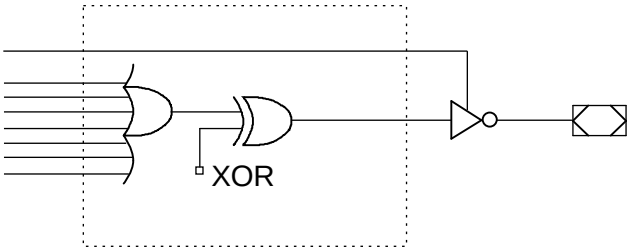
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1(2) and 12(14) are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pin 15(18) through Pin 21(25) are configured to this function.



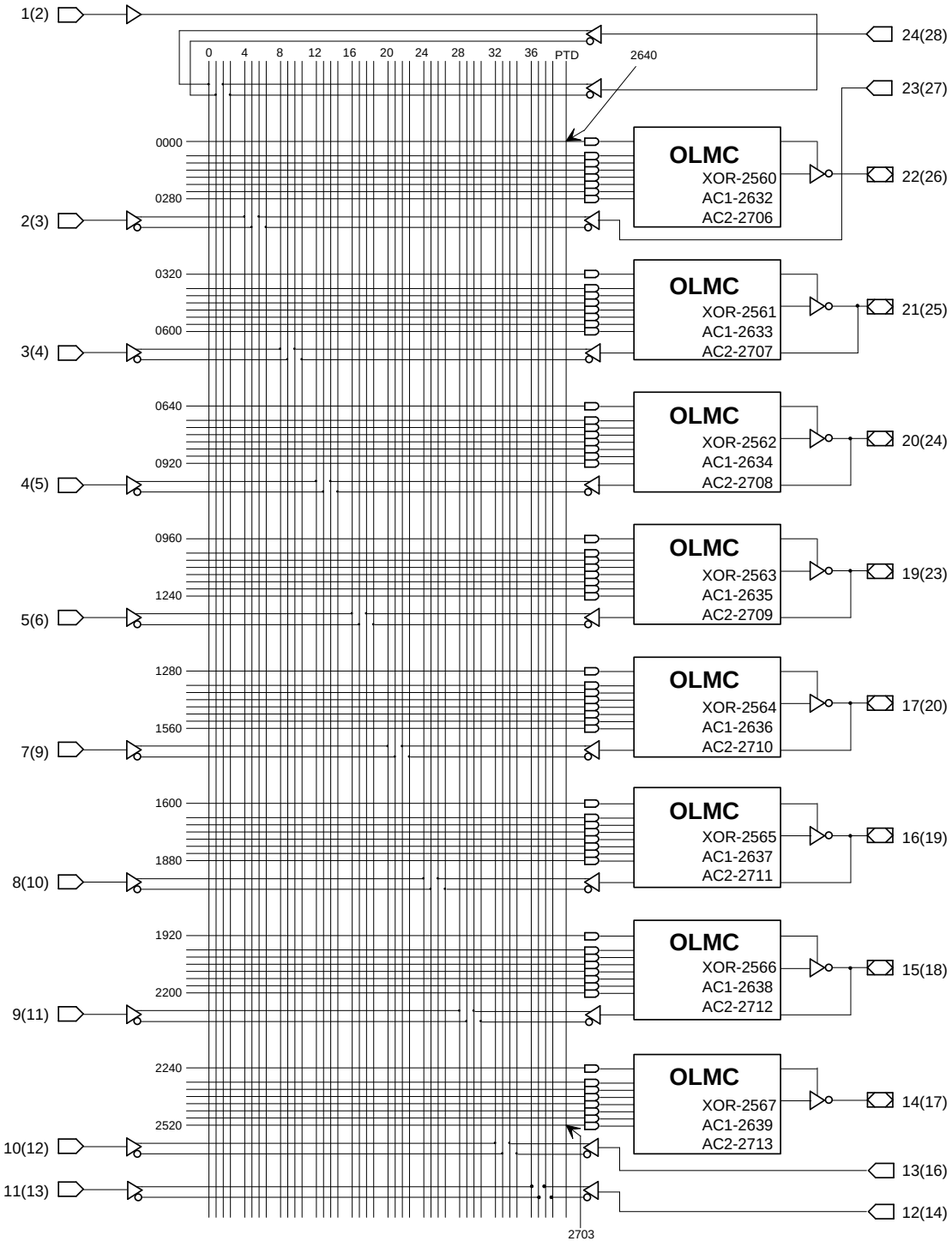
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pin 14(17) and Pin 22(26) are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

COMPLEX MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte7 | Byte6	.... Byte1 | Byte0

MSB LSB

SYN-2704
AC0-2705

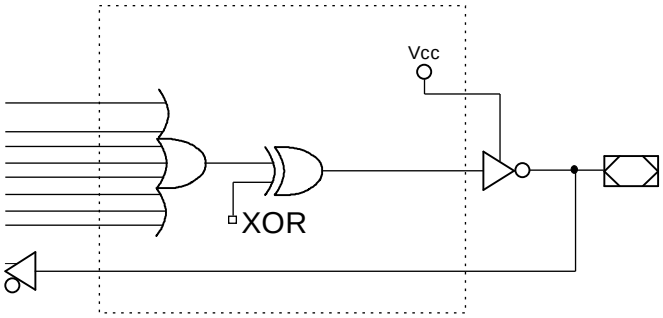
SIMPLE MODE

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

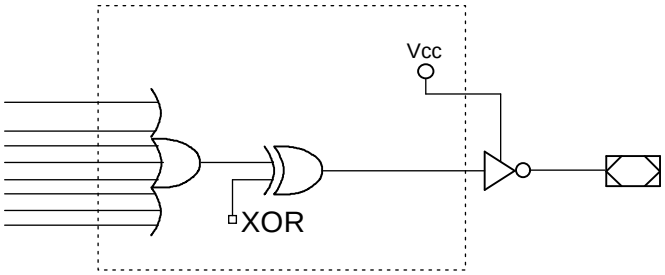
Pins 1(2) and 12(14) are always available as data inputs into the AND array. The center two macrocells (pins 17(20) & 19(23)) cannot be used in the input configuration.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



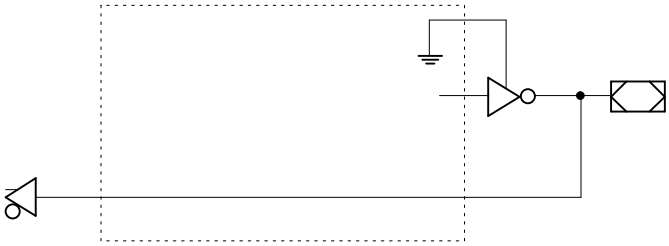
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- All OLMC **except** pins 17(20) & 19(23) can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pins 17(20) & 19(23) are permanently configured to this function.



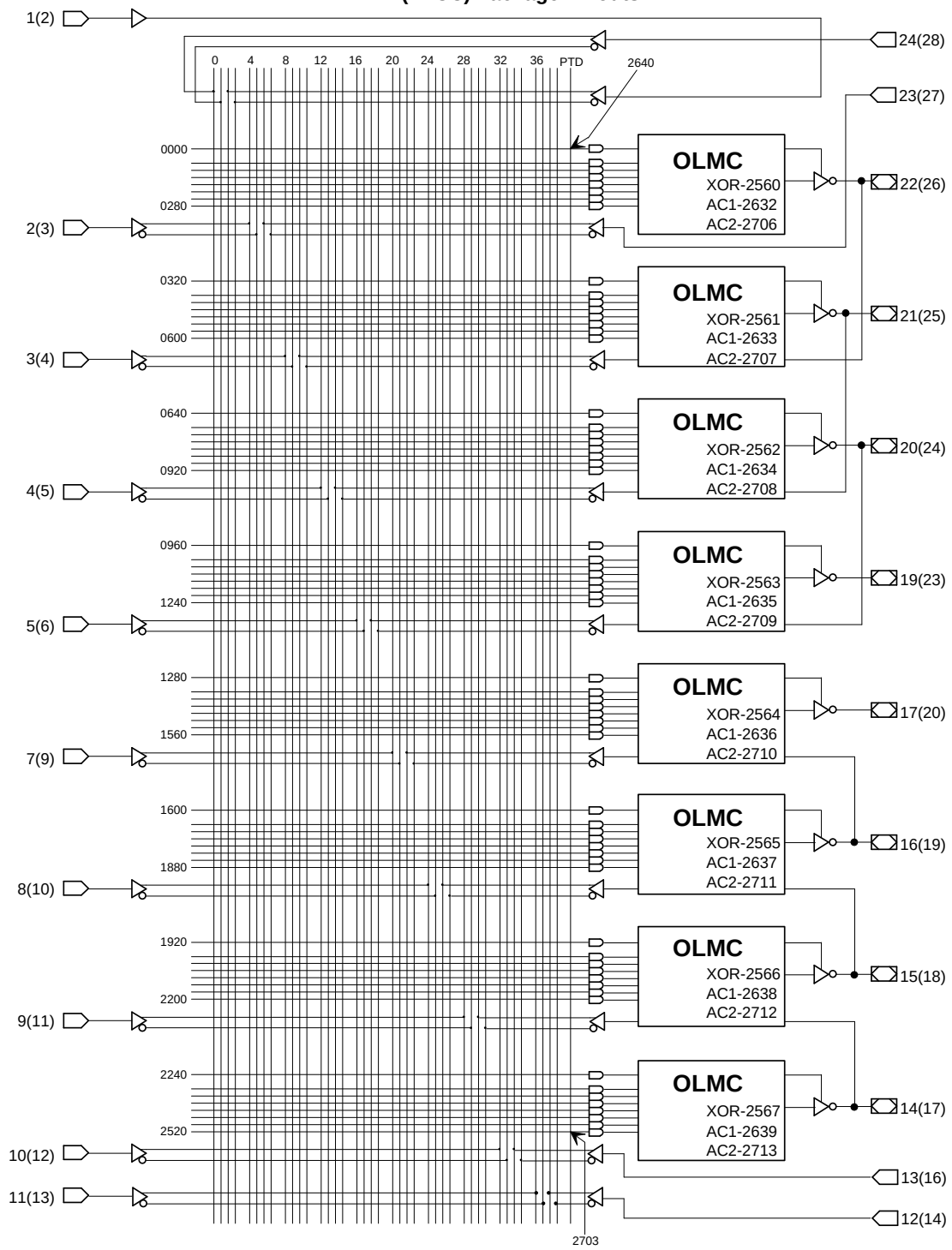
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- All OLMC **except** pins 17(20) & 19(23) can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

SIMPLE MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte7 Byte6	.... Byte1 Byte0

MSB LSB

SYN-2704
AC0-2705

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[4]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
V_{I}[1]	Input Clamp Voltage	Vcc = Min. I_{IN} = –32mA	—		–1.2	V
I_{IL}[2]	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	64	mA
I_{OH}	High Level Output Current		—	—	–32	mA
I_{OS}[3]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–60	—	–400	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -15/-25	—	90	115	mA

1) Guaranteed but not 100% tested.
2) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
3) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
4) Typical values are at Vcc = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -15 MIN.	COM -15 MAX.	COM -25 MIN.	COM -25 MAX.	UNITS
tpd	A	Input or I/O to Combinational Output	3	15	3	25	ns
tco	A	Clock to Output Delay	2	10	2	15	ns
tcf[2]	—	Clock to Feedback Delay	—	4.5	—	10	ns
tsu	—	Setup Time, Input or Feedback before Clock ↑	8	—	10	—	ns
th	—	Hold Time, Input or Feedback after Clock ↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	55.5	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	80	—	50	—	MHz
	A	Maximum Clock Frequency with No Feedback	80	—	50	—	MHz
twh	—	Clock Pulse Duration, High	6	—	10	—	ns
twl	—	Clock Pulse Duration, Low	6	—	10	—	ns
ten	B	Input or I/O to Output Enabled	—	15	—	20	ns
	B	$\overline{OE}$ to Output Enabled	—	12	—	15	ns
tdis	C	Input or I/O to Output Disabled	—	15	—	20	ns
	C	$\overline{OE}$ to Output Disabled	—	12	—	15	ns

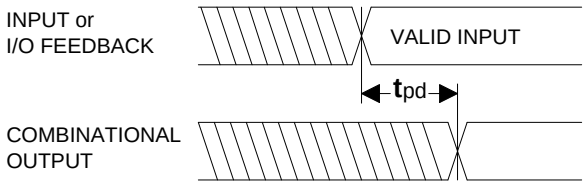
1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Specification section.
3) Refer to fmax Specification section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

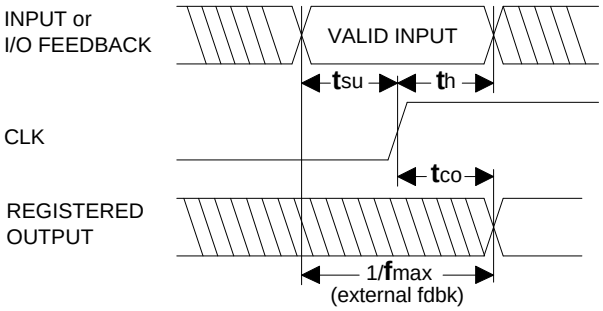
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	15	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

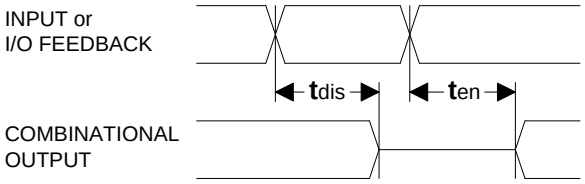
SWITCHING WAVEFORMS



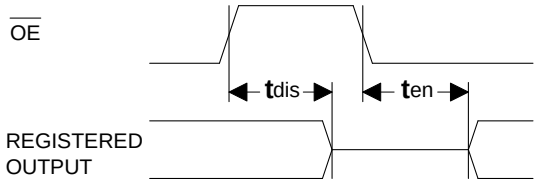
Combinatorial Output



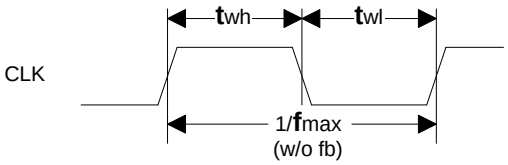
Registered Output



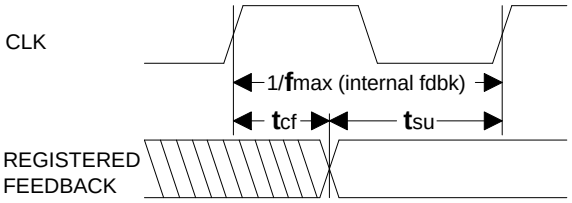
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

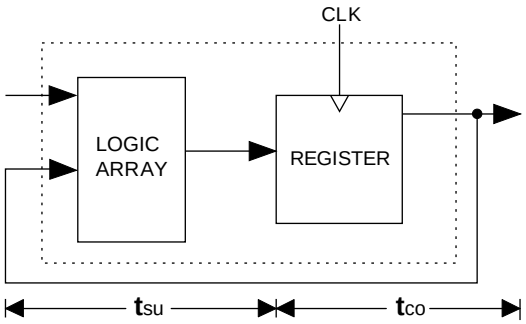


Clock Width



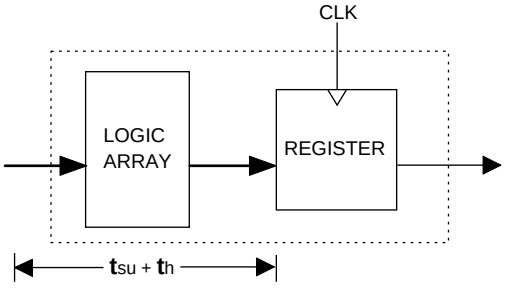
fmax with Feedback

fmax DESCRIPTIONS



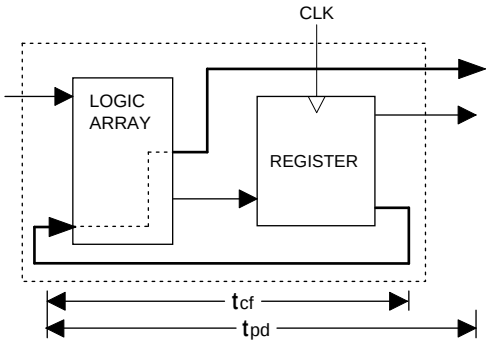
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

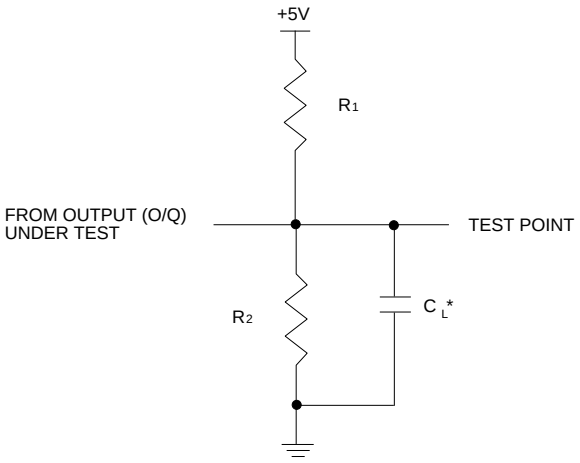
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		500Ω	500Ω	50pF
B	Active High	∞	500Ω	50pF
	Active Low	500Ω	500Ω	50pF
C	Active High	∞	500Ω	5pF
	Active Low	500Ω	500Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL20VP8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

SECURITY CELL

The security cell is provided on all GAL20VP8 devices to prevent unauthorized copying of the array patterns. Once programmed, the circuitry enabling array is disabled, preventing further programming or verification of the array. The cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. Signature data is always available to the user.

LATCH-UP PROTECTION

GAL20VP8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

BULK ERASE MODE

During a programming cycle, a clear function performs a bulk erase of the array and the architecture word. In addition, the electronic signature word and the security cell are erased. This mode resets a previously configured device back to its original state, which is all JEDEC ones.

SCHMITT TRIGGER INPUTS

One of the enhancements of the GAL20VP8 for bus interface logic implementation is input hysteresis. The threshold of the positive going edge is 1.5V, while the threshold of the negative going edge is 1.3V. This provides a typical hysteresis of 200mV between positive and negative transitions of the inputs.

HIGH DRIVE OUTPUTS

All eight outputs of the GAL20VP8 are capable of driving 64 mA loads when driving low and 32 mA loads when driving high. Near symmetrical high and low output drive capability provides small skews between high-to-low and low-to-high output transitions.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

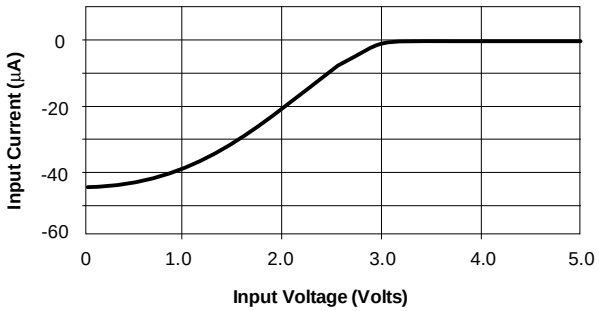
The GAL20VP8 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors can perform output register preload automatically.

INPUT BUFFERS

The GAL20VP8 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

GAL20VP8 input buffers have active pull-ups within their input structure. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

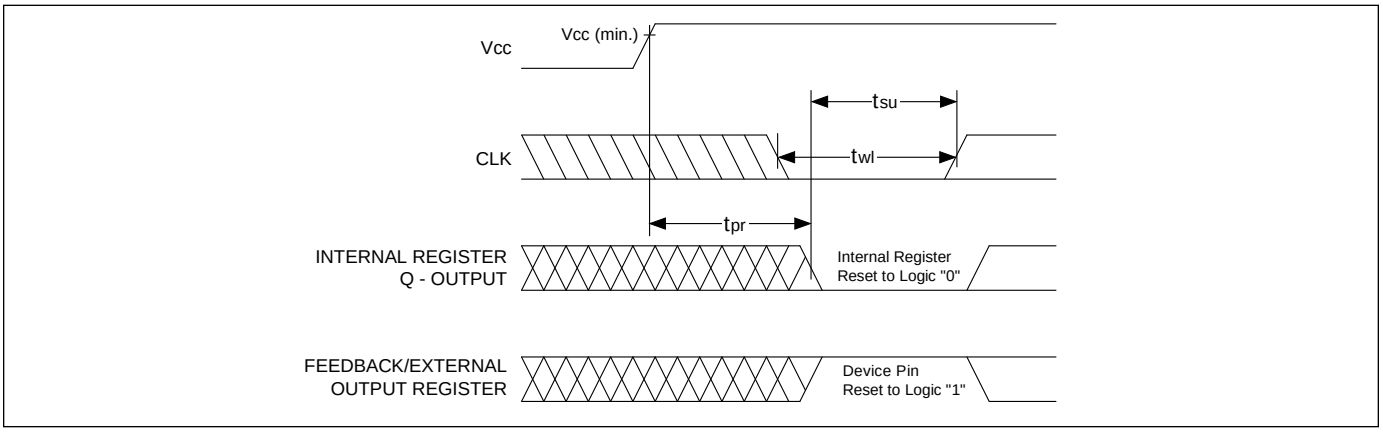
Typical Input Pull-up Characteristic



PROGRAMMABLE OPEN-DRAIN OUTPUTS

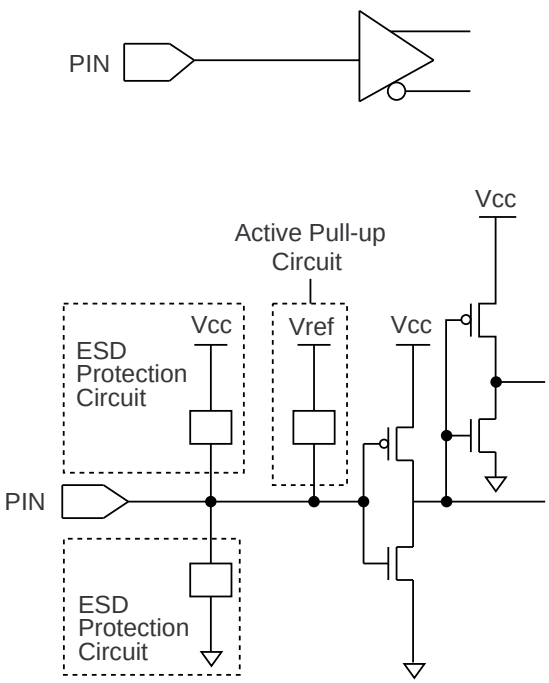
In addition to the standard GAL20V8 type configuration, the outputs of the GAL20VP8 are individually programmable either as a standard totempole output or an open-drain output. The totempole output drives the specified V_{OH} and V_{OL} levels whereas the open-drain output drives only the specified V_{OL}. The V_{OH} level on the open-drain ouput depends on the external loading and pull-up. This output configuration is controlled by the AC2 fuse. When AC2 cell is erased (JEDEC "1") the output is configured as a totempole output and when AC2 cell is programmed (JEDEC "0") the output is configured as an open-drain. The default configuration when the device is in bulk erased state is totempole configuration. The AC2 fuses associated with each of the outputs is included in all of the logic diagrams.

POWER-UP RESET



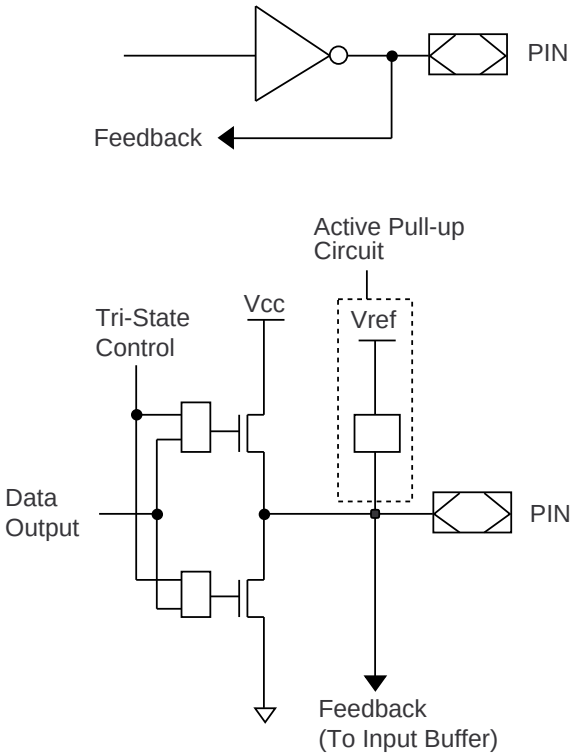
Circuitry within the GAL20VP8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20VP8. First, the V_{CC} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Vref = 3.1V

Typical Input

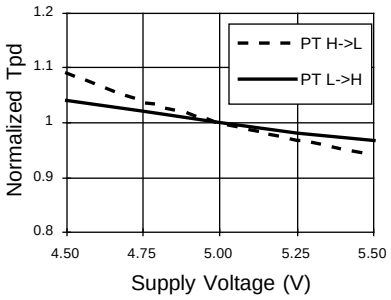


Vref = 3.1V

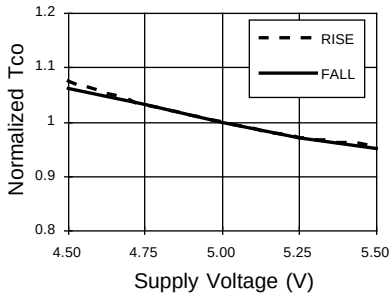
Typical Output

TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

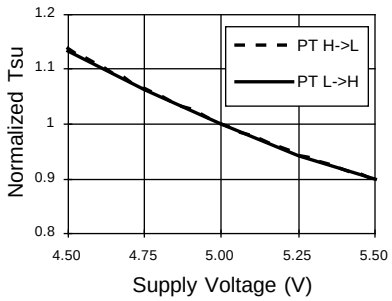
Normalized Tpd vs Vcc



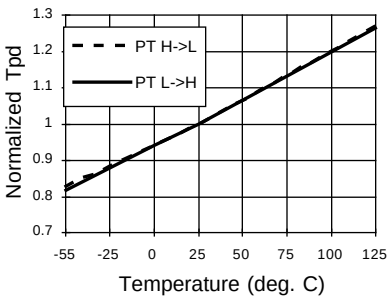
Normalized Tco vs Vcc



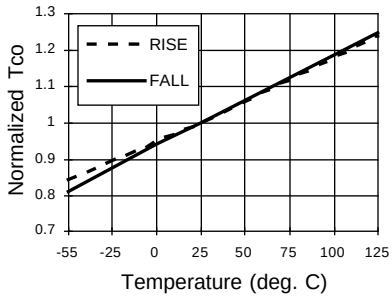
Normalized Tsu vs Vcc



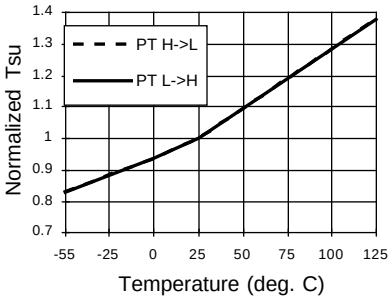
Normalized Tpd vs Temp



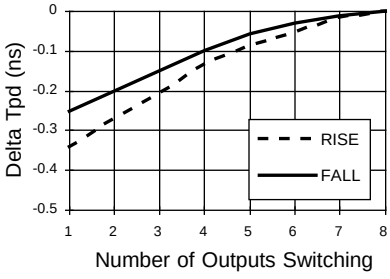
Normalized Tco vs Temp



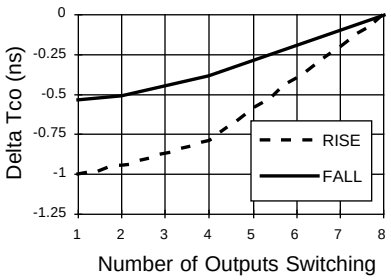
Normalized Tsu vs Temp



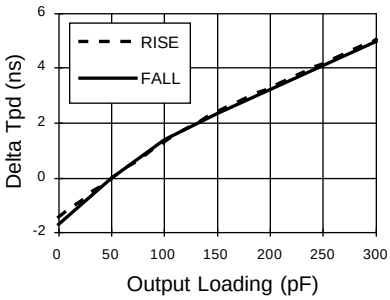
Delta Tpd vs # of Outputs Switching



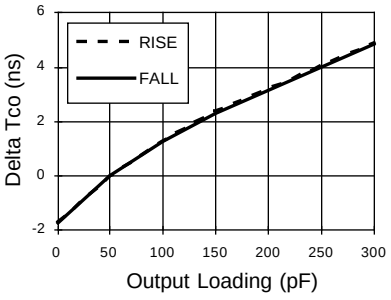
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

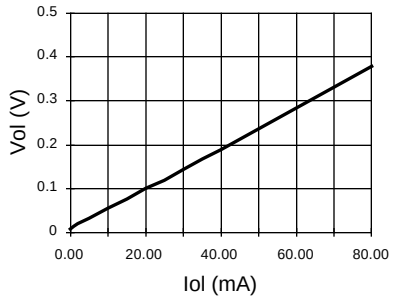


Delta Tco vs Output Loading

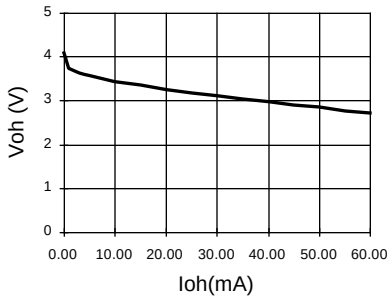


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

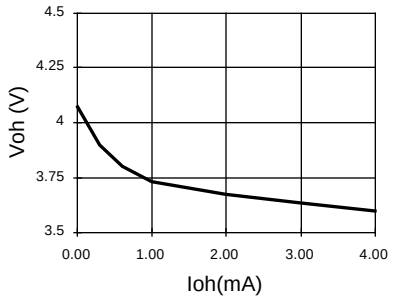
Vol vs Iol



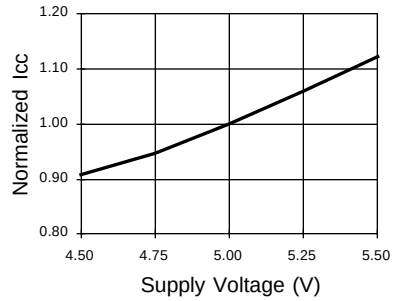
Voh vs Ioh



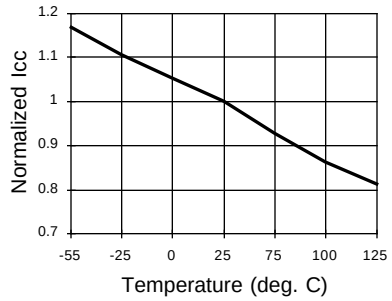
Voh vs Ioh



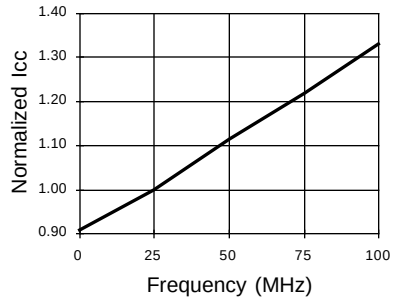
Normalized Icc vs Vcc



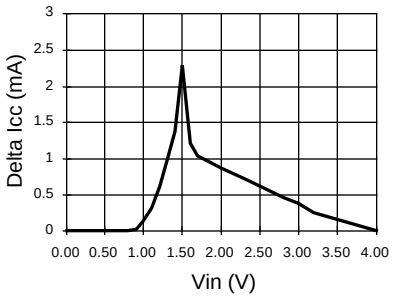
Normalized Icc vs Temp



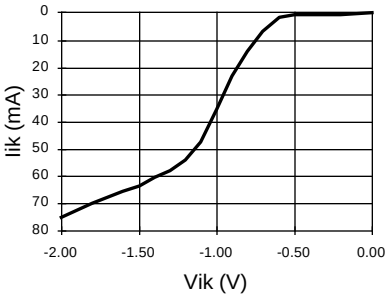
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



GAL20XV10

High-Speed E²CMOS PLD Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 10 ns Maximum Propagation Delay**
  - **— Fmax = 100 MHz**
  - **— 7 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 16 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - **— 90mA Maximum Icc**
  - **— 75mA Typical Icc**
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100 ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— XOR Gate Capability on all Outputs**
  - **— Full Function and Parametric Compatibility with PAL12L10, 20L10, 20X10, 20X8, 20X4**
  - **— Registered or Combinatorial with Polarity**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
- **APPLICATIONS INCLUDE:**
  - **— High Speed Counters**
  - **— Graphics Processing**
  - **— Comparators**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

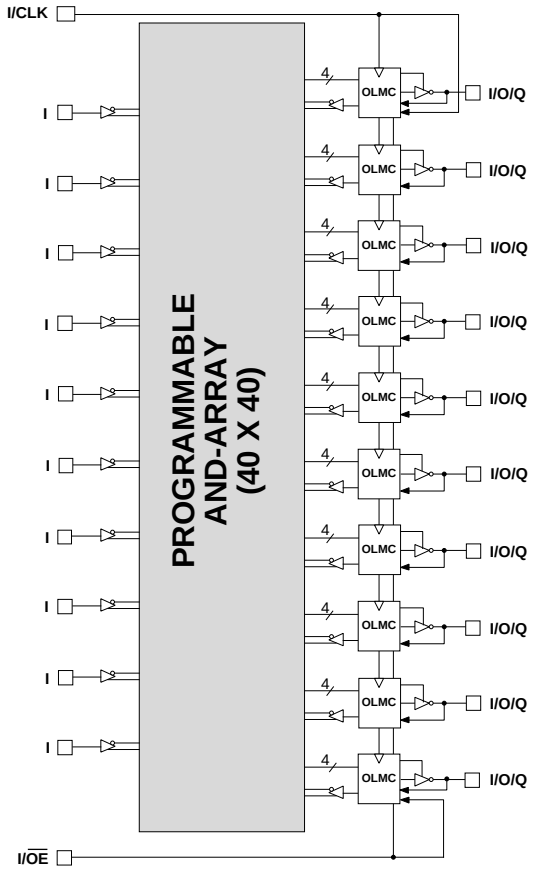
DESCRIPTION

The GAL20XV10 combines a high performance CMOS process with electrically erasable (E²) floating gate technology to provide the highest speed Exclusive-OR PLD available in the market. At 90mA maximum Icc (75mA typical Icc), the GAL20XV10 provides a substantial savings in power when compared to bipolar counterparts. E²CMOS technology offers high speed (<100ms) erase times providing the ability to reprogram, reconfigure or test the devices quickly and efficiently.

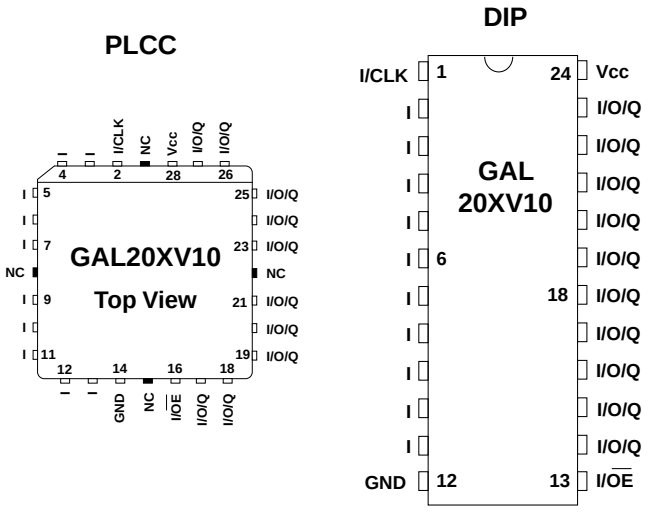
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL20XV10 are the PAL® architectures listed in the macrocell description section of this document. The GAL20XV10 is capable of emulating these PAL architectures with full function and parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacturing. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



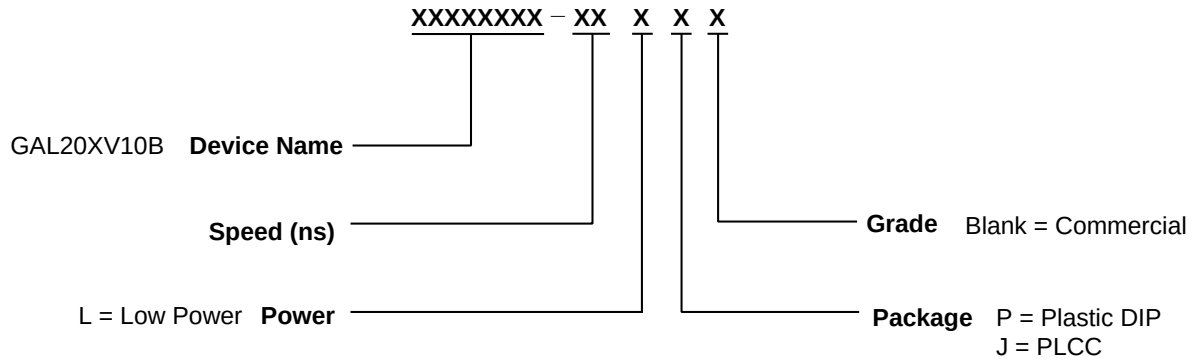
LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL20XV10 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	6	7	90	GAL20XV10B-10LP	24-Pin Plastic DIP
				GAL20XV10B-10LJ	28-Lead PLCC
15	8	8	90	GAL20XV10B-15LP	24-Pin Plastic DIP
				GAL20XV10B-15LJ	28-Lead PLCC
20	10	10	90	GAL20XV10B-20LP	24-Pin Plastic DIP
				GAL20XV10B-20LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the Output Logic Macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

The GAL20XV10 has two global architecture configurations that allow it to emulate PAL architectures. The Input mode emulates combinatorial PAL devices, with the I/CLK and I/$\overline{OE}$ pins used as inputs. The Feedback mode emulates registered PAL devices with the I/CLK pin used as the register clock and the I/$\overline{OE}$ pin as an output enable for all registers. The following is a list of PAL architectures that the GAL20XV10 can emulate. It also shows the global architecture mode used to emulate the PAL architecture.

PAL Architectures Emulated by GAL20XV10	GAL20XV10 Global OLMC Mode
PAL12L10	Input Mode
PAL20L10	Input Mode
PAL20X10	Feedback Mode
PAL20X8	Feedback Mode
PAL20X4	Feedback Mode

INPUT MODE
The Input mode architecture is defined when the global architecture bit SYN = 1. In this mode, the I/CLK pin becomes an input to the AND array and also provides the clock source for all registers. The I/OE pin becomes an input into the AND array and provides the output enable control for any macrocell configured as an Exclusive-OR function. Feedback into the AND array is provided from macrocells 2 through 9 only. In this mode, macrocells 1 and 10 have no feedback into the AND array.

FEEDBACK MODE
The Feedback mode architecture is defined when the global architecture bit SYN = 0. In this mode the I/CLK pin becomes a dedicated clock source for all registers. The I/$\overline{OE}$ pin is a dedicated output enable control for any macrocell configured as an Exclusive-OR function. The I/CLK and I/$\overline{OE}$ pins are not available to the AND array in this mode. Feedback into the AND array is provided on all macrocells 1 through 10.

FEATURES
Each Output Logic Macrocell has four possible logic function configurations controlled by architecture control bits AC0 and AC1. Four product terms are fed into each macrocell.

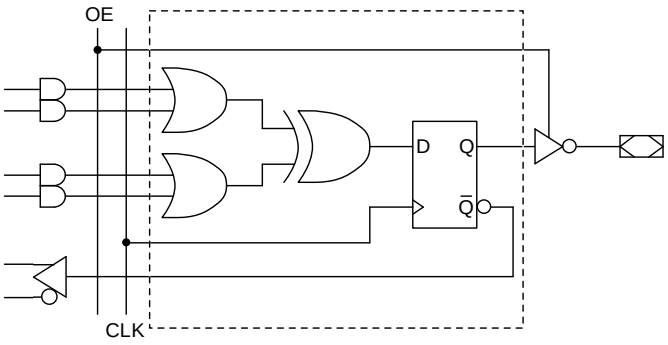
XOR REGISTERED CONFIGURATION
The Macrocell is set to the Exclusive-OR Registered configuration when AC0 = 0 and AC1 = 0. The four product terms are segmented into two OR-sums of two product terms each, which are then combined by an Exclusive-OR gate and fed into a D-type register. The register is clocked by the low-to-high transition of the I/CLK pin. The inverting output buffer is enabled by the I/$\overline{OE}$ pin, which is an active low output enable common to all Exclusive-OR macrocells. In Feedback mode, the state of the register is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the register is available to the AND array via an internal feedback path on macrocells 2 through 9 only, macrocells 1 and 10 have no feedback into the AND array.

REGISTERED CONFIGURATION
The Macrocell is set to Registered configuration when AC0 = 1 and AC1 = 0. Three of the four product terms are used as sum-of-product terms for the D input of the register. The inverting output buffer is enabled by the fourth product term. The output is enabled while this product term is true. The XOR bit controls the polarity of the output. The register is clocked by the low-to-high transition of the I/CLK. In Feedback mode, the state of the register is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the register is available to the AND array via an internal feedback path on macrocells 2 through 9 only, macrocells 1 and 10 have no feedback into the AND array.

XOR COMBINATORIAL CONFIGURATION
The Macrocell is set to the Exclusive-OR Combinatorial configuration when AC0 = 0 and AC1 = 1. The four product terms are segmented into two OR-sums of two product terms each, which are then combined by an Exclusive-OR gate and fed to an output buffer. The inverting output buffer is enabled by the I/$\overline{OE}$ pin, which is an active low output enable that is common to all XOR macrocells. In Feedback mode, the state of the I/O pin is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the I/O pin is available to the AND array via an input buffer path on macrocells 2 through 9 only, macrocells 1 and 10 have no input into the AND array.

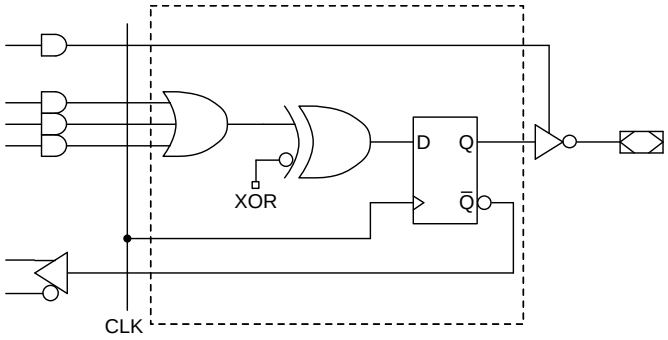
COMBINATORIAL CONFIGURATION
The Macrocell is set to Combinatorial mode when AC0 = 1 and AC1 = 1. Three of the four product terms are used as sum-of-product terms for the combinatorial output. The XOR bit controls the polarity of the output. The inverting output buffer is enabled by the fourth product term. The output is enabled while this product term is true. In Feedback mode, the state of the I/O pin is available to the AND array via an internal feedback path on all macrocells. In Input mode, the state of the I/O pin is available to the AND array via an input buffer path on macrocells 2 through 9 only, macrocells 1 and 10 have no input into the AND array.

INPUT MODE



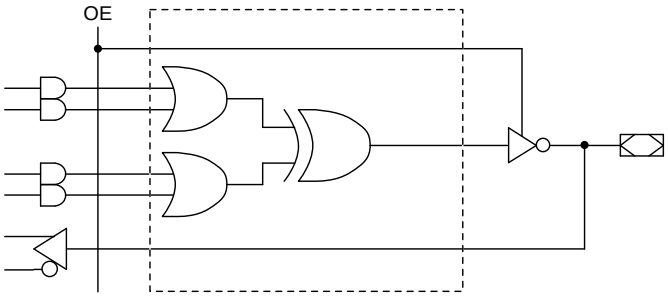
XOR Registered Configuration

- SYN = 1.
- AC0 = 0.
- AC1 = 0.
- OLMC 1 and OLMC10 do not have the feedback path.
- Pin 1(2) can be CLK and/or Input.
- Pin 13(16) can be $\overline{OE}$ and/or Input.



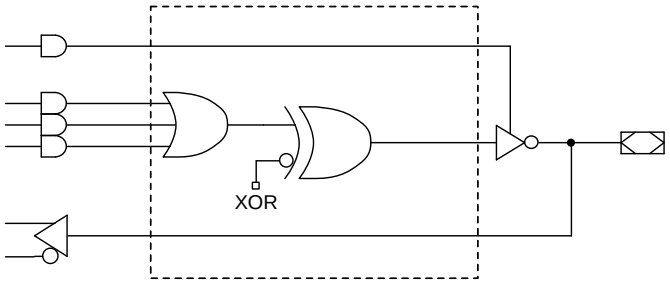
Registered Configuration

- SYN = 1.
- AC0 = 1.
- AC1 = 0.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- OLMC 1 and OLMC10 do not have the feedback path.
- Pin 1(2) can be CLK and/or Input.
- OE controlled by product term.



XOR Combinatorial Configuration

- SYN = 1.
- AC0 = 0.
- AC1 = 1.
- OLMC 1 and OLMC10 do not have the feedback path.
- Pin 13(16) can be $\overline{OE}$ and/or Input.

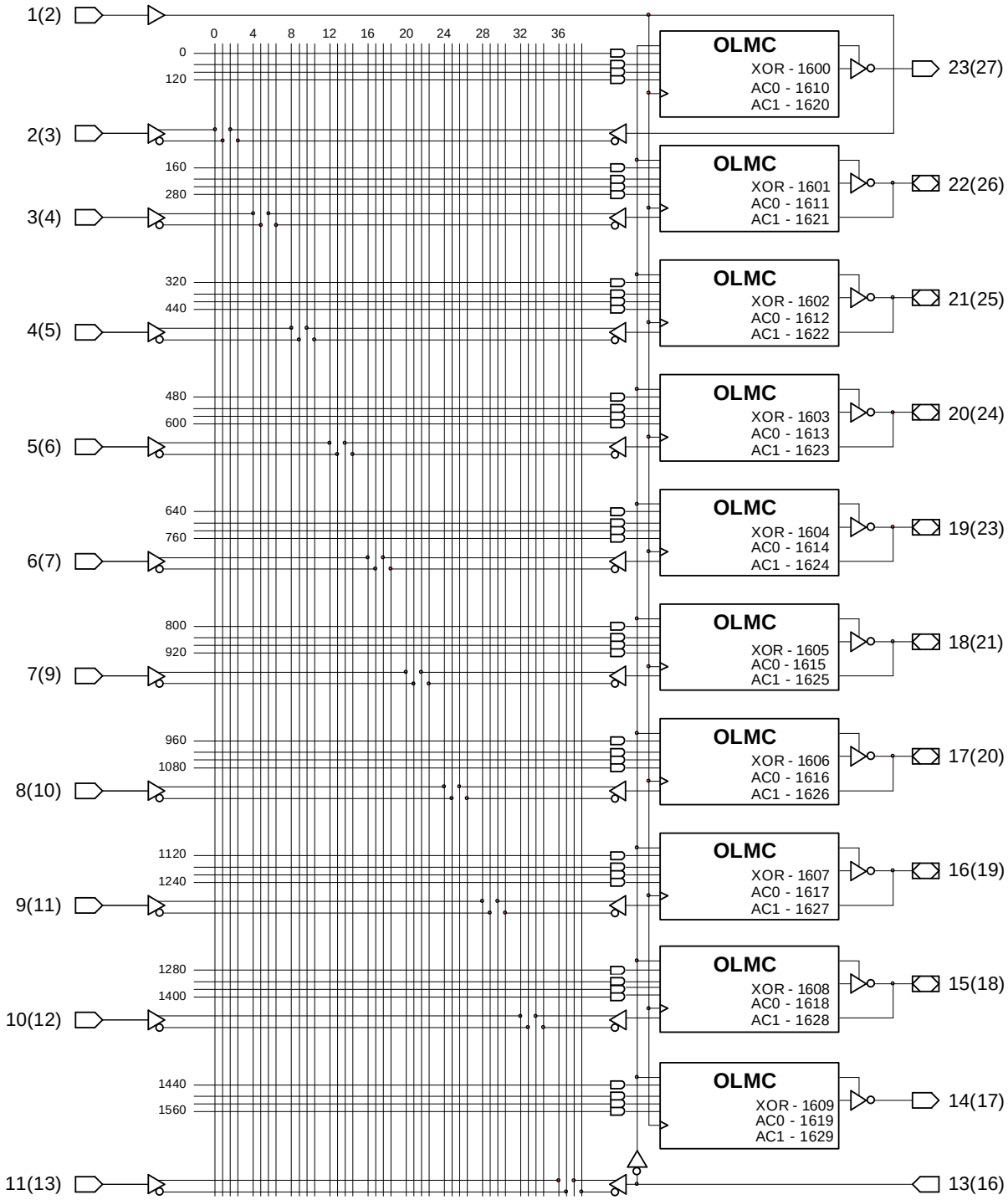


Combinatorial Configuration

- SYN = 1.
- AC0 = 1.
- AC1 = 1.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- OLMC 1 and OLMC10 do not have the feedback path.
- OE controlled by product term.

INPUT MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts

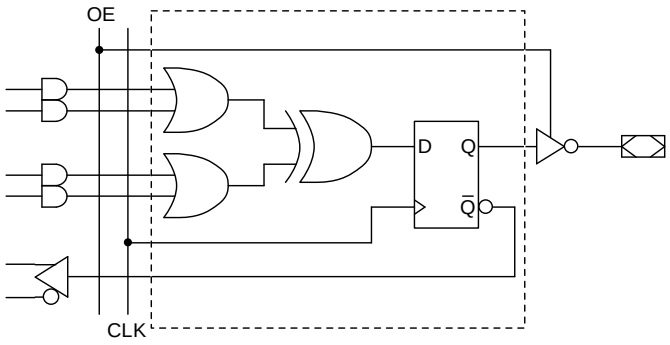


40-USER ELECTRONIC SIGNATURE FUSES

1631, 1632, ...			.... 1669, 1670
Byte4	Byte3	.... Byte1	Byte0

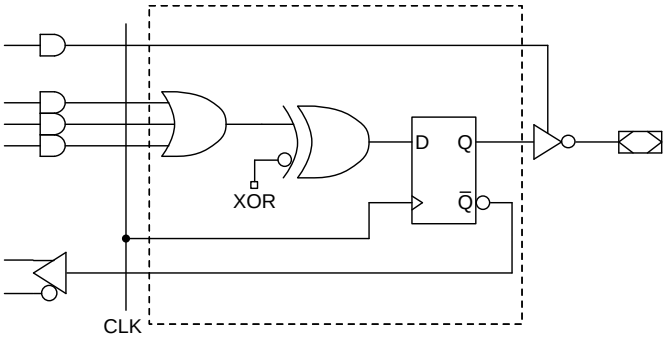
SYN - 1630

FEEDBACK MODE



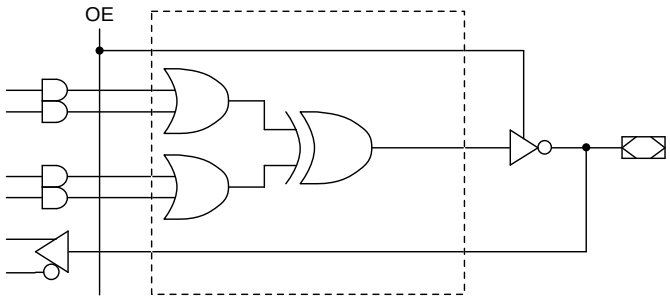
XOR Registered Configuration

- SYN = 0.
- AC0 = 0.
- AC1 = 0.
- Dedicated CLK input on Pin 1(2).
- Dedicated $\overline{OE}$ input on Pin 13(16).



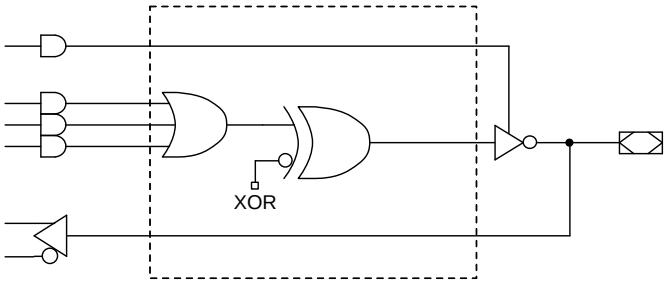
Registered Configuration

- SYN = 0.
- AC0 = 1.
- AC1 = 0.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- Dedicated CLK input on Pin 1(2).
- OE controlled by product term.
- Pin 13(16) is not connected to this configuration.



XOR Combinatorial Configuration

- SYN = 0.
- AC0 = 0.
- AC1 = 1.
- Dedicated $\overline{OE}$ input on Pin 13(16).
- Pin 1(2) is not connected to this configuration.

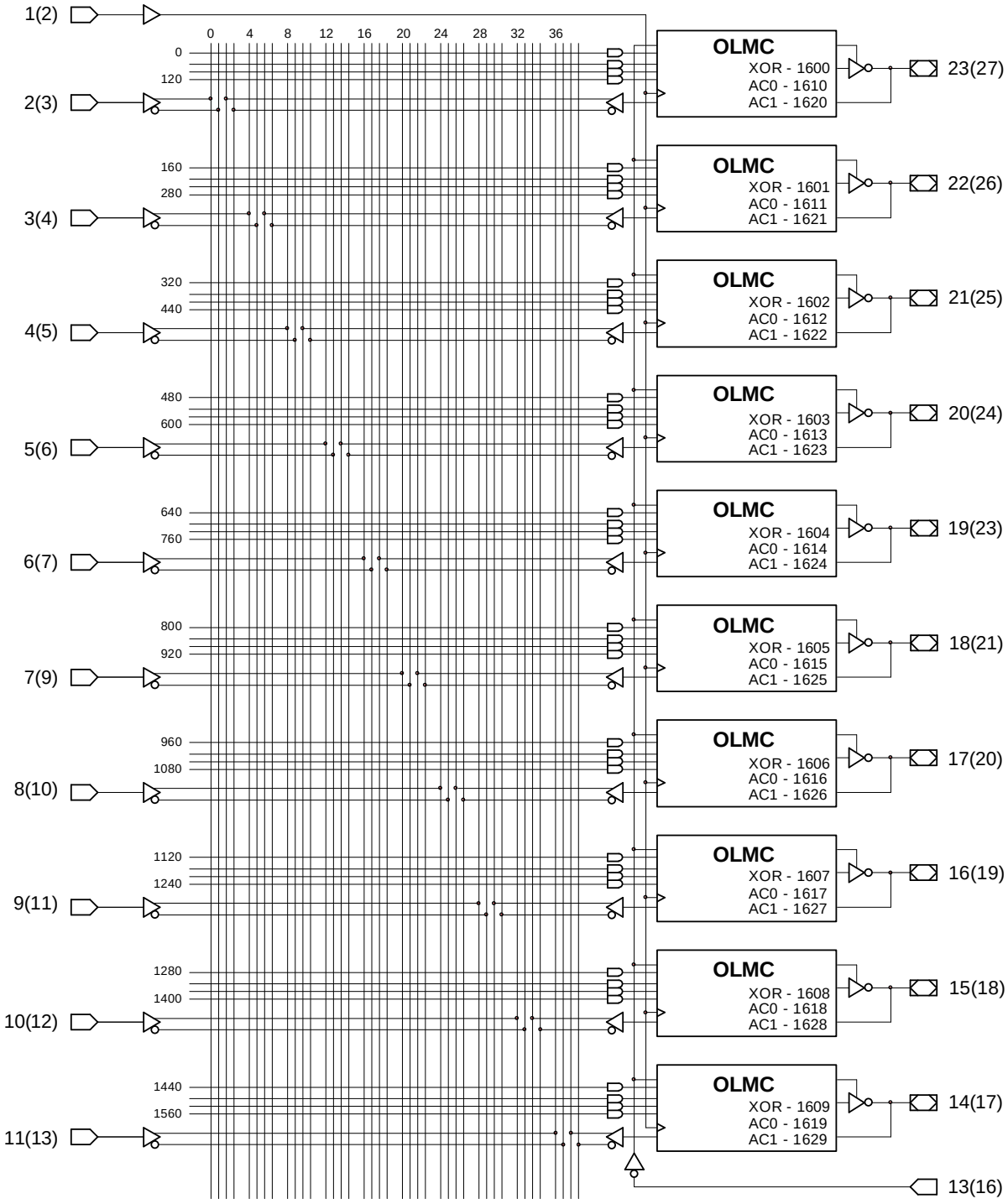


Combinatorial Configuration

- SYN = 0.
- AC0 = 1.
- AC1 = 1.
- XOR = 1 defines Active Low Output.
- XOR = 0 defines Active High Output.
- OE controlled by product term.
- Both pin1(2) and pin 13(16) are not connected to this configuration.

FEEDBACK MODE LOGIC DIAGRAM

DIP (PLCC) Package Pinouts



40-USER ELECTRONIC SIGNATURE FUSES

1631, 1632, ...			.... 1669, 1670
Byte4	Byte3	.... Byte1	Byte0

SYN - 1630

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage Vcc ..... –0.5 to+7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1.Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		V_{SS} – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	V_{CC}+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A= 25°C	–50	—	–150	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -10/-15/-20	—	75	90	mA

1) The leakage current is due to the internal pull-up on all input and I/O pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at V_{CC} = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	COM -10		COM -15		COM -20		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	3	10	3	15	3	20	ns
t_{co}	A	Clock to Output Delay	2	7	2	8	2	10	ns
t_{cf}[2]	—	Clock to Feedback Delay	—	4	—	4	—	4	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	6	—	8	—	10	—	ns
t_{h}	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
f_{max}[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	76.9	—	62.5	—	50	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	100	—	83.3	—	71.4	—	MHz
	A	Maximum Clock Frequency with No Feedback	100	—	83.3	—	71.4	—	MHz
t_{wh}	—	Clock Pulse Duration, High	4	—	6	—	7	—	ns
t_{wl}	—	Clock Pulse Duration, Low	4	—	6	—	7	—	ns
t_{en}	B	Input or I/O to Output Enabled	3	10	3	15	3	20	ns
	B	$\overline{OE}$ to Output Enabled	2	9	2	10	2	15	ns
t_{dis}	C	Input or I/O to Output Disabled	3	9	3	15	3	20	ns
	C	$\overline{OE}$ to Output Disabled	2	9	2	10	2	15	ns

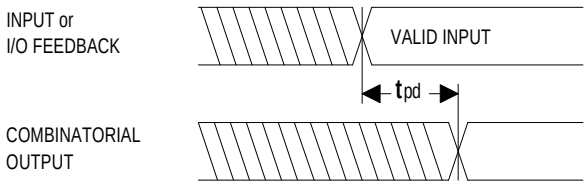
1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Description section.
3) Refer to fmax Description section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

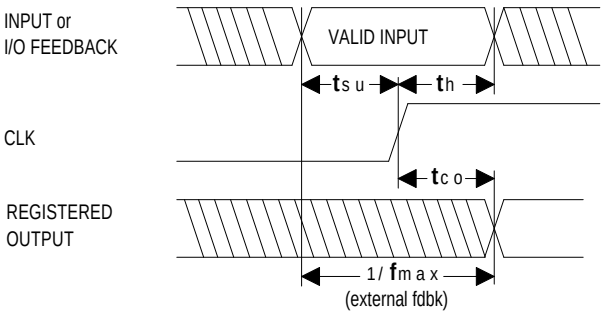
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

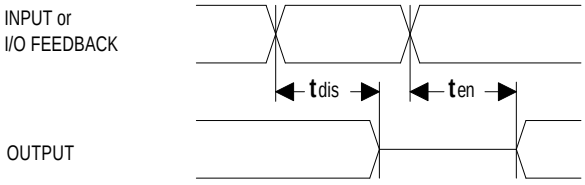
SWITCHING WAVEFORMS



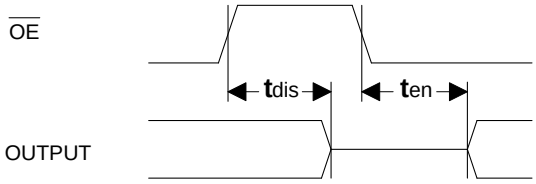
Combinatorial Output



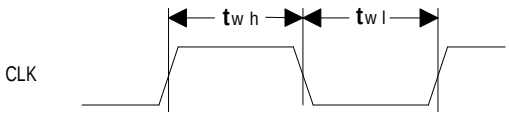
Registered Output



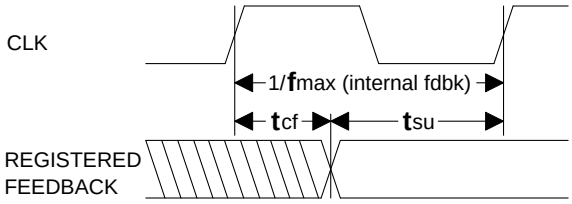
Input or I/O Feedback to Enable/Disable



$\overline{OE}$ to Output Enable/Disable

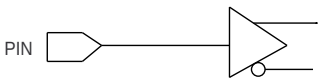


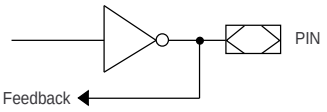
Clock Width

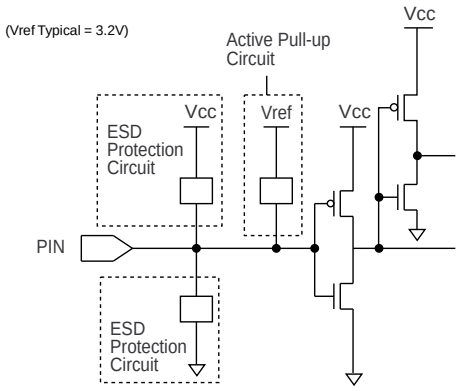


fmax with Feedback

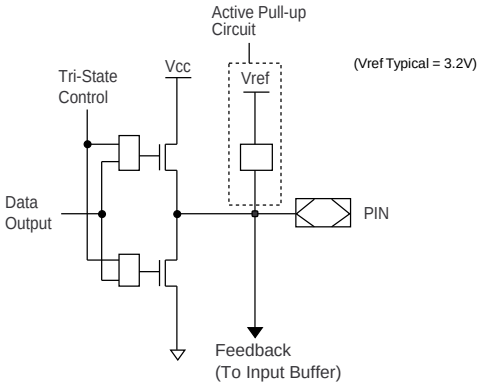
INPUT/OUTPUT EQUIVALENT SCHEMATICS





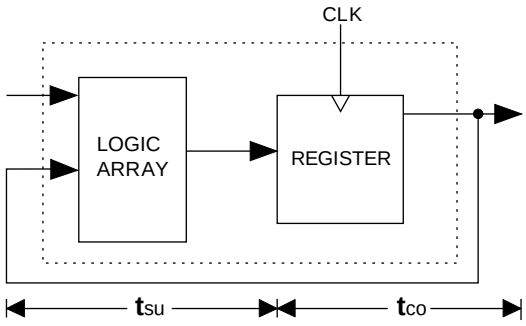


Typical Input



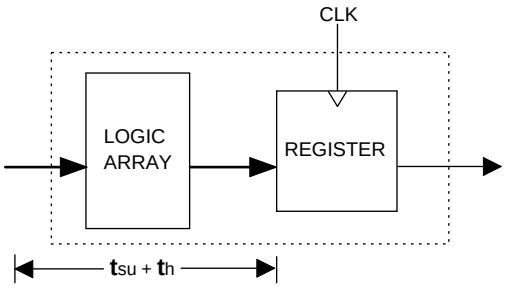
Typical Output

fmax DESCRIPTIONS



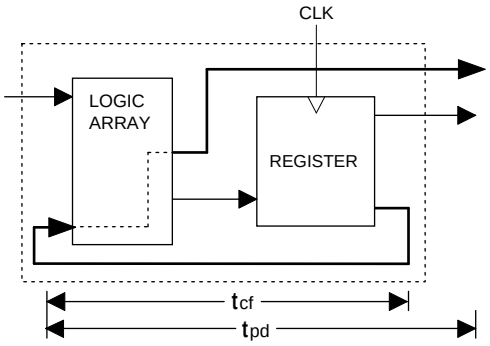
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

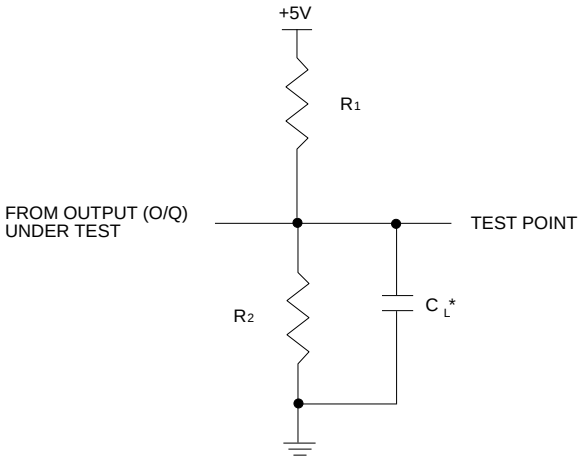
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature word is provided in every GAL20XV10 device. It contains 40 bits of reprogrammable memory that contains user defined data. Some uses include user ID codes, revision numbers, pattern identification or inventory control codes. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature bits, if programmed to any value other then zero(0) will alter the checksum of the device.

SECURITY CELL

A security cell is provided in every GAL20XV10 device as a deterrent to unauthorized copying of the device pattern. Once programmed, this cell prevents further read access of the device pattern information. This cell can be only be reset by reprogramming the device. The original pattern can never be examined once this cell is programmed. The Electronic Signature is always available regardless of the security cell state.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes less than a second. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

LATCH-UP PROTECTION

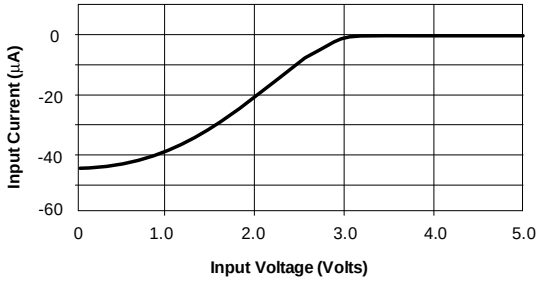
GAL20XV10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

GAL20XV10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

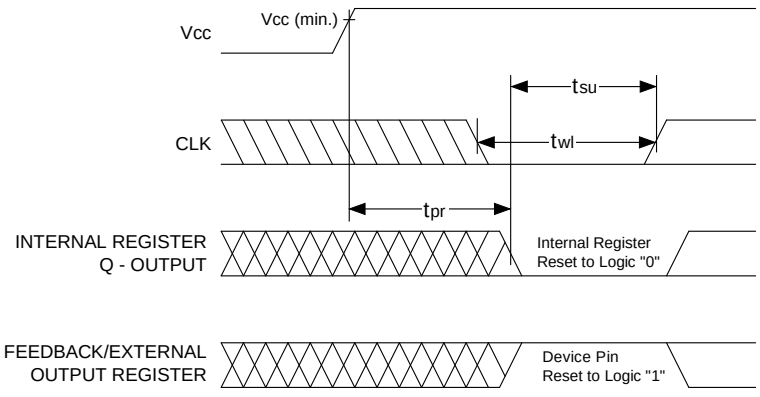
GAL20XV10 input buffers have active pull-ups within their input structure. This pull-up will cause any un-terminated input or I/O to float to a TTL high (logical 1). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce Icc for the device.

Typical Input Pull-up Characteristic



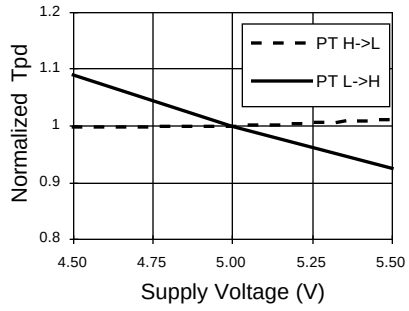
POWER-UP RESET

Circuitry within the GAL20XV10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20XV10. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

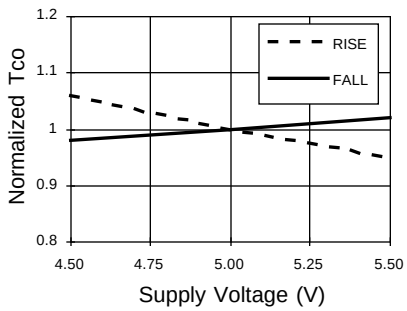


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

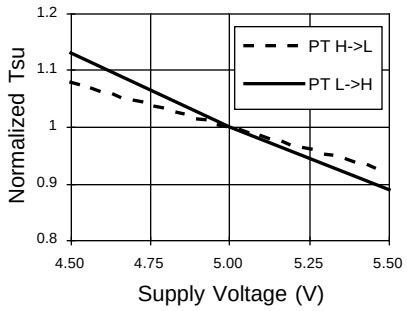
Normalized Tpd vs Vcc



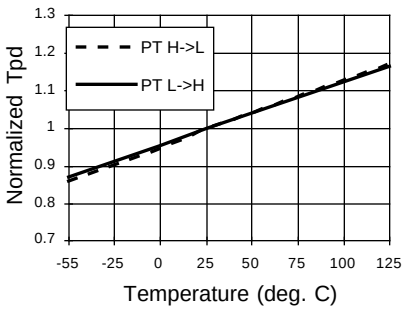
Normalized Tco vs Vcc



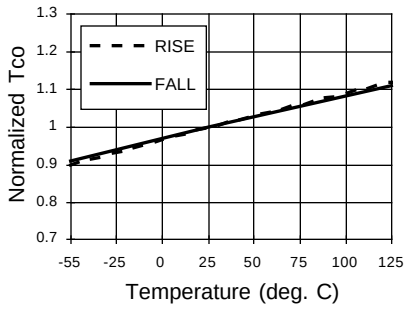
Normalized Tsu vs Vcc



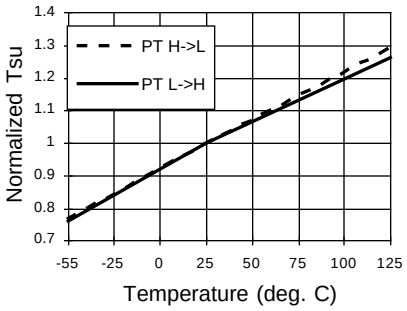
Normalized Tpd vs Temp



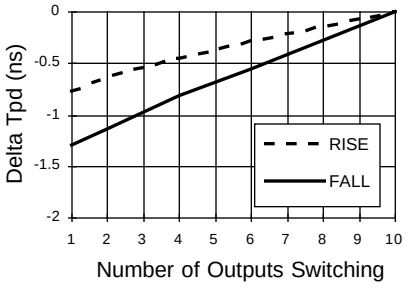
Normalized Tco vs Temp



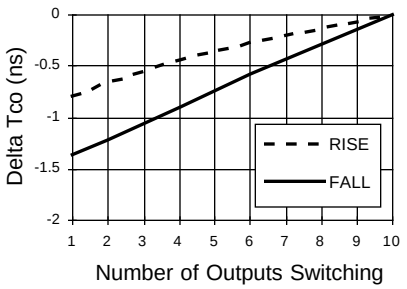
Normalized Tsu vs Temp



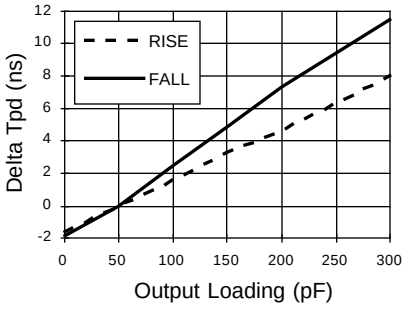
Delta Tpd vs # of Outputs Switching



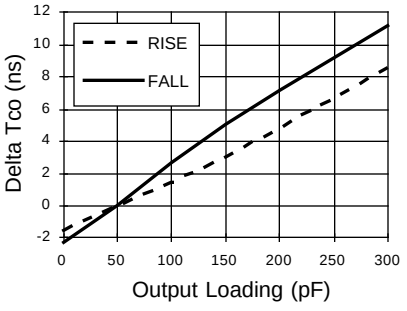
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

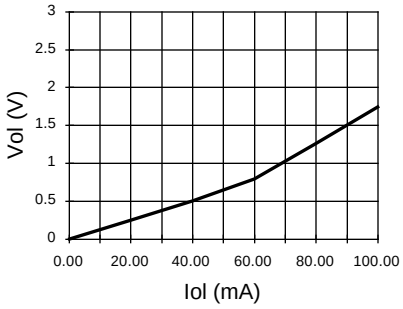


Delta Tco vs Output Loading

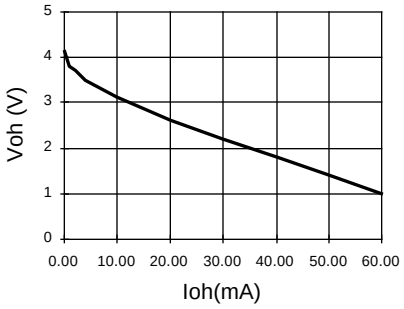


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

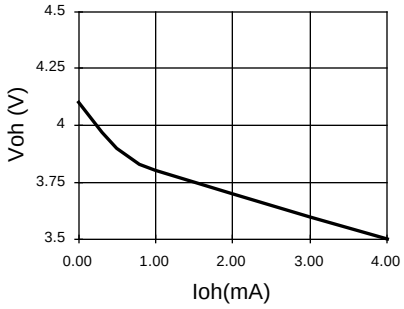
Vol vs Iol



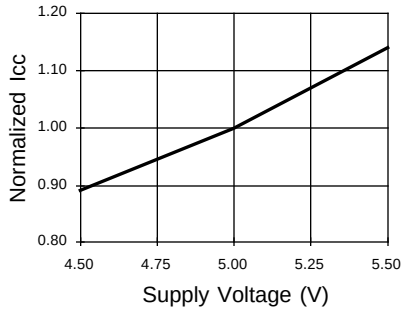
Voh vs Ioh



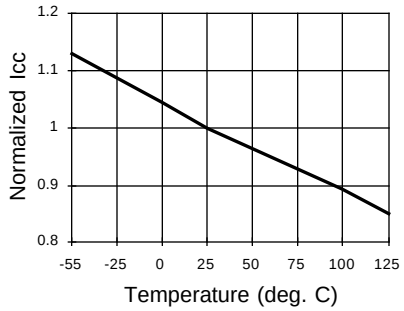
Voh vs Ioh



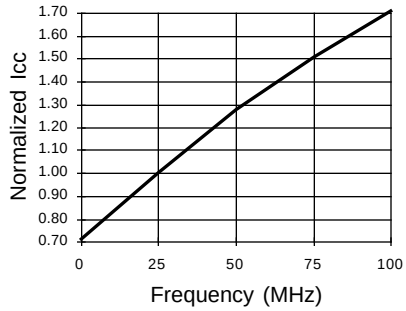
Normalized Icc vs Vcc



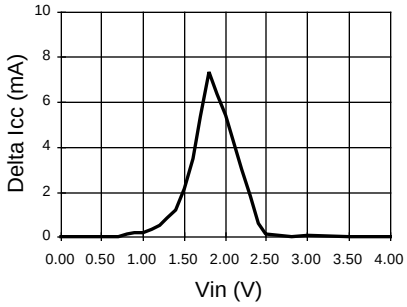
Normalized Icc vs Temp



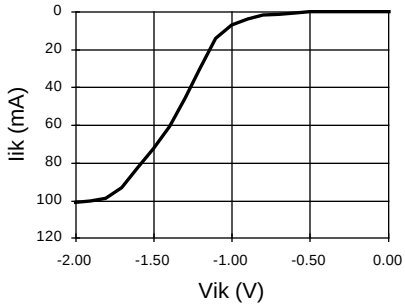
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



GAL22LV10

Low Voltage E²CMOS PLD Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 4 ns Maximum Propagation Delay**
  - **— Fmax = 250 MHz**
  - **— 3 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **3.3V LOW VOLTAGE 22V10 ARCHITECTURE**
  - **— JEDEC-Compatible 3.3V Interface Standard**
  - **— Interfaces with Standard 5V TTL Devices (GAL22LV10C)**
- **ACTIVE PULL-UPS ON ALL PINS (GAL22LV10D)**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— Glue Logic for 3.3V Systems**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

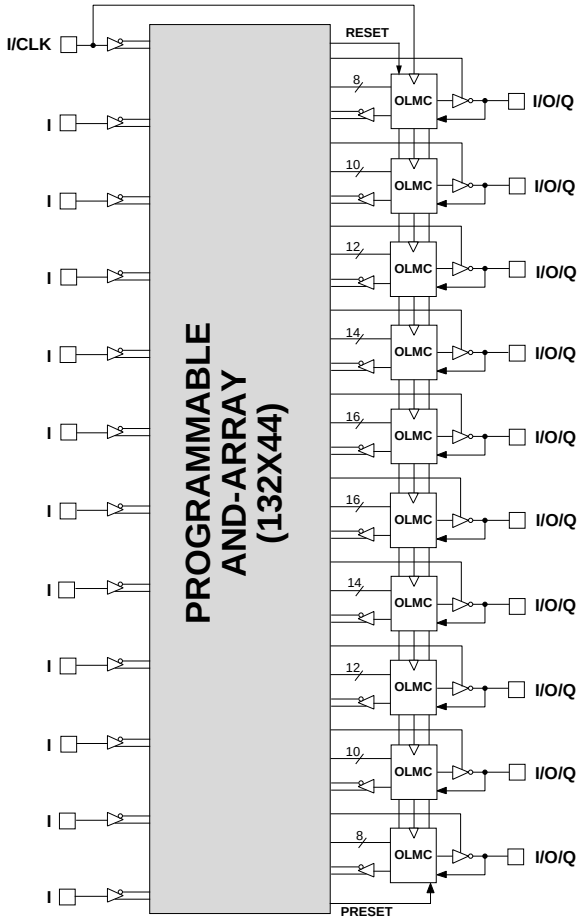
DESCRIPTION

The GAL22LV10D, at 4 ns maximum propagation delay time, provides the highest speed performance available in the PLD market. The GAL22LV10C can interface with both 3.3V and 5V signal levels. The GAL22LV10 is manufactured using Lattice Semiconductor's advanced 3.3V E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user.

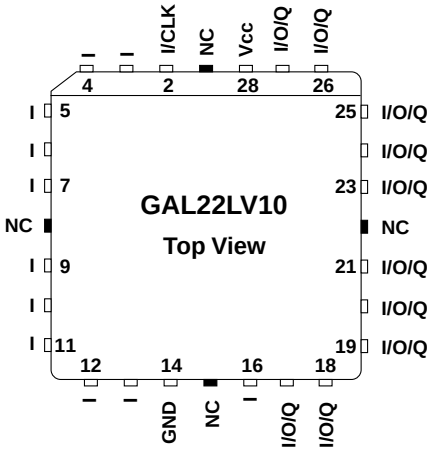
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

PLCC



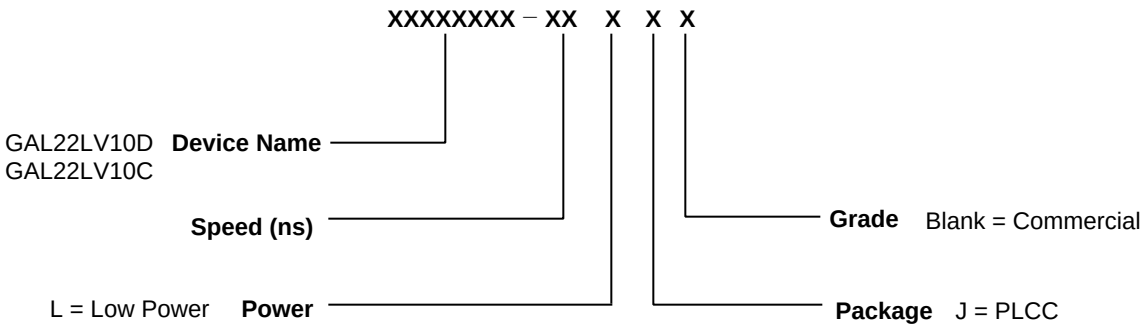
LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL22LV10 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
4	3	3	130	GAL22LV10D-4LJ	28-Lead PLCC
5	3.5	3.5	130	GAL22LV10D-5LJ	28-Lead PLCC
7.5	6.5	5	75	GAL22LV10C-7LJ	28-Lead PLCC
10	7.5	6.5	75	GAL22LV10C-10LJ	28-Lead PLCC
15	10	10	75	GAL22LV10C-15LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



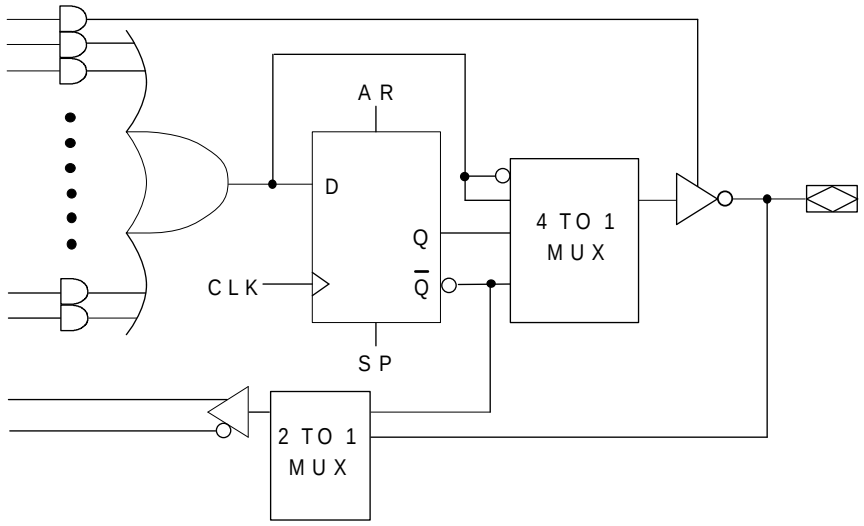
OUTPUT LOGIC MACROCELL (OLMC)

The GAL22LV10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 17 and 27), two have ten product terms (pins 18 and 26), two have twelve product terms (pins 19 and 25), two have fourteen product terms (pins 20 and 24), and two OLMCs have sixteen product terms (pins 21 and 23). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL22LV10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL22LV10 OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL22LV10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

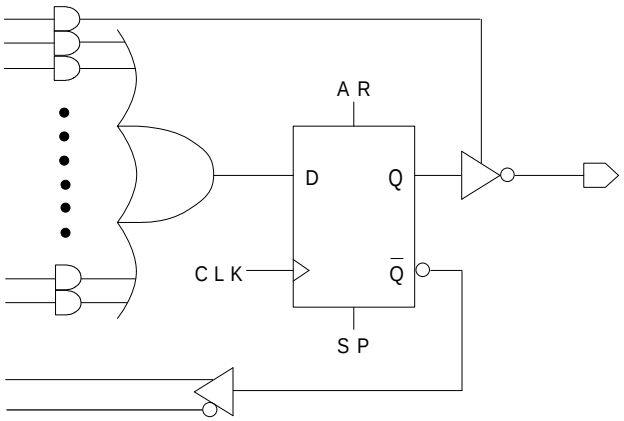
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

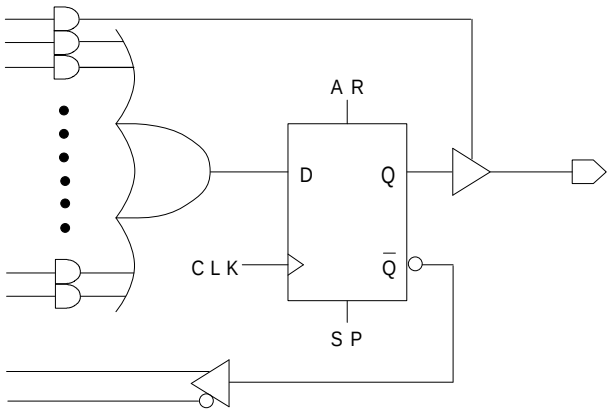
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE



ACTIVE LOW

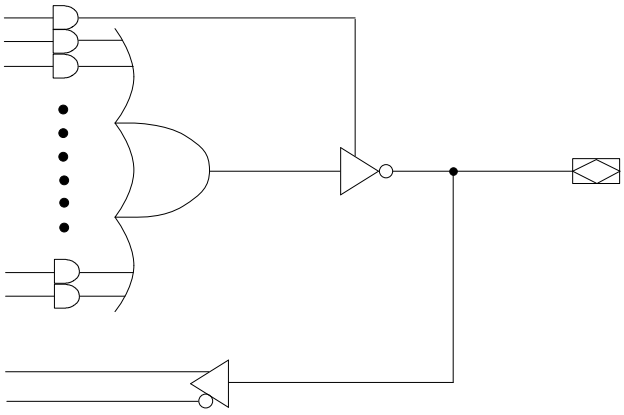
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

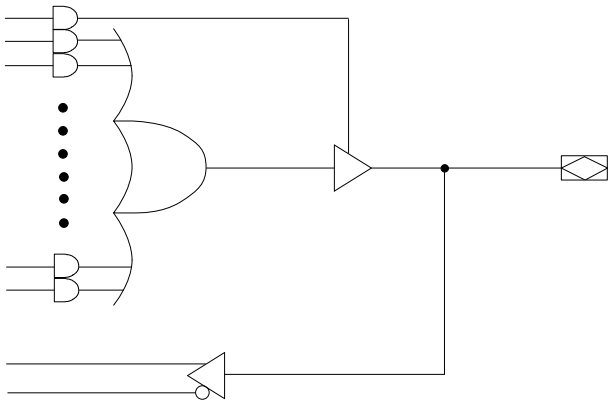
$S_0 = 1$
$S_1 = 0$

COMBINATORIAL MODE



ACTIVE LOW

$S_0 = 0$
$S_1 = 1$

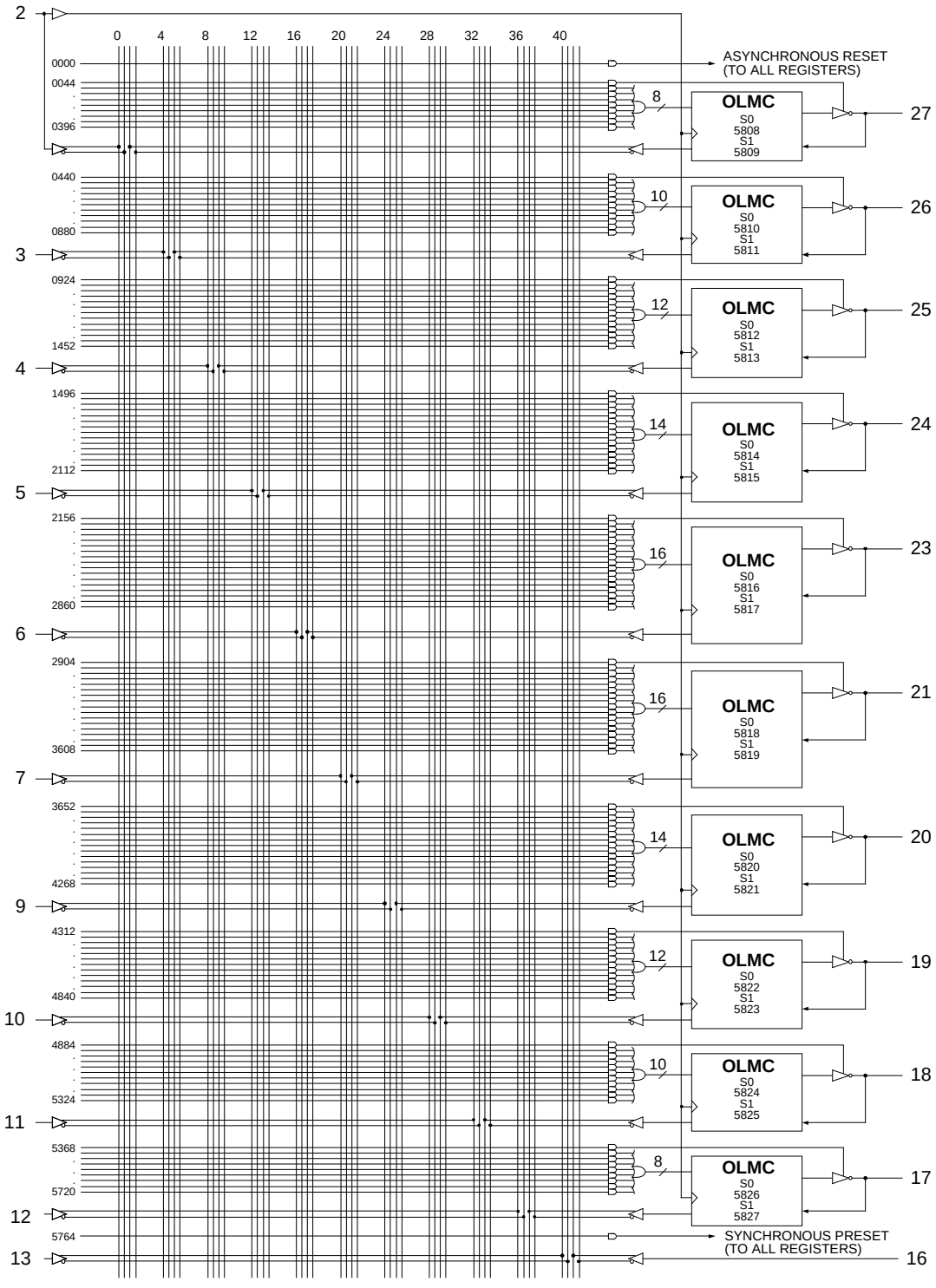


ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

GAL22LV10 LOGIC DIAGRAM / JEDEC FUSE MAP

PLCC Package Pinout



5828, 5829 ... Electronic Signature ... 5890, 5891							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
MSB							LSB

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +4.6V
Input voltage applied ..... –0.5 to +4.6V
Off-state output voltage applied ..... –0.5 to +4.6V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.3	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+0.5	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$Vcc\text{-}0.2V \le V_{IN} \le V_{CC}$	—	—	10	µA
		$Vcc \le V_{IN} \le$ 4.6V	—	—	20	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.4	V
		I_{OL} = 500µA Vin = V_{IL} or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -100µA Vin = V_{IL} or V_{IH}	Vcc-0.2	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	–8	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = 0.5V T_A = 25°C	–15	—	–80	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0V V_{IH} = 3.0V Unused Inputs at V_{IL} f_{toggle} = 1MHz Outputs Open	—	90	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 3.3V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -4 MIN.	COM -4 MAX.	COM -5 MIN.	COM -5 MAX.	UNITS
tpd[2]	A	Input or I/O to Combinational Output	1	4	1	5	ns
tco[2]	A	Clock to Output Delay	1	3	1	3.5	ns
tcf[3]	—	Clock to Feedback Delay	—	2.5	—	3	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	3	—	3.5	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[4]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	167	—	143	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	182	—	154	—	MHz
	A	Maximum Clock Frequency with No Feedback	250	—	200	—	MHz
twh[4]	—	Clock Pulse Duration, High	2	—	2.5	—	ns
twl[4]	—	Clock Pulse Duration, Low	2	—	2.5	—	ns
ten	B	Input or I/O to Output Enabled	1	5	1	6	ns
tdis	C	Input or I/O to Output Disabled	1	5	1	6	ns
tar	A	Input or I/O to Asynchronous Reset of Register	1	4.5	1	5.5	ns
tarw	—	Asynchronous Reset Pulse Duration	4.5	—	5.5	—	ns
tarr	—	Asynchronous Reset to Clock↑ Recovery Time	3.5	—	4	—	ns
tspr	—	Synchronous Preset to Clock↑ Recovery Time	3.5	—	4	—	ns

1) Refer to Switching Test Conditions section.
2) Minimum values for tpd and tco are not 100% tested but established by characterization.
3) Calculated from fmax with internal feedback. Refer to fmax Descriptions section.
4) Refer to fmax Descriptions section. Guaranteed by characterization.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TYPICAL*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	5	pF	V_{CC} = 3.3V, V_I = 0V
$C_{I/O}$	I/O Capacitance	5	pF	V_{CC} = 3.3V, $V_{I/O}$ = 0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +5.6V

Input voltage applied ..... -0.5 to +5.6V

Off-state output voltage applied ..... -0.5 to +5.6V

Storage Temperature ..... -65 to 150°C

Ambient Temperature with Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) ..... 0 to +75°C

Supply voltage (V_{CC}) with Respect to Ground ..... +3.0 to +3.6V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	5.25	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CC} - 0.2)V \le V_{IN} \le V_{CC}$	—	—	10	µA
		$V_{CC} \le V_{IN} \le 5.25V$	—	—	30	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.4	V
		I_{OL} = 0.5 mA Vin = V_{IL} or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -0.5 mA Vin = V_{IL} or V_{IH}	Vcc-0.45	—	—	V
		I_{OH} = -100 µA Vin = V_{IL} or V_{IH}	Vcc-0.2	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-4	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = 0.5V T_A = 25°C	-15	—	-60	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.0V V_{IH} = 3.0V f_{toggle} = 1MHz Outputs Open	—	45	75	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.

2) Typical values are at Vcc = 3.3V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM	TEST COND.[1]	DESCRIPTION	COM -7 MIN.	COM -7 MAX.	COM -10 MIN.	COM -10 MAX.	COM -15 MIN.	COM -15 MAX.	UNITS
tpd[2]	A	Input or I/O to Combinatorial Output	2	7.5	2	10	2	15	ns
tco[2]	A	Clock to Output Delay	1	5	1	6.5	1	10	ns
tcf[3]	—	Clock to Feedback Delay	—	3	—	5	—	5	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑	6.5	—	7.5	—	10	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	0	—	ns
fmax[4]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	87	—	71	—	50	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	105	—	80	—	66	—	MHz
	A	Maximum Clock Frequency with No Feedback	125	—	111	—	83	—	MHz
twh	—	Clock Pulse Duration, High	3.5	—	4	—	6	—	ns
twl	—	Clock Pulse Duration, Low	3.5	—	4	—	6	—	ns
ten	B	Input or I/O to Output Enabled	2	10	2	12	2	15	ns
tdis	C	Input or I/O to Output Disabled	2	10	2	12	2	15	ns
tar	A	Input or I/O to Asynch. Reset of Reg.	2	11	2	13	2	20	ns
tarw	—	Asynch. Reset Pulse Duration	7	—	8	—	12	—	ns
tarr	—	Asynch. Reset to Clk↑ Recovery Time	7	—	8	—	10	—	ns
tspr	—	Synch. Preset to Clk↑ Recovery Time	8	—	10	—	10	—	ns

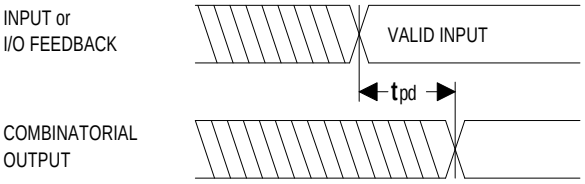
1) Refer to Switching Test Conditions section.
2) Minimum values for **t**pd and **t**co are not 100% tested but established by characterization.
3) Calculated from **f**max with internal feedback. Refer to fmax Description section.
4) Refer to fmax Description section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

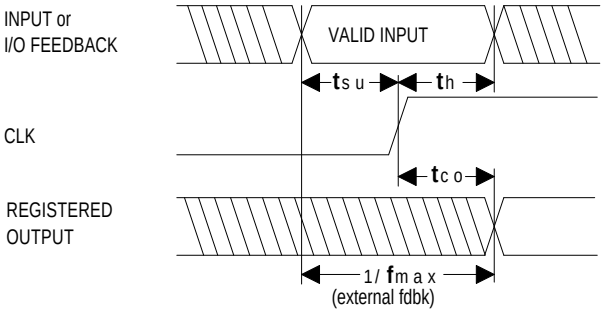
SYMBOL	PARAMETER	TYPICAL*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 3.3V, V_I = 0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 3.3V, $V_{I/O}$ = 0V

*Guaranteed but not 100% tested.

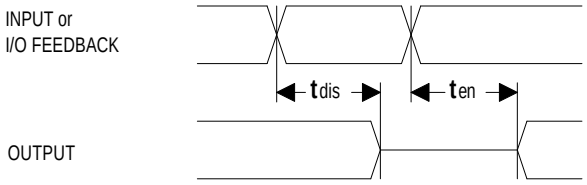
SWITCHING WAVEFORMS



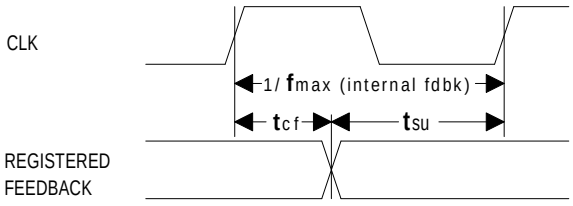
Combinatorial Output



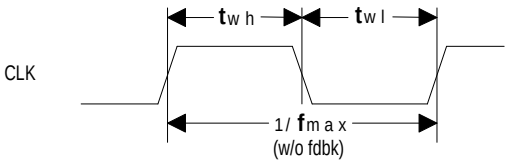
Registered Output



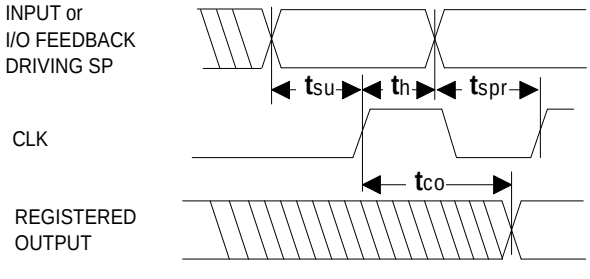
Input or I/O to Output Enable/Disable



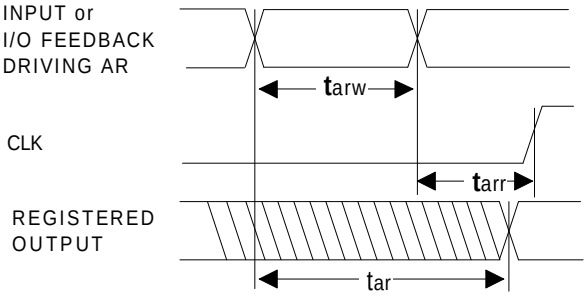
fmax with Feedback



Clock Width

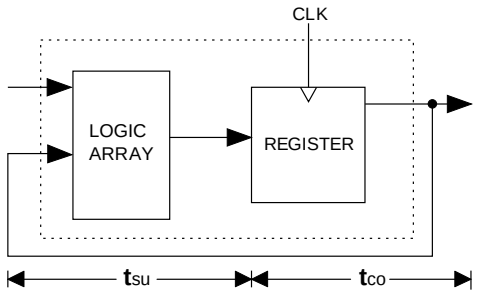


Synchronous Preset



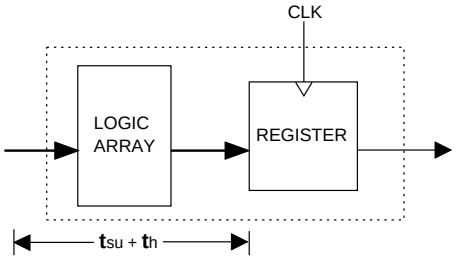
Asynchronous Reset

fmax DESCRIPTIONS



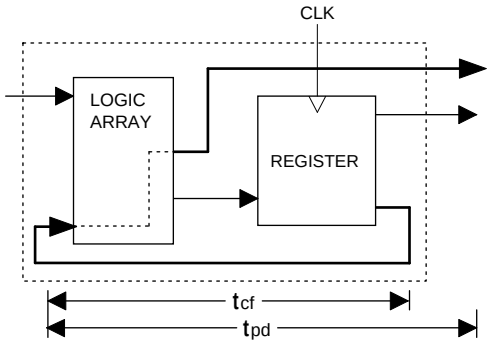
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

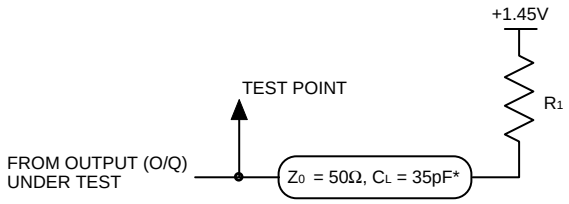
Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

GAL22LV10D: SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	1.5ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Output Load Conditions (see figure)

Test Condition		R_1	C_L
A		50Ω	35pF
B	High Z to Active High at 1.9V	50Ω	35pF
	High Z to Active Low at 1.0V	50Ω	35pF
C	Active High to High Z at 1.9V	50Ω	35pF
	Active Low to High Z at 1.0V	50Ω	35pF



*C_L includes test fixture and probe capacitance.

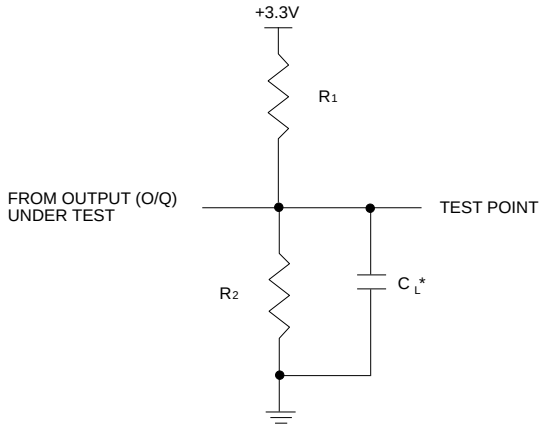
GAL22LV10C: SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	2.0ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		316Ω	348Ω	35pF
B	Active High	316Ω	348Ω	35pF
	Active Low	316Ω	348Ω	35pF
C	Active High	316Ω	348Ω	5pF
	Active Low	316Ω	348Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided in every GAL22LV10 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

The electronic signature is an additional feature not present in other manufacturers' 22V10 devices. To use the extra feature of the user-programmable electronic signature it is necessary to choose a Lattice Semiconductor 22V10 device type when compiling a set of logic equations. In addition, many device programmers have two separate selections for the device, typically a GAL22LV10 and a GAL22V10-UES (UES = User Electronic Signature) or GAL22V10-ES. This allows users to maintain compatibility with existing 22V10 designs, while still having the option to use the GAL device's extra feature.

The JEDEC map for the GAL22LV10 contains the 64 extra fuses for the electronic signature, for a total of 5892 fuses. However, the GAL22LV10 device can still be programmed with a standard 22V10 JEDEC map (5828 fuses) with any qualified device programmer.

SECURITY CELL

A security cell is provided in every GAL22LV10 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL22LV10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

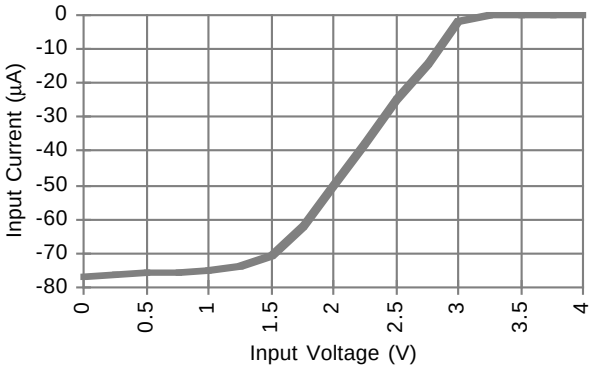
The GAL22LV10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

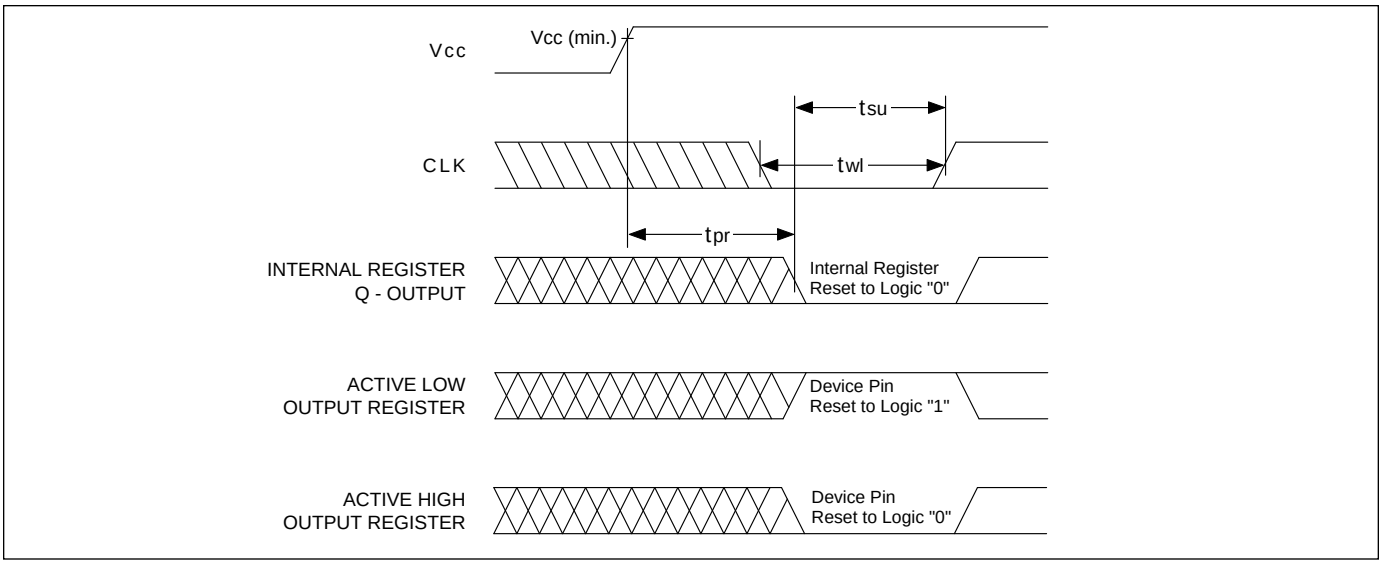
GAL22LV10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The input and I/O pins on the GAL22LV10D also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device. (See equivalent input and I/O schematics on the following page.)

Typical Input Pull-up Characteristic

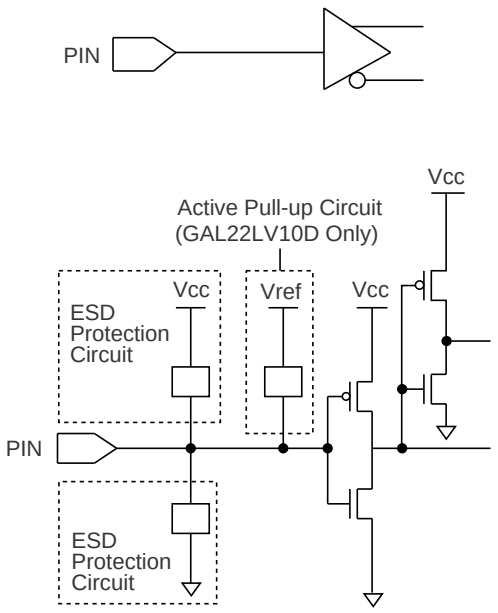


POWER-UP RESET



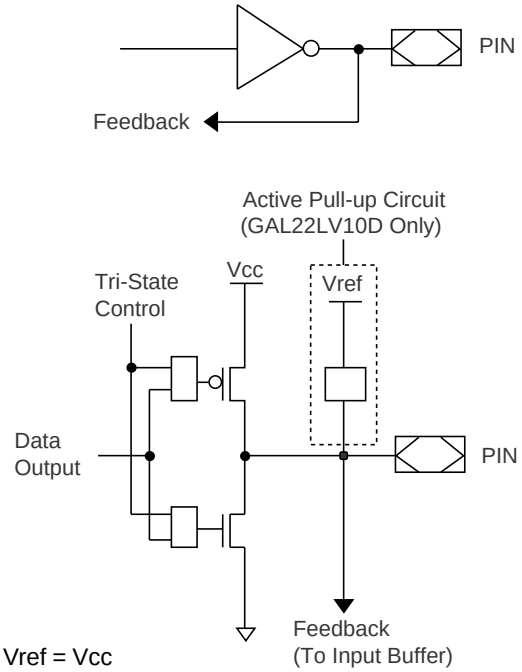
Circuitry within the GAL22V10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL22V10. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typ. Vref = Vcc

Typical Input

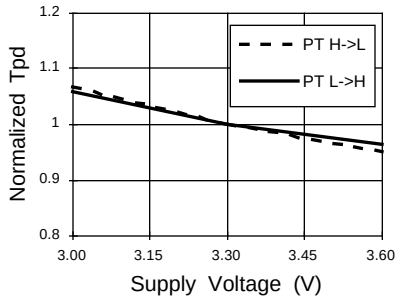


Typ. Vref = Vcc

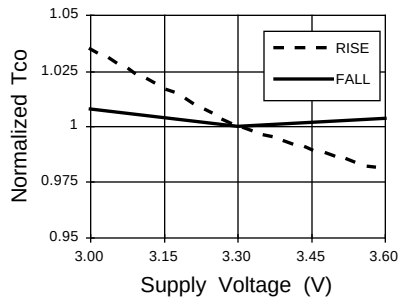
Typical Output

GAL22LV10D: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

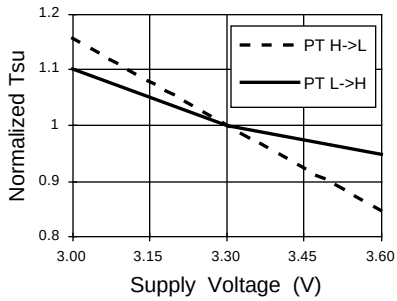
Normalized Tpd vs Vcc



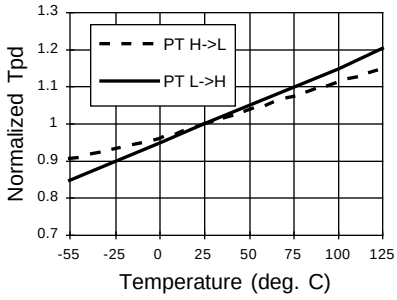
Normalized Tco vs Vcc



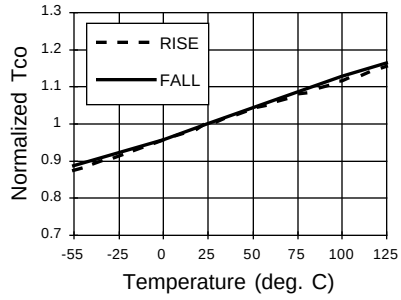
Normalized Tsu vs Vcc



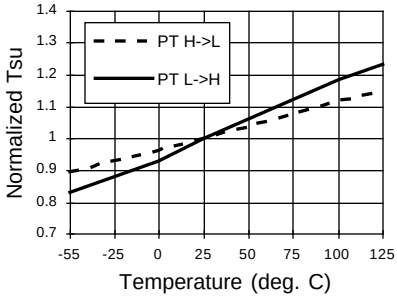
Normalized Tpd vs Temp



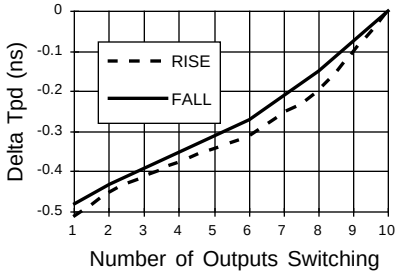
Normalized Tco vs Temp



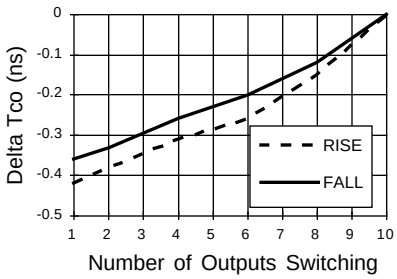
Normalized Tsu vs Temp



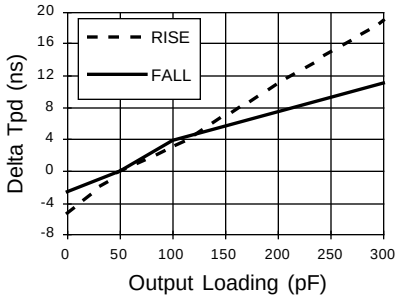
Delta Tpd vs # of Outputs Switching



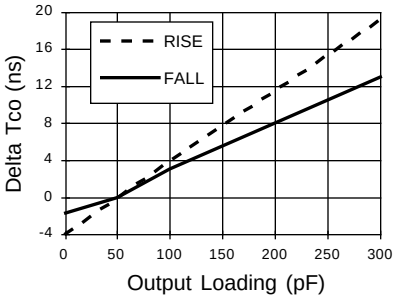
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

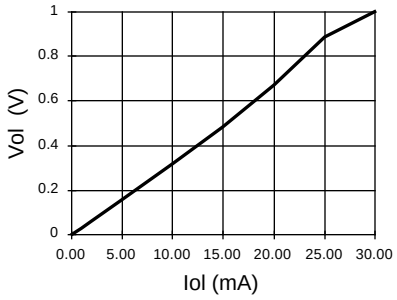


Delta Tco vs Output Loading

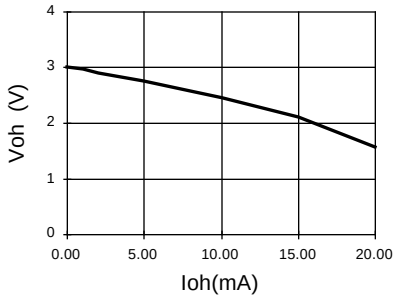


GAL22LV10D: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

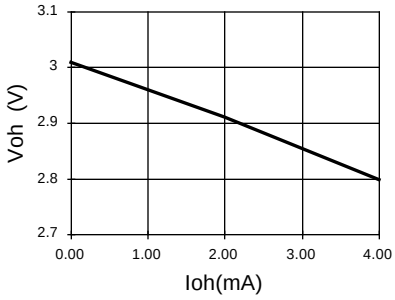
Vol vs Iol



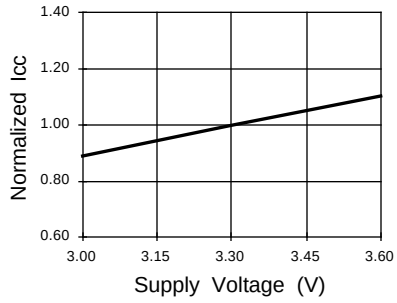
Voh vs Ioh



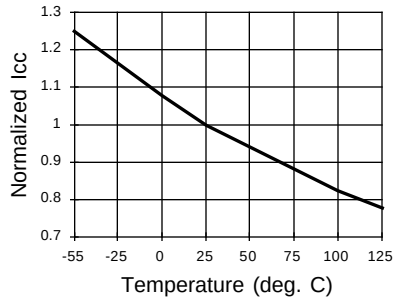
Voh vs Ioh



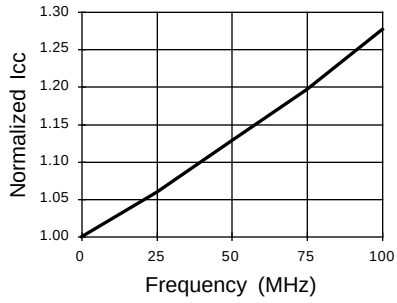
Normalized Icc vs Vcc



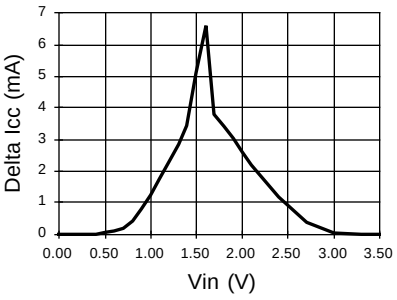
Normalized Icc vs Temp



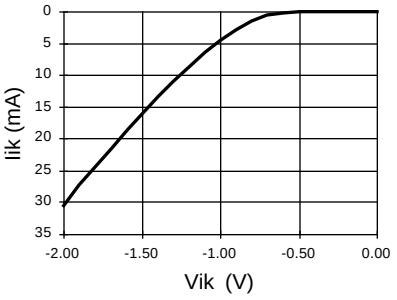
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

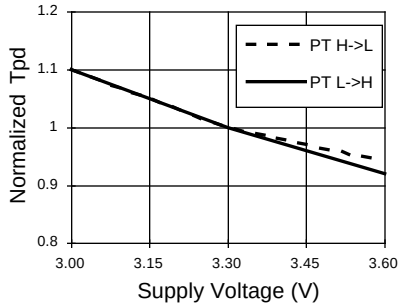


Input Clamp (Vik)

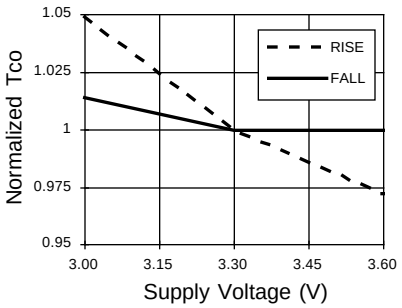


GAL22LV10C: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

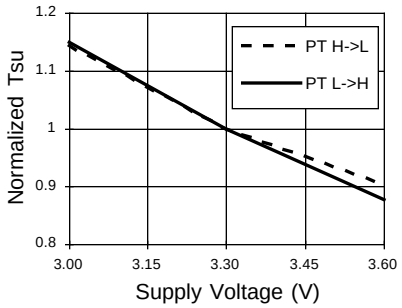
Normalized Tpd vs Vcc



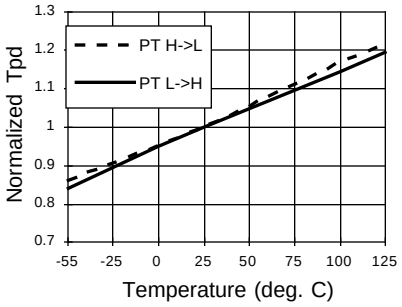
Normalized Tco vs Vcc



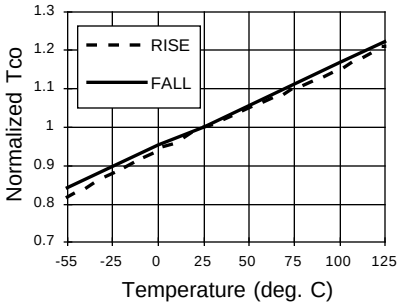
Normalized Tsu vs Vcc



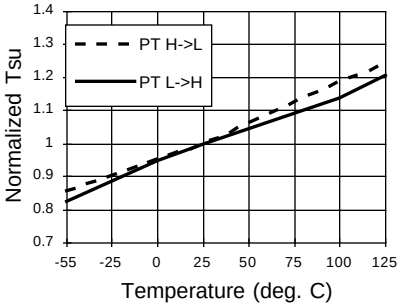
Normalized Tpd vs Temp



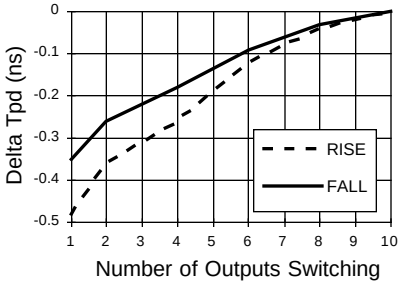
Normalized Tco vs Temp



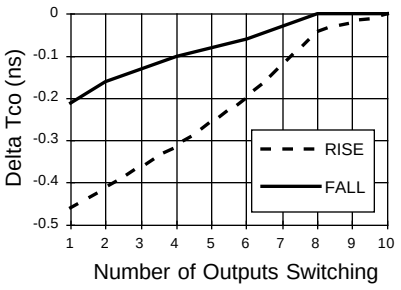
Normalized Tsu vs Temp



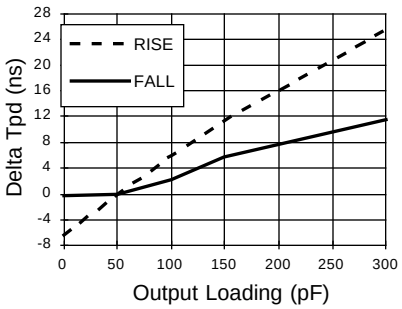
Delta Tpd vs # of Outputs Switching



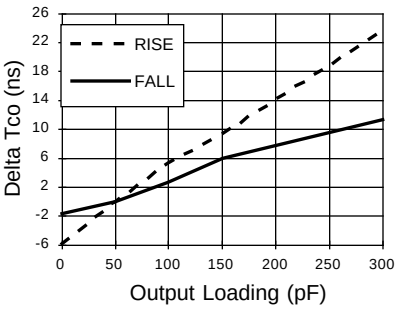
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

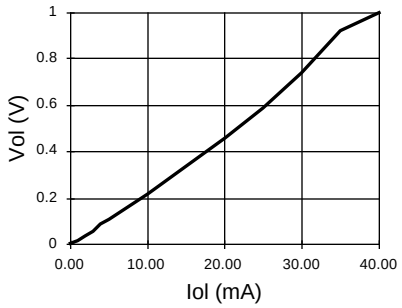


Delta Tco vs Output Loading

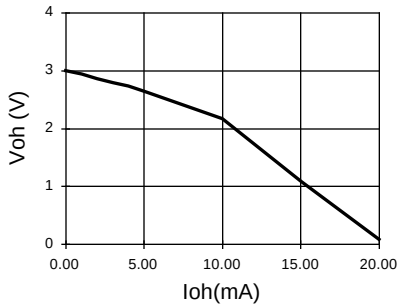


GAL22LV10C: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

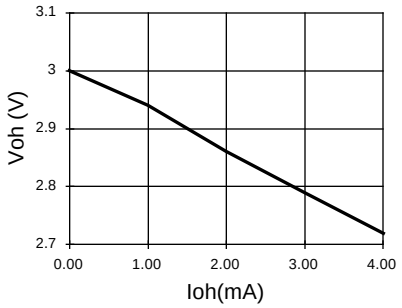
Vol vs Iol



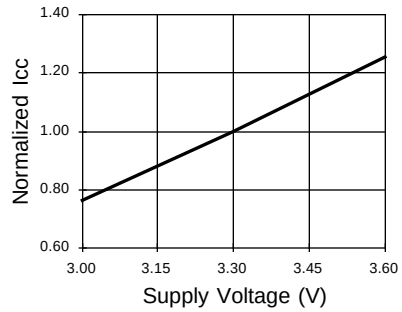
Voh vs Ioh



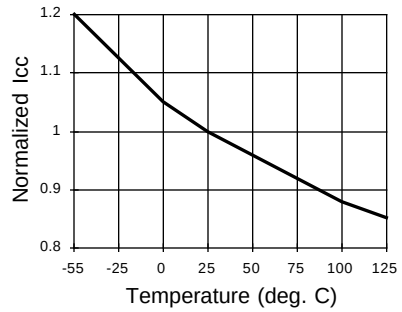
Voh vs Ioh



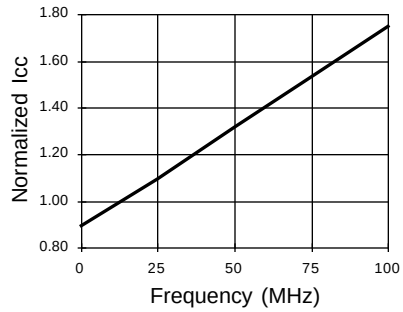
Normalized Icc vs Vcc



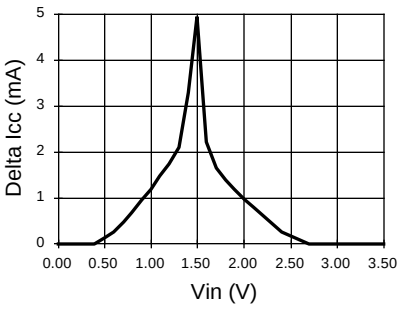
Normalized Icc vs Temp



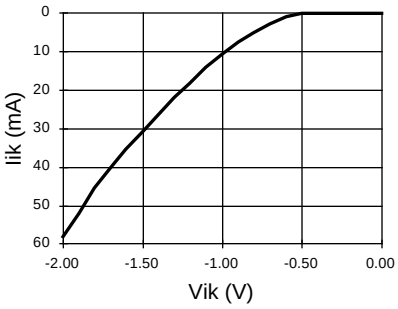
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



GAL22V10

High Performance E²CMOS PLD
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 5 ns Maximum Propagation Delay**
  - **— Fmax = 200 MHz**
  - **— 4 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **ACTIVE PULL-UPS ON ALL PINS**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
  - **— Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVCMOS 22V10 Devices**
- **50% to 75% REDUCTION IN POWER VERSUS BIPOLAR**
  - **— 90mA Typical Icc on Low Power Device**
  - **— 45mA Typical Icc on Quarter Power Device**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

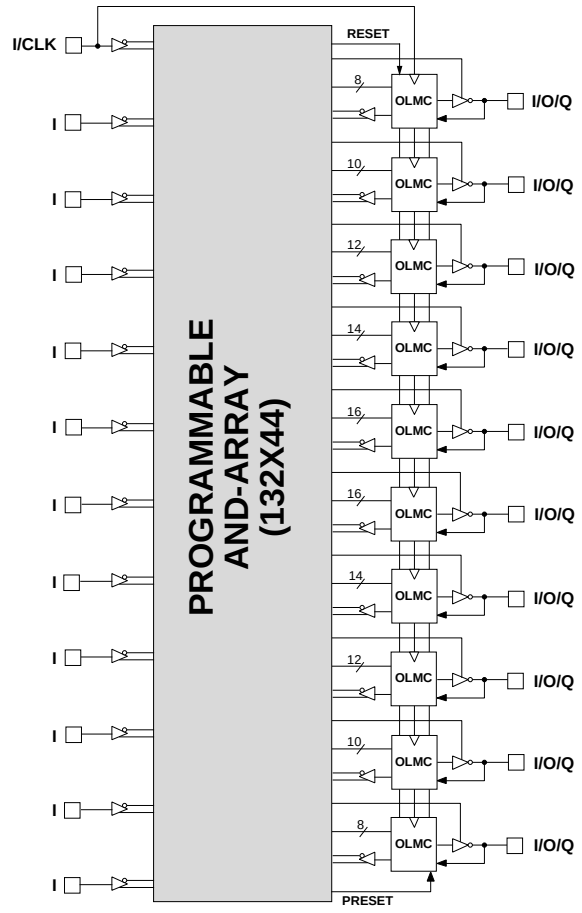
DESCRIPTION

The GAL22V10C, at 5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance available of any 22V10 device on the market. CMOS circuitry allows the GAL22V10 to consume much less power when compared to bipolar 22V10 devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

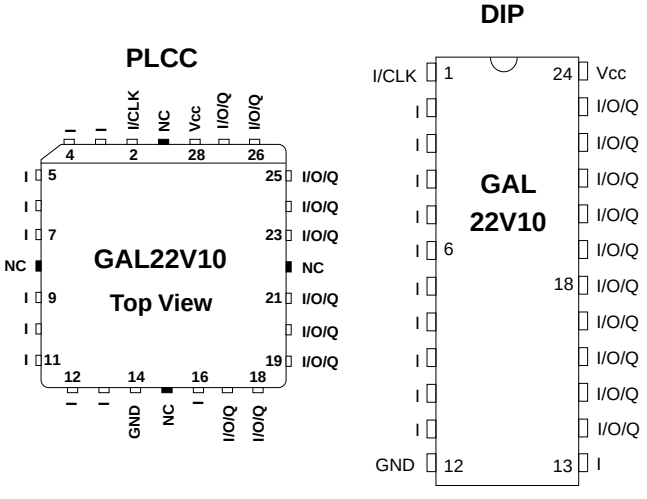
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10 is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL22V10 ORDERING INFORMATION

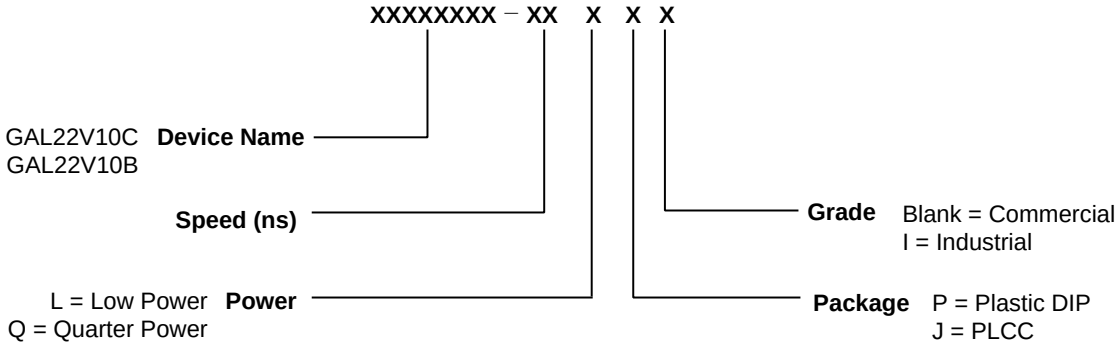
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
5	3	4	150	GAL22V10C-5LJ	28-Lead PLCC
7.5	5	4.5	140	GAL22V10C-7LP	24-Pin Plastic DIP
	4.5	4.5	140	GAL22V10C-7LJ	28-Lead PLCC
	6.5	5	140	GAL22V10B-7LP	24-Pin Plastic DIP
			140	GAL22V10B-7LJ	28-Lead PLCC
10	7	7	130	GAL22V10C-10LP	24-Pin Plastic DIP
			130	GAL22V10C-10LJ	28-Lead PLCC
			130	GAL22V10B-10LP	24-Pin Plastic DIP
			130	GAL22V10B-10LJ	28-Lead PLCC
15	10	8	55	GAL22V10B-15QP	24-Pin Plastic DIP
			55	GAL22V10B-15QJ	28-Lead PLCC
			130	GAL22V10B-15LP	24-Pin Plastic DIP
			130	GAL22V10B-15LJ	28-Lead PLCC
25	15	15	55	GAL22V10B-25QP	24-Pin Plastic DIP
			55	GAL22V10B-25QJ	28-Lead PLCC
			90	GAL22V10B-25LP	24-Pin Plastic DIP
			90	GAL22V10B-25LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	5	4.5	160	GAL22V10C-7LPI	24-Pin Plastic DIP
	4.5	4.5	160	GAL22V10C-7LJI	28-Lead PLCC
10	7	7	160	GAL22V10C-10LPI	24-Pin Plastic DIP
			160	GAL22V10C-10LJI	28-Lead PLCC
15	10	8	150	GAL22V10B-15LPI	24-Pin Plastic DIP
			150	GAL22V10B-15LJI	28-Lead PLCC
20	14	10	150	GAL22V10B-20LPI	24-Pin Plastic DIP
			150	GAL22V10B-20LJI	28-Lead PLCC
25	15	15	150	GAL22V10B-25LPI	24-Pin Plastic DIP
			150	GAL22V10B-25LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



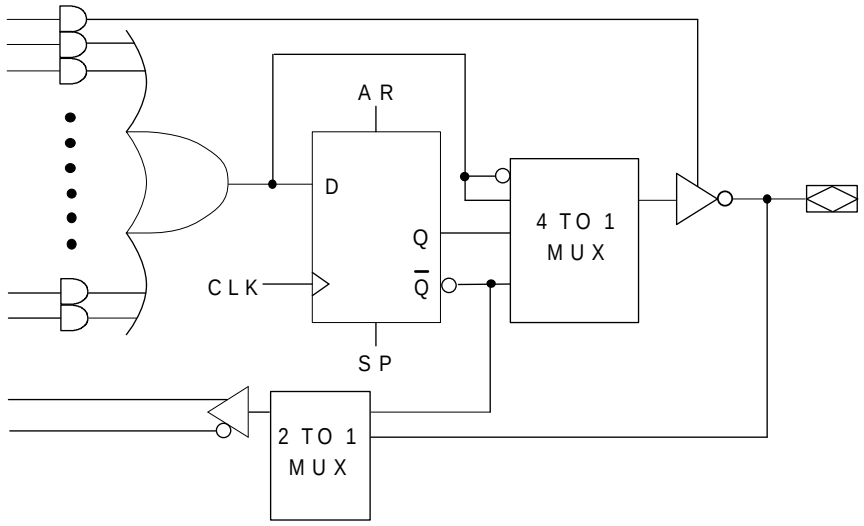
OUTPUT LOGIC MACROCELL (OLMC)

The GAL22V10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 14 and 23, DIP pinout), two have ten product terms (pins 15 and 22), two have twelve product terms (pins 16 and 21), two have fourteen product terms (pins 17 and 20), and two OLMCs have sixteen product terms (pins 18 and 19). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL22V10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL22V10 OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL22V10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

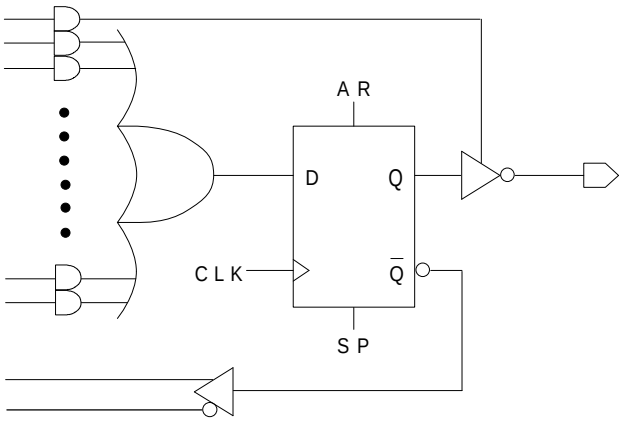
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

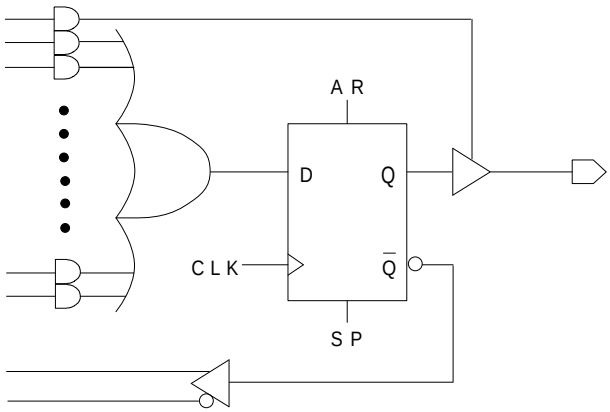
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE



ACTIVE LOW

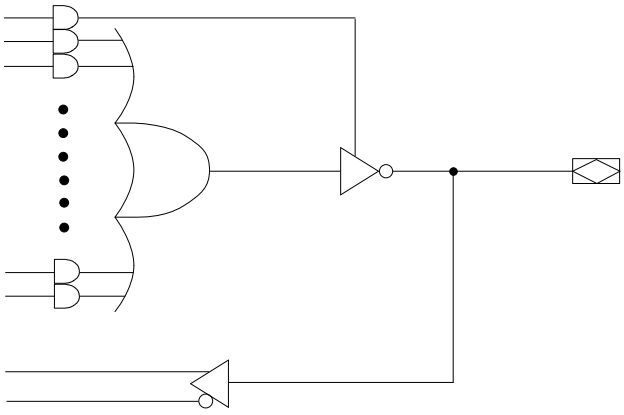
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

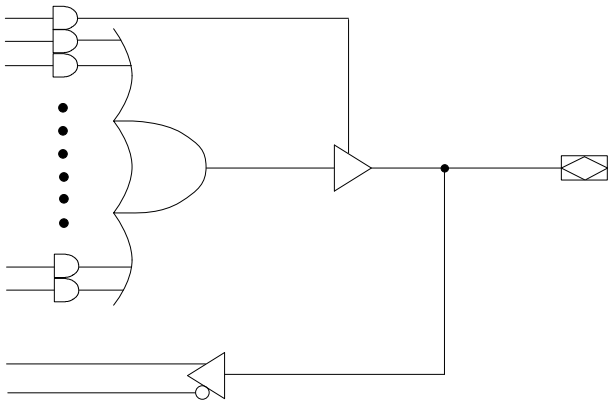
$S_0 = 1$
$S_1 = 0$

COMBINATORIAL MODE



ACTIVE LOW

$S_0 = 0$
$S_1 = 1$

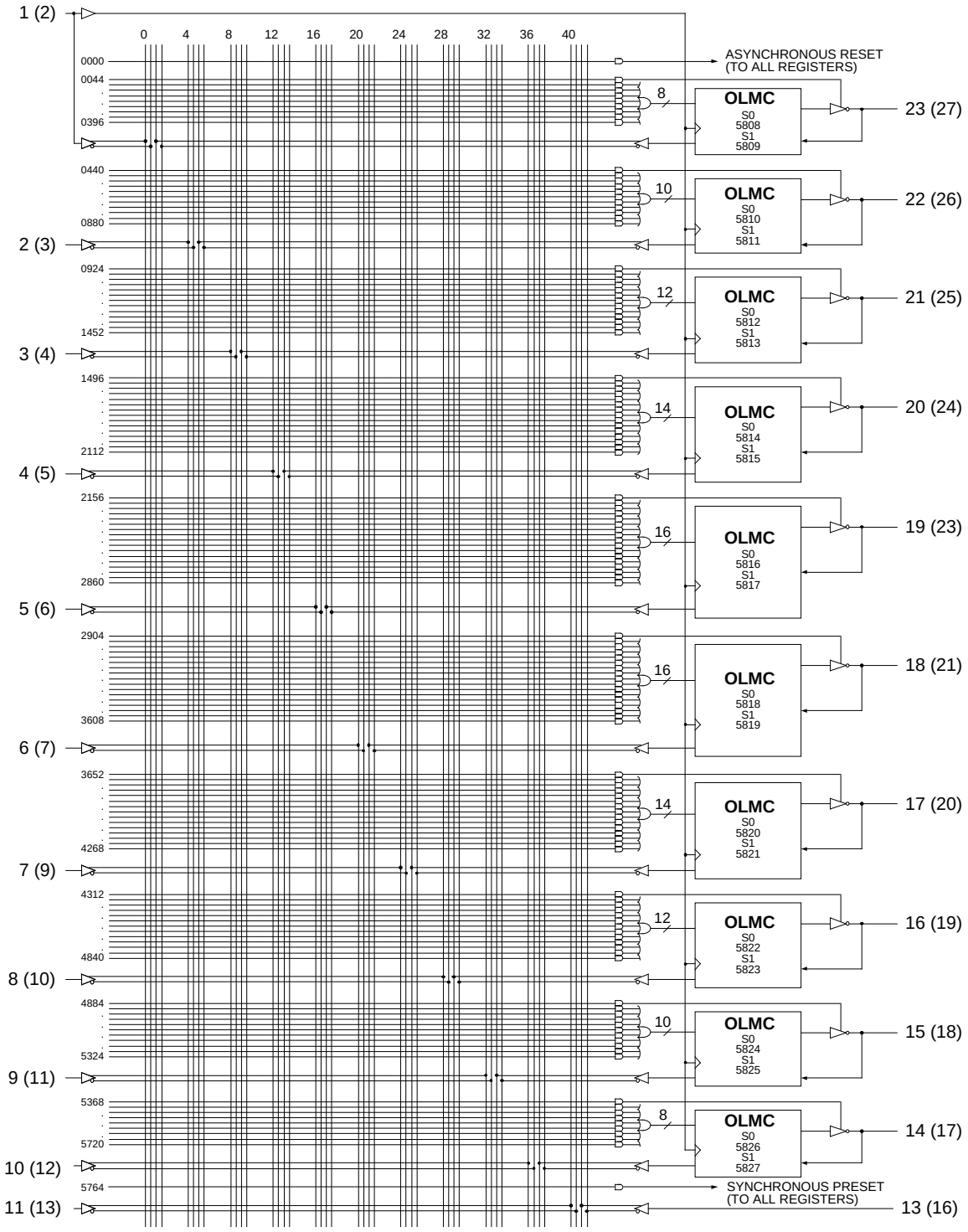


ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

GAL22V10 LOGIC DIAGRAM / JEDEC FUSE MAP

DIP (PLCC) Package Pinouts



5828, 5829 ... Electronic Signature ... 5890, 5891							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
MSB							LSB

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V

Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... -40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	16	mA
I_{OH}	High Level Output Current			—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C		–30	—	–130	mA
COMMERCIAL							
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L-5	—	90	150	mA
			L-7	—	90	140	mA
			L-10	—	90	130	mA
INDUSTRIAL							
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L-7/-10	—	90	160	mA

1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM	TEST COND.[1]	DESCRIPTION	COM -5		COM/IND -7 (PLCC)		COM/IND -7 (PDIP)		COM -10		IND -10		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinatorial Output	1	5	1	7.5	1	7.5	3	10	1	10	ns
tco	A	Clock to Output Delay	1	4	1	4.5	1	4.5	2	7	1	7	ns
tcf[2]	—	Clock to Feedback Delay	—	3	—	3	—	3	—	2.5	—	2.5	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑	3	—	4.5	—	5	—	7	—	7	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	142.8	—	111	—	105	—	71.4	—	71.4	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	166	—	133	—	125	—	105	—	105	—	MHz
	A	Maximum Clock Frequency with No Feedback	200	—	166	—	142.8	—	105	—	105	—	MHz
twh	—	Clock Pulse Duration, High	2.5	—	3	—	3.5	—	4	—	4	—	ns
twl	—	Clock Pulse Duration, Low	2.5	—	3	—	3.5	—	4	—	4	—	ns
ten	B	Input or I/O to Output Enabled	1	6	1	7.5	1	7.5	3	10	1	10	ns
tdis	C	Input or I/O to Output Disabled	1	6	1	7.5	1	7.5	3	9	1	9	ns
tar	A	Input or I/O to Asynch. Reset of Reg.	1	5.5	1	9	1	9	3	13	1	13	ns
tarw	—	Asynch. Reset Pulse Duration	5.5	—	7	—	7	—	8	—	8	—	ns
tarr	—	Asynch. Reset to Clk↑ Recovery Time	4	—	5	—	5	—	8	—	8	—	ns
tspr	—	Synch. Preset to Clk↑ Recovery Time	4	—	5	—	5	—	10	—	10	—	ns

1) Refer to Switching Test Conditions section.
2) Calculated from fmax with internal feedback. Refer to fmax Description section.
3) Refer to fmax Description section. Characterized initially and after any design or process changes that may affect these parameters.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V

Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... -40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–130	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L-7	—	90	140	mA
			L-10/-15	—	90	130	mA
			L-25	—	75	90	mA
			Q-15/-25	—	45	55	mA

INDUSTRIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L-15/-20/-25	—	90	150	mA

1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM.	TEST COND.[1]	DESCRIPTION	COM -7		COM -10		COM / IND -15		IND -20		COM / IND -25		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Comb. Output	3	7.5	3	10	3	15	3	20	3	25	ns
tco	A	Clock to Output Delay	2	5	2	7	2	8	2	10	2	15	ns
tcf[2]	—	Clock to Feedback Delay	—	2.5	—	2.5	—	2.5	—	8	—	13	ns
tsu_1	—	Setup Time, Input or Fdbk before Clk↑	6.5	—	7	—	10	—	14	—	15	—	ns
tsu_2	—	Setup Time, SP before Clock↑	10	—	10	—	10	—	14	—	15	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	87	—	71.4	—	55.5	—	41.6	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	111	—	105	—	80	—	45.4	—	35.7	—	MHz
	A	Maximum Clock Frequency with No Feedback	111	—	105	—	83.3	—	50	—	38.5	—	MHz
twh	—	Clock Pulse Duration, High	4	—	4	—	6	—	10	—	13	—	ns
twl	—	Clock Pulse Duration, Low	4	—	4	—	6	—	10	—	13	—	ns
ten	B	Input or I/O to Output Enabled	3	8	3	10	3	15	3	20	3	25	ns
tdis	C	Input or I/O to Output Disabled	3	8	3	9	3	15	3	20	3	25	ns
tar	A	Input or I/O to Asynch. Reset of Reg.	3	13	3	13	3	20	3	25	3	25	ns
tarw	—	Asynch. Reset Pulse Duration	8	—	8	—	15	—	20	—	25	—	ns
tarr	—	Asynch. Reset to Clk↑ Recovery Time	8	—	8	—	10	—	20	—	25	—	ns
tspr	—	Synch. Preset to Clk↑ Recovery Time	10	—	10	—	10	—	14	—	15	—	ns

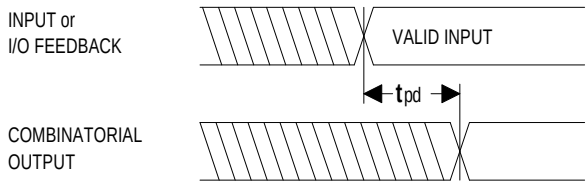
1) Refer to Switching Test Conditions section.
2) Calculated from fmax with internal feedback. Refer to fmax Description section.
3) Refer to fmax Description section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

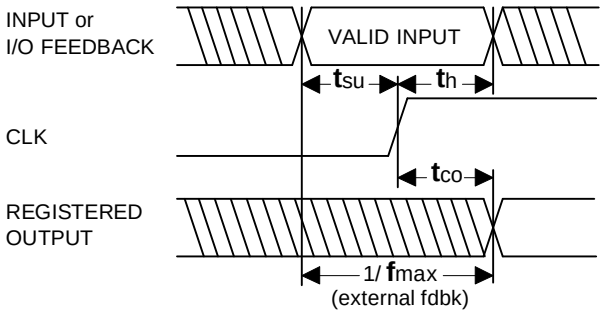
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

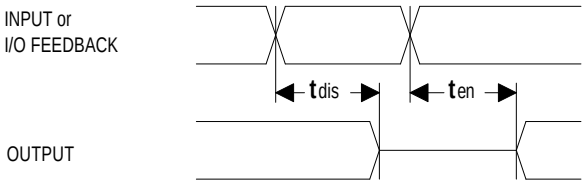
SWITCHING WAVEFORMS



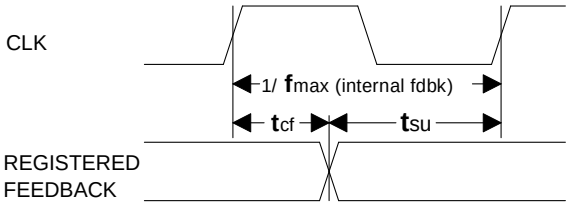
Combinatorial Output



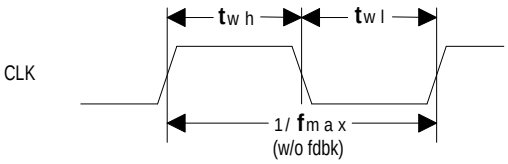
Registered Output



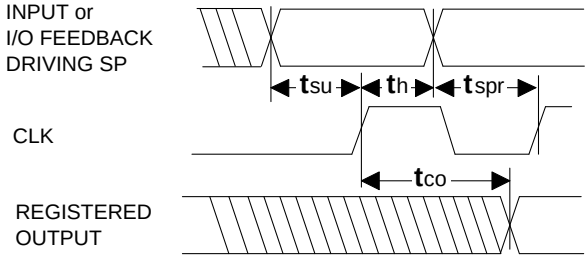
Input or I/O to Output Enable/Disable



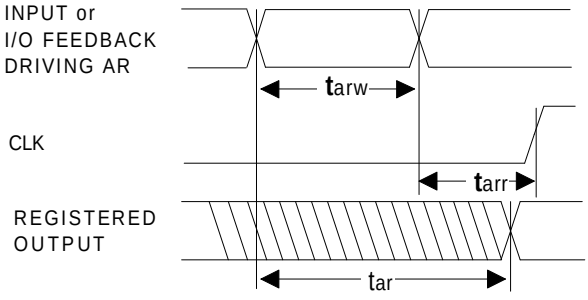
fmax with Feedback



Clock Width

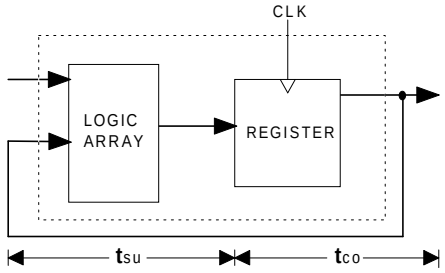


Synchronous Preset



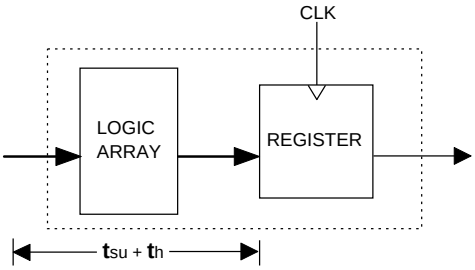
Asynchronous Reset

fmax DESCRIPTIONS



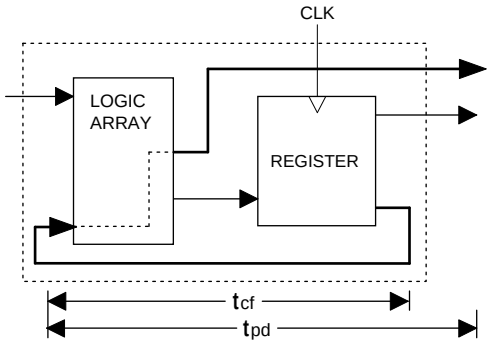
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

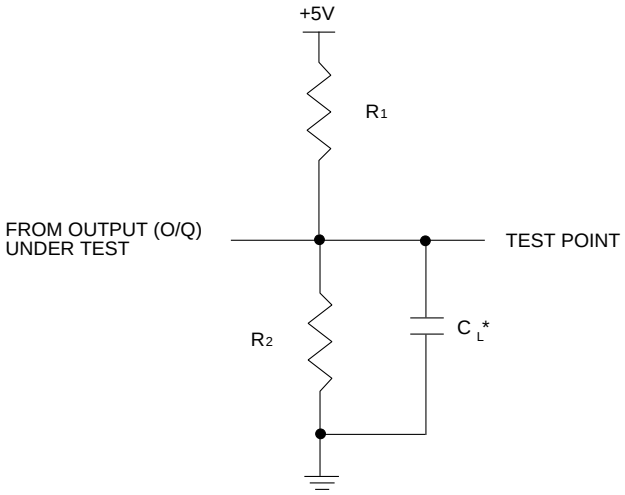
SWITCHING TEST CONDITIONS

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	-5	1.5ns 10% – 90%
	-7/-10	2.0ns 10% – 90%
	-15/-20/-25	3ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided in every GAL22V10 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

The electronic signature is an additional feature not present in other manufacturers' 22V10 devices. To use the extra feature of the user-programmable electronic signature it is necessary to choose a Lattice Semiconductor 22V10 device type when compiling a set of logic equations. In addition, many device programmers have two separate selections for the device, typically a GAL22V10 and a GAL22V10-UES (UES = User Electronic Signature) or GAL22V10-ES. This allows users to maintain compatibility with existing 22V10 designs, while still having the option to use the GAL device's extra feature.

The JEDEC map for the GAL22V10 contains the 64 extra fuses for the electronic signature, for a total of 5892 fuses. However, the GAL22V10 device can still be programmed with a standard 22V10 JEDEC map (5828 fuses) with any qualified device programmer.

SECURITY CELL

A security cell is provided in every GAL22V10 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL22V10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

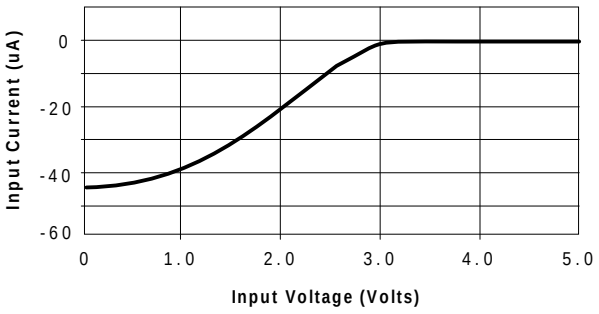
The GAL22V10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

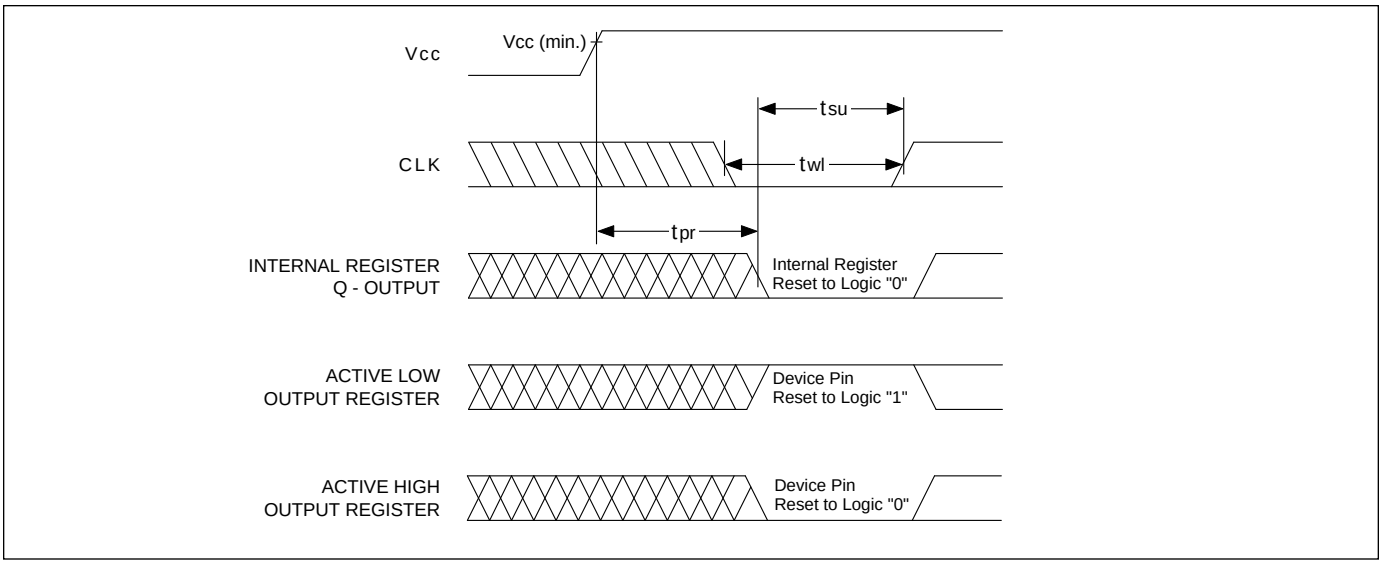
GAL22V10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device. (See equivalent input and I/O schematics on the following page.)

Typical Input Current

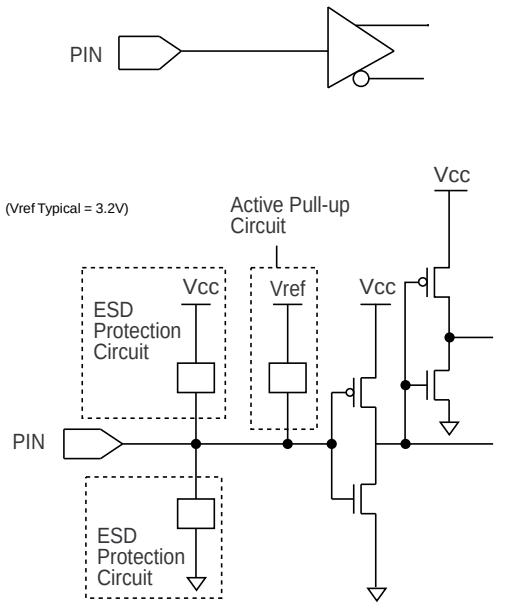


POWER-UP RESET

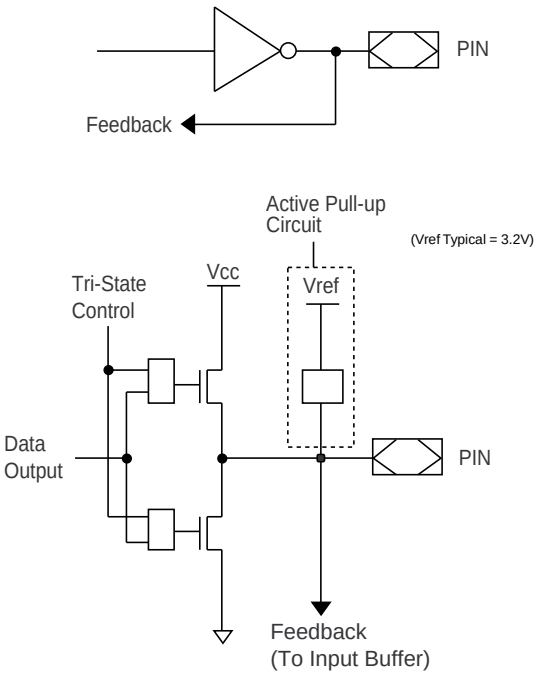


Circuitry within the GAL22V10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL22V10. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



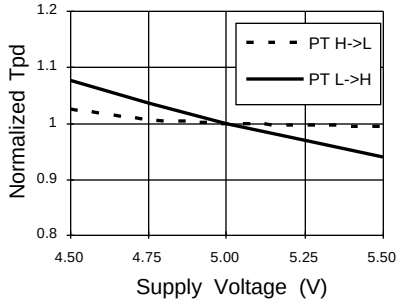
Typical Input



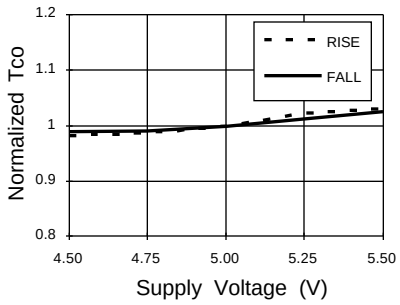
Typical Output

GAL22V10C-5/-7/-10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

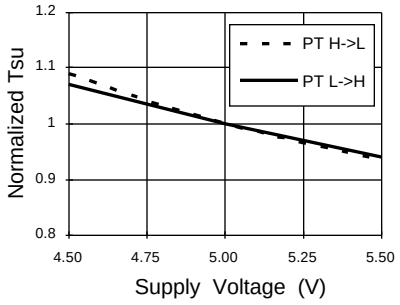
Normalized Tpd vs Vcc



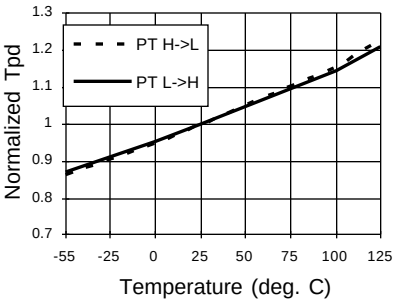
Normalized Tco vs Vcc



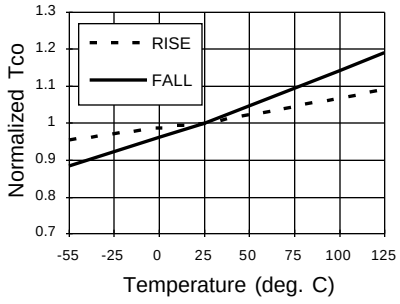
Normalized Tsu vs Vcc



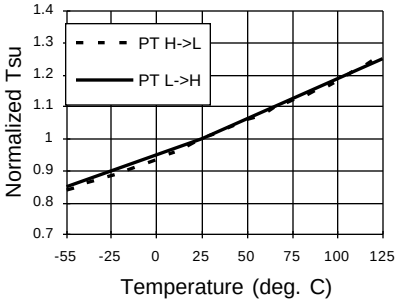
Normalized Tpd vs Temp



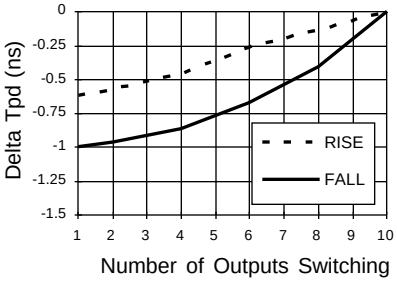
Normalized Tco vs Temp



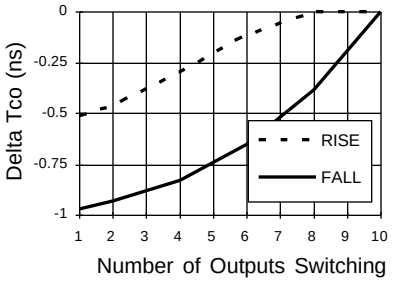
Normalized Tsu vs Temp



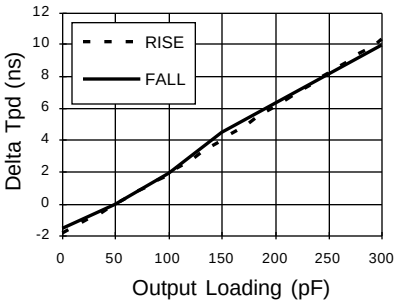
Delta Tpd vs # of Outputs Switching



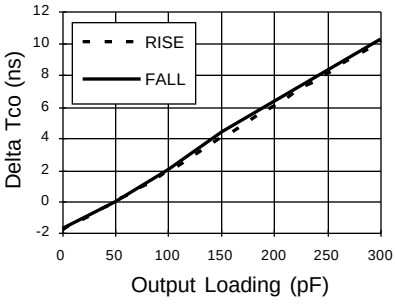
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

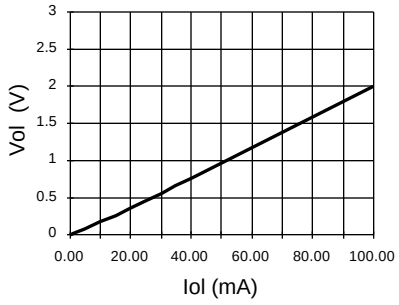


Delta Tco vs Output Loading

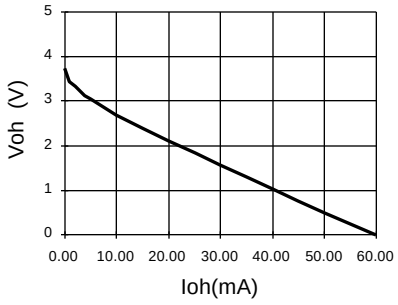


GAL22V10C-5/-7/-10: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

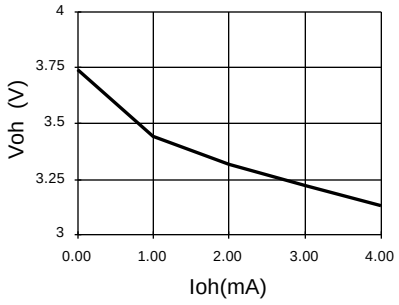
Vol vs Iol



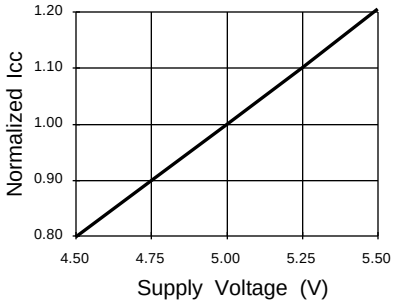
Voh vs Ioh



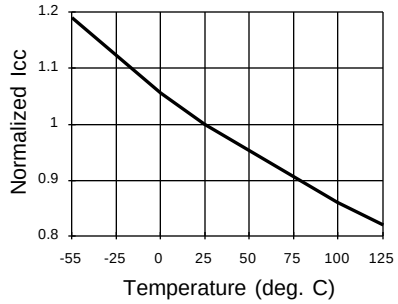
Voh vs Ioh



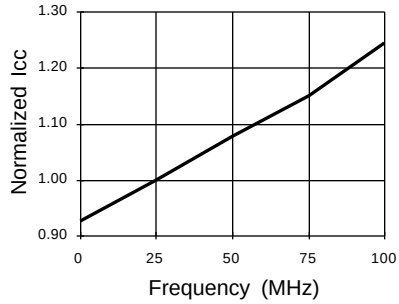
Normalized Icc vs Vcc



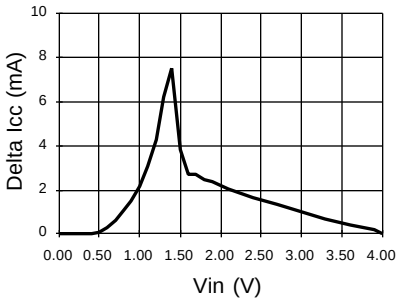
Normalized Icc vs Temp



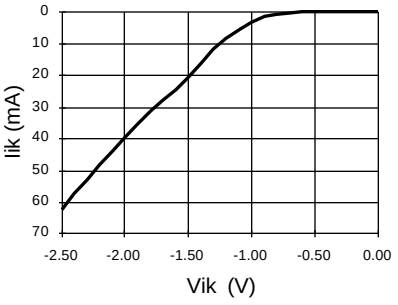
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

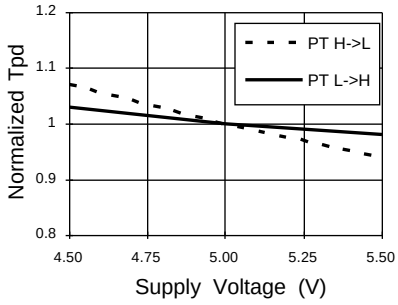


Input Clamp (Vik)

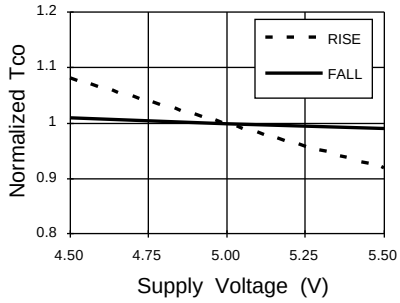


GAL22V10B-7/-10/-15/-25L: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

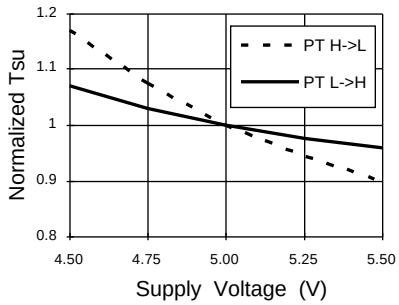
Normalized Tpd vs Vcc



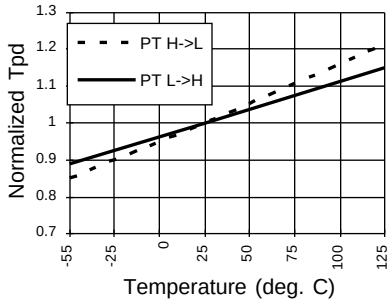
Normalized Tco vs Vcc



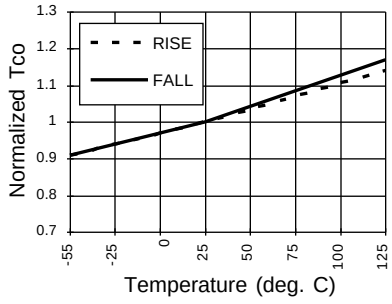
Normalized Tsu vs Vcc



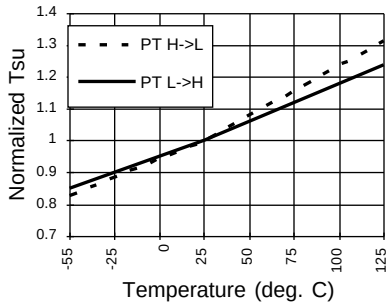
Normalized Tpd vs Temp



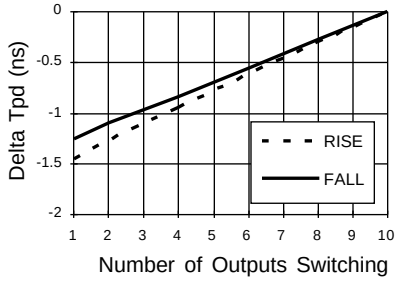
Normalized Tco vs Temp



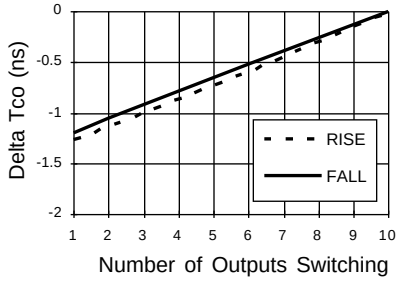
Normalized Tsu vs Temp



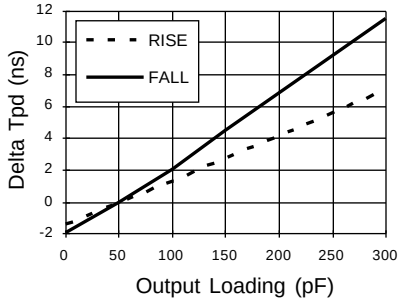
Delta Tpd vs # of Outputs Switching



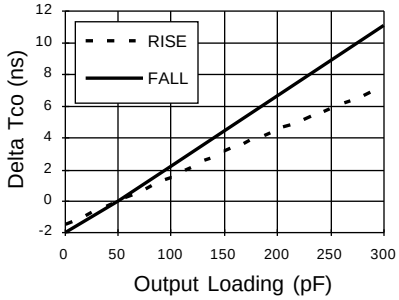
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

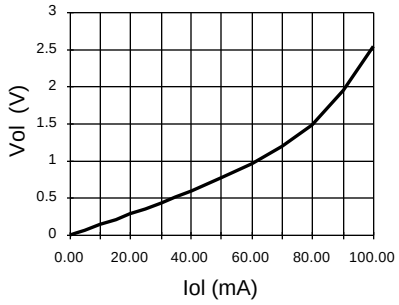


Delta Tco vs Output Loading

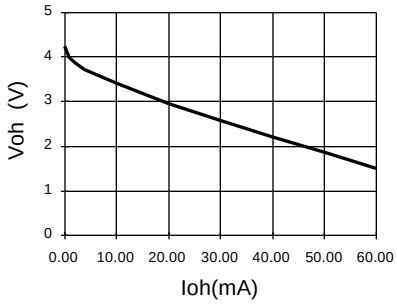


GAL22V10B-7/-10/-15/-25L: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

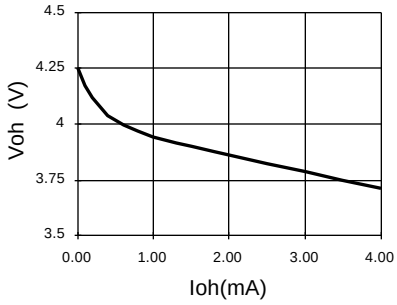
Vol vs Iol



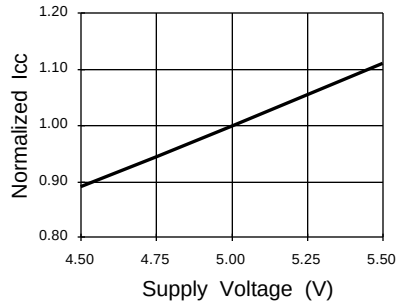
Voh vs Ioh



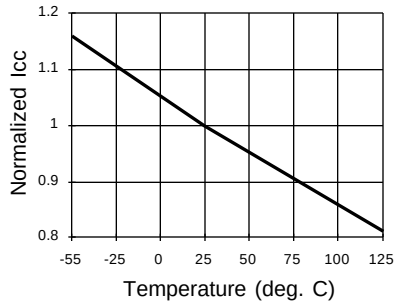
Voh vs Ioh



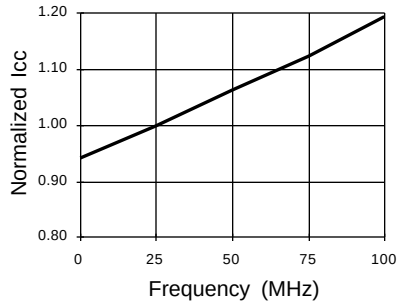
Normalized Icc vs Vcc



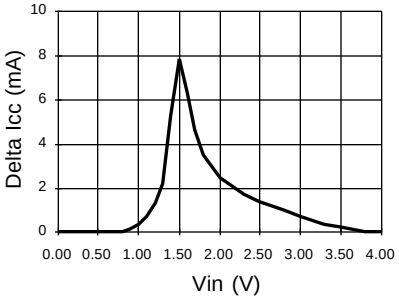
Normalized Icc vs Temp



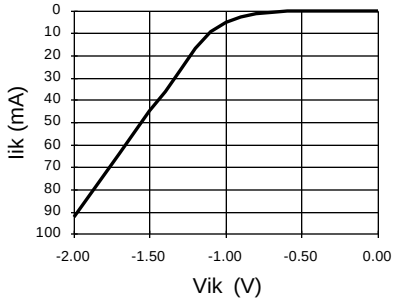
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

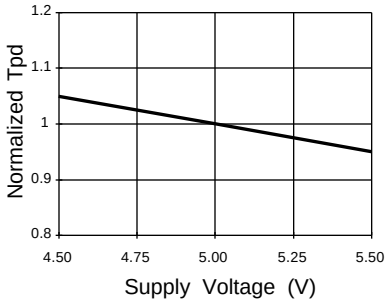


Input Clamp (Vik)

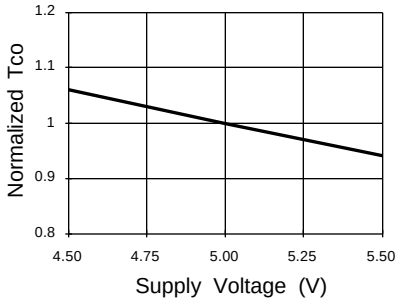


GAL22V10B-15/-25Q: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

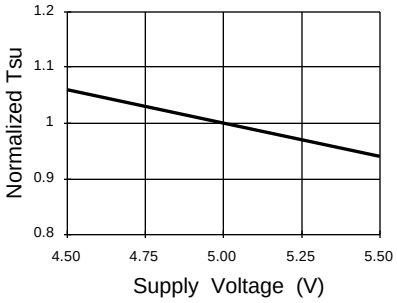
Normalized Tpd vs Vcc



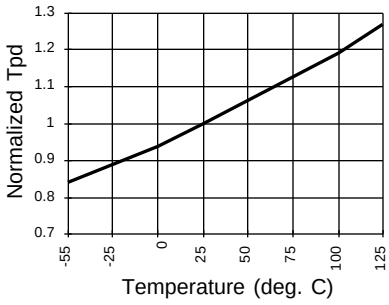
Normalized Tco vs Vcc



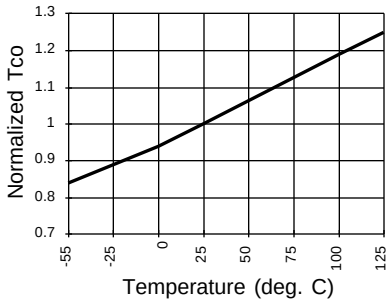
Normalized Tsu vs Vcc



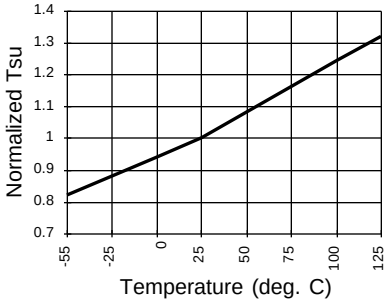
Normalized Tpd vs Temp



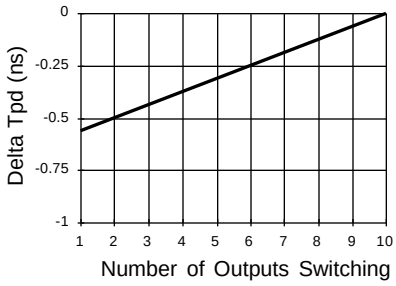
Normalized Tco vs Temp



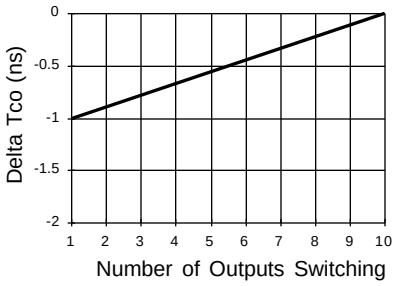
Normalized Tsu vs Temp



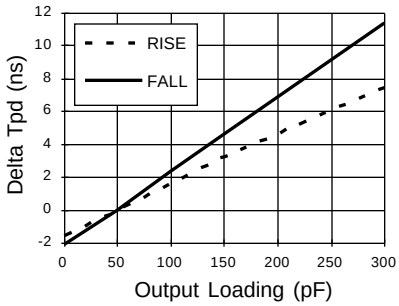
Delta Tpd vs # of Outputs Switching



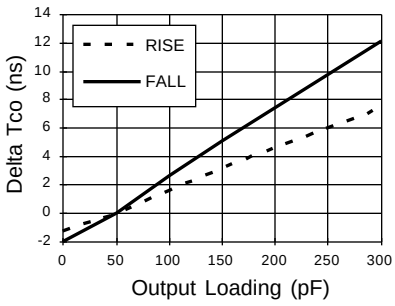
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

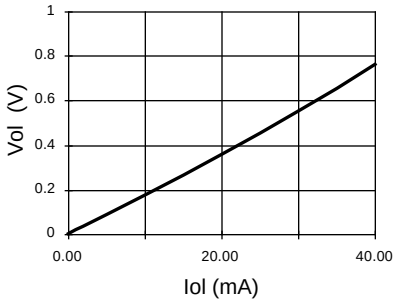


Delta Tco vs Output Loading

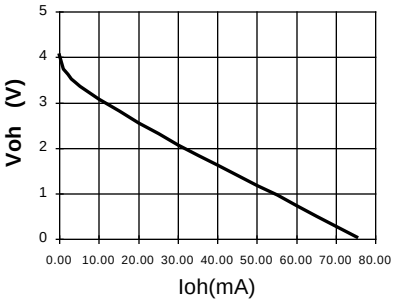


GAL22V10B-15/-25Q: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

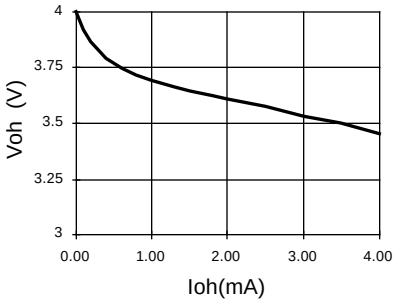
Vol vs Iol



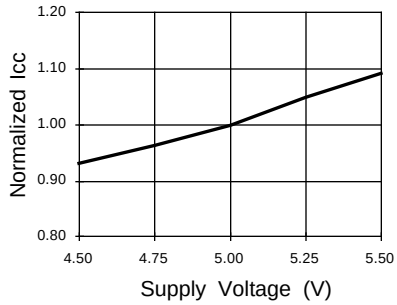
Voh vs Ioh



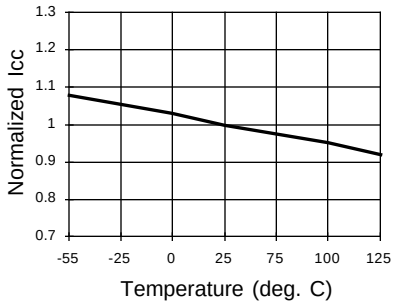
Voh vs Ioh



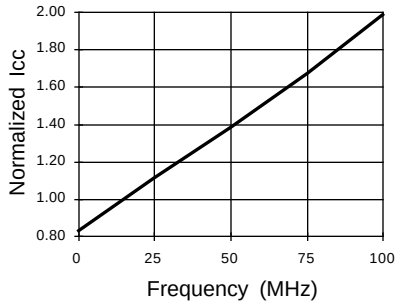
Normalized Icc vs Vcc



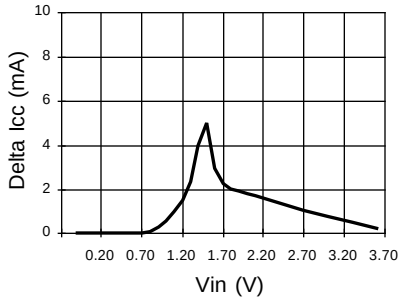
Normalized Icc vs Temp



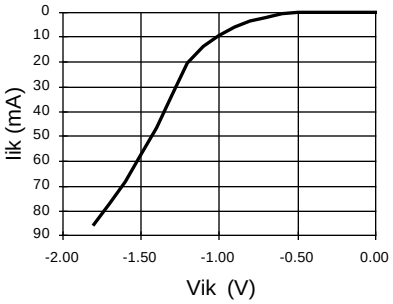
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



ispGAL22V10

In-System Programmable E²CMOS PLD Generic Array Logic™

FEATURES

- **IN-SYSTEM PROGRAMMABLE™ (5-V ONLY)**
  - **— 4-Wire Serial Programming Interface**
  - **— Minimum 10,000 Program/Erase Cycles**
  - **— Built-in Pull-Down on SDI Pin Eliminates Discrete Resistor on Board (ispGAL22V10C Only)**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 7.5 ns Maximum Propagation Delay**
  - **— Fmax = 111 MHz**
  - **— 5 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **ACTIVE PULL-UPS ON ALL LOGIC INPUT AND I/O PINS**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
  - **— Fully Function/Fuse-Map/Parametric Compatible with Bipolar and CMOS 22V10 Devices**
- **E² CELL TECHNOLOGY**
  - **— In-System Programmable Logic**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Software-Driven Hardware Configuration**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

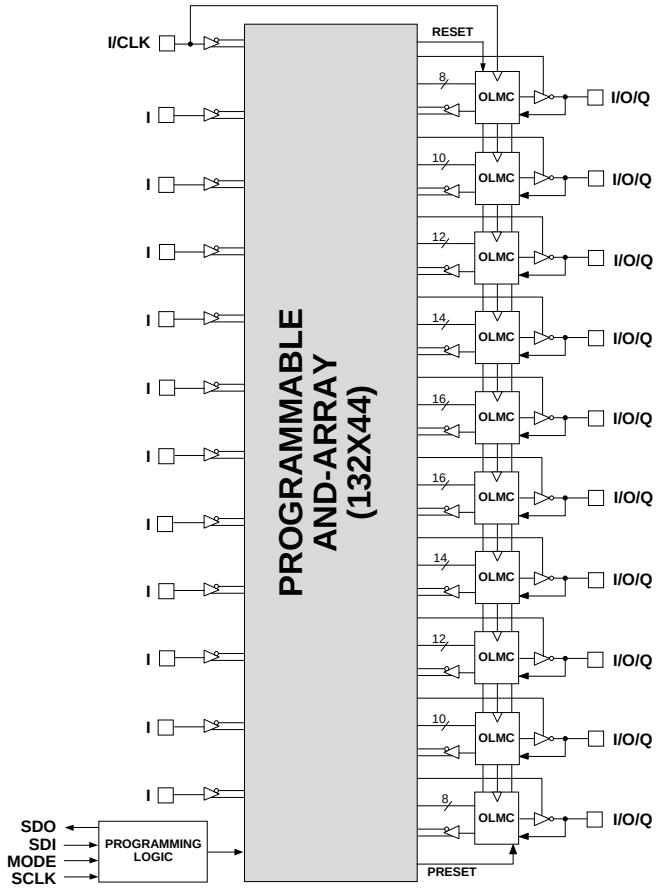
DESCRIPTION

The ispGAL22V10, at 7.5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E^2) floating gate technology to provide the industry's first in-system programmable 22V10 device. E^2 technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The ispGAL22V10 is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices. The standard PLCC package provides the same functional pinout as the standard 22V10 PLCC package with No-Connect pins being used for the ISP interface signals.

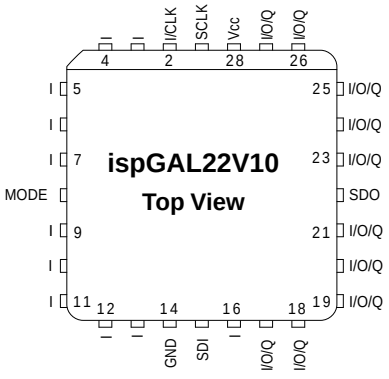
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

PLCC



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

ORDERING INFORMATION

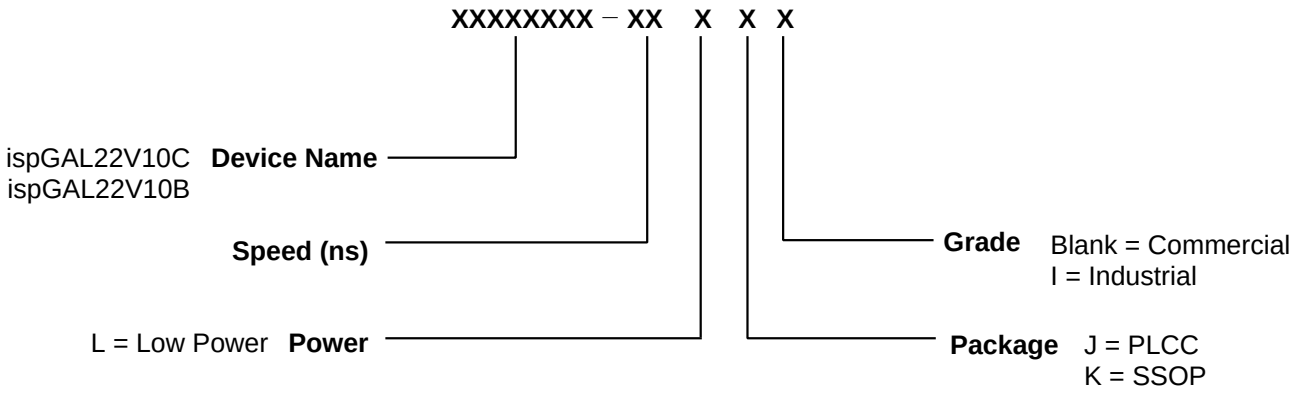
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	6.5	5	140	ispGAL22V10C-7LJ	28-Lead PLCC
				ispGAL22V10C-7LK	28-Lead SSOP
				ispGAL22V10B-7LJ	28-Lead PLCC
10	7	7	140	ispGAL22V10C-10LJ	28-Lead PLCC
				ispGAL22V10C-10LK	28-Lead SSOP
				ispGAL22V10B-10LJ	28-Lead PLCC
15	10	8	140	ispGAL22V10C-15LJ	28-Lead PLCC
				ispGAL22V10C-15LK	28-Lead SSOP
				ispGAL22V10B-15LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	10	8	165	ispGAL22V10C-15LJI	28-Lead PLCC
				ispGAL22V10C-15LKI	28-Lead SSOP

PART NUMBER DESCRIPTION



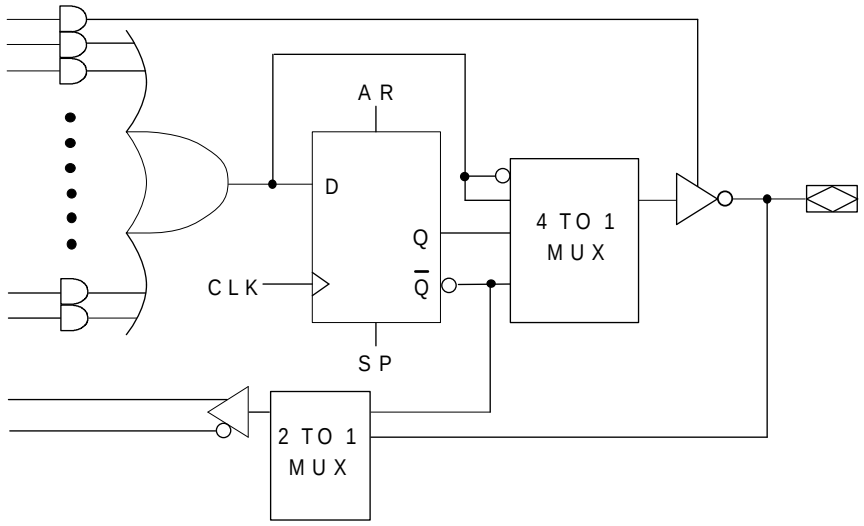
OUTPUT LOGIC MACROCELL (OLMC)

The ispGAL22V10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 17 and 27), two have ten product terms (pins 18 and 26), two have twelve product terms (pins 19 and 25), two have fourteen product terms (pins 20 and 24), and two OLMCs have sixteen product terms (pins 21 and 23). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The ispGAL22V10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



ispGAL22V10 OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the ispGAL22V10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

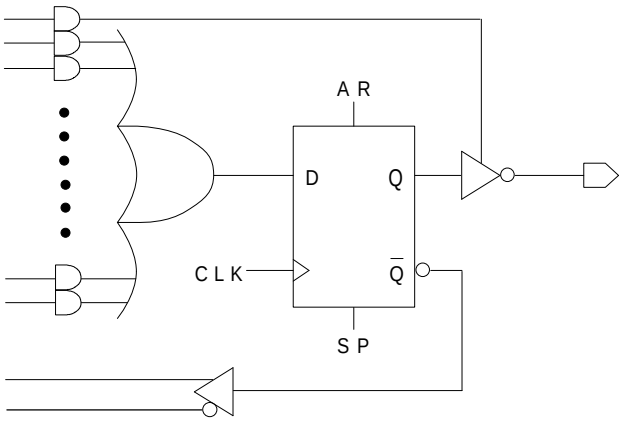
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

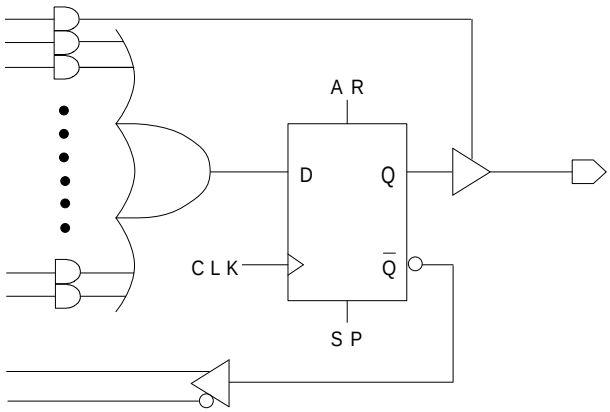
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE



ACTIVE LOW

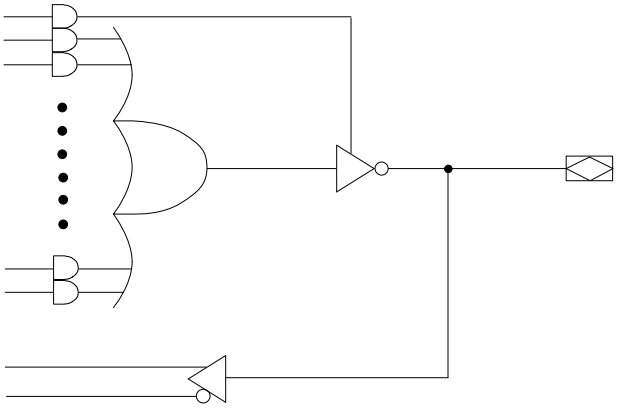
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

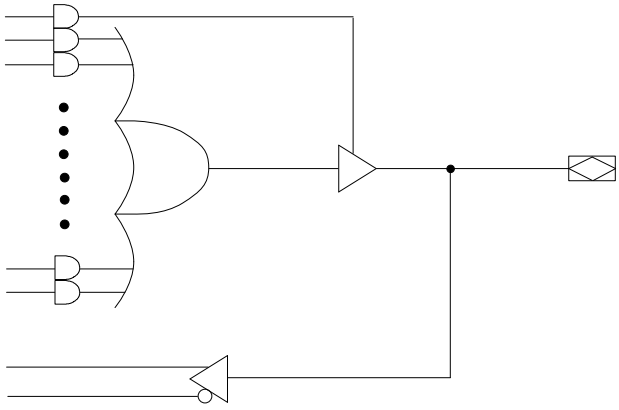
$S_0 = 1$
$S_1 = 0$

COMBINATORIAL MODE



ACTIVE LOW

$S_0 = 0$
$S_1 = 1$

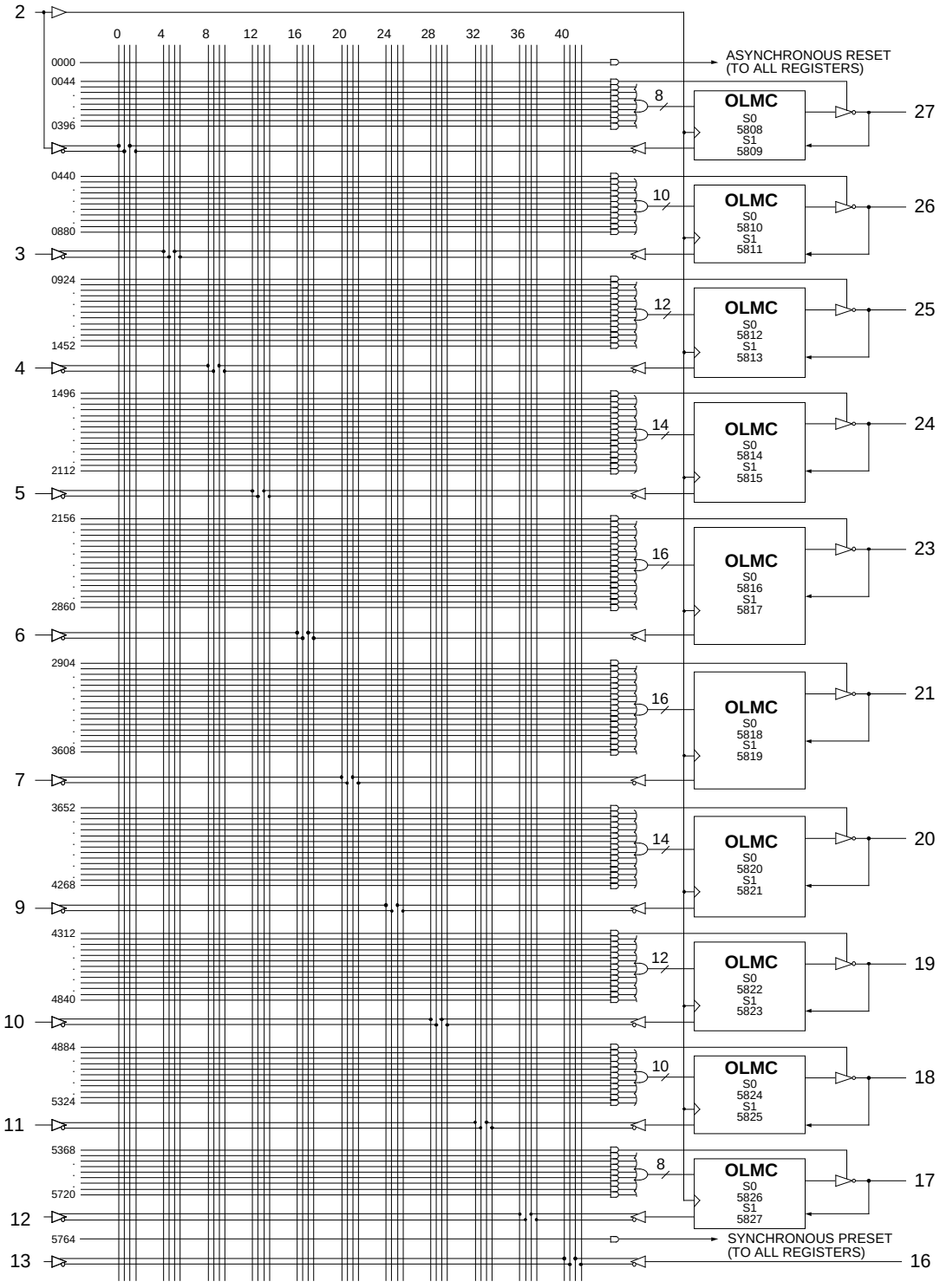


ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

ispGAL22V10 LOGIC DIAGRAM / JEDEC FUSE MAP

PLCC Package Pinout



5828, 5829 ... Electronic Signature ... 5890, 5891							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
MSB							LSB

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V

Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... -40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[4]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current[1]	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
	SDI Low Leakage Current[2]	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	250	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
	SDI High Leakage Current[2]	$V_{IN} = V_{OH}$ (MIN.)	—	—	1	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[3]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–130	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -7/-10/-15	—	90	140	mA

INDUSTRIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -15	—	90	165	mA

1) The leakage current is due to the internal pull-up on all pins (except SDI on ispGAL22V10C). See **Input Buffer** section for more information.
2) The leakage current is due to the internal pull-down on the SDI pin (ispGAL22V10C only). See **Input Buffer** section for more information.
3) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
4) Typical values are at Vcc = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	COM -7		COM -10		COM/IND -15		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	—	7.5	—	10	—	15	ns
t_{co}	A	Clock to Output Delay	—	5	—	7	—	8	ns
t_{cf}[2]	—	Clock to Feedback Delay	—	2.5	—	2.5	—	2.5	ns
t_{su_1}	—	Setup Time, Input or Feedback before Clock↑	6.5	—	7		10	—	ns
t_{su_2}	—	Setup Time, SP before Clock↑	10	—	10	—	10	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
f_{max}[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	87	—	71.4	—	55.5	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	111	—	105	—	80	—	MHz
	A	Maximum Clock Frequency with No Feedback	111	—	105	—	83.3	—	MHz
t_{wh}	—	Clock Pulse Duration, High	4	—	4	—	6	—	ns
t_{wl}	—	Clock Pulse Duration, Low	4	—	4	—	6	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	8	—	10	—	15	ns
t_{dis}	C	Input or I/O to Output Disabled	—	8	—	10	—	15	ns
t_{ar}	A	Input or I/O to Asynchronous Reset of Register	—	13	—	13	—	20	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	8	—	8	—	15	—	ns
t_{arr}	—	Asynchronous Reset to Clock Recovery Time	8	—	8	—	10	—	ns
t_{spr}	—	Synchronous Preset to Clock Recovery Time	10	—	10	—	10	—	ns

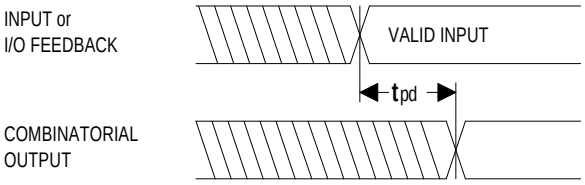
1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

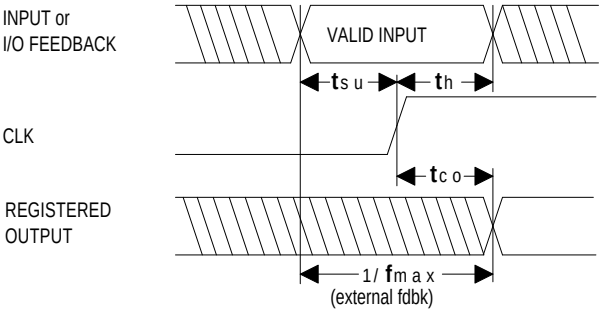
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

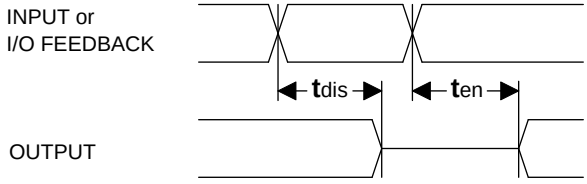
SWITCHING WAVEFORMS



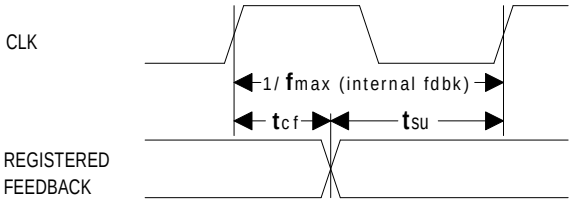
Combinatorial Output



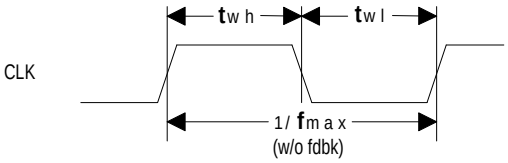
Registered Output



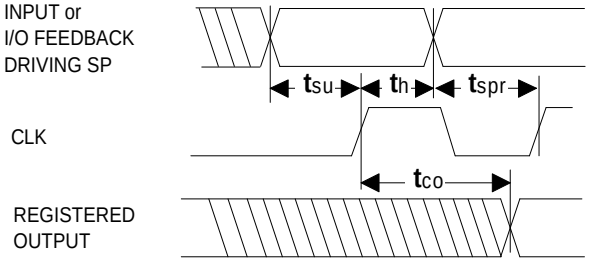
Input or I/O to Output Enable/Disable



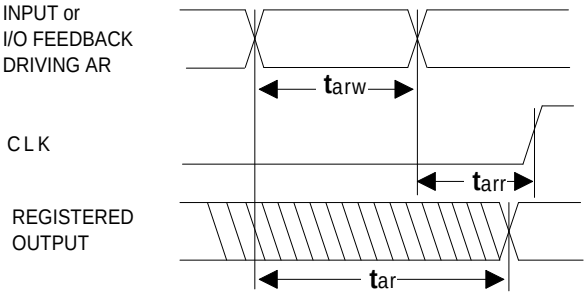
fmax with Feedback



Clock Width

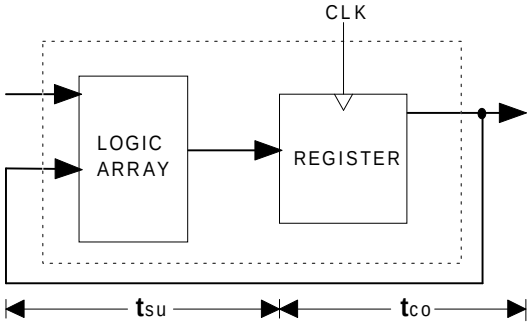


Synchronous Preset



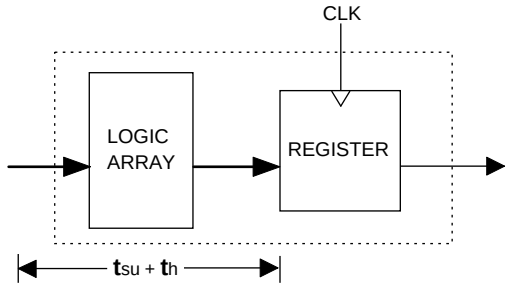
Asynchronous Reset

fmax DESCRIPTIONS



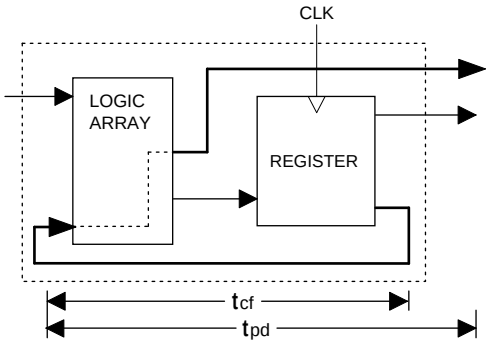
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/**t**wh + **t**wl. This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

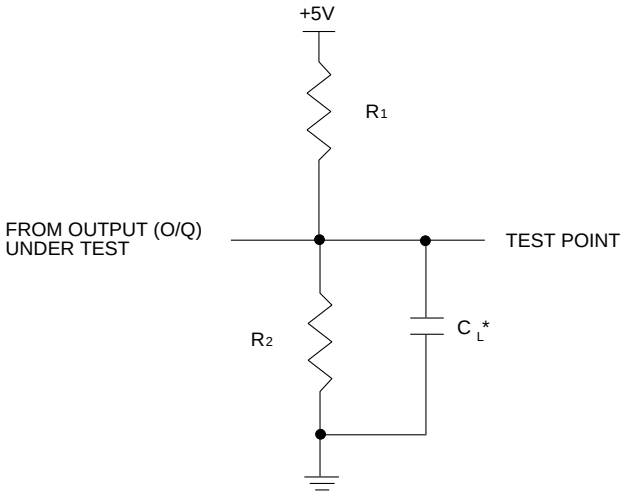
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided in every ispGAL22V10 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

The electronic signature is an additional feature not present in other manufacturers' 22V10 devices. To use the extra feature of the user-programmable electronic signature it is necessary to choose a Lattice Semiconductor 22V10 device type when compiling a set of logic equations. In addition, many device programmers have two separate selections for the device, typically an ispGAL22V10 and a ispGAL22V10-UES (UES = User Electronic Signature) or ispGAL22V10-ES. This allows users to maintain compatibility with existing 22V10 designs, while still having the option to use the GAL device's extra feature.

The JEDEC map for the ispGAL22V10 contains the 64 extra fuses for the electronic signature, for a total of 5892 fuses. However, the ispGAL22V10 device can still be programmed with a standard 22V10 JEDEC map (5828 fuses) with any qualified device programmer.

SECURITY CELL

A security cell is provided in every ispGAL22V10 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

ispGAL22V10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

DEVICE PROGRAMMING

The ispGAL22V10 device uses a standard 22V10 JEDEC fusemap file to describe the device programming information. Any third party logic compiler can produce the JEDEC file for this device.

IN-SYSTEM PROGRAMMABILITY

The ispGAL22V10 device features In-System Programmable technology. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via four TTL level logic interface signals. These four signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. For details on the operation of the internal state machine and programming of ispGAL22V10 devices please refer to the ISP Architecture and Programming section in this Data Book.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

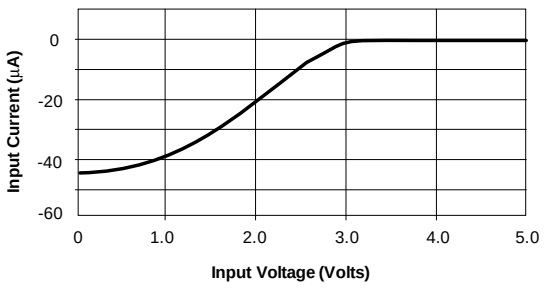
The ispGAL22V10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

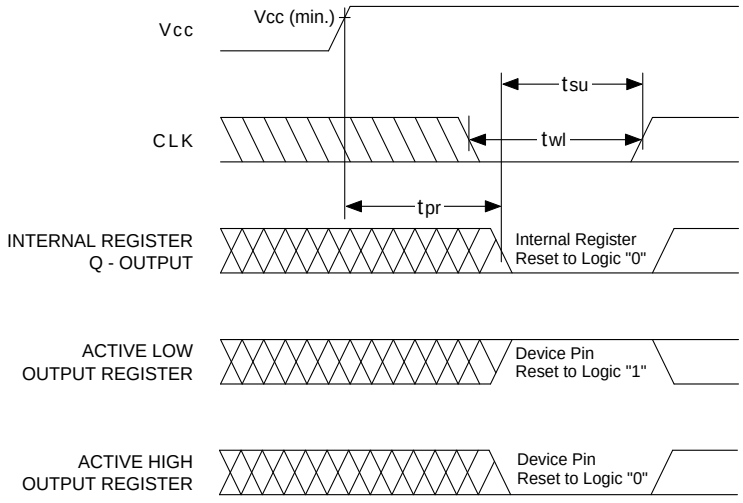
ispGAL22V10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

All input and I/O pins (except SDI on the ispGAL22V10C) also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). The SDI pin on the ispGAL22V10C has a built-in pull-down to keep the device out of the programming state if the pin is not actively driven. However, Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device. (See equivalent input and I/O schematics on the following page.)

Typical Input Current

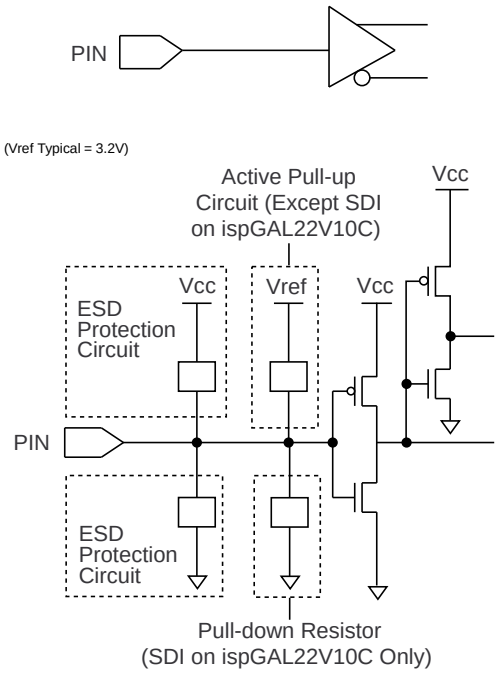


POWER-UP RESET

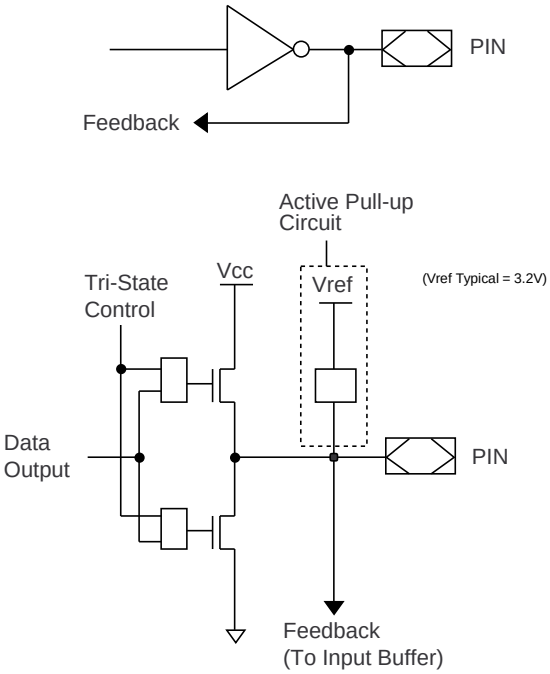


Circuitry within the ispGAL22V10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the ispGAL22V10. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



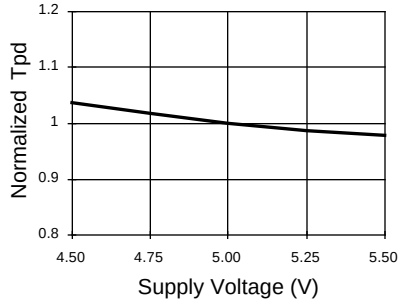
Input



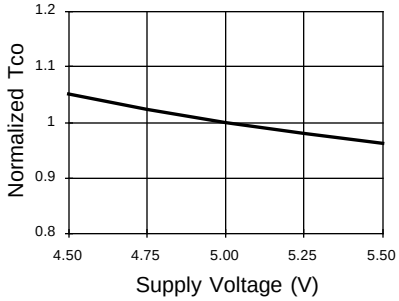
Output

ispGAL22V10C: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

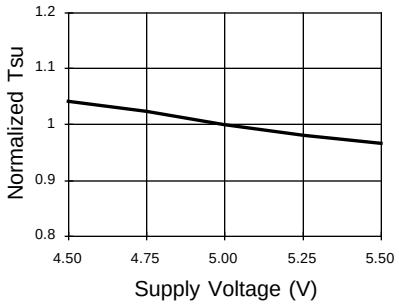
Normalized Tpd vs Vcc



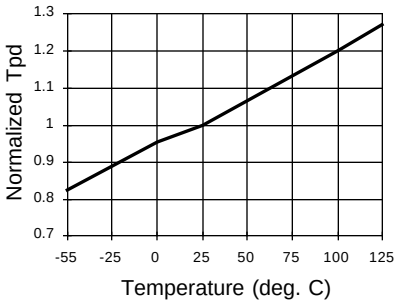
Normalized Tco vs Vcc



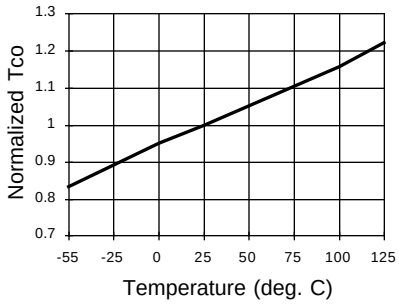
Normalized Tsu vs Vcc



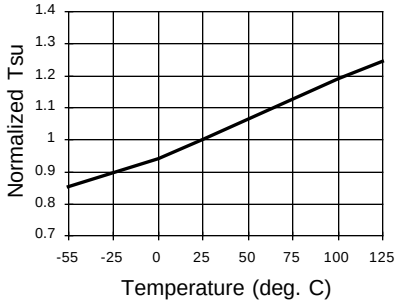
Normalized Tpd vs Temp



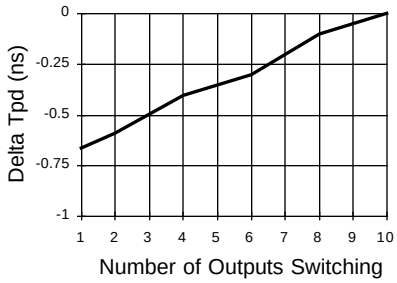
Normalized Tco vs Temp



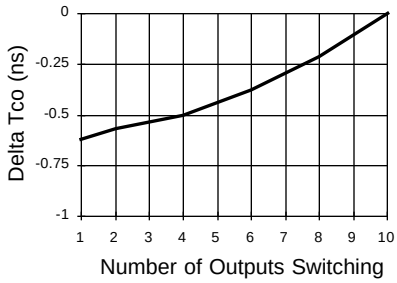
Normalized Tsu vs Temp



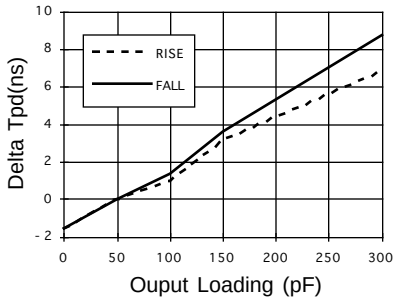
Delta Tpd vs # of Outputs Switching



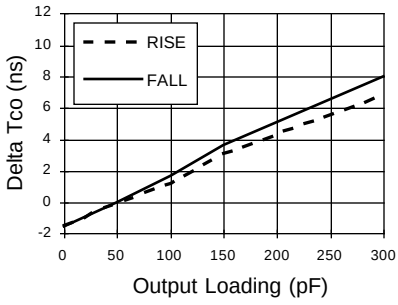
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

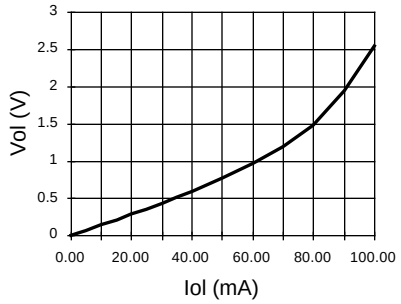


Delta Tco vs Output Loading

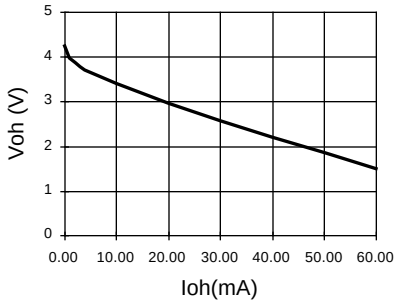


ispGAL22V10C: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

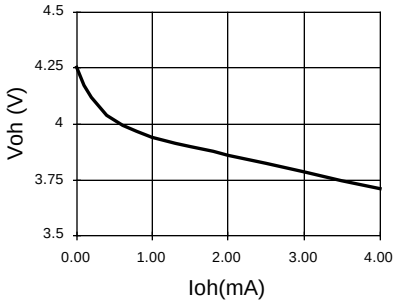
Vol vs Iol



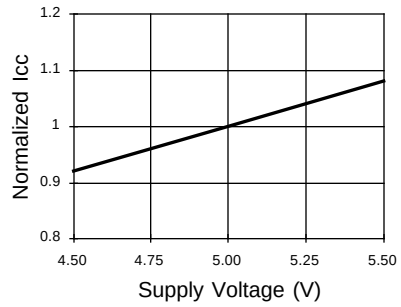
Voh vs Ioh



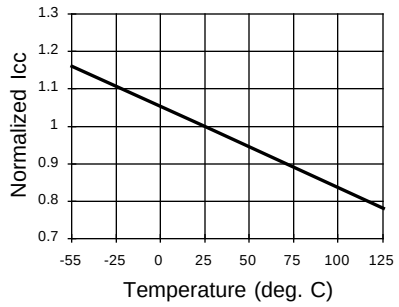
Voh vs Ioh



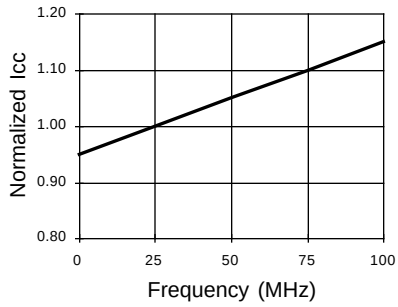
Normalized Icc vs Vcc



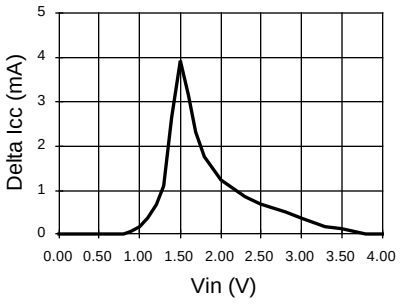
Normalized Icc vs Temp



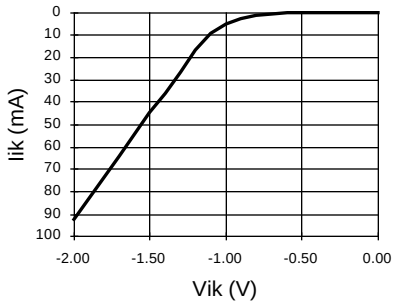
Normalized Icc vs Freq.



Delta Icc vs Vcc



Input Clamp (Vik)



GAL26CV12

High Performance E²CMOS PLD
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 7.5 ns Maximum Propagation Delay**
  - **— Fmax = 142.8 MHz**
  - **— 4.5ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 16 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **ACTIVE PULL-UPS ON ALL PINS**
- **LOW POWER CMOS**
  - **— 90 mA Typical Icc**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **TWELVE OUTPUT LOGIC MACROCELLS**
  - **— Uses Standard 22V10 Macrocells**
  - **— Maximum Flexibility for Complex Logic Designs**
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

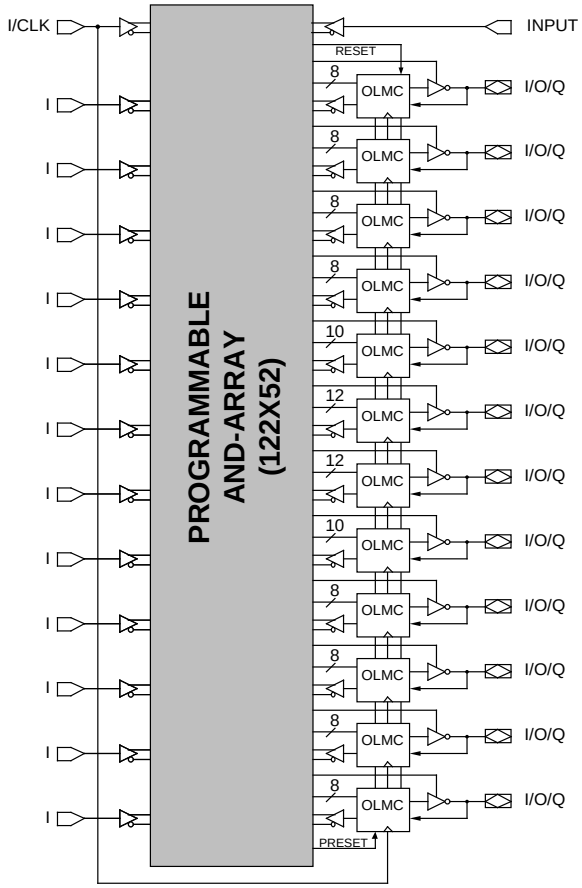
DESCRIPTION

The GAL26CV12, at 7.5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance 28-pin PLD available on the market. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

Expanding upon the industry standard 22V10 architecture, the GAL26CV12 eliminates the learning curve typically associated with using a new device architecture. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL26CV12 OLMC is fully compatible with the OLMC in standard bipolar and CMOS 22V10 devices.

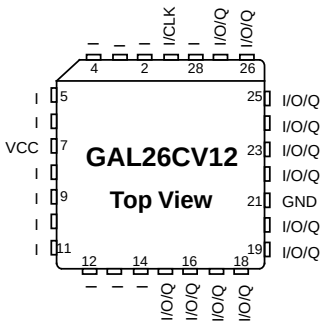
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM

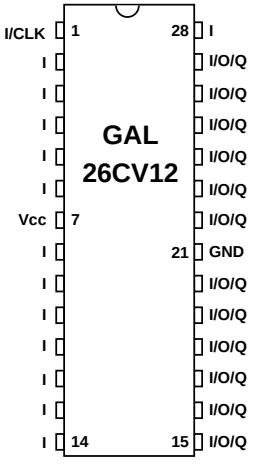


PIN CONFIGURATION

PLCC



DIP



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL26CV12 ORDERING INFORMATION

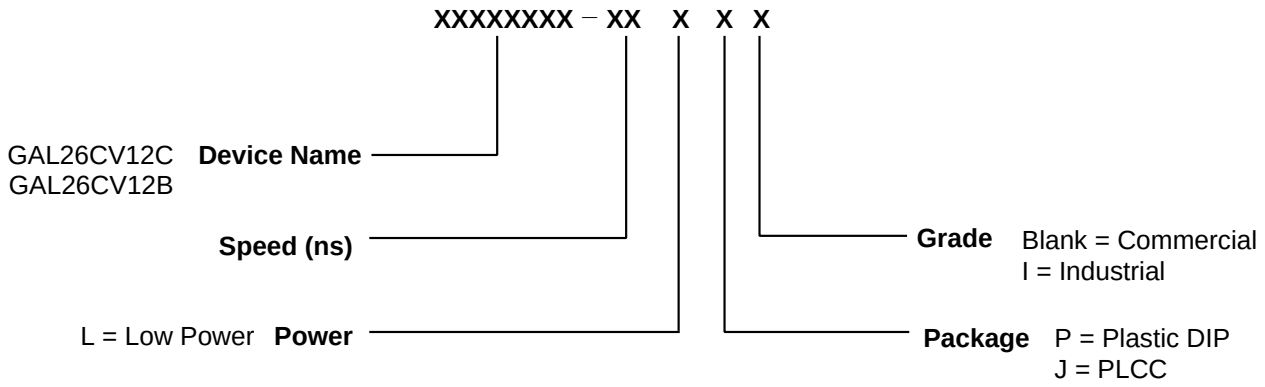
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	6	4.5	130	GAL26CV12C-7LP	28-Pin Plastic DIP
			130	GAL26CV12C-7LJ	28-Lead PLCC
10	7	7	130	GAL26CV12C-10LP	28-Pin Plastic DIP
			130	GAL26CV12C-10LJ	28-Lead PLCC
			130	GAL26CV12B-10LP	28-Pin Plastic DIP
			130	GAL26CV12B-10LJ	28-Lead PLCC
15	10	8	130	GAL26CV12C-15LP	28-Pin Plastic DIP
			130	GAL26CV12C-15LJ	28-Lead PLCC
			130	GAL26CV12B-15LP	28-Pin Plastic DIP
			130	GAL26CV12B-15LJ	28-Lead PLCC
20	12	12	130	GAL26CV12B-20LP	28-Pin Plastic DIP
			130	GAL26CV12B-20LJ	28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	7	7	150	GAL26CV12C-10LPI	28-Pin Plastic DIP
			150	GAL26CV12C-10LJI	28-Lead PLCC
15	10	8	150	GAL26CV12C-15LPI	28-Pin Plastic DIP
			150	GAL26CV12C-15LJI	28-Lead PLCC
			150	GAL26CV12B-15LPI	28-Pin Plastic DIP
			150	GAL26CV12B-15LJI	28-Lead PLCC
20	12	12	150	GAL26CV12B-20LPI	28-Pin Plastic DIP
			150	GAL26CV12B-20LJI	28-Lead PLCC

PART NUMBER DESCRIPTION



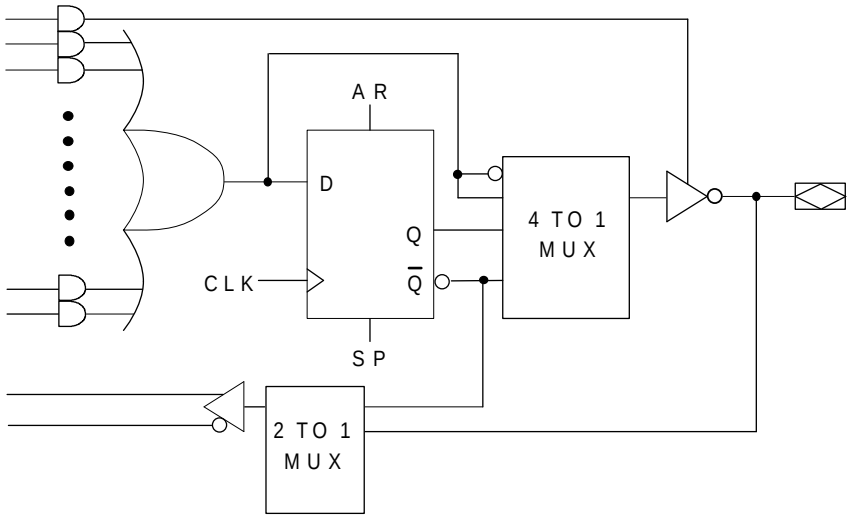
OUTPUT LOGIC MACROCELL (OLMC)

The GAL26CV12 has a variable number of product terms per OLMC. Of the twelve available OLMCs, two OLMCs have access to twelve product terms (pins 20 and 22), two have access to ten product terms (pins 19 and 23), and the other eight OLMCs have eight product terms each. In addition to the product terms available for logic, each OLMC has an additional product term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL26CV12 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registered outputs to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL26CV12 OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL26CV12 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the the following page.

REGISTERED

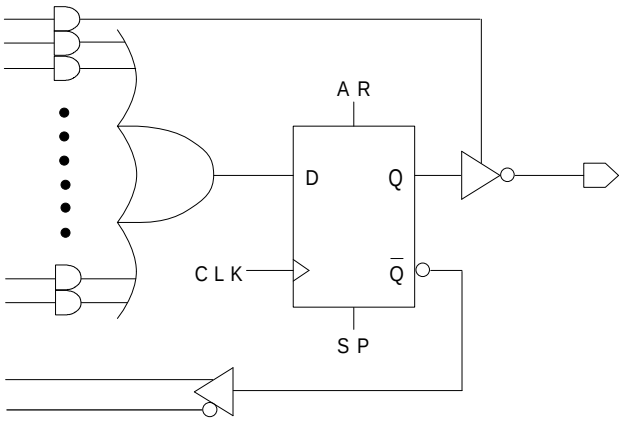
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

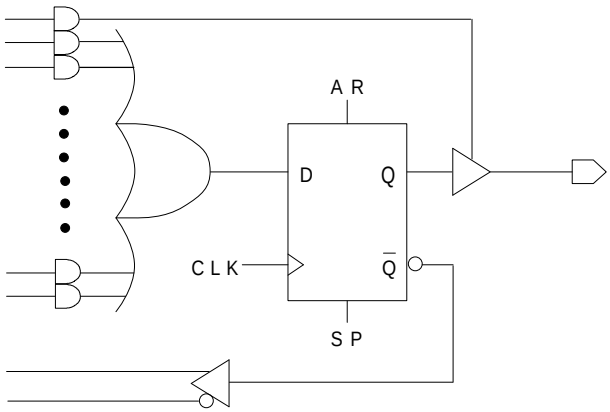
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE



ACTIVE LOW

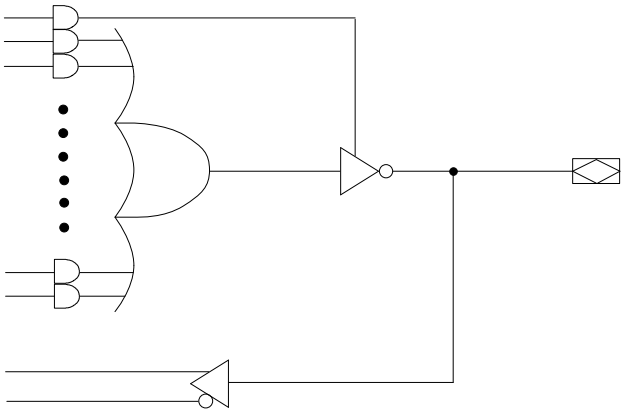
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

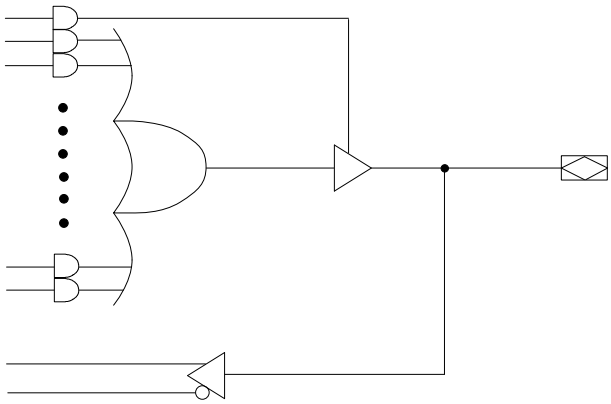
$S_0 = 1$
$S_1 = 0$

COMBINATORIAL MODE



ACTIVE LOW

$S_0 = 0$
$S_1 = 1$

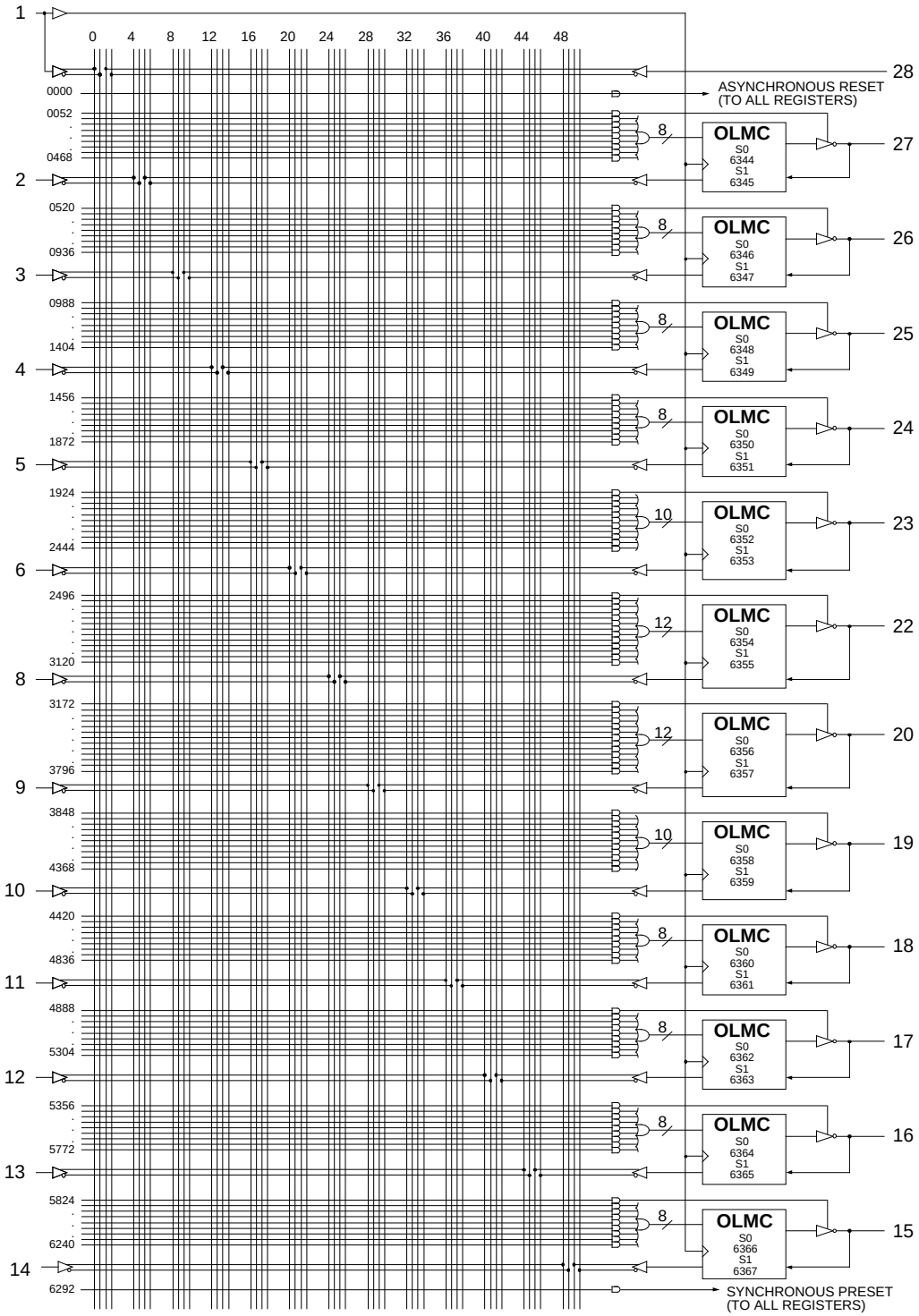


ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

GAL26CV12 LOGIC DIAGRAM / JEDEC FUSE MAP

DIP & PLCC Package Pinouts



6368, 6369 ... Electronic Signature ... 6430, 6431							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0

MSB LSB

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... –40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.5 to +5.5V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–130	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L-7/-10/-15	—	90	130	mA

INDUSTRIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L-10/-15	—	90	150	mA

1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM	TEST COND.[1]	DESCRIPTION	COM -7		COM -10		IND -10		COM / IND -15		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Comb. Output	1	7.5	3	10	1	10	3	15	ns
tco	A	Clock to Output Delay	1	4.5	2	7	1	7	2	8	ns
tcf[2]	—	Clock to Feedback Delay	—	2.5	—	2.5	—	2.5	—	2.5	ns
tsu_1	—	Setup Time, Input or Fdbk before Clk ↑	6	—	7	—	7	—	10	—	ns
tsu_2	—	Setup Time, SP before Clock ↑	6	—	10	—	7	—	10	—	ns
th	—	Hold Time, Input or Fdbk after Clk ↑	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	95.2	—	71.4	—	71.4	—	55.5	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	117.6	—	105	—	105	—	80	—	MHz
	A	Maximum Clock Frequency with No Feedback	142.8	—	105	—	105	—	83.3	—	MHz
twh	—	Clock Pulse Duration, High	3.5	—	4	—	4	—	6	—	ns
twl	—	Clock Pulse Duration, Low	3.5	—	4	—	4	—	6	—	ns
ten	B	Input or I/O to Output Enabled	1	7.5	3	10	1	10	3	15	ns
tdis	C	Input or I/O to Output Disabled	1	7.5	3	10	1	9	3	15	ns
tar	A	Input or I/O to Asynch. Reset of Reg.	1	9	3	13	1	13	3	20	ns
tarw	—	Asynchronous Reset Pulse Duration	7	—	8	—	8	—	10	—	ns
tarr	—	Asynch. Reset to Clk↑ Recovery Time	5	—	8	—	8	—	10	—	ns
tspr	—	Synch. Preset to Clk ↑ Recovery Time	5	—	10	—	10	—	10	—	ns

1) Refer to Switching Test Conditions section.
2) Calculated from fmax with internal feedback. Refer to fmax Specification section.
3) Refer to fmax Specification section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... –40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.5 to +5.5V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–130	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L-10/-15/-20	—	90	130	mA

INDUSTRIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L-15/-20	—	90	150	mA

1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	COM -10		COM / IND -15		COM / IND -20		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinatorial Output	3	10	3	15	3	20	ns
tco	A	Clock to Output Delay	2	7	2	8	2	12	ns
tcf[2]	—	Clock to Feedback Delay	—	2.5	—	2.5	—	10	ns
tsu_1	—	Setup Time, Input or Feedback before Clock ↑	7	—	10	—	12	—	ns
tsu_2	—	Setup Time, SP before Clock ↑	10	—	10	—	12	—	ns
th	—	Hold Time, Input or Feedback after Clock ↑	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	71.4	—	55.5	—	41.6	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	105	—	80	—	45.4	—	MHz
	A	Maximum Clock Frequency with No Feedback	105	—	83.3	—	62.5	—	MHz
twh	—	Clock Pulse Duration, High	4	—	6	—	8	—	ns
twl	—	Clock Pulse Duration, Low	4	—	6	—	8	—	ns
ten	B	Input or I/O to Output Enabled	3	10	3	15	3	20	ns
tdis	C	Input or I/O to Output Disabled	3	10	3	15	3	20	ns
tar	A	Input or I/O to Asynchronous Reset of Register	3	13	3	20	3	25	ns
tarw	—	Asynchronous Reset Pulse Duration	8	—	10	—	15	—	ns
tarr	—	Asynchronous Reset to Clock Recovery Time	8	—	10	—	15	—	ns
tspr	—	Synchronous Preset to Clock Recovery Time	10	—	10	—	12	—	ns

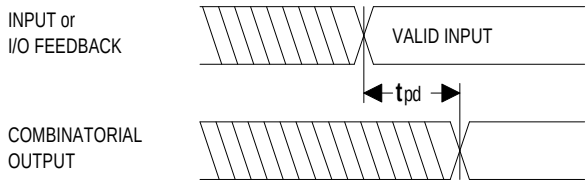
1) Refer to Switching Test Conditions section.
2) Calculated from fmax with internal feedback. Refer to fmax Specification section.
3) Refer to fmax Specification section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

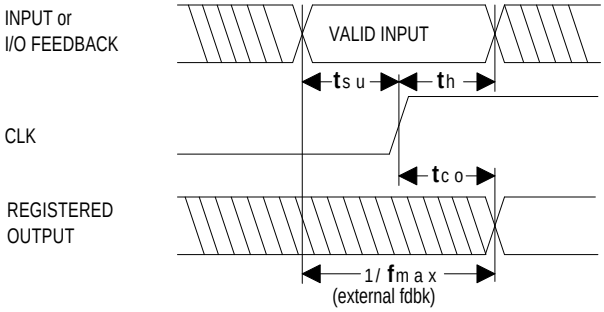
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

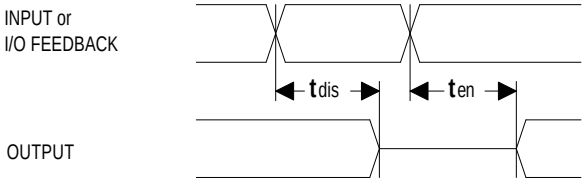
SWITCHING WAVEFORMS



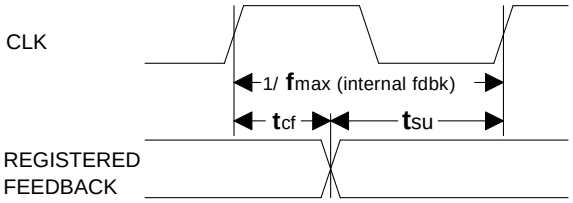
Combinatorial Output



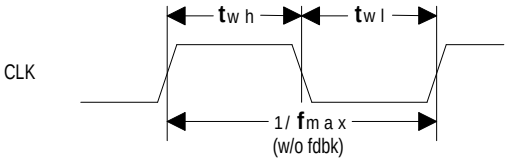
Registered Output



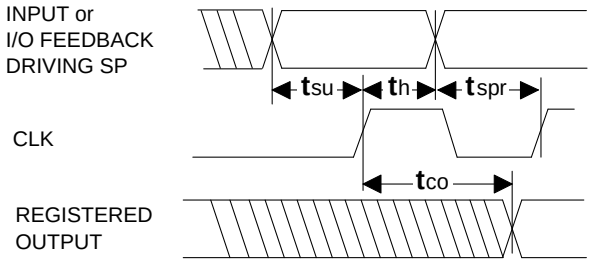
Input or I/O to Output Enable/Disable



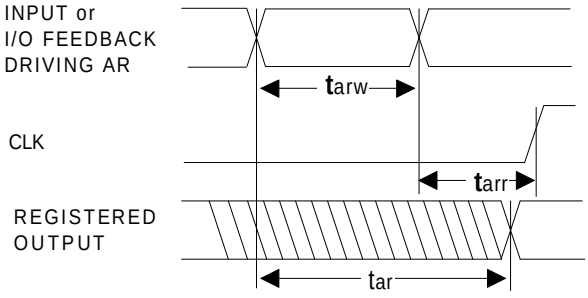
fmax with Feedback



Clock Width

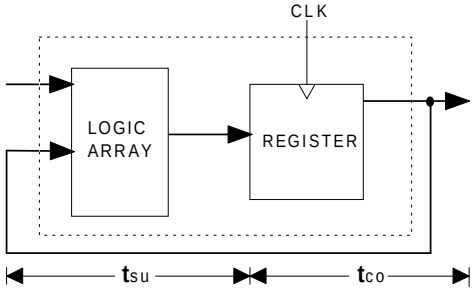


Synchronous Preset



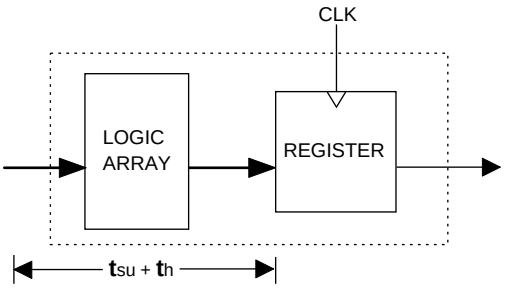
Asynchronous Reset

fmax SPECIFICATIONS



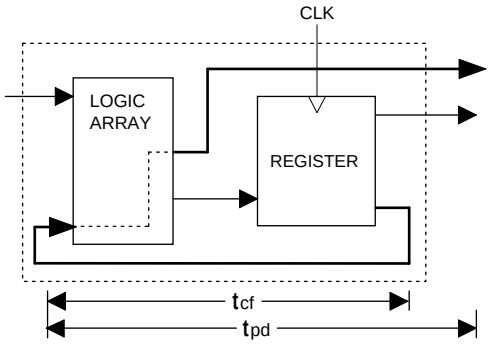
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

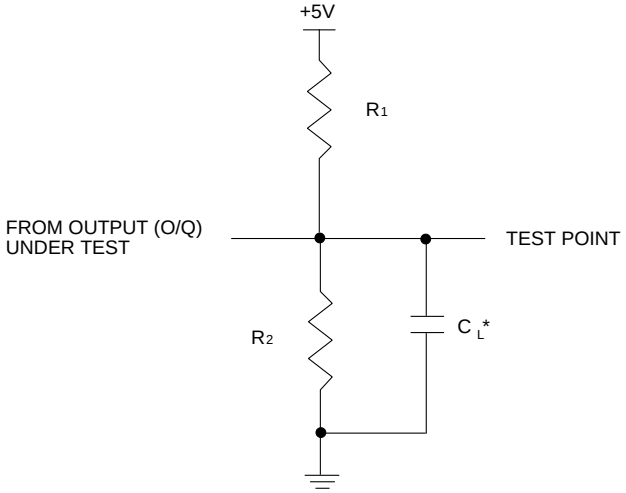
SWITCHING TEST CONDITIONS

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	C-7/-10/-15	1.5ns 10% – 90%
	B-10/-15/-20	3ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See Figure

3-state levels are measured 0.5V from steady-state active level.

GAL26CV12 Output Load Conditions (see figure)

Test Condition		R1	R2	CL
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL26CV12 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

SECURITY CELL

A security cell is provided in every GAL26CV12 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

LATCH-UP PROTECTION

GAL26CV12 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias minimizes the potential for latch-up caused by negative input undershoots. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups in order to eliminate latch-up due to output overshoots.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in normal machine operation. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

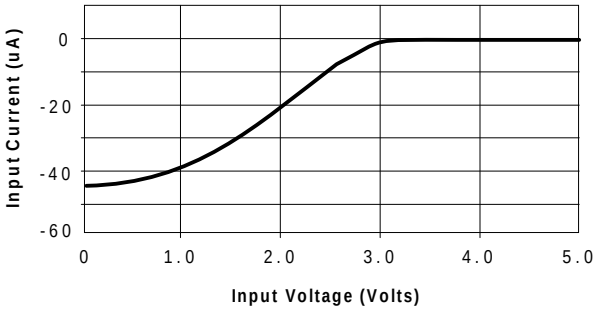
The GAL26CV12 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

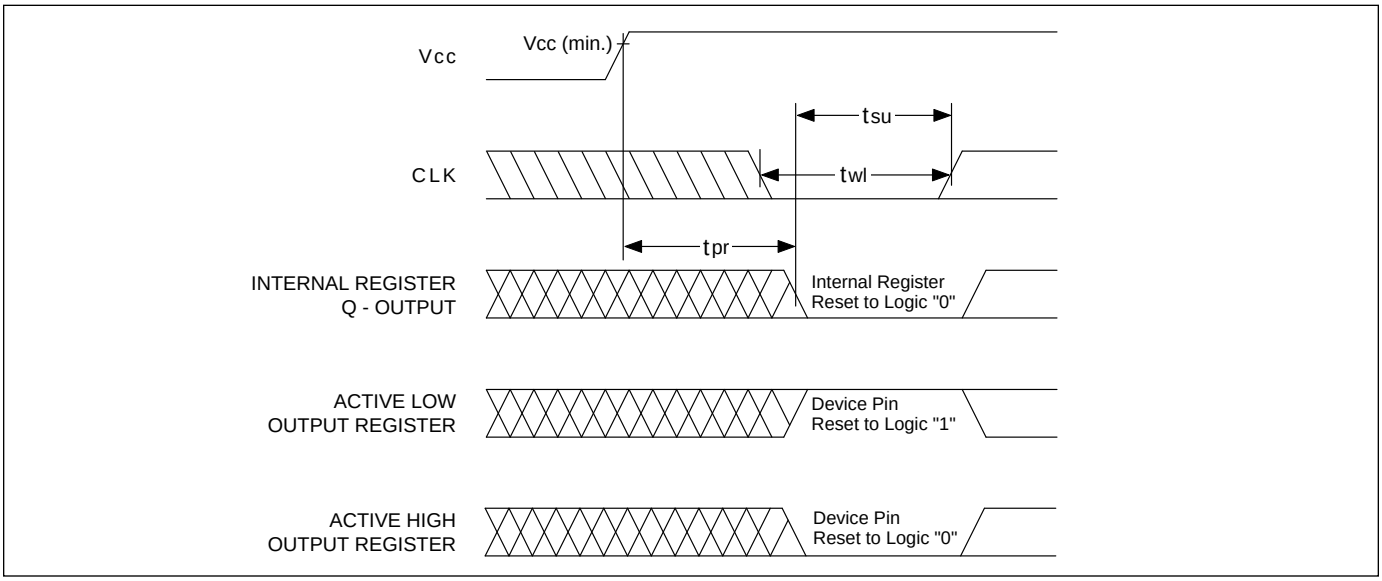
GAL26CV12 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL logic.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device.

Typical Input Current

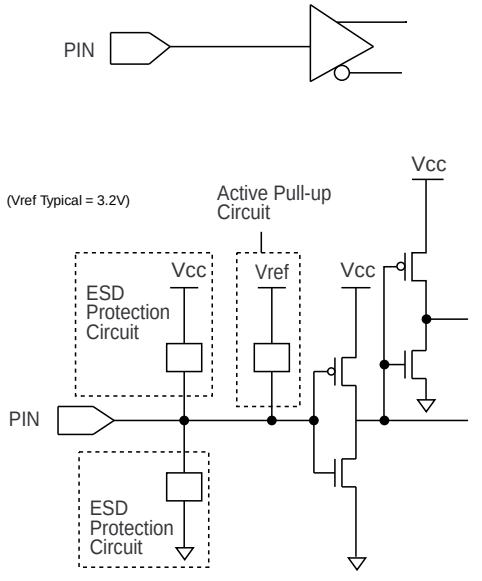


POWER-UP RESET

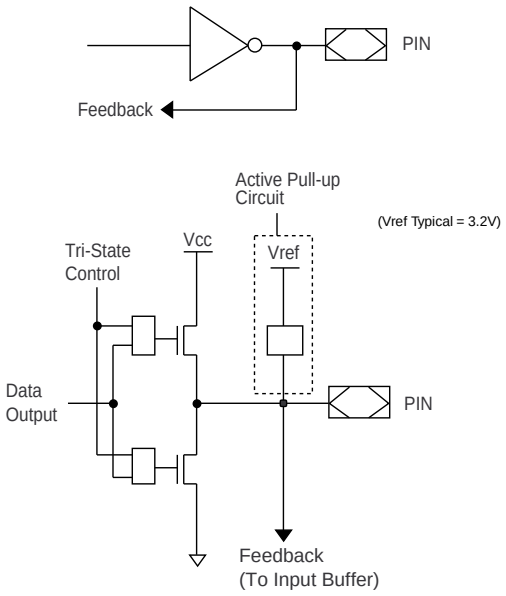


Circuitry within the GAL26CV12 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the device. First, the V_{CC} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



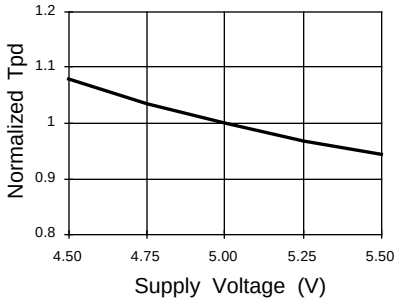
Typical Input



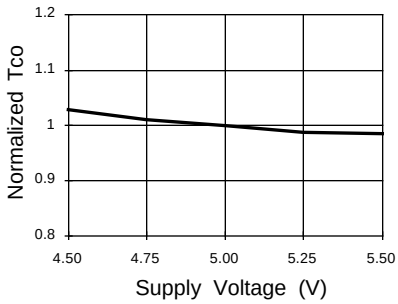
Typical Output

GAL26CV12C: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

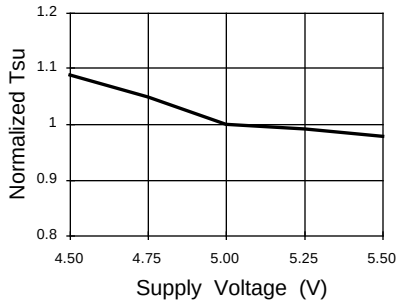
Normalized Tpd vs Vcc



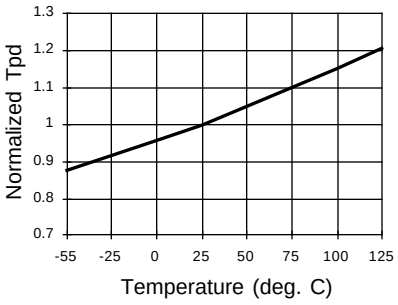
Normalized Tco vs Vcc



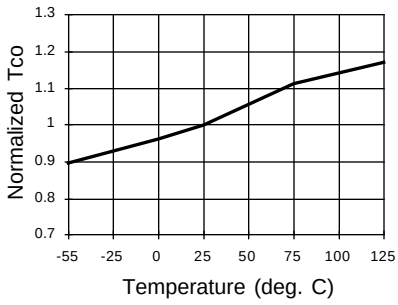
Normalized Tsu vs Vcc



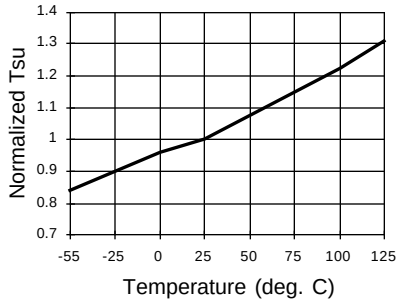
Normalized Tpd vs Temp



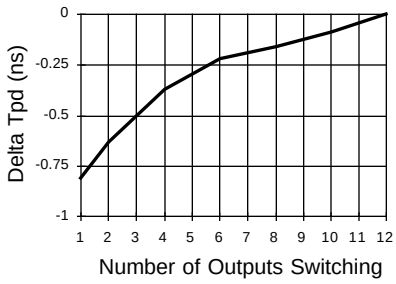
Normalized Tco vs Temp



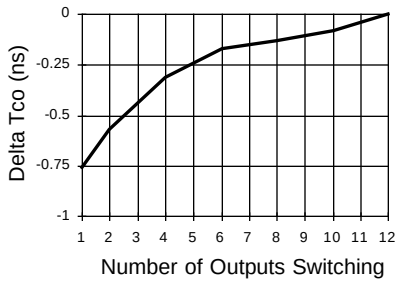
Normalized Tsu vs Temp



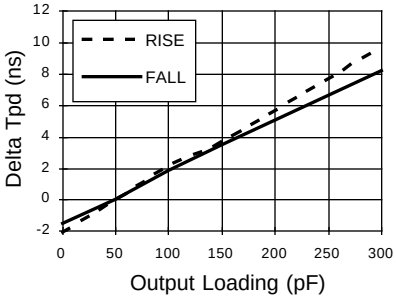
Delta Tpd vs # of Outputs Switching



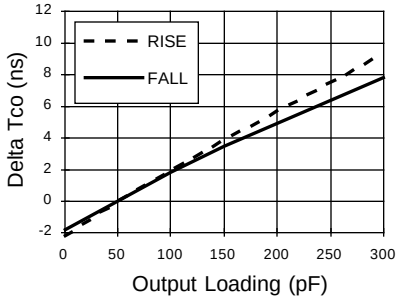
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

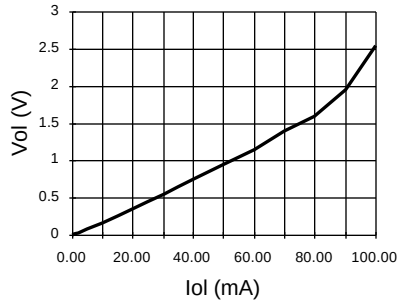


Delta Tco vs Output Loading

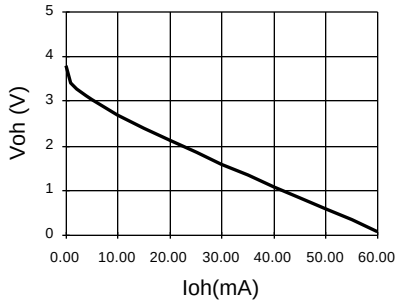


GAL26CV12C: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

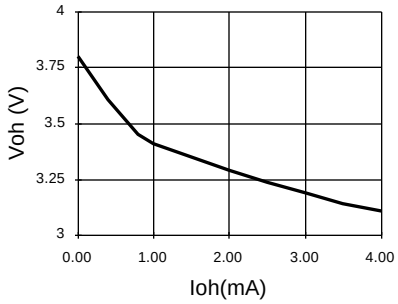
Vol vs Iol



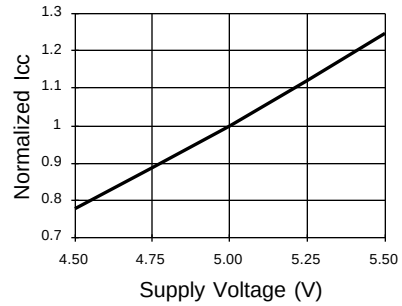
Voh vs Ioh



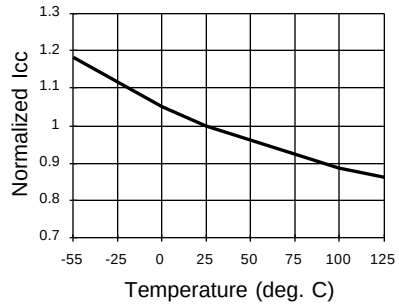
Voh vs Ioh



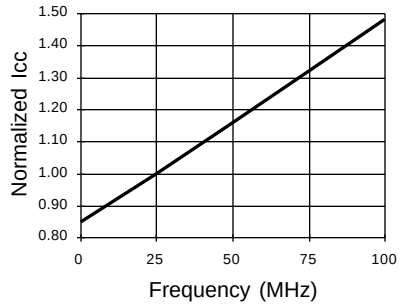
Normalized Icc vs Vcc



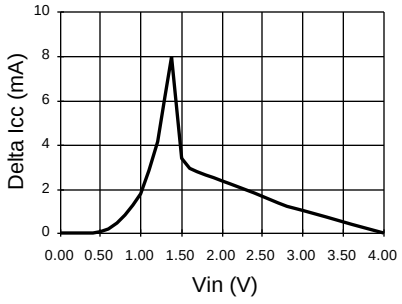
Normalized Icc vs Temp



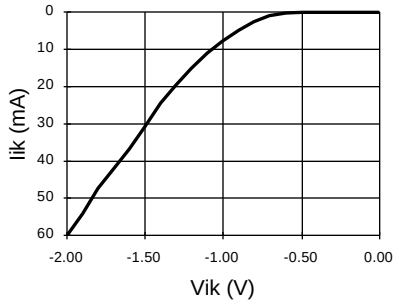
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)

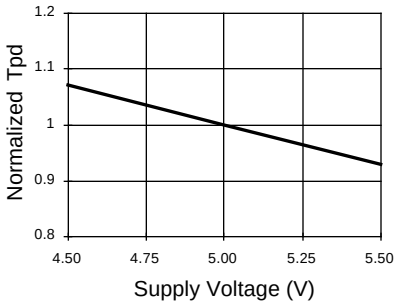


Input Clamp (Vik)

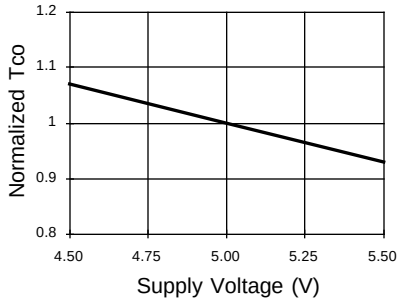


GAL26CV12B: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

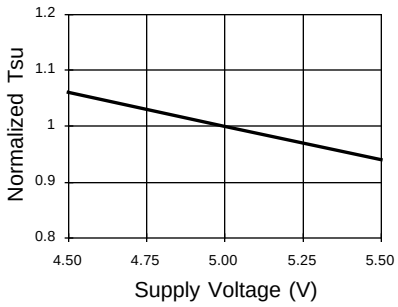
Normalized Tpd vs Vcc



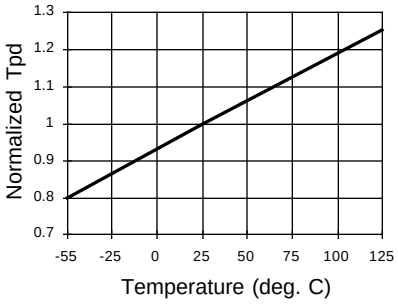
Normalized Tco vs Vcc



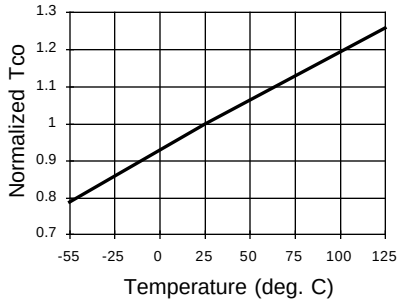
Normalized Tsu vs Vcc



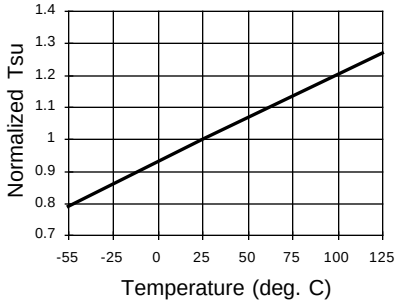
Normalized Tpd vs Temp



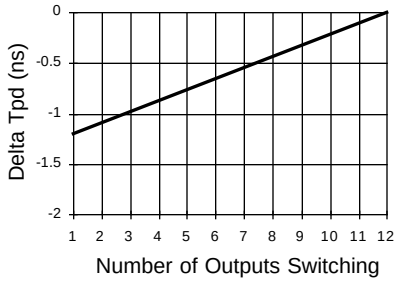
Normalized Tco vs Temp



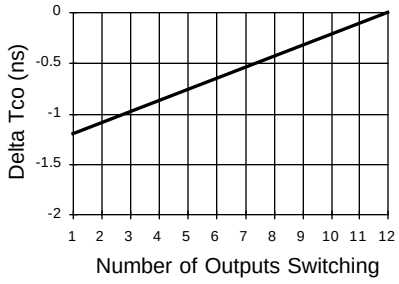
Normalized Tsu vs Temp



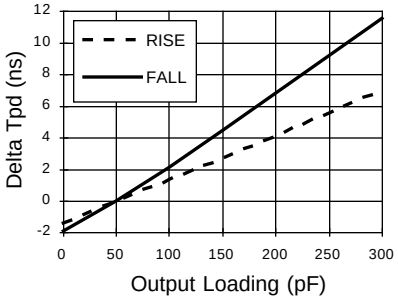
Delta Tpd vs # of Outputs Switching



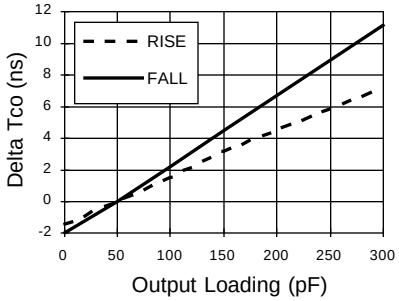
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

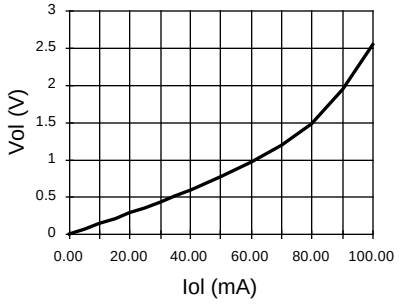


Delta Tco vs Output Loading

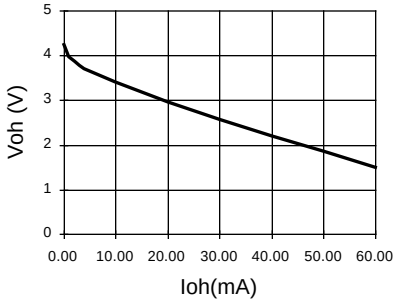


GAL26CV12B: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

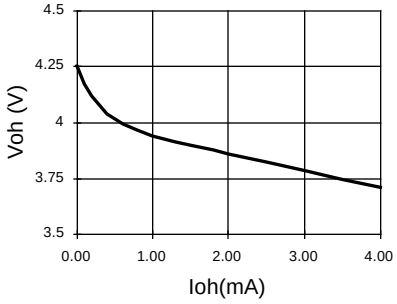
Vol vs Iol



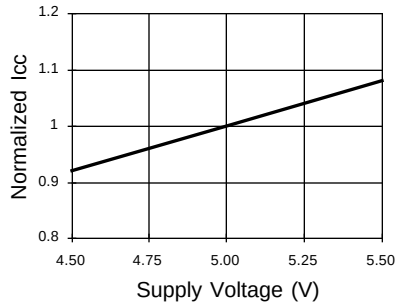
Voh vs Ioh



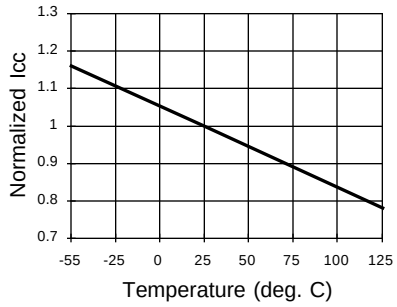
Voh vs Ioh



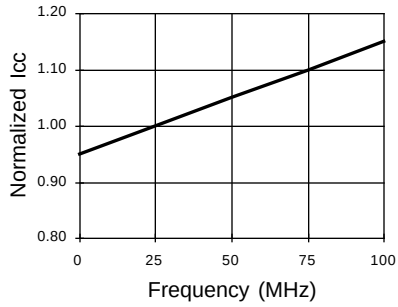
Normalized Icc vs Vcc



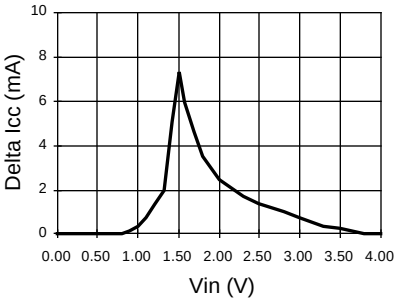
Normalized Icc vs Temp



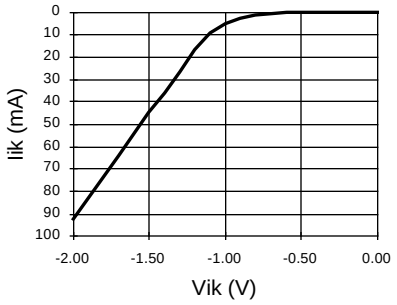
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



GAL6001

High Performance E²CMOS FPLA
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 30ns Maximum Propagation Delay**
  - **— 27MHz Maximum Frequency**
  - **— 12ns Maximum Clock to Output Delay**
  - **— TTL Compatible 16mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **LOW POWER CMOS**
  - **— 90mA Typical Icc**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **UNPRECEDENTED FUNCTIONAL DENSITY**
  - **— 78 x 64 x 36 FPLA Architecture**
  - **— 10 Output Logic Macrocells**
  - **— 8 Buried Logic Macrocells**
  - **— 20 Input and I/O Logic Macrocells**
- **HIGH-LEVEL DESIGN FLEXIBILITY**
  - **— Asynchronous or Synchronous Clocking**
  - **— Separate State Register and Input Clock Pins**
  - **— Functional Superset of Existing 24-pin PAL® and FPLA Devices**
- **APPLICATIONS INCLUDE:**
  - **— Sequencers**
  - **— State Machine Control**
  - **— Multiple PLD Device Integration**

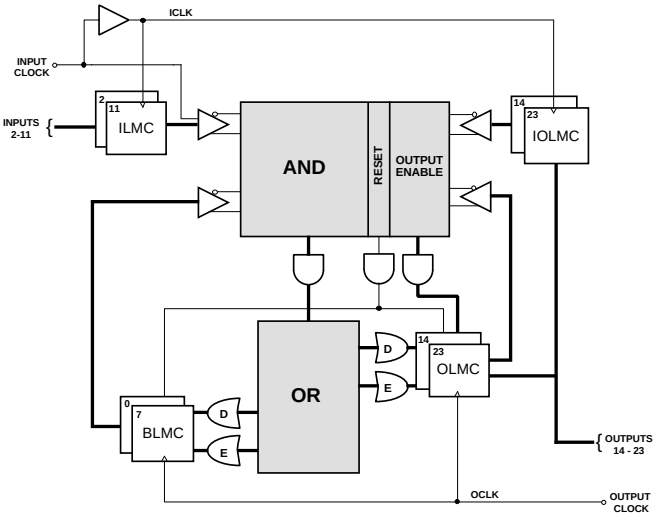
DESCRIPTION

Using a high performance E²CMOS technology, Lattice Semiconductor has produced a next-generation programmable logic device, the GAL6001. Having an FPLA architecture, known for its superior flexibility in state-machine design, the GAL6001 offers a high degree of functional integration and flexibility in a 24-pin, 300-mil package.

The GAL6001 has 10 programmable Output Logic Macrocells (OLMC) and 8 programmable Buried Logic Macrocells (BLMC). In addition, there are 10 Input Logic Macrocells (ILMC) and 10 I/O Logic Macrocells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

Advanced features that simplify programming and reduce test time, coupled with E²CMOS reprogrammable cells, enable 100% AC, DC, programmability, and functionality testing of each GAL6001 during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



MACROCELL NAMES

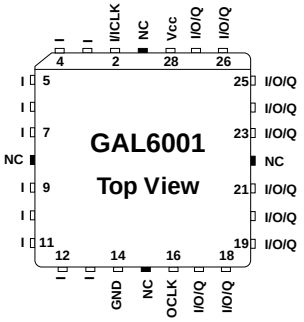
ILMC	INPUT LOGIC MACROCELL
IOLMC	I/O LOGIC MACROCELL
BLMC	BURIED LOGIC MACROCELL
OLMC	OUTPUT LOGIC MACROCELL

PIN NAMES

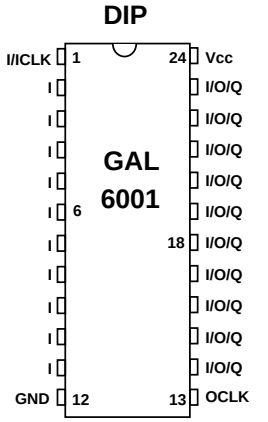
I_0 - I_{10}	INPUT	I/O/Q	BIDIRECTIONAL
ICLK	INPUT CLOCK	V_{CC}	POWER (+5)
OCLK	OUTPUT CLOCK	GND	GROUND

PIN CONFIGURATION

PLCC



DIP



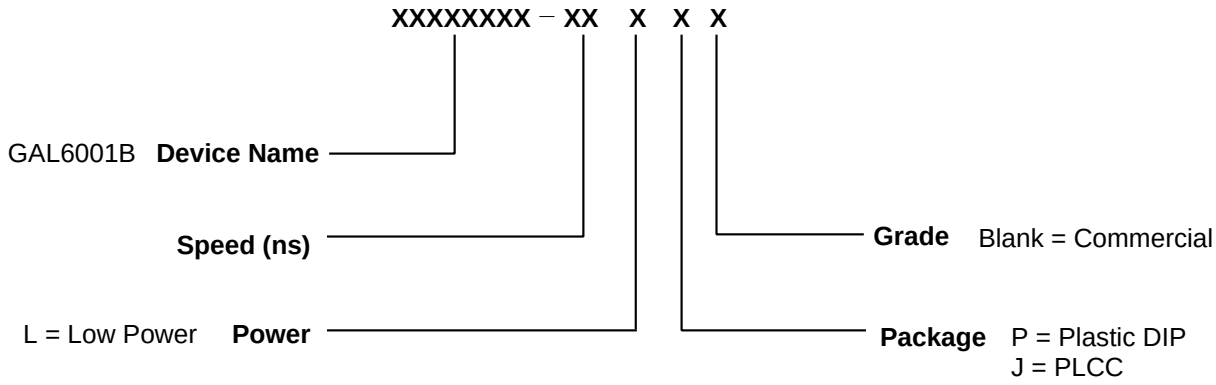
LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL6001 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Fmax (MHz)	Icc (mA)	Ordering #	Package
30	27	150	GAL6001B-30LP	24-Pin Plastic DIP
		150	GAL6001B-30LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



INPUT LOGIC MACROCELL (ILMC) AND I/O LOGIC MACROCELL (IOLMC)

The GAL6001 features two configurable input sections. The ILMC section corresponds to the dedicated input pins (2-11) and the IOLMC to the I/O pins (14-23). Each input section is configurable as a block for asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells or as a clock input for registered macrocells. Configurable input blocks provide system designers with unparalleled design flexibility. With the GAL6001, external registers and latches are not necessary.

Both the ILMC and the IOLMC are block configurable. However, the ILMC can be configured independently of the IOLMC. The three valid macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

OUTPUT LOGIC MACROCELL (OLMC) AND BURIED LOGIC MACROCELL (BLMC)

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the Buried Logic Macrocells (BLMC), and are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic Macrocells (OLMC).

The Output and Buried Logic Macrocells are configurable on a macrocell by macrocell basis. Buried and Output Logic Macrocells may be set to one of three configurations: combinatorial, D-type register with sum term (asynchronous) clock, or D/E-type register. Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selected through the “D” XOR. Polarity selection is available for BLMCs, since both the true and complemented forms of their outputs are available in the AND array. Polarity of all “E” sum terms is selected through the “E” XOR.

When the macrocell is configured as a D/E type register, it is clocked from the common OCLK and the register clock enable input is controlled by the associated “E” sum term. This configuration is useful for building counters and state-machines with state hold functions.

When the macrocell is configured as a D-type register with a sum term clock, the register is always enabled and its “E” sum term is routed directly to the clock input. This permits asynchronous programmable clocking, selected on a register-by-register basis.

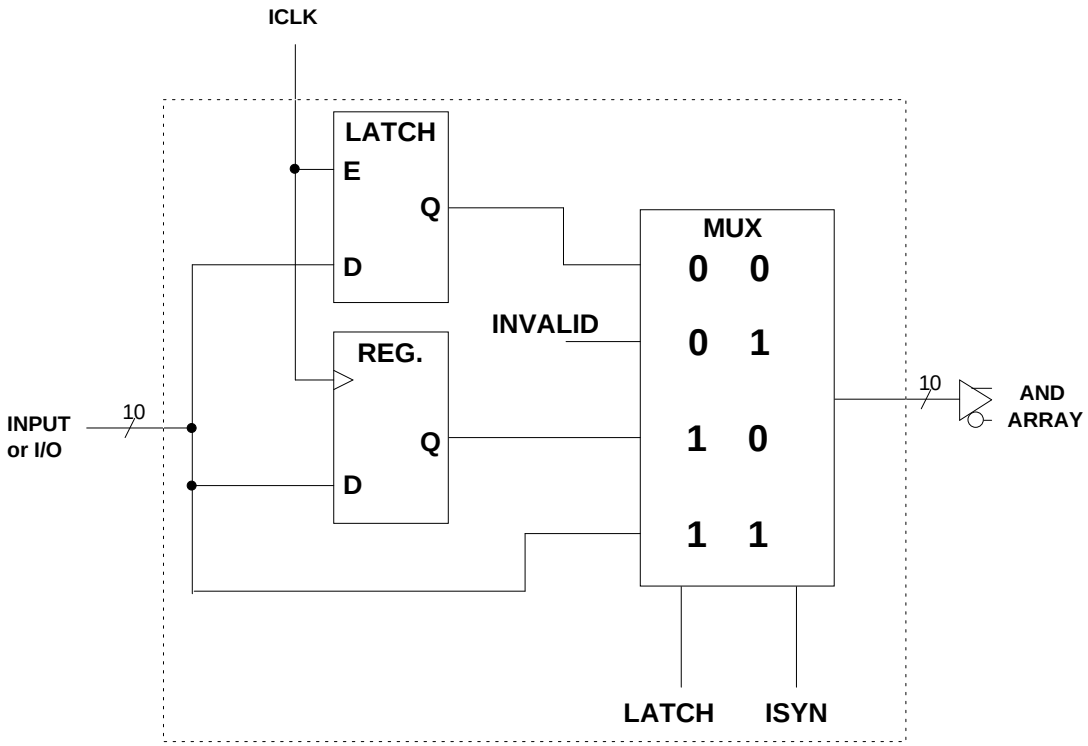
Registers in both the Output and Buried Logic Macrocells feature a common RESET product term. This active high product term allows the registers to be asynchronously reset. Registers are reset to a logic zero. If connected to an output pin, a logic one will occur because of the inverting output buffer.

There are two possible feedback paths from each OLMC. The first path is directly from the OLMC (this feedback is before the output buffer and always present). When the OLMC is used as an output, the second feedback path is through the IOLMC. With this dual feedback arrangement, the OLMC can be permanently buried (the associated OLMC pin is an input), or dynamically buried with the use of the output enable product term.

The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register architecture can emulate RS-, JK-, and T-type registers with the same efficiency as a dedicated RS-, JK-, or T-register.

The three macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

ILMC AND IOLMC CONFIGURATIONS



ILMC/IOLMC

Generic Logic Block Diagram

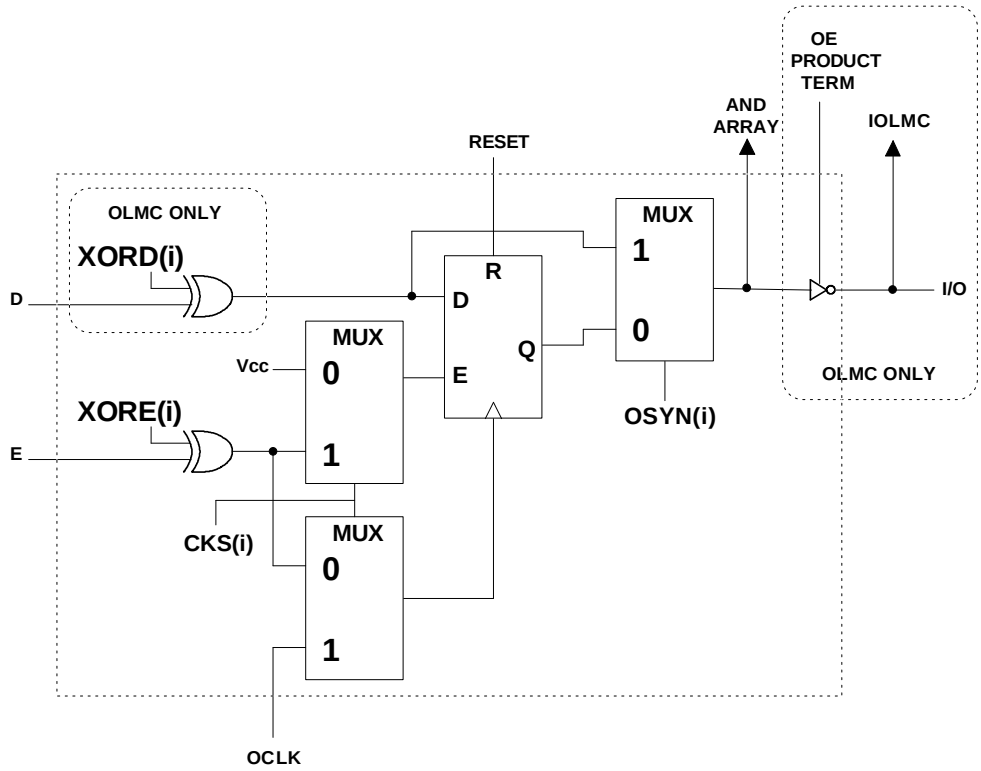
ILMC (Input Logic Macrocell)
JEDEC Fuse Numbers

ISYN	LATCH
8218	8219

IOLMC (I/O Logic Macrocell)
JEDEC Fuse Numbers

ISYN	LATCH
8220	8221

OLMC AND BLMC CONFIGURATIONS



OLMC/BLMC

Generic Logic Block Diagram

OLMC (Output Logic Macrocell)

JEDEC Fuse Numbers

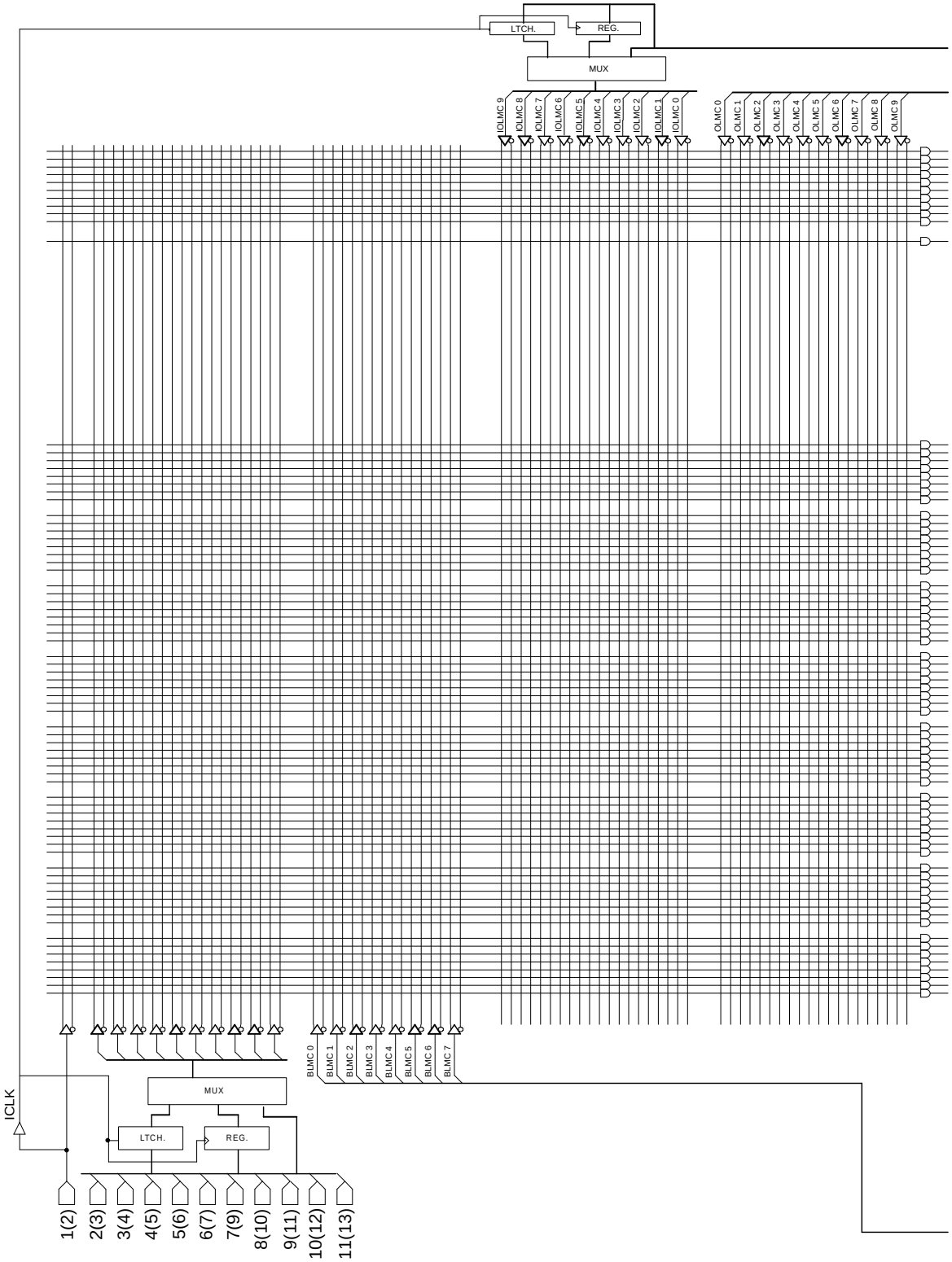
OLMC	OCLK	OSYN	XORE	XORD
0	8178	8179	8180	8181
1	8182	8183	8184	8185
2	8186	8187	8188	8189
3	8190	8191	8192	8193
4	8194	8195	8196	8197
5	8198	8199	8200	8201
6	8202	8203	8204	8205
7	8206	8207	8208	8209
8	8210	8211	8212	8213
9	8214	8215	8216	8217

BLMC (Buried Logic Macrocell)

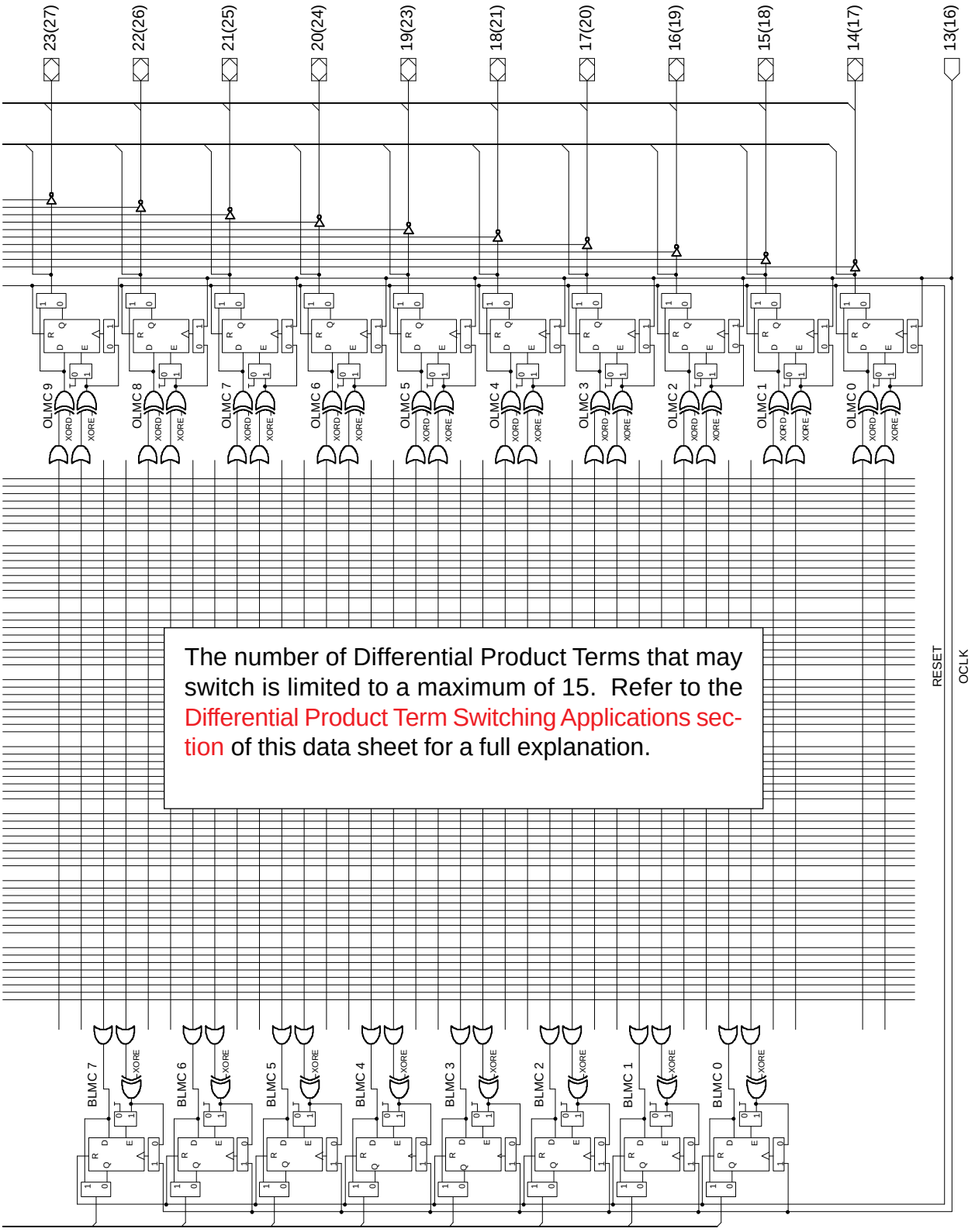
JEDEC Fuse Numbers

BLMC	OCLK	OSYN	XORE
7	8175	8176	8177
6	8172	8173	8174
5	8169	8170	8171
4	8166	8167	8168
3	8163	8164	8165
2	8160	8161	8162
1	8157	8158	8159
0	8154	8155	8156

GAL6001 LOGIC DIAGRAM



GAL6001 LOGIC DIAGRAM (Cont.)



The number of Differential Product Terms that may switch is limited to a maximum of 15. Refer to the Differential Product Term Switching Applications section of this data sheet for a full explanation.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V_{IH} \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V	–30	—	–130	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -30	—	90	150	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

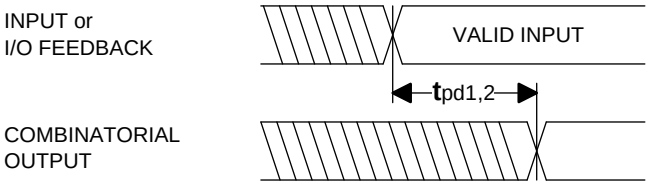
AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

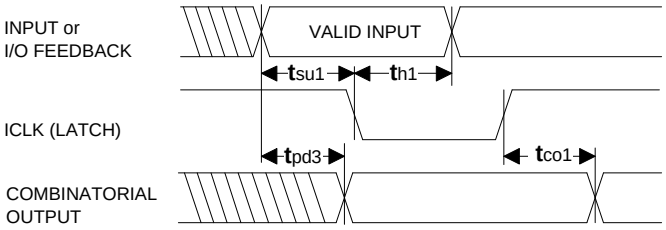
PARAMETER	TEST COND[1].	DESCRIPTION	COM -30 MIN.	COM -30 MAX.	UNITS
tpd1	A	Combinatorial Input to Combinatorial Output	—	30	ns
tpd2	A	Feedback or I/O to Combinatorial Output	—	30	ns
tpd3	A	Transparent Latch Input to Combinatorial Output	—	35	ns
tco1	A	Input Latch ICLK to Combinatorial Output Delay	—	35	ns
tco2	A	Input Reg. ICLK to Combinatorial Output Delay	—	35	ns
tco3	A	Output D/E Reg. OCLK to Output Delay	—	12	ns
tco4	A	Output D Reg. Sum Term CLK to Output Delay	—	35	ns
tsu1	—	Setup Time, Input before Input Latch ICLK	2.5	—	ns
tsu2	—	Setup Time, Input before Input Reg. ICLK	2.5	—	ns
tsu3	—	Setup Time, Input or Feedback before D/E Reg. OCLK	25	—	ns
tsu4	—	Setup Time, Input or Feedback before D Reg. Sum Term CLK	7.5	—	ns
tsu5	—	Setup Time, Input Reg. ICLK before D/E Reg. OCLK	30	—	ns
tsu6	—	Setup Time, Input Reg. ICLK before D Reg. Sum Term CLK	15	—	ns
th1	—	Hold Time, Input after Input Latch ICLK	5	—	ns
th2	—	Hold Time, Input after Input Reg. ICLK	5	—	ns
th3	—	Hold Time, Input or Feedback after D/E Reg. OCLK	0	—	ns
th4	—	Hold Time, Input or Feedback after D Reg. Sum Term CLK	10	—	ns
fmax	—	Maximum Clock Frequency, OCLK	27	—	MHz
twh1	—	ICLK or OCLK Pulse Duration, High	10	—	ns
twh2	—	Sum Term CLK Pulse Duration, High	15	—	ns
twl1	—	ICLK or OCLK Pulse Duration, Low	10	—	ns
twl2	—	Sum Term CLK Pulse Duration, Low	15	—	ns
tarw	—	Reset Pulse Duration	15	—	ns
ten	B	Input or I/O to Output Enabled	—	25	ns
tdis	C	Input or I/O to Output Disabled	—	25	ns
tar	A	Input or I/O to Asynchronous Reg. Reset	—	35	ns
tarr1	—	Asynchronous Reset to OCLK Recovery Time	20	—	ns
tarr2	—	Asynchronous Reset to Sum Term CLK Recovery Time	10	—	ns

1) Refer to Switching Test Conditions section.

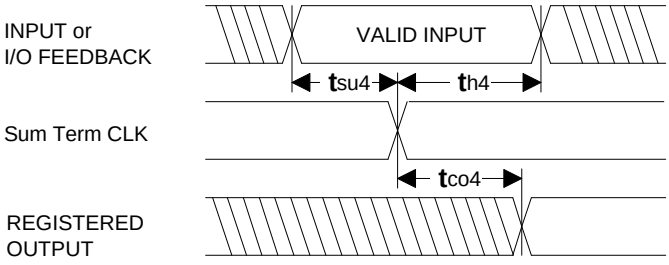
SWITCHING WAVEFORMS



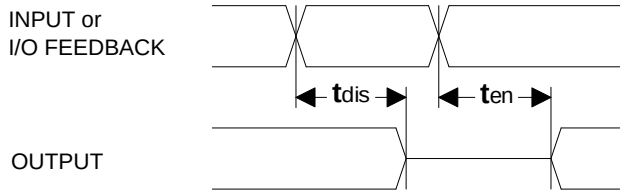
Combinatorial Output



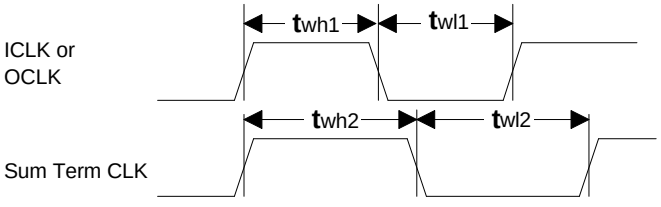
Latched Input



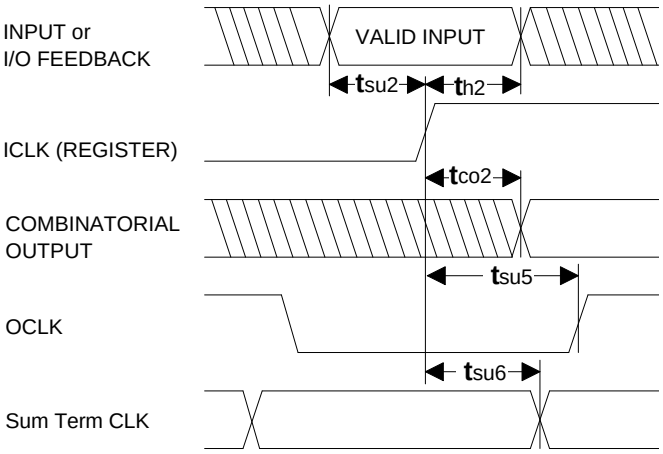
Registered Output (Sum Term CLK)



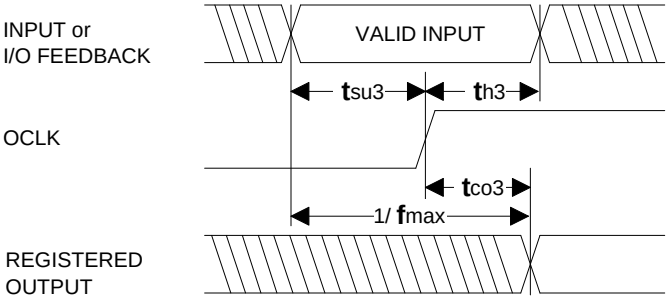
Input or I/O to Output Enable/Disable



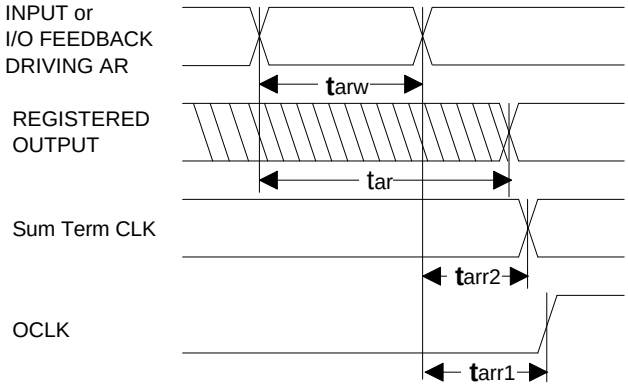
Clock Width



Registered Input

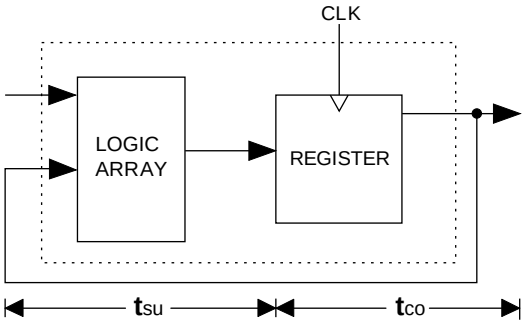


Registered Output (OCLK)



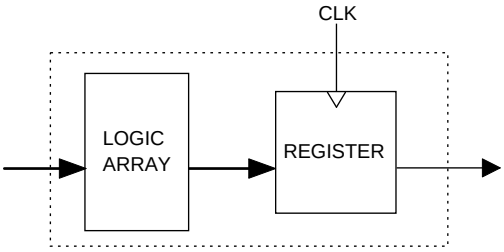
Asynchronous Reset

fmax DESCRIPTIONS



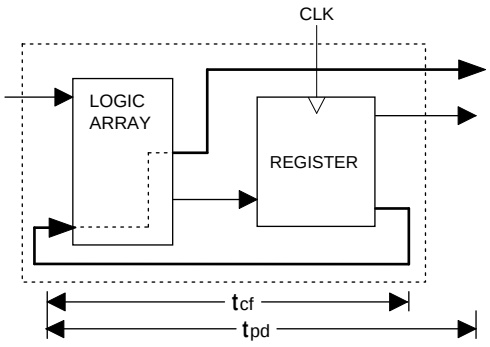
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

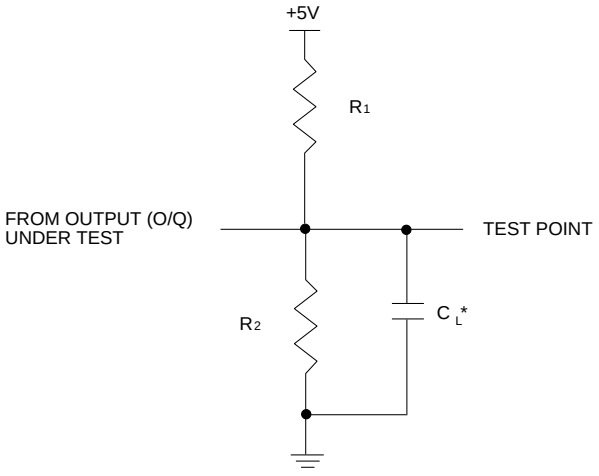
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ARRAY DESCRIPTION

The GAL6001 contains two E^2 reprogrammable arrays. The first is an AND array and the second is an OR array. These arrays are described in detail below.

AND ARRAY

The AND array is organized as 78 inputs by 75 product term outputs. The 10 ILMCs, 10 IOLMCs, 8 BLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise the 39 inputs to this array (each available in true and complement forms). 64 product terms serve as inputs to the OR array. The RESET product term generates the RESET signal described in the Output and Buried Logic Macrocells section. There are 10 output enable product terms which allow device pins 14-23 to be bi-directional or tri-state.

OR ARRAY

The OR array is organized as 64 inputs by 36 sum term outputs. 64 product terms from the AND array serve as the inputs to the OR array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 BLMCs, one "D" term and one "E" term to each.

The programmable OR array offers unparalleled versatility in product term usage. This programmability allows from 1 to 64 product terms to be connected to a single sum term. A programmable OR array is more flexible than a fixed, shared, or variable product term architecture.

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided in every GAL6001 device. It contains 72 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

SECURITY CELL

A security cell is provided in every GAL6001 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND and OR arrays. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal operations. This is because in system operation, certain events may occur that cause the logic to assume an illegal state: power-up, brown out, line voltage glitches, etc. To test a design for proper treatment of these conditions, a method must be provided to break the feedback paths and force any desired state (i.e., illegal) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation.

All of the registers in the GAL6001 can be preloaded, including the ILMC, IOLMC, OLMC, and BLMC registers. In addition, the contents of the state and output registers can be examined in a special diagnostics mode. Programming hardware takes care of all preload timing and voltage requirements.

LATCH-UP PROTECTION

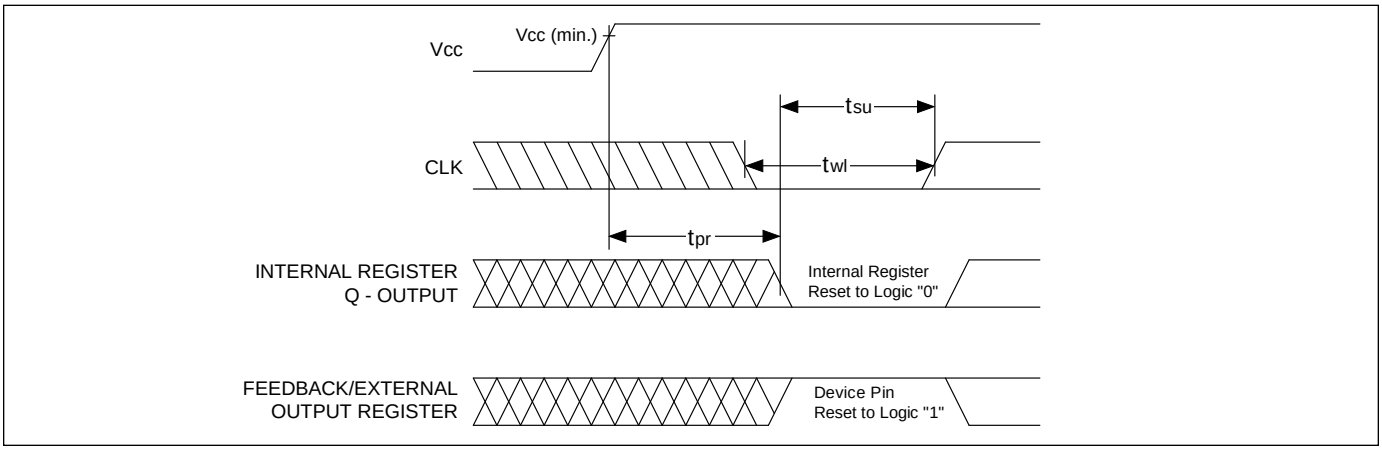
GAL6001 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

GAL devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL6001 devices do not possess active pull-ups within their input structures. As a result, Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce Icc for the device.

POWER-UP RESET



Circuitry within the GAL6001 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL6001. First, the VCC rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

DIFFERENTIAL PRODUCT TERM SWITCHING (DPTS) APPLICATIONS

The number of Differential Product Term Switching (DPTS) for a given design is calculated by subtracting the total number of product terms that are switching from a Logical HI to a Logical LO from those switching from a Logical LO to a Logical HI within a 5ns period. After subtracting take the absolute value.

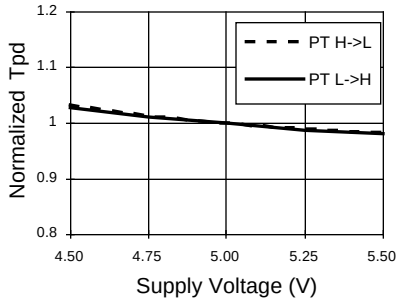
$$DPTS = \left| (P\text{-}Terms)_{LH} - (P\text{-}Terms)_{HL} \right|$$

DPTS restricts the number of product terms that can be switched simultaneously - there is no limit on the number of product terms that can be used.

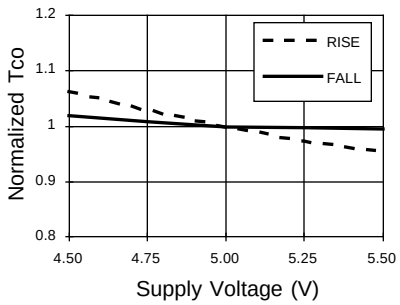
A software utility is available from Lattice Semiconductor Applications Engineering that will perform this calculation on any GAL6001 JEDEC file. This program, DPTS, and additional information may be obtained from your local Lattice Semiconductor representative or by contacting Lattice Semiconductor's Applications Engineering Dept. (Tel: 503-681-0118 or 800-FASTGAL; FAX: 681-3037).

TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

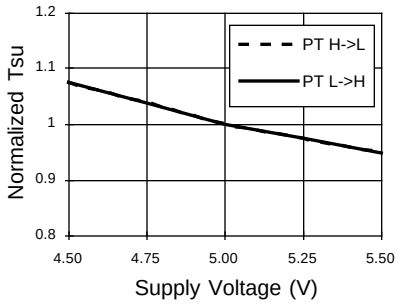
Normalized Tpd vs Vcc



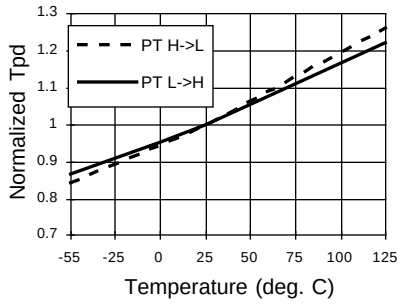
Normalized Tco vs Vcc



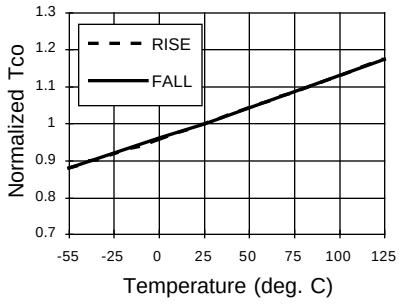
Normalized Tsu vs Vcc



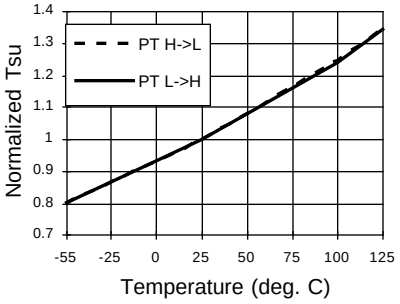
Normalized Tpd vs Temp



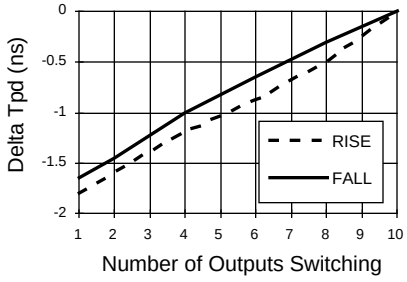
Normalized Tco vs Temp



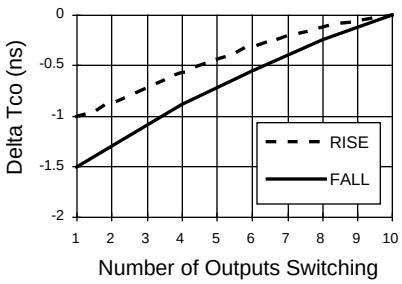
Normalized Tsu vs Temp



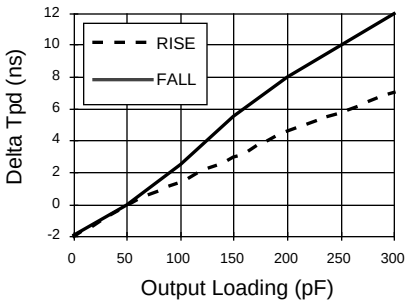
Delta Tpd vs # of Outputs Switching



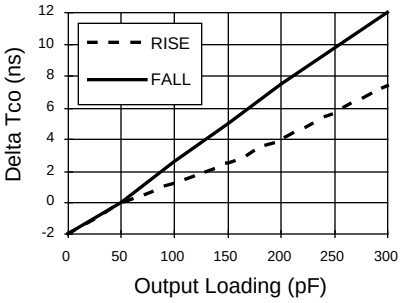
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

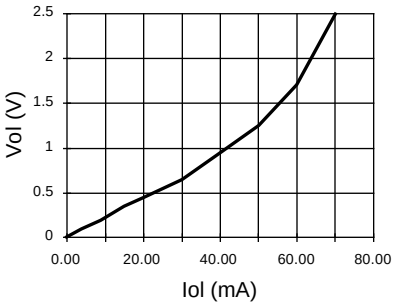


Delta Tco vs Output Loading

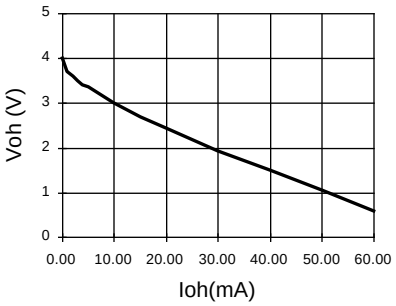


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

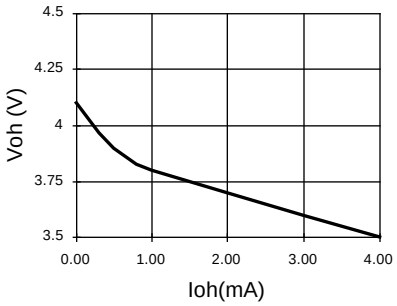
Vol vs Iol



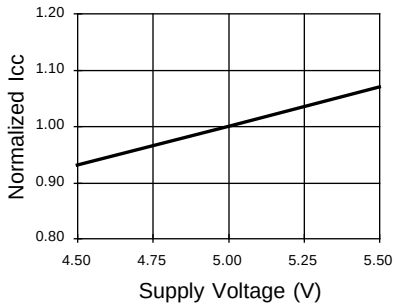
Voh vs Ioh



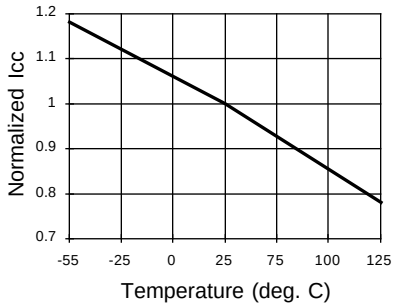
Voh vs Ioh



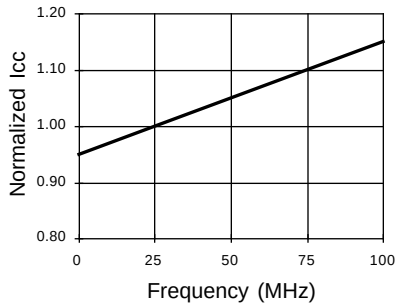
Normalized Icc vs Vcc



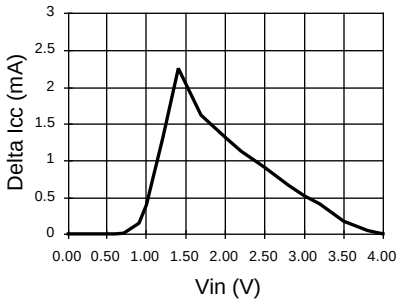
Normalized Icc vs Temp



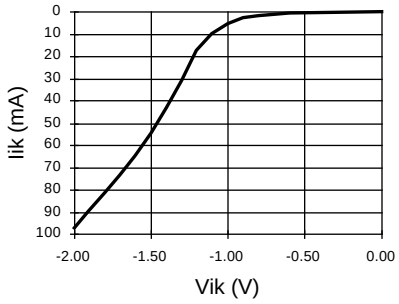
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



GAL6002

High Performance E²CMOS FPLA
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 15ns Maximum Propagation Delay**
  - **— 75MHz Maximum Frequency**
  - **— 6.5ns Maximum Clock to Output Delay**
  - **— TTL Compatible 16mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **ACTIVE PULL-UPS ON ALL PINS**
- **LOW POWER CMOS**
  - **— 90mA Typical Icc**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **UNPRECEDENTED FUNCTIONAL DENSITY**
  - **— 78 x 64 x 36 FPLA Architecture**
  - **— 10 Output Logic Macrocells**
  - **— 8 Buried Logic Macrocells**
  - **— 20 Input and I/O Logic Macrocells**
- **HIGH-LEVEL DESIGN FLEXIBILITY**
  - **— Asynchronous or Synchronous Clocking**
  - **— Separate State Register and Input Clock Pins**
  - **— Functional Superset of Existing 24-pin PAL® and FPLA Devices**
- **APPLICATIONS INCLUDE:**
  - **— Sequencers**
  - **— State Machine Control**
  - **— Multiple PLD Device Integration**

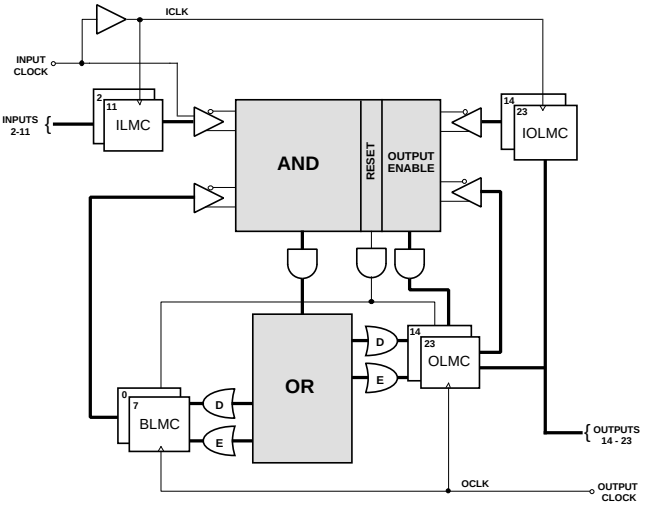
DESCRIPTION

Having an FPLA architecture, the GAL6002 provides superior flexibility in state-machine design. The GAL6002 offers the highest degree of functional integration, flexibility, and speed currently available in a 24-pin, 300-mil package. E²CMOS technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The GAL6002 has 10 programmable Output Logic Macrocells (OLMC) and 8 programmable Buried Logic Macrocells (BLMC). In addition, there are 10 Input Logic Macrocells (ILMC) and 10 I/O Logic Macrocells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacturing. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



MACROCELL NAMES

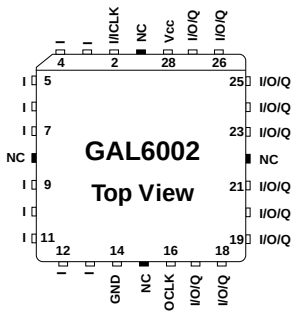
ILMC	INPUT LOGIC MACROCELL
IOLMC	I/O LOGIC MACROCELL
BLMC	BURIED LOGIC MACROCELL
OLMC	OUTPUT LOGIC MACROCELL

PIN NAMES

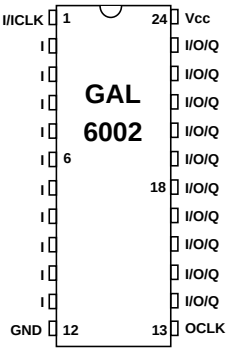
I_0 - I_{10}	INPUT	I/O/Q	BIDIRECTIONAL
ICLK	INPUT CLOCK	V_{CC}	POWER (+5V)
OCLK	OUTPUT CLOCK	GND	GROUND

PIN CONFIGURATION

PLCC



DIP



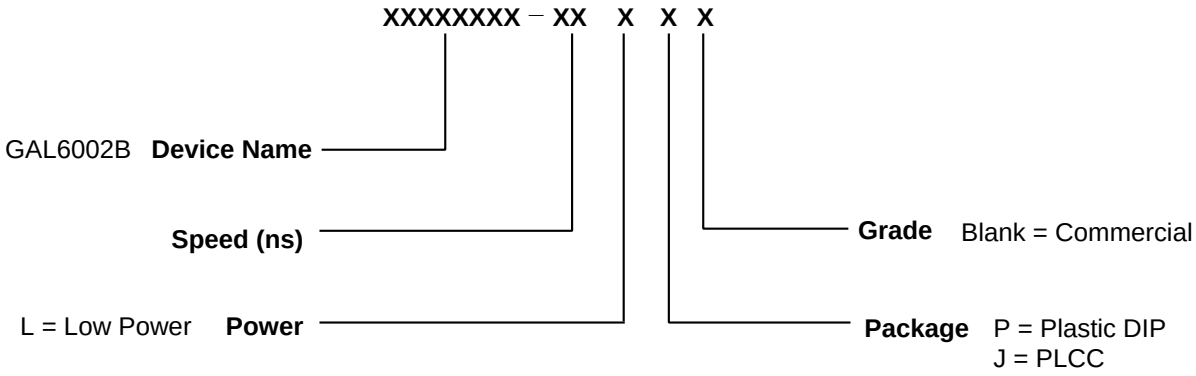
LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

GAL6002 COMMERCIAL DEVICE ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Fmax (MHz)	Icc (mA)	Ordering #	Package
15	75	135	GAL6002B-15LP	24-Pin Plastic DIP
		135	GAL6002B-15LJ	28-Lead PLCC
20	60	135	GAL6002B-20LP	24-Pin Plastic DIP
		135	GAL6002B-20LJ	28-Lead PLCC

PART NUMBER DESCRIPTION



INPUT LOGIC MACROCELL (ILMC) AND I/O LOGIC MACROCELL (IOLMC)

The GAL6002 features two configurable input sections. The ILMC section corresponds to the dedicated input pins (2-11) and the IOLMC to the I/O pins (14-23). Each input section is individually configurable as asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells or as a clock input for registered macrocells. Individually configurable inputs provide system designers with unparalleled design flexibility. With the GAL6002, external input registers and latches are not necessary.

Both the ILMC and the IOLMC are individually configurable and the ILMC can be configured independently of the IOLMC. The three valid macrocell configurations and its associated fuse numbers are shown in the diagrams on the following pages. Note that these programmable cells are configured by the logic compiler software. The user does not need to manually manipulate these architecture bits.

OUTPUT LOGIC MACROCELL (OLMC) AND BURIED LOGIC MACROCELL (BLMC)

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the Buried Logic Macrocells (BLMC), and are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic Macrocells (OLMC).

The Output and Buried Logic Macrocells are configurable on a macrocell by macrocell basis. Buried and Output Logic Macrocells may be set to one of three configurations: combinational, D-type register with sum term (asynchronous) clock, or D/E-type register. Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selected through the programmable polarity control cell called XORD. Polarity selection for BLMCs is selected through the true and complement forms of their feedbacks to the AND array. Polarity of all E (Enable) sum terms is selected through the XORE programmable cells.

When the output or buried logic macrocell is configured as a D/E type register, the register is clocked from the common OCLK and the register clock enable input is controlled by the associated "E" sum term. This configuration is useful for building counters and state-machines with count hold and state hold functions.

When the macrocell is configured as a D type register with a sum term clock, the register is always enabled and the associated “E” sum term is routed directly to the clock input. This permits asynchronous programmable clocking, selected on a register-by-register basis.

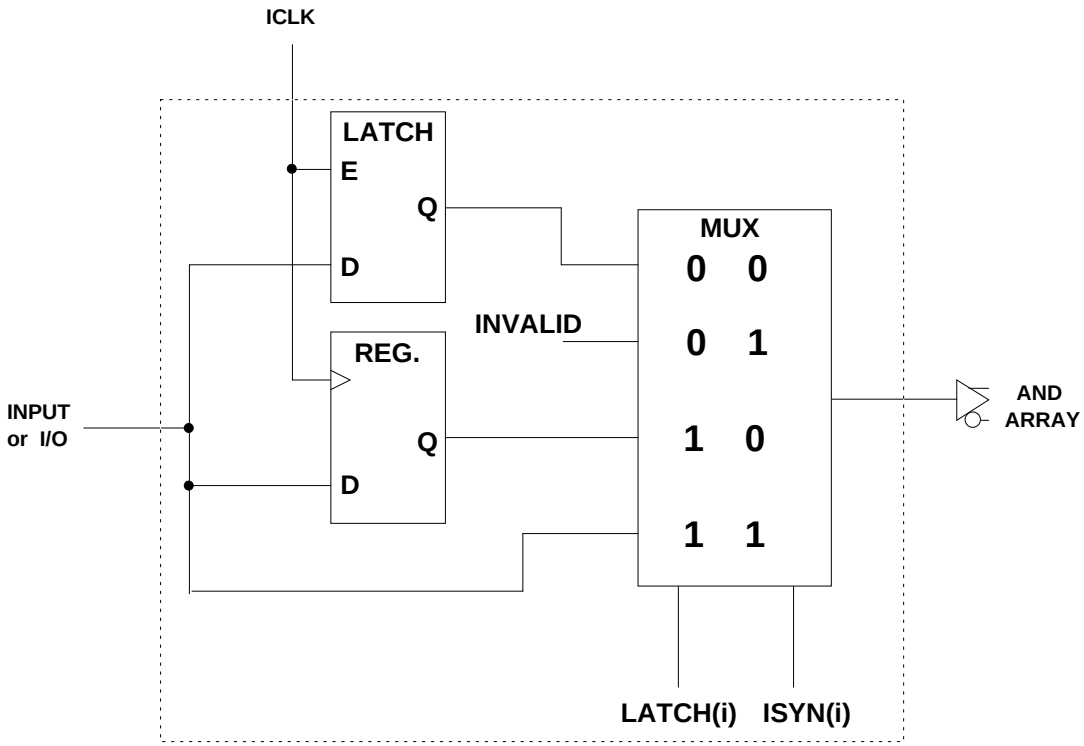
Registers in both the Output and Buried Logic Macrocells feature a common RESET product term. This active high product term allows the registers to be asynchronously reset. All registers reset to logic zero. With the inverting output buffers, the output pins will reset to logic one.

There are two possible feedback paths from each OLMC. The first path is directly from the OLMC (this feedback is before the output buffer). When the OLMC is used as an output, the second feedback path is through the IOLMC. With this dual feedback arrangement, the OLMC can be permanently buried without losing the use of the associated OLMC pin as an input, or dynamically buried with the use of the output enable product term.

The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register architecture can emulate RS, JK, and T registers with the same efficiency as a dedicated RS, JK, or T registers.

The three macrocell configurations are shown in the diagrams on the following pages. These programmable cells are also configured by the logic compiler software. The user does not need to manually manipulate these architecture bits.

ILMC AND IOLMC CONFIGURATIONS



ILMC/IOLMC
Generic Logic Block Diagram

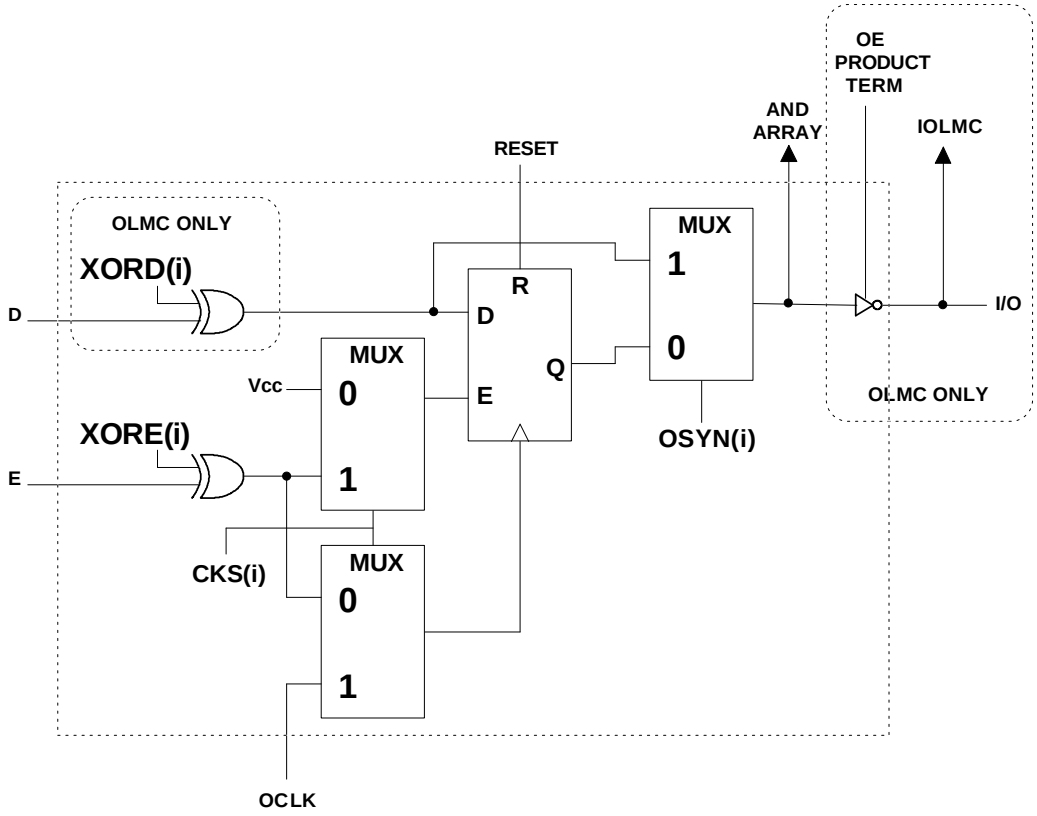
Input Macrocell JEDEC Fuse Numbers

INSYNC	INLATCH	ILMC
8218	8219	0
8220	8221	1
8222	8223	2
8224	8225	3
8226	8227	4
8228	8229	5
8230	8231	6
8232	8233	7
8234	8235	8
8236	8237	9

I/O Macrocell JEDEC Fuse Numbers

IOSYNC	IOLATCH	IOLMC
8238	8239	9
8240	8241	8
8242	8243	7
8244	8245	6
8246	8247	5
8248	8249	4
8250	8251	3
8252	8253	2
8254	8255	1
8256	8257	0

OLMC AND BLMC CONFIGURATIONS



OLMC/BLMC
Generic Logic Block Diagram

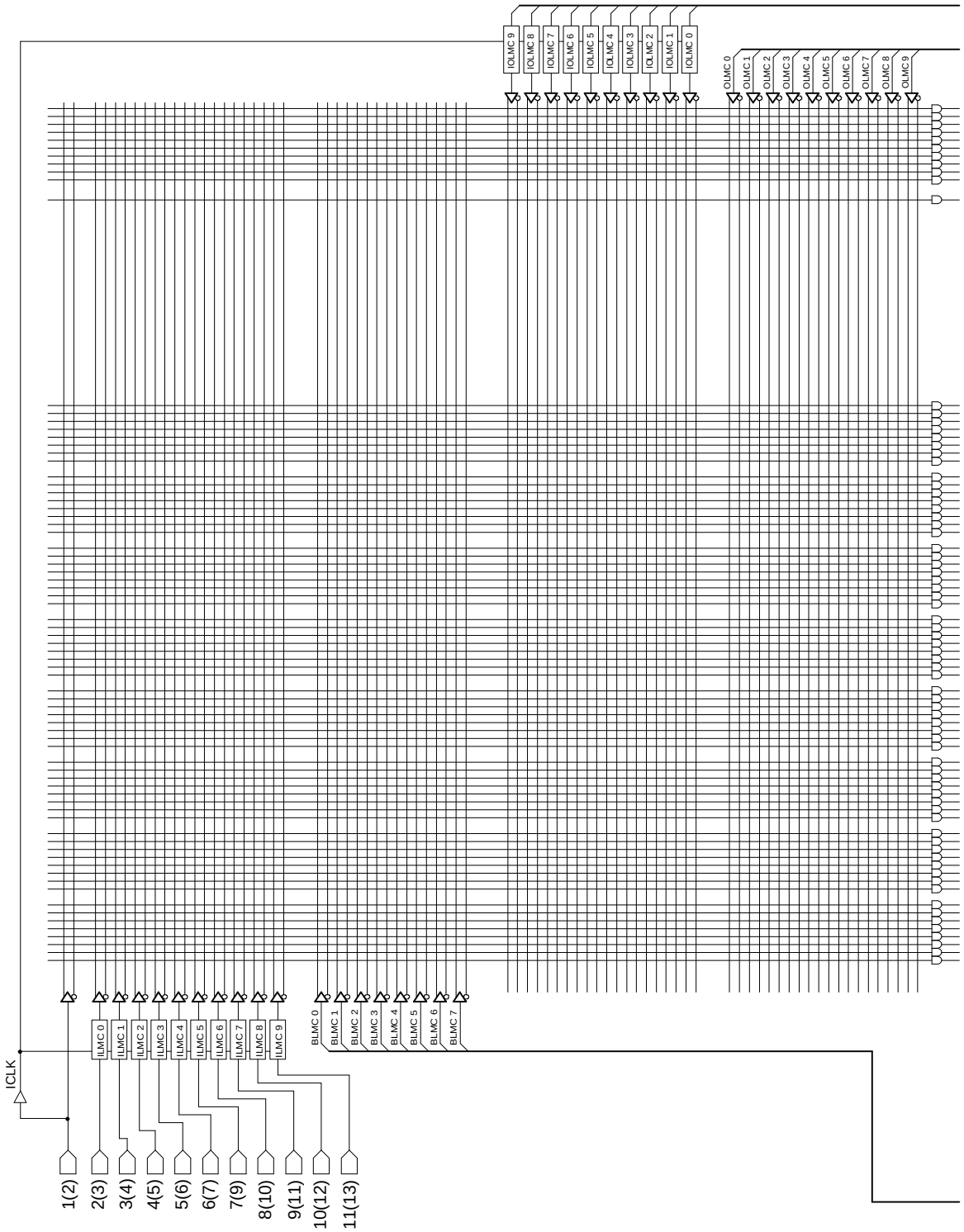
OLMC JEDEC Fuse Numbers

OLMC	CKS	OUTSYNC	XORE	XORD
0	8178	8179	8180	8181
1	8182	8183	8184	8185
2	8186	8187	8188	8189
3	8190	8191	8192	8193
4	8194	8195	8196	8197
5	8198	8199	8200	8201
6	8202	8203	8204	8205
7	8206	8207	8208	8209
8	8210	8211	8212	8213
9	8214	8215	8216	8217

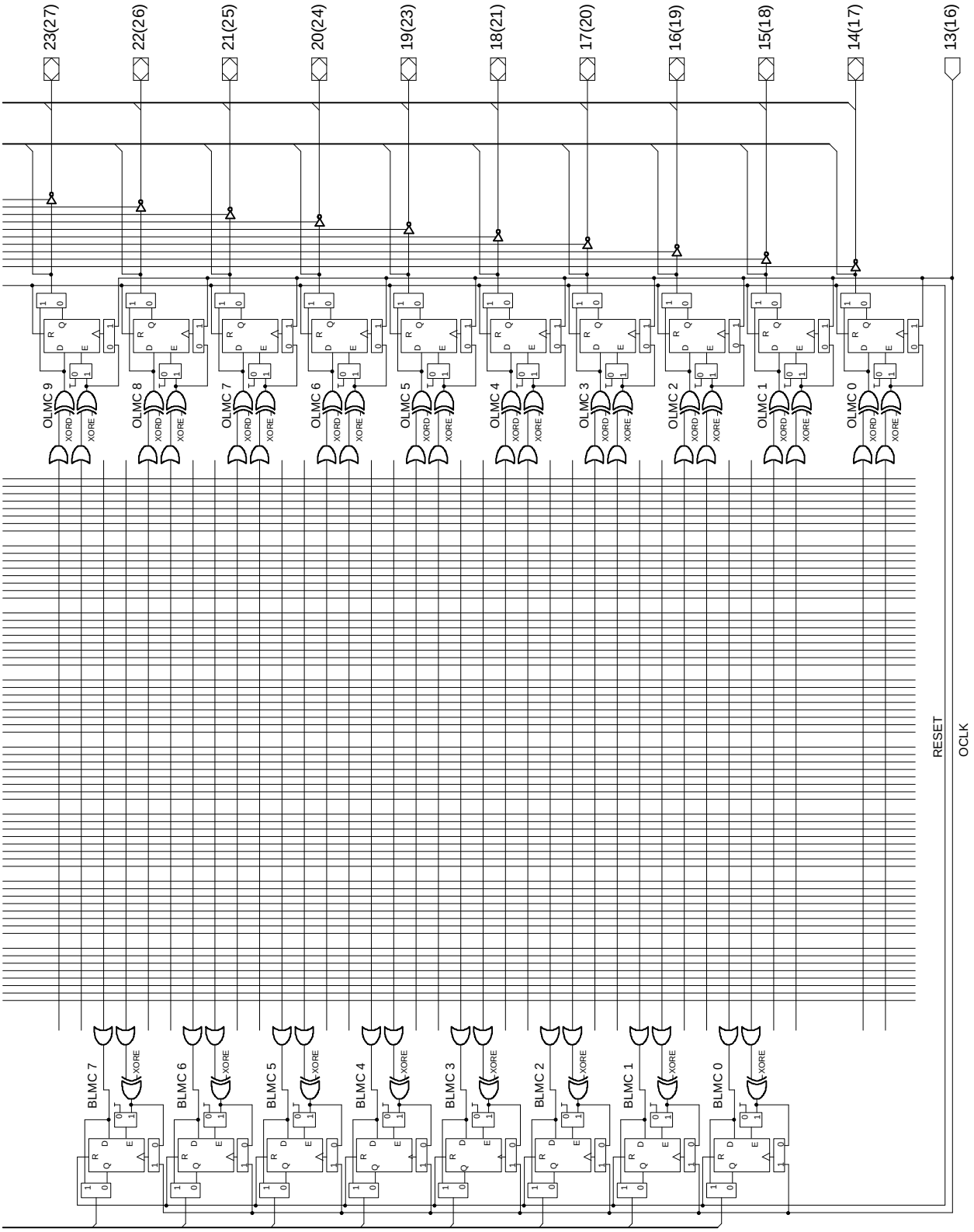
BLMC JEDEC Fuse Numbers

BLMC	CKS	OUTSYNC	XORE
7	8175	8176	8177
6	8172	8173	8174
5	8169	8170	8171
4	8166	8167	8168
3	8163	8164	8165
2	8160	8161	8162
1	8157	8158	8159
0	8154	8155	8156

LOGIC DIAGRAM



LOGIC DIAGRAM (CONT.)



ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:

Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–130	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -15/-20	—	90	135	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM.	TEST COND[1].	DESCRIPTION	COM -15		COM -20		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	Combinatorial Input to Combinatorial Output	—	15	—	20	ns
t_{pd2}	A	Feedback or I/O to Combinational Output	—	15	—	20	ns
t_{pd3}	A	Transparent Latch Input to Combinatorial Output	—	18	—	23	ns
t_{co1}	A	Input Latch ICLK to Combinatorial Output Delay	—	20	—	25	ns
t_{co2}	A	Input Reg. ICLK to Combinatorial Output Delay	—	20	—	25	ns
t_{co3}	A	Output D/E Reg. OCLK to Output Delay	—	6.5	—	8	ns
t_{co4}	A	Output D Reg. Sum Term CLK to Output Delay	—	18	—	20	ns
t_{cf1}[2]	—	Output D/E Reg. OCLK to Buried Feedback Delay	—	3.6	—	7	ns
t_{cf2}[2]	—	Output D Reg. STCLK to Buried Feedback Delay	—	10.1	—	13	ns
t_{su1}	—	Setup Time, Input before Input Latch ICLK	1.5	—	2	—	ns
t_{su2}	—	Setup Time, Input before Input Reg. ICLK	1.5	—	2	—	ns
t_{su3}	—	Setup Time, Input or Fdbk before D/E Reg. OCLK	11.5	—	13	—	ns
t_{su4}	—	Setup Time, Input or Fdbk before D Reg. Sum Term CLK	5	—	7	—	ns
t_{su5}	—	Setup Time, Input Reg. ICLK before D/E Reg. OCLK	15	—	20	—	ns
t_{su6}	—	Setup Time, Input Reg. ICLK before D Reg. Sum Term CLK	7	—	9	—	ns
t_{h1}	—	Hold Time, Input after Input Latch ICLK	3	—	4	—	ns
t_{h2}	—	Hold Time, Input after Input Reg. ICLK	3	—	4	—	ns
t_{h3}	—	Hold Time, Input or Feedback after D/E Reg. OCLK	0	—	0	—	ns
t_{h4}	—	Hold Time, Input or Feedback after D Reg. Sum Term CLK	4	—	6	—	ns
f_{max1}[3]	—	Max. Clock Frequency w/External Feedback, $1/(t_{su3}+t_{co3})$	55.5	—	47.6	—	MHz
f_{max2}[3]	—	Max. Clock Frequency w/External Feedback, $1/(t_{su4}+t_{co4})$	43.4	—	37	—	MHz
f_{max3}[3]	—	Max. Clock Frequency w/Internal Feedback, $1/(t_{su3}+t_{cf1})$	66	—	50	—	MHz
f_{max4}[3]	—	Max. Clock Frequency w/Internal Feedback, $1/(t_{su4}+t_{cf2})$	66	—	50	—	MHz
f_{max5}[3]	—	Max. Clock Frequency w/No Feedback, OCLK	75	—	60	—	MHz
f_{max6}[3]	—	Max. Clock Frequency w/No Feedback, STCLK	70	—	60	—	MHz
t_{wh1}	—	ICLK Pulse Duration, High	6	—	7	—	ns
t_{wh2}	—	OCLK Pulse Duration, High	6	—	7	—	ns
t_{wh3}	—	STCLK Pulse Duration, High	7	—	8	—	ns

1) Refer to Switching Test Conditions section.
2) Calculated from fmax with internal feedback. Refer to fmax Description section.
3) Refer to fmax Description section.

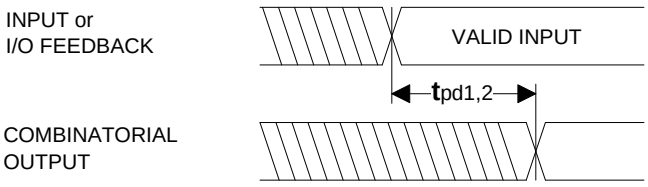
AC SWITCHING CHARACTERISTICS (CONT.)

Over Recommended Operating Conditions

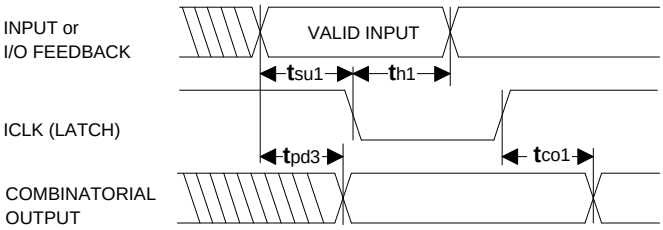
PARAMETER	TEST COND[1].	DESCRIPTION	COM -15		COM -20		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{wl1}	—	ICLK Pulse Duration, Low	6	—	7	—	ns
t_{wl2}	—	OCLK Pulse Duration, Low	6	—	7	—	ns
t_{wl3}	—	STCLK Pulse Duration, Low	7	—	8	—	ns
t_{arw}	—	Reset Pulse Duration	12	—	15	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	15	—	20	ns
t_{dis}	C	Input or I/O to Output Disabled	—	15	—	20	ns
t_{ar}	A	Input or I/O to Asynchronous Reg. Reset	—	16	—	20	ns
t_{arr1}	—	Asynchronous Reset to OCLK Recovery Time	11	—	14	—	ns
t_{arr2}	—	Asynchronous Reset to Sum Term CLK Recovery Time	4	—	6	—	ns

1) Refer to Switching Test Conditions section.

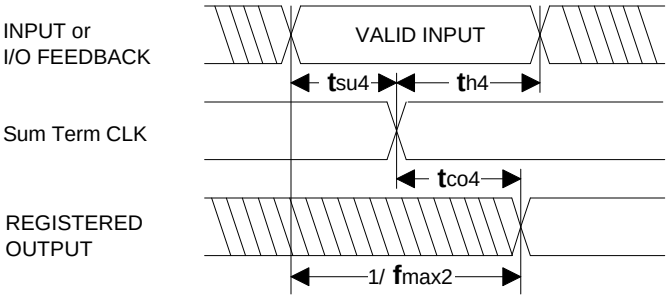
SWITCHING WAVEFORMS



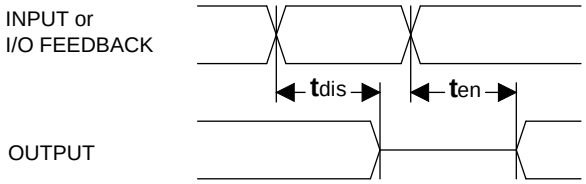
Combinatorial Output



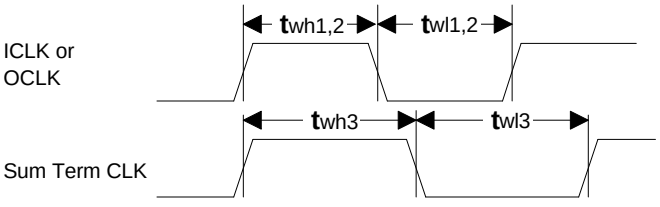
Latched Input



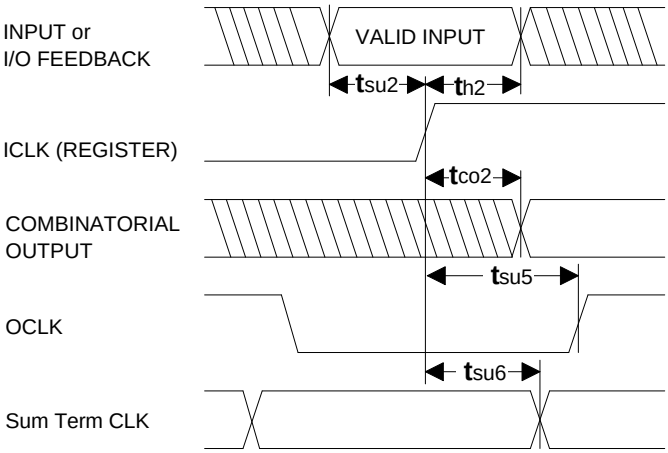
Registered Output (Sum Term CLK)



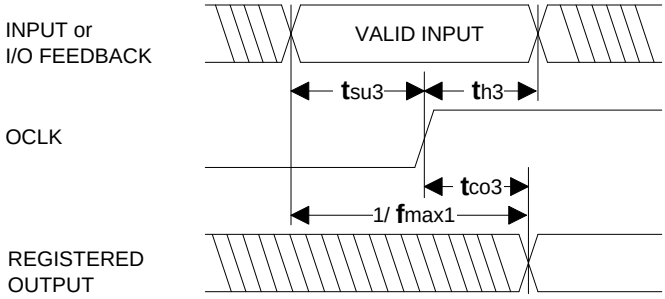
Input or I/O to Output Enable/Disable



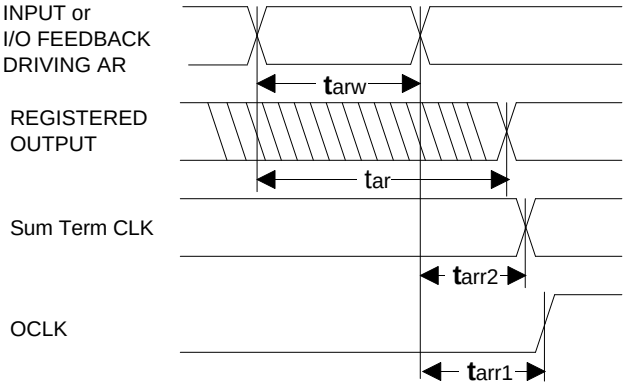
Clock Width



Registered Input

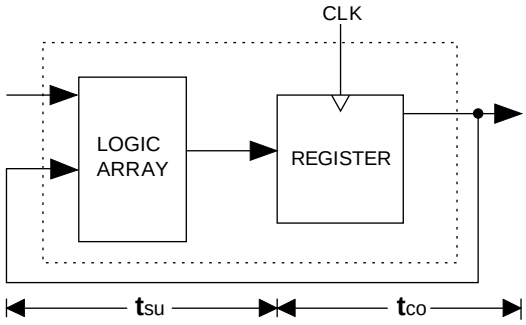


Registered Output (OCLK)



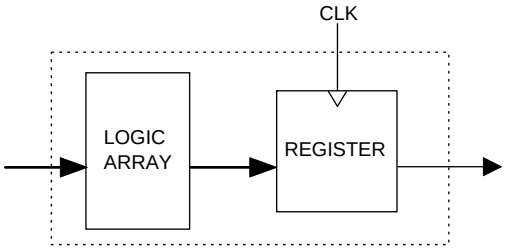
Asynchronous Reset

fmax DESCRIPTIONS



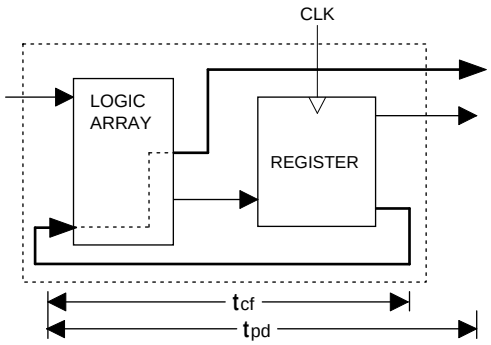
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

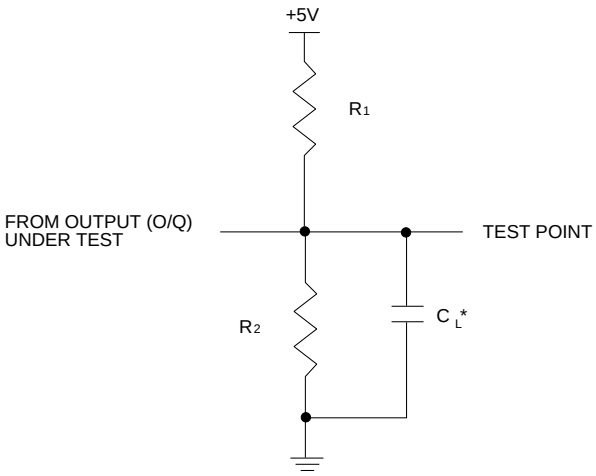
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ARRAY DESCRIPTION

The GAL6002 contains two E^2 reprogrammable arrays. The first is an AND array and the second is an OR array. These arrays are described in detail below.

AND ARRAY

The AND array is organized as 78 inputs by 75 product term outputs. The 10 ILMCs, 10 IOLMCs, 8 BLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise the 39 inputs to this array (each available in true and complement forms). 64 product terms serve as inputs to the OR array. The RESET product term generates the RESET signal described in the Output and Buried Logic Macrocells section. There are 10 output enable product terms which allow device I/O pins to be bi-directional or tri-state.

OR ARRAY

The OR array is organized as 64 inputs by 36 sum term outputs. 64 product terms from the AND array serve as the inputs to the OR array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 BLMCs, one "D" term and one "E" term to each.

The programmable OR array offers unparalleled versatility in product term usage. This programmability allows from 1 to 64 product terms to be connected to a single sum term. A programmable OR array is more flexible than a fixed, shared, or variable product term architecture.

ELECTRONIC SIGNATURE

An electronic signature is provided with every GAL6002 device. It contains 72 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

SECURITY CELL

A security cell is provided with every GAL6002 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal operations. This is because certain events may occur during system operation that cause the logic to be in an illegal state (power-up, line voltage glitches, brown-out, etc.). To test a design for proper treatment of these conditions, a method must be provided to break the feedback paths and force any desired state (i.e., illegal) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation.

All of the registers in the GAL6002 can be preloaded, including the ILMC, IOLMC, OLMC, and BLMC registers. In addition, the contents of the state and output registers can be examined in a special diagnostics mode. Programming hardware takes care of all preload timing and voltage requirements.

LATCH-UP PROTECTION

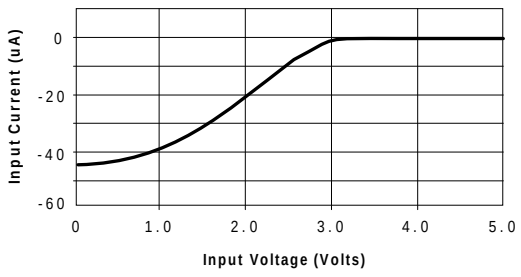
GAL6002 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

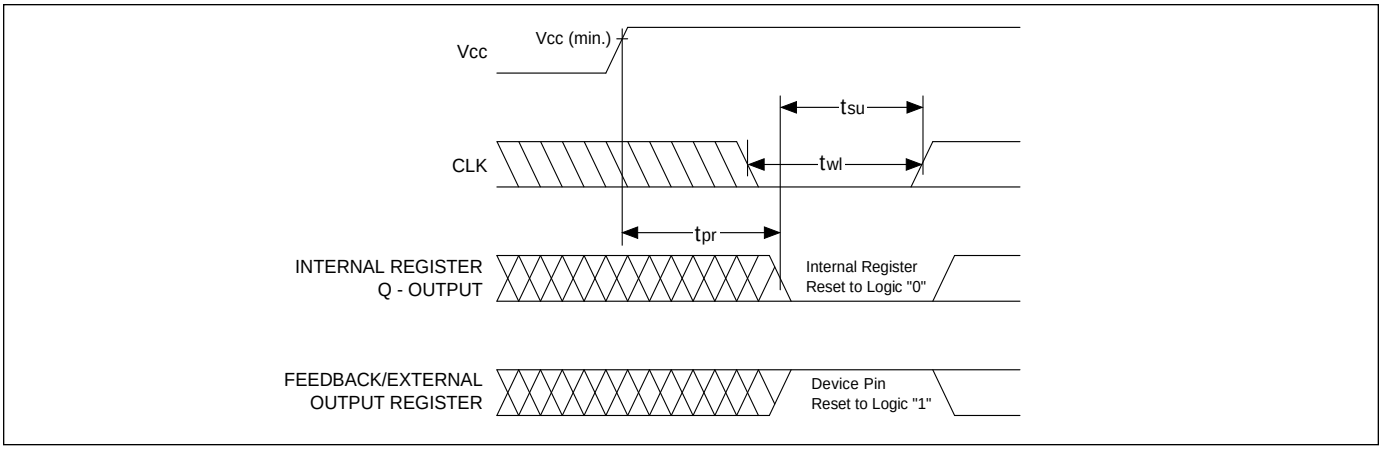
GAL6002 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

GAL6002 input buffers have active pull-ups within their input structure. This pull-up will cause any un-terminated input or I/O to float to a TTL high (logical 1). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, Vcc, or GND. Doing this will tend to improve noise immunity and reduce Icc for the device.

Typical Input Pull-up Characteristic



POWER-UP RESET



Circuitry within the GAL6002 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (**t**pr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL6002. First, the **V**CC rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of **t**pr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

DIFFERENTIAL PRODUCT TERM SWITCHING (DPTS) APPLICATIONS

The number of Differential Product Term Switching (DPTS) for a given design is calculated by subtracting the total number of product terms that are switching from a Logical HI to a Logical LO from those switching from a Logical LO to a Logical HI within a 5ns period. After subtracting take the absolute value.

$$DPTS = \left| (P\text{-}Terms)_{LH} - (P\text{-}Terms)_{HL} \right|$$

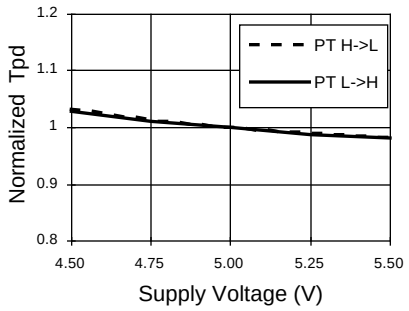
DPTS restricts the number of product terms that can be switched simultaneously - there is no limit on the number of product terms that can be used.

The majority of designs fall below 15 DPTS, with the upper limit being approximately 25 DPTS. Lattice Semiconductor guarantees and tests the commercial grade GAL6002 for functionality at DPTS ≤30.

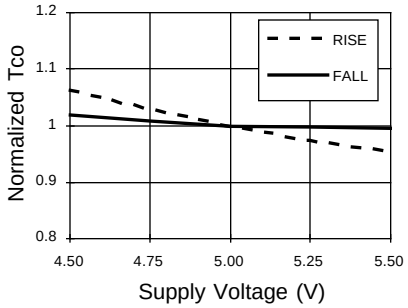
A software utility is available from Lattice Semiconductor Applications Engineering that will perform this calculation on any GAL6002 JEDEC file. This program, DPTS, and additional information may be obtained from your local Lattice Semiconductor representative or by contacting Lattice Semiconductor Applications Engineering Dept. (Tel: 503-681-0118 or 1-800-FASTGAL; FAX: 681-3037).

TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

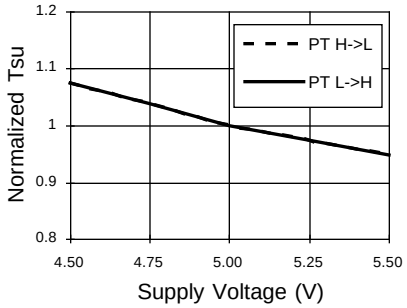
Normalized Tpd vs Vcc



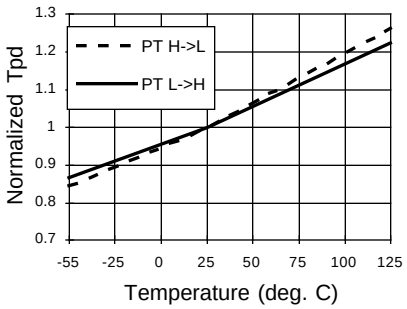
Normalized Tco vs Vcc



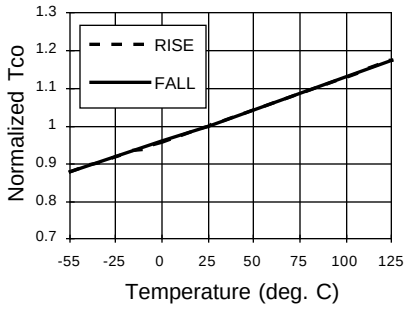
Normalized Tsu vs Vcc



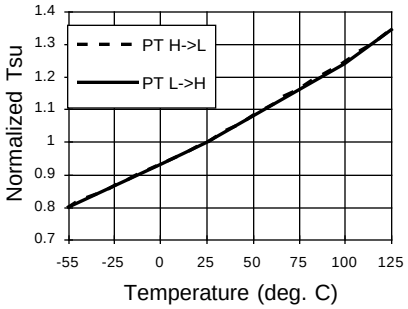
Normalized Tpd vs Temp



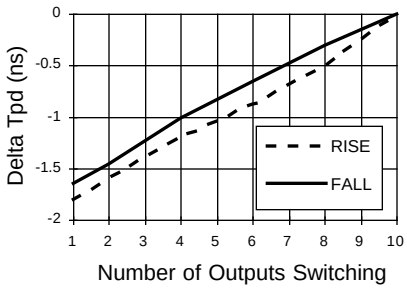
Normalized Tco vs Temp



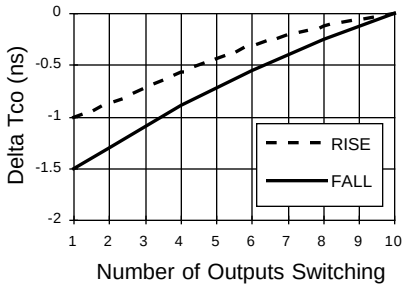
Normalized Tsu vs Temp



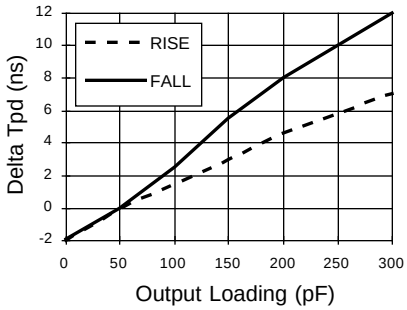
Delta Tpd vs # of Outputs Switching



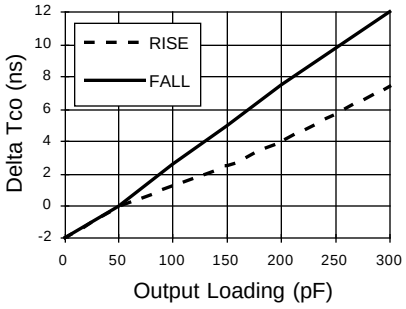
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

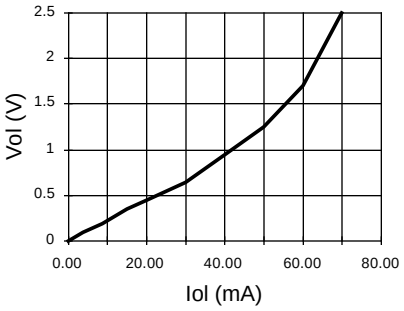


Delta Tco vs Output Loading

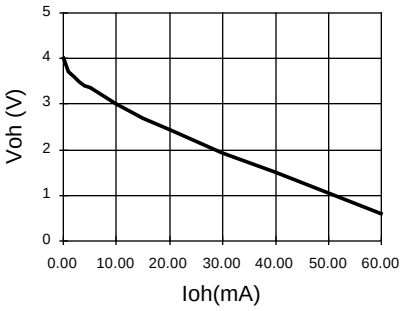


TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

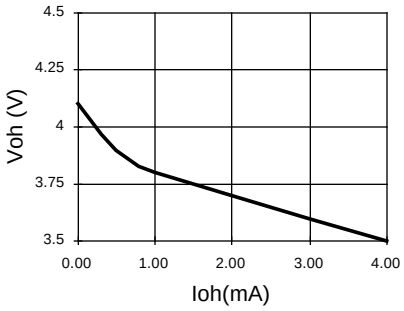
Vol vs Iol



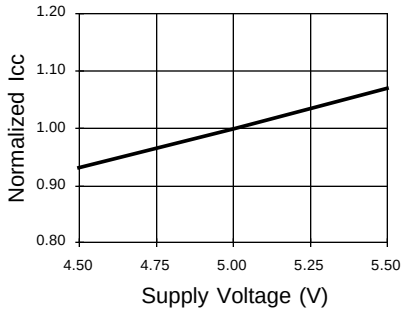
Voh vs Ioh



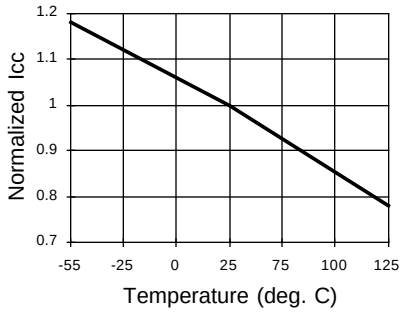
Voh vs Ioh



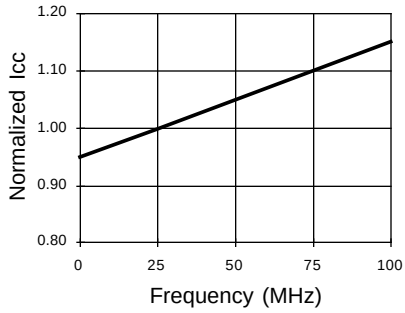
Normalized Icc vs Vcc



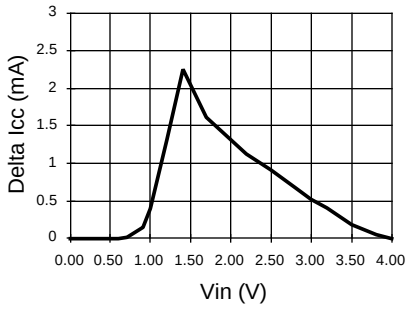
Normalized Icc vs Temp



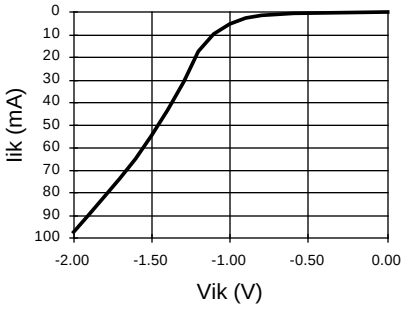
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



Section 4

Introduction to ispGDS™

Lattice Semiconductor Corporation (LSC), the pioneer of non-volatile in-system programmable (ISP™) logic has now expanded the application of ISP to include programmable system interconnect. The new ispGDS (Generic Digital Switch) family combines the in-system programmability, high performance and low power of LSC's GAL programmable logic technology with a switch matrix architecture, resulting in an innovative programmable signal router. The ispGDS is a configurable switch matrix which provides the ability to quickly implement and change p.c. board connections without changing mechanical switches or other system hardware. ISP allows the connections to be reprogrammed without removal from the PC board via a simple 5V, 4 wire serial interface. This capability allows the system designer to define hardware which can be reconfigured in-system to meet a variety of applications. The ispGDS also conserves board real estate, providing up to 22 I/Os in about a quarter square inch of board space.

With today's demand for user-friendly systems, there is an increasing need for hardware which is easily reconfigured under software control without manual intervention. The ispGDS family is an ideal solution for end-system feature reconfiguration and signal routing applications. The fast 7.5ns propagation delay through the devices supports high-performance signal routing applications. Easier system upgrades, user feature selection and system manufacturing are the results.

The ispGDS also provides higher quality and reliability than other switch solutions due to the nature of E^2CMOS technology. E^2CMOS technology supports 100% testability which guarantees you 100% in-system programmability and functionality.

There are three members of the ispGDS family: the ispGDS22, ispGDS18, and ispGDS14. Each of the devices operate identically with the only difference being the number of I/O cells available.

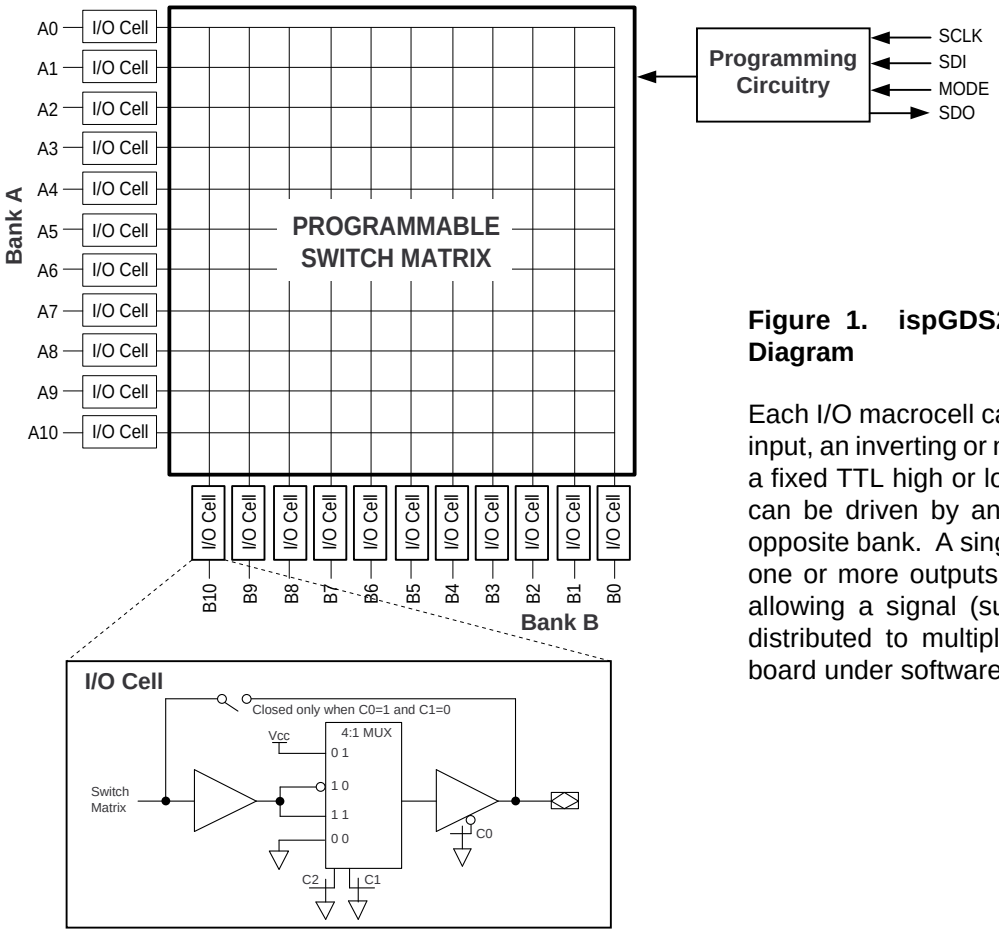


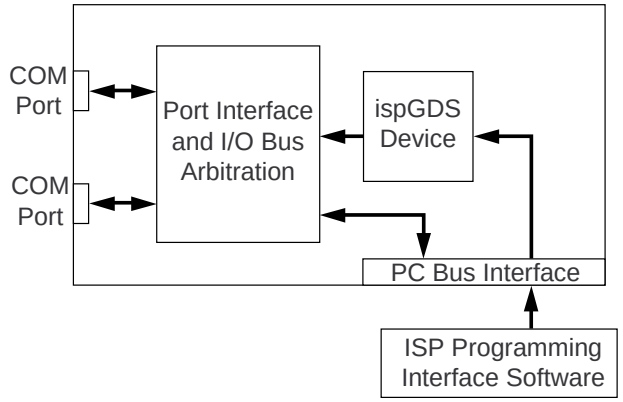
Figure 1. ispGDS22 Functional Block Diagram

Each I/O macrocell can be configured as an input, an inverting or non-inverting output, or a fixed TTL high or low output. Any I/O pin can be driven by any other I/O pin in the opposite bank. A single input can also drive one or more outputs in the opposite bank, allowing a signal (such as a clock) to be distributed to multiple destinations on the board under software control.

Introduction to ispGDS

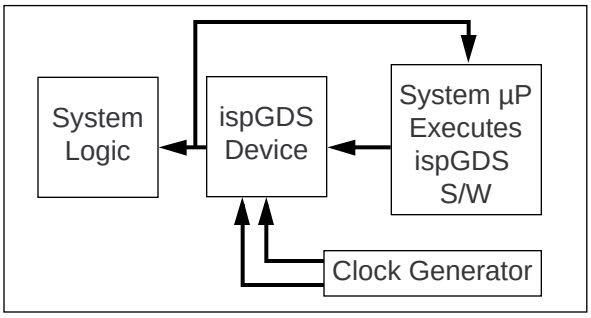
ispGDS Applications

With the ispGDS, designs can be reconfigured without mechanical devices or user intervention. Provision for easier system upgrades and feature selection can now be included in the system's original design. A few examples of actual ispGDS applications demonstrate the possibilities.



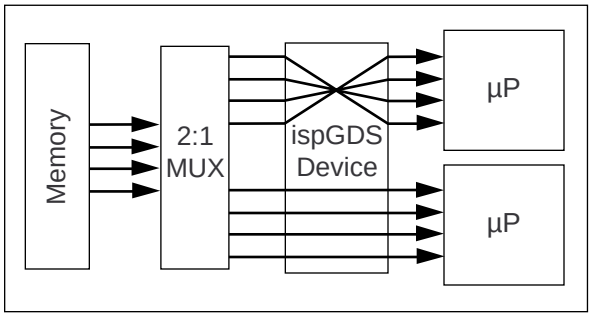
PC add-on cards can be configured for plug-and-play applications with an ispGDS device.

The ispGDS supports reconfiguration of COM port characteristics and interrupt levels via software updates through the PC bus interface. The ispGDS provides the flexibility so one generic PC card can be reconfigured by software for multiple applications.



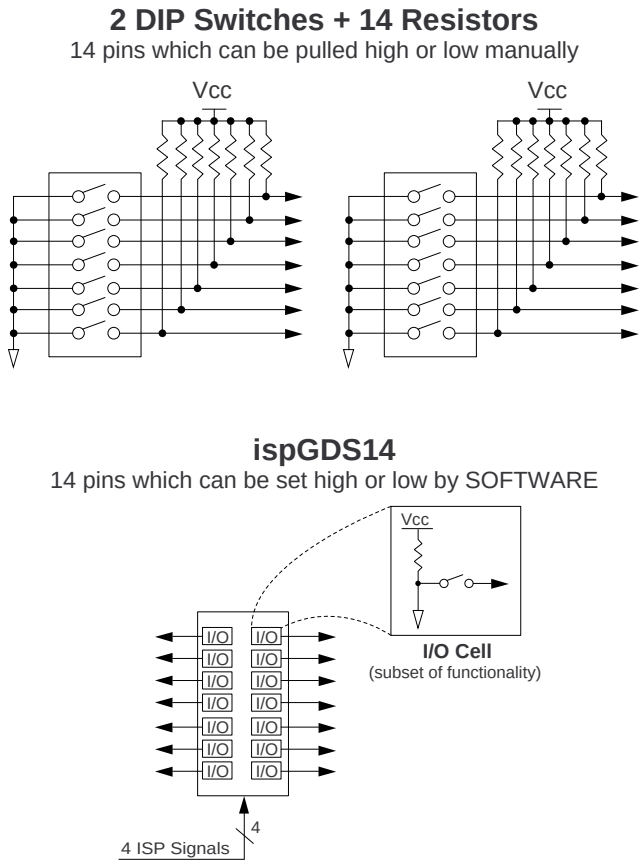
One board design can support two different microprocessor speeds with the ispGDS.

Based on the motherboard processor configuration, the software directs the ispGDS to set the clock speed and the hardware for the correct configuration. The ispGDS eliminates the need to manually reconfigure the hardware to support manufacturing motherboards with different processors.



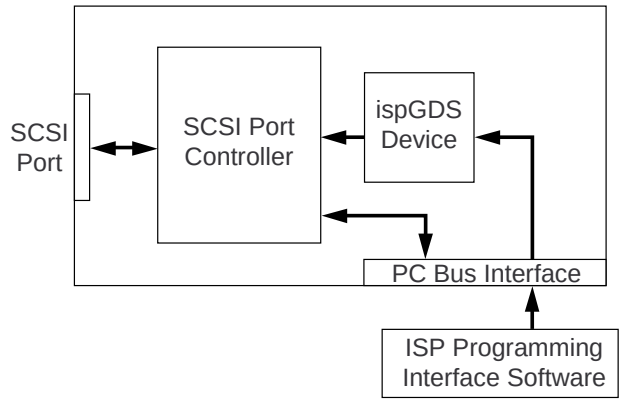
Create a cross point switch with the ispGDS

A crosspoint switch enables the MSB and LSB bytes on a bus to be swapped. The ispGDS acts as a crosspoint switch and swaps MSB and LSB bytes of the data for the different microprocessors.



Replace DIP switches with a software controlled switch alternative

The ispGDS can be configured as a programmable replacement for standard DIP switches, providing space savings, in-system reconfigurability, higher reliability as well as ease of use. The programmable nature of the ispGDS eliminates the need to manually select DIP switch settings.



SCSI port interface configurations can be set using the ispGDS

Software can reconfigure the ispGDS via the PC bus which in turn controls the SCSI port and interrupt level selection. Hardware changes become transparent to the user as the ispGDS is reconfigured by software while in-system, eliminating the need for manual intervention.

In-System Programming

The ispGDS devices can be programmed in-system using 5 volt only signals through a simple 4-wire programming interface using TTL level signals. Programming and erasure of the entire device can be done in less than one second.

In addition to third party programmers, the ispGDS can be programmed from your automatic test equipment (ATE) or even from a PC on your manufacturing line. For more flexibility, you can have your product's embedded microprocessor configure the ispGDS devices though one of its I/O ports, making a field upgrade a snap.

Lattice Semiconductor provides free compiler support and "ISP Download Software" to support the software side of these programming options. The ispGDS Download routines are written in ANSI-standard C language which can be integrated directly into your system.

Designing with the ispGDS will provide you with the flexibility to reconfigure your design while in-system. It will revolutionize the way systems are designed and maintained. Call 1-800-327-8425 for a data sheet and begin designing today!

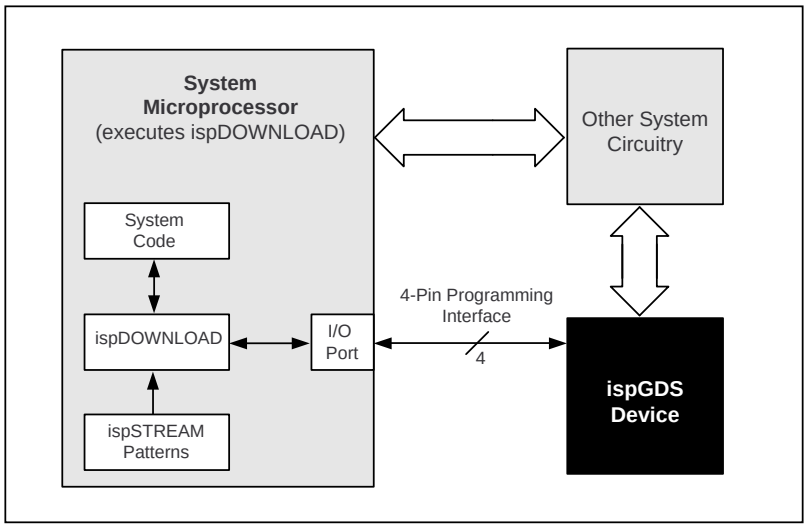


Figure 2. In-System Programming Using ispGDS Download Routines

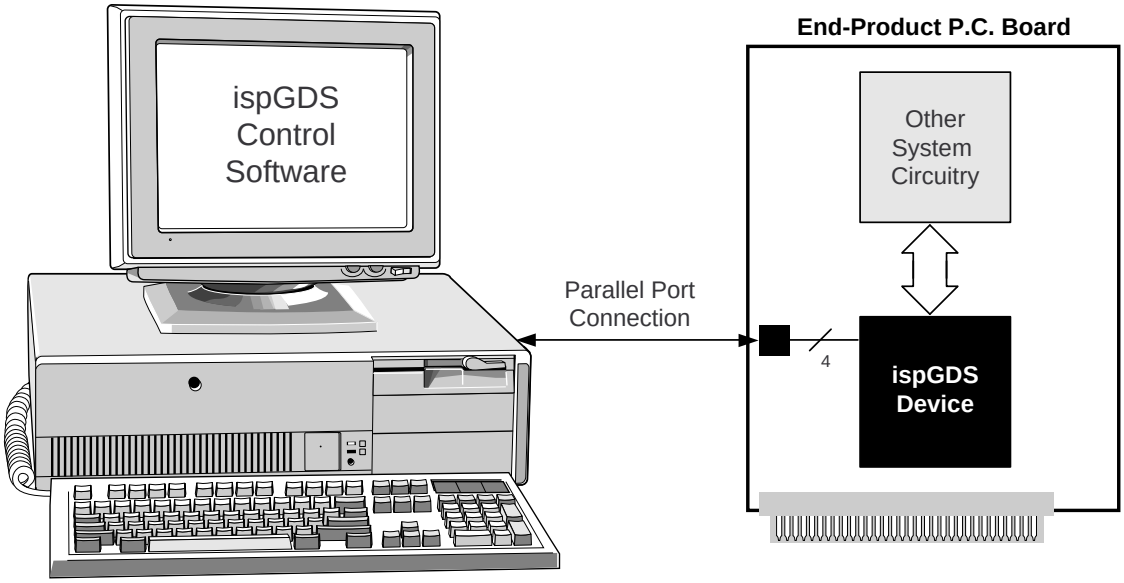


Figure 3. Configuring an ispGDS Device from a Remote System

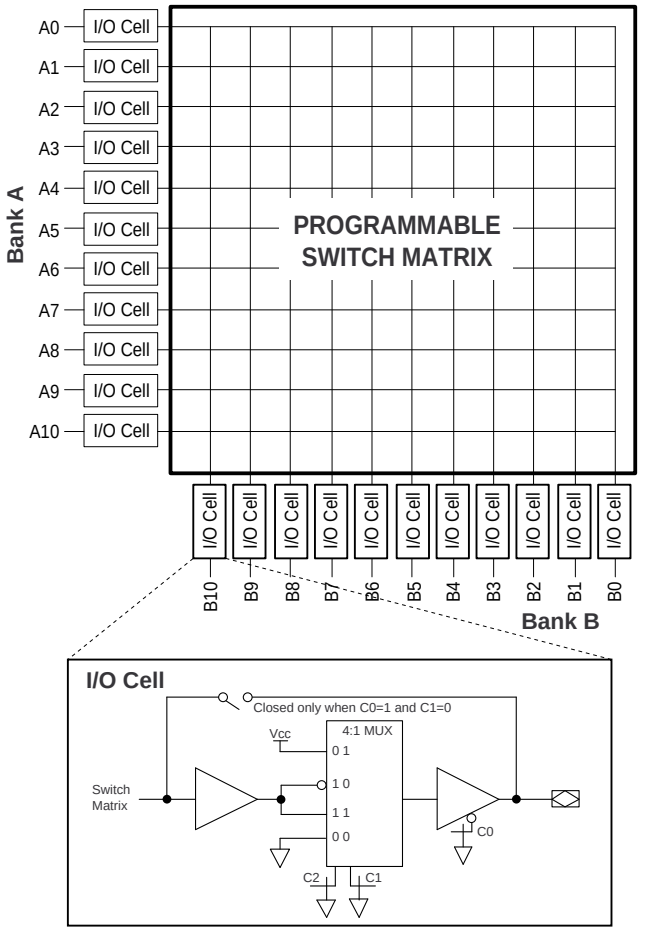
ispGDS22/18/14

in-system programmable Generic Digital Switch™

FEATURES

- **HIGH-SPEED SWITCH MATRIX**
  - **— 7.5 ns Maximum Propagation Delay**
  - **— Typical Icc = 25 mA**
  - **— UltraMOS® Advanced CMOS Technology**
- **FLEXIBLE I/O MACROCELL**
  - **— Any I/O Pin Can be Input, Output, or Fixed TTL High or Low**
  - **— Programmable Output Polarity**
  - **— Multiple Outputs Can be Driven by One Input**
- **IN-SYSTEM PROGRAMMABLE (5-VOLT ONLY)**
  - **— Programming Time of Less Than One Second**
  - **— 4-Wire Programming Interface**
  - **— Minimum 10,000 Program/Erase Cycles**
- **E^2 CELL TECHNOLOGY**
  - **— Non-Volatile Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **APPLICATIONS INCLUDE:**
  - **— Software-Driven Hardware Configuration**
  - **— Multiple DIP Switch Replacement**
  - **— Software Configuration of Add-In Boards**
  - **— Configurable Addressing of I/O Boards**
  - **— Multiple Clock Source Selection**
  - **— Cross-Matrix Switch**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM (ispGDS22)



DESCRIPTION

The Lattice Semiconductor ispGDS™ family is an ideal solution for reconfiguring system signal routing or replacing DIP switches used for feature selection. With today's demands for customer ease of use, there is a need for hardware which is easily reconfigured electronically without dismantling the system. The ispGDS devices address this challenge by replacing conventional switches with a software configurable solution. Since each I/O pin can be set to an independent logic level, the ispGDS devices can replace most DIP switch functions with about half the pin count, and without the need for additional pull-up resistors. In addition to DIP switch replacement, the ispGDS devices are useful as signal routing cross-matrix switches. This is the only non-volatile device on the market which can provide this flexibility.

With a maximum tpd of 7.5ns, and a typical active Icc of only 25 mA, these devices provide maximum performance at very low power levels. The ispGDS devices may be programmed in-system, using 5 volt only signals, through a simple 4-wire programming interface. The ispGDS devices are manufactured using Lattice Semiconductor's advanced non-volatile E^2CMOS process which combines CMOS with Electrically Erasable (E^2) floating gate technology. High speed erase times (**<**100ms) allow the devices to be reprogrammed quickly and efficiently.

Each I/O macrocell can be configured as an input, an inverting or non-inverting output, or a fixed TTL high or low output. Any I/O pin can be driven by any other I/O pin in the opposite bank. A single input can drive one or more outputs in the opposite bank, allowing a signal (such as a clock) to be distributed to multiple destinations on the board, under software control. The I/Os accept and drive TTL voltage levels.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor is able to guarantee 100% field programmability and functionality of all Lattice Semiconductor products. In addition, 10,000 erase/write cycles and data retention in excess of 20 years are guaranteed.

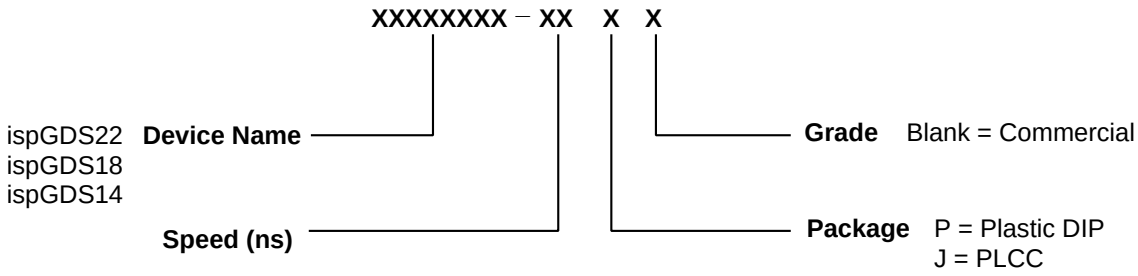
LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-327-8425; FAX (503) 681-3037; http://www.latticesemi.com

ispGDS Ordering Information

Commercial Grade Specifications

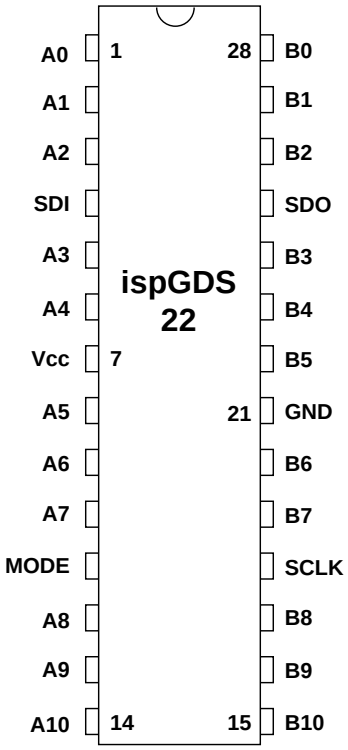
Matrix Size	I/O Pins	Tpd (ns)	Isb (mA)	Icc (mA)	Ordering #	Package
11 x 11	22	7.5	25	40	ispGDS22-7P	28-Pin Plastic DIP
					ispGDS22-7J	28-Lead PLCC
9 x 9	18	7.5	25	40	ispGDS18-7P	24-Pin Plastic DIP
7 x 7	14	7.5	25	40	ispGDS14-7P	20-Pin Plastic DIP
					ispGDS14-7J	20-Lead PLCC

Part Number Description

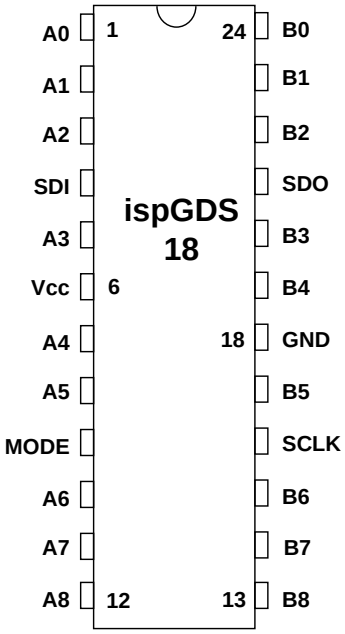


Pin Configuration

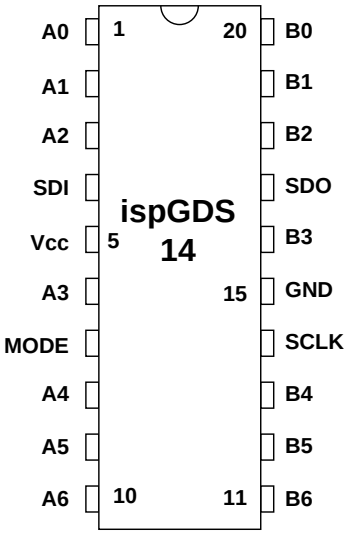
28-Pin DIP



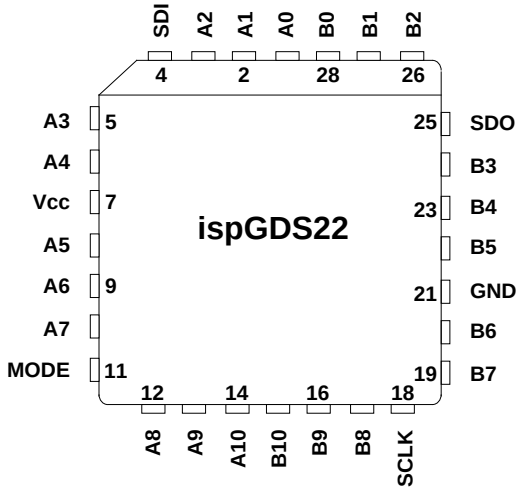
24-Pin DIP



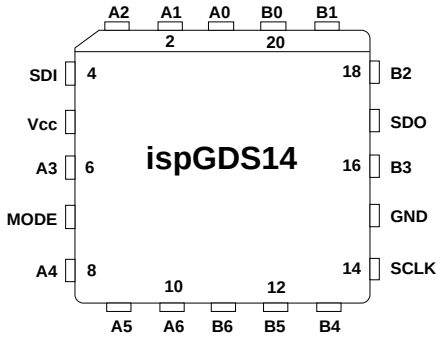
20-Pin DIP



28-Pin PLCC



20-Pin PLCC



ispGDS Family Overview

There are three members of the ispGDS family, the ispGDS22, ispGDS18, and ispGSD14. The numerical portion of the part name indicates the number of I/O cells available. All of the devices are available in a DIP package, with the ispGDS22 and ispGDS14 also available in a PLCC package. Each of the devices operate identically, with the only difference being the number of I/O cells available.

The ispGDS devices are all programmed through a four-pin interface, using TTL level signals. The four dedicated programming pins are named MODE, SDI, SDO, and SCLK. No high-voltage is needed, as the voltages needed for programming are generated internally. Programming of the entire device, including erasure, can be done in less than one second. During the programming operation, all I/O pins will be tri-stated. Further details of the programming process can be found in the In-System Programming section later in this datasheet.

The I/O cells in each device are divided equally into two banks (Bank A and Bank B). Each I/O cell can be configured as an input, an inverting output, a non-inverting output, or set to a fixed TTL high or low. A switch matrix connects the I/O banks, allowing an I/O cell in one bank to be connected to any of the I/O cells in the other bank. A single I/O cell configured as an input can drive one or more I/O cells in the other bank. The full I/O macrocell, which is identical for each of the I/O pins, is shown below. The allowable configurations are shown on the following page.

In-System Programmability

The ispGDS family of devices feature In-System Programmable technology. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via four TTL level logic interface signals. These four signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. For details on the operation of the internal state machine and programming of ispGDS devices please refer to the ISP Architecture and Programming section in this Data Book.

Device Programming

The ispGDS family of devices uses a standard JEDEC file, as used for programmable logic devices, to describe device programming information. Popular logic compilers, such as ABEL and CUPL, can produce the JEDEC files for these devices.

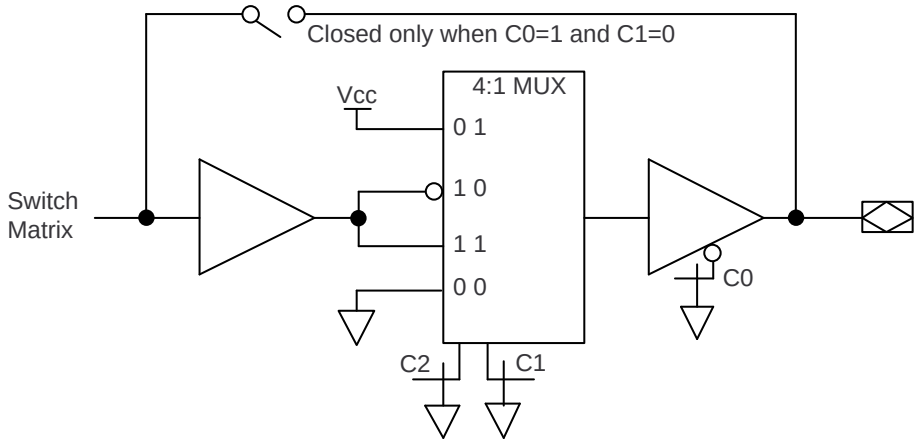
The JEDEC files can be used to program the ispGDS devices in a number of ways, which are shown in the In-System Programming Overview section later in this datasheet.

Electronic Signature

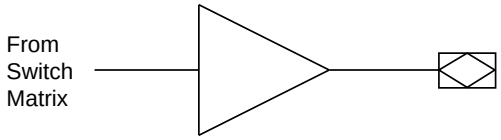
An electronic signature word is provided with every ispGDS device. It contains 32 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the fuse checksum in the JEDEC fusemap.

I/O Macrocell

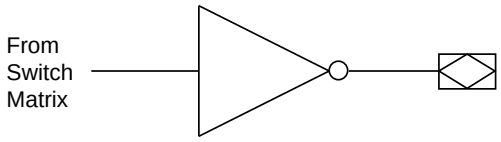


I/O Macrocell Configurations



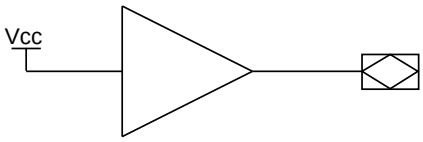
Configuration for Active High Output

- C0 = 0.
- C1 = 1.
- C2 = 1.



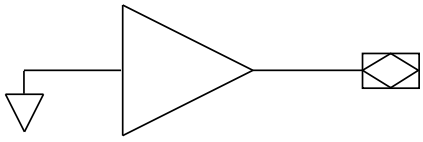
Configuration for Active Low Output

- C0 = 0.
- C1 = 0.
- C2 = 1.



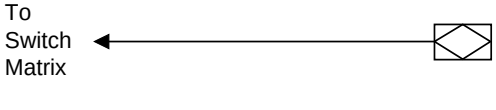
Configuration for Fixed TTL High Output

- C0 = 0.
- C1 = 1.
- C2 = 0.



Configuration for Fixed TTL Low Output

- C0 = 0.
- C1 = 0.
- C2 = 0.



Configuration for Dedicated Input

- C0 = 1.
- C1 = 0.
- C2 = 1.

Note 1: The development software configures all of the architecture control bits and checks for proper pin usage automatically.
Note 2: The default configuration for unused pins is for all configuration bits set to one, which produces a tri-stated output.

Absolute Maximum Ratings(1)

Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Cond.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–130	mA

COMMERCIAL

I_{SB}	Standby Power Supply Current	Inputs = 0V Outputs open	L-7	—	15	25	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -7	—	25	40	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
$C_{I/O}$	I/O Capacitance (as input or output)	8	pF	V_{CC} = 5.0V, V_I = 2.0V

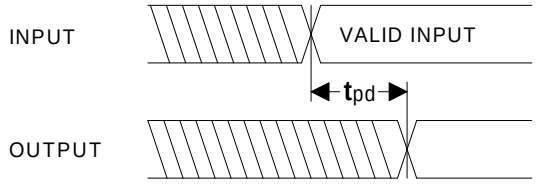
*Guaranteed but not 100% tested.

AC Switching Characteristics

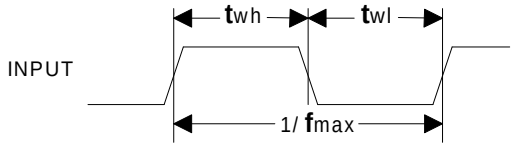
Over Recommended Operating Conditions

PARAMETER	TEST COND.	DESCRIPTION		COM MIN.	COM MAX.	UNITS
t_{pd}	A	Input to Output Delay	One Input Driving One Output	1	7.5	ns
f_{max}	A	Maximum Input Frequency	One Output Switching	—	50	MHz
t_{wh}	A	Input Pulse Duration, High		10	—	ns
t_{wl}	A	Input Pulse Duration, Low		10	—	ns

Switching Waveforms



Input to Output Delay



Input Pulse Width/ Fmax

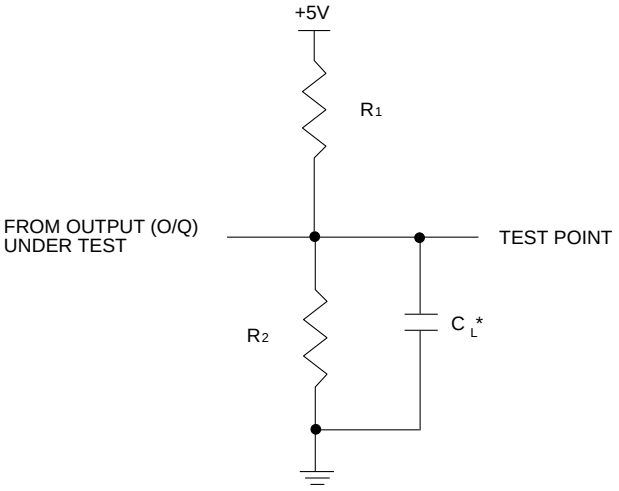
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	2ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

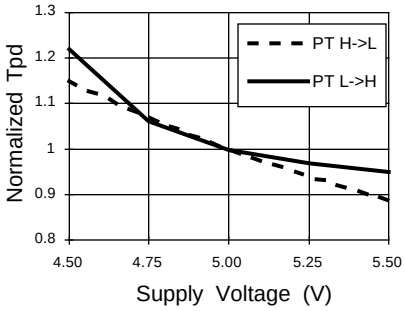
Test Condition	R_1	R_2	C_L
A	470Ω	390Ω	50pF



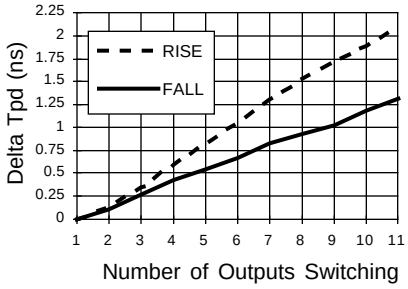
*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

Typical AC and DC Characteristic Diagrams

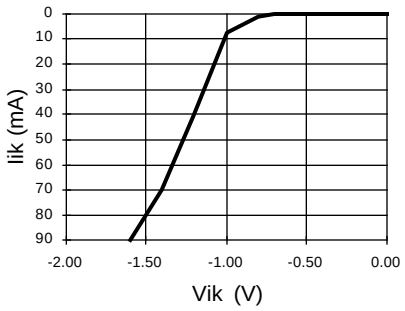
Normalized Tpd vs Vcc



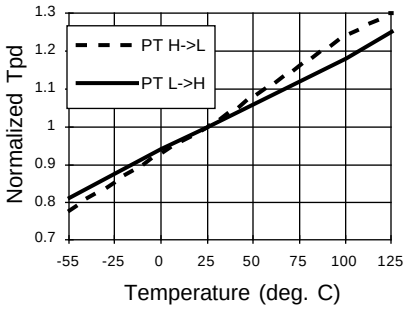
Delta Tpd vs # of Outputs Switching



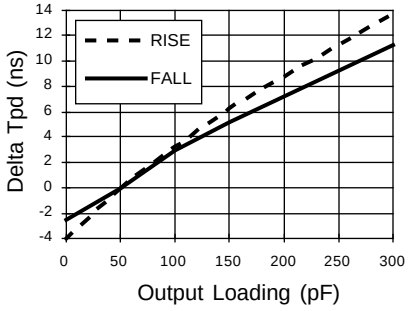
Input Clamp (Vik)



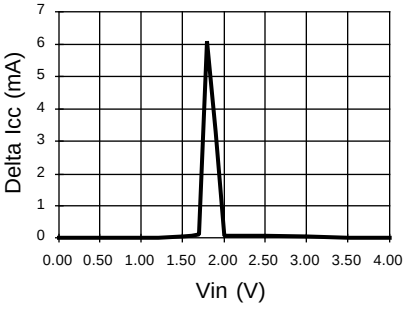
Normalized Tpd vs Temp



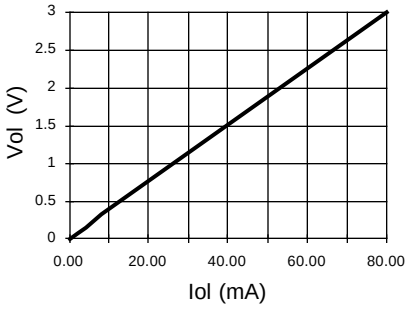
Delta Tpd vs Output Loading



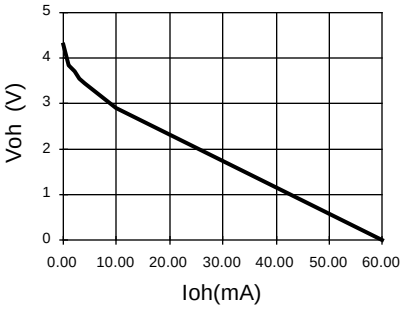
Delta Icc vs Vin (1 input)



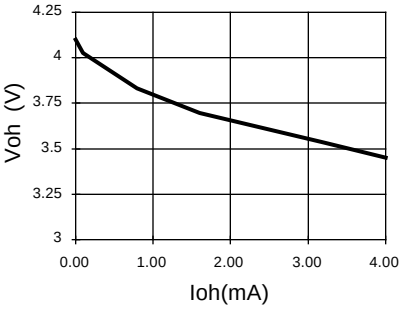
Vol vs Iol



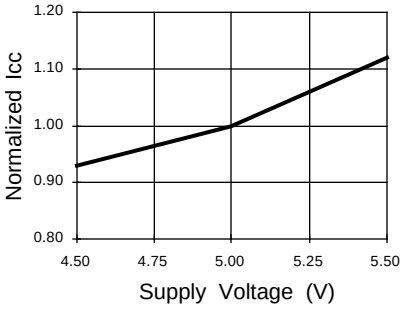
Voh vs Ioh



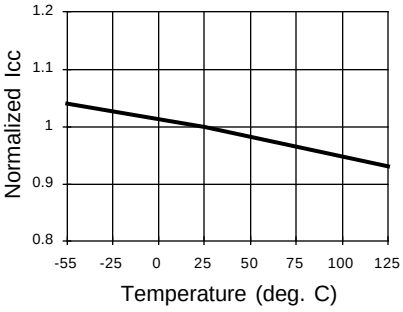
Voh vs Ioh



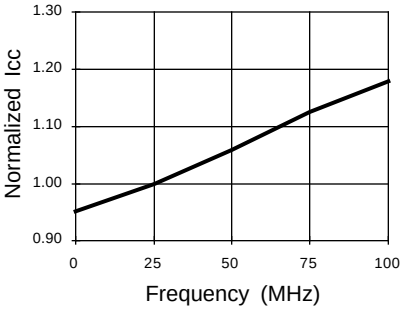
Normalized Icc vs Vcc



Normalized Icc vs Temp



Normalized Icc vs Freq.



Section 5

Military Program Overview

Corporate Philosophy

Lattice Semiconductor Corporation (LSC) is committed to leadership in device performance and quality. Our family of military ispLSI, pLSI and GAL devices is a reflection of this philosophy. LSC manufactures all devices under strict Quality Assurance guidelines. All grades, Commercial through Military 883, are monitored under a quality program conformant to MIL-I-38535 Appendix C with inspections conformant to MIL-I-45208.

Quality and Testability

Lattice Semiconductor processes its devices to strict conformance with MIL-STD-883 Class B. In conjunction with the military flow, the inherent testability of E^2CMOS technology allows LSC to achieve a quality level superior to other PLD technologies.

All devices are patterned and tested dozens of times throughout the manufacturing flow. Every device is tested under worst case configurations to assure customers achieve 100% yields. Tests are performed using the same E^2 cell array that will be used for the final patterning of the devices. This 100% "actual test" philosophy does away with the correlated and simulated testing that is necessary with bipolar and UV (EPROM) based PLD devices.

Reliability

Lattice Semiconductor performs extensive reliability testing prior to product release. This testing continues in the form of Reliability Monitors that are run on an ongoing basis to assure continued process integrity.

The reliability testing performed includes extensive analysis of fundamental design and process integrity. The reprogrammable nature of LSC devices allows an inherently more thorough reliability evaluation than with other programmable alternatives.

MIL-STD-883 Compliance

MIL-STD-883 defines a uniform and precise method for environmental, mechanical and electrical testing which ensures the suitability of microelectronic devices for use in military and aerospace systems. Table I summarizes the MIL-STD-883, Method 5004 Class B flow. Table II summarizes the conformance testing required by MIL-STD-883, Method 5005, for quality conformance testing of LSC military microcircuits.

MIL-I-38535

MIL-I-38535 Appendix A and C, when used in conjunction with MIL-STD-883, define design, packaging, material, marking, sampling, qualification and quality system requirements for LSC military devices.

Group Data

Group A and B data is taken on every inspection lot per MIL-STD-883, Class B requirements. This data, along with Generic Group C and D data can be supplied, upon written request, with your device shipment. Your LSC sales representative can advise you of charges and leadtime necessary for providing this data.

Standard Military Drawings

LSC actively supports the DESC Standard Military Drawing (SMD) Program. The SMD Program offers a cost effective alternative to source control drawings and provides standardized MIL-STD-883 product specifications to simplify military procurement.

A list of currently available SMD qualified devices is provided (see Military Ordering Information).

MILITARY SCREENING FLOW (TABLE I)

Screen	Method	Requirement
Internal Visual	2010 Cond. B	100%
Temp. Cycling	1010 Cond. C	100%
Constant Acceleration	2001 Cond. E	100%
Hermeticity Fine Gross	1014 Cond. A or B Cond. C	100%
Endurance Test	1033	100%
Retention Test	Unbiased Bake 24 HRS. T_A = 180°C	100%
Pre Burn-In Electrical	Applicable Device Specification Tc = 25°C	100%
Dynamic Burn-In	1015 Cond. D	100%
Post Burn-In Electrical	Applicable Device Specification Tc = 25°C PDA = 5%	100%
Final Electrical Test	Applicable Device Specification Tc = 125°C	100%
Final Electrical Test	Applicable Device Specification Tc = - 55°C	100%
Final Electrical Test	Applicable Device Specification Tc = 25°C	100%
External Visual	2009	100%
QCI Sample Selection	MIL-M-38535, Appendix A Sec. 4.5 and MIL-STD-883 Sec. 1.2	Sample

MILITARY QUALITY CONFORMANCE INSPECTIONS (TABLE II)

Subgroup	Method	Sample
GROUP A: Electrical Tests		
Subgroups 1, 7, 9	Applicable Device Spec.	LTPD = 2
Electrical Test	25°C	
Subgroups 2, 8A, 10	Applicable Device Spec.	LTPD = 2
Electrical Test	Max. Operating Temp.	
Subgroups 3, 8B, 11	Applicable Device Spec.	LTPD = 2
Electrical Test	Min. Operating Temp.	
GROUP B: Mechanical Tests		
Subgroup 2		4(0)
Solvent Resistance	2015	
Subgroup 3		LTPD = 10
Solderability	2003	
Subgroup 5		LTPD = 15
Bond Strength	2011	
GROUP C: Chip Integrity Tests		
Subgroup 1		LTPD = 5
Dynamic Life Test	1005, 1,000 HRS. 125°C	
End Point Electrical	Applicable Device Spec.	
Subgroup 2		LTPD = 5
Unbiased Retention	Applicable Device Spec.	
End Point Electrical	Applicable Device Spec.	
GROUP D: Environmental Integrity		
Subgroup 1		LTPD = 15
Physical Dimensions	2016	
Subgroup 2		LTPD = 5
Lead Integrity	2004, Cond. B	
Hermeticity	1014	
Subgroup 3		LTPD = 15
Thermal Shock	1011, Cond. B, 15 Cycles	
Temp. Cycle	1010, Cond. C, 100 Cycles	
Moisture Resistance	1004	
Endpoint Electrical	Applicable Device Spec.	
Hermeticity	1014	
Visual Examination	1004, 1010	
Subgroup 4		LTPD = 15
Mechanical Shock	2002, Cond. B	
Vibration	2007, Cond. A	
Constant Acceleration	2001, Cond. E	
Hermeticity	1014	
Visual Examination	1010, 1011	
Endpoint Electrical	Applicable Device Spec.	
Subgroup 5		LTPD = 15
Salt Atmosphere	1009, Cond. A	
Hermeticity	1014	
Visual Examination	1009	
Subgroup 6		3(0)
Internal Water Vapor	1018 < 5,000 PPM, 100°C	
Subgroup 7		LTPD = 15
Lead Finish Adhesion	2025	
Subgroup 8		5(0)
Lid Torque	2024	

Military Ordering Information

Lattice Semiconductor Corporation (LSC) offers the most comprehensive line of high- and low-density military E^2CMOS Programmable Logic Devices. LSC recognizes the trend in military device procurement towards using SMD compliant devices and encourages customers to use the SMD number where it exists, when ordering parts. Listed below are LSC's military qualified devices and their corresponding SMD numbers. Please contact your local Lattice representative for the latest product listing.

Military Products Selector Guide

Family	Part #	SMD #	Tpd (ns)	Fmax (MHz)	Icc		Package
					Typ (mA)	Max (mA)	
ispLSI	ispLSI 1016-60LH/883	5962-9476201MXC	20	60	100	170	44-Pin JLCC
	ispLSI 1024-60LH/883	5962-9476101MXC	20	60	135	220	68-Pin JLCC
	ispLSI 1032-60LG/883	5962-9308501MXC	20	60	135	220	84-Pin CPGA
	ispLSI 1048C-50LG/883	5962-9558701MXC *	22	50	165	235	133-Pin CPGA
pLSI	pLSI 1016-60LH/883	5962-9476301MXC	20	60	100	170	44-Pin JLCC
	pLSI 1024-60LH/883	5962-9476001MXC	20	60	135	220	68-Pin JLCC
	pLSI 1032-60LG/883	5962-9466801MXC	20	60	135	220	84-Pin CPGA
	pLSI 1048C-50LG/883	5962-9558801MXC *	22	50	165	235	133-Pin CPGA
GAL16V8	GAL16V8C-7LD/883	5962-8983907RA	7.5	100	75	130	20-Pin CERDIP
	GAL16V8C-7LR/883	5962-89839072A	7.5	100	75	130	20-Pin LCC
	GAL16V8B-10LD/883	5962-8983904RA	10	62.5	75	130	20-Pin CERDIP
	GAL16V8B-10LR/883	5962-89839042A	10	62.5	75	130	20-Pin LCC
	GAL16V8B-15LD/883	5962-8983903RA	15	50	75	130	20-Pin CERDIP
	GAL16V8B-15LR/883	5962-89839032A	15	50	75	130	20-Pin LCC
	GAL16V8B-20LD/883	5962-8983902RA	20	41.6	75	130	20-Pin CERDIP
	GAL16V8B-20LR/883	5962-89839022A	20	41.6	75	130	20-Pin LCC
	GAL16V8B-30LD/883	5962-8983901RA	30	33.3	75	130	20-Pin CERDIP
GAL20V8	GAL20V8B-10LD/883	5962-8984004LA	10	62.5	75	130	24-Pin CERDIP
	GAL20V8B-10LR/883	5962-89840043A	10	62.5	75	130	28-Pin LCC
	GAL20V8B-15LD/883	5962-8984003LA	15	50	75	130	24-Pin CERDIP
	GAL20V8B-15LR/883	5962-89840033A	15	50	75	130	28-Pin LCC
	GAL20V8B-20LD/883	5962-8984002LA	20	41.6	75	130	24-Pin CERDIP
	GAL20V8B-20LR/883	5962-89840023A	20	41.6	75	130	28-Pin LCC
GAL22V10	GAL22V10C-10LD/883	5962-8984106LA	10	166	90	150	24-Pin CERDIP
	GAL22V10C-10LR/883	5962-89841063A	10	166	90	150	28-Pin LCC
	GAL22V10B-15LD/883	5962-8984103LA	15	62.5	90	150	24-Pin CERDIP
	GAL22V10B-15LR/883	5962-89841033A	15	62.5	90	150	28-Pin LCC
	GAL22V10B-20LD/883	5962-8984102LA	20	33	90	150	24-Pin CERDIP
	GAL22V10B-20LR/883	5962-89841023A	20	33	90	150	28-Pin LCC
	GAL22V10B-25LD/883	5962-8984104LA	25	33	90	150	24-Pin CERDIP
	GAL22V10B-30LD/883	5962-8984101LA	30	25	90	150	24-Pin CERDIP

* Preliminary

Military Ordering Information

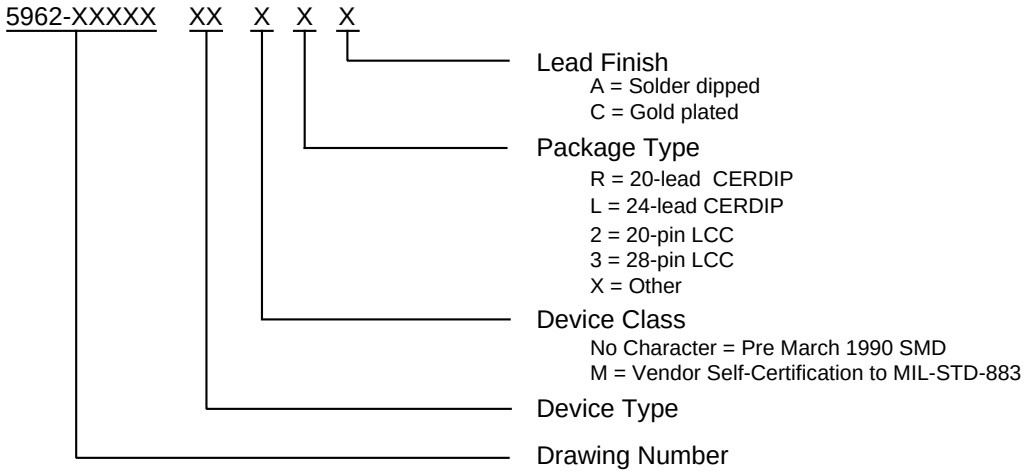
DESC Standard Military Drawing Listing

SMD #	LATTICE PART #
5962-8983901RA	GAL16V8B-30LD/883
5962-89839022A	GAL16V8B-20LR/883
5962-8983902RA	GAL16V8B-20LD/883
5962-89839032A	GAL16V8B-15LR/883
5962-8983903RA	GAL16V8B-15LD/883
5962-89839042A	GAL16V8B-10LR/883
5962-8983904RA	GAL16V8B-10LD/883
5962-89839072A	GAL16V8C-7LR/883
5962-8983907RA	GAL16V8C-7LD/883
5962-89840023A	GAL20V8B-20LR/883
5962-8984002LA	GAL20V8B-20LD/883
5962-89840033A	GAL20V8B-15LR/883
5962-8984003LA	GAL20V8B-15LD/883
5962-89840043A	GAL20V8B-10LR/883
5962-8984004LA	GAL20V8B-10LD/883

SMD #	LATTICE PART #
5962-8984101LA	GAL22V10B-30LD/883
5962-89841023A	GAL22V10B-20LR/883
5962-8984102LA	GAL22V10B-20LD/883
5962-89841033A	GAL22V10B-15LR/883
5962-8984103LA	GAL22V10B-15LD/883
5962-8984104LA	GAL22V10B-25LD/883
5962-89841063A	GAL22V10C-10LR/883
5962-8984106LA	GAL22V10C-10LD/883
5962-9308501MXC	ispLSI 1032-60LG/883
5962-9466801MXC	pLSI 1032-60LG/883
5962-9476001MXC	pLSI 1024-60LH/883
5962-9476101MXC	ispLSI 1024-60LH/883
5962-9476201MXC	ispLSI 1016-60LH/883
5962-9476301MXC	pLSI 1016-60LH/883
5962-9558701MXC*	ispLSI 1048C-50LG/883
5962-9558801MXC*	pLSI 1048C-50LG/883

*Preliminary

Standard Military Drawing Number Description



GAL16V8/883

High Performance E²CMOS PLD
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 7.5 ns Maximum Propagation Delay**
  - **— Fmax = 100 MHz**
  - **— 6 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 12 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **50% REDUCTION IN POWER FROM BIPOLAR**
  - **— 75mA Typ Icc**
- **ACTIVE PULL-UPS ON ALL PINS (GAL16V8C-7 and GAL16V8B-10)**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

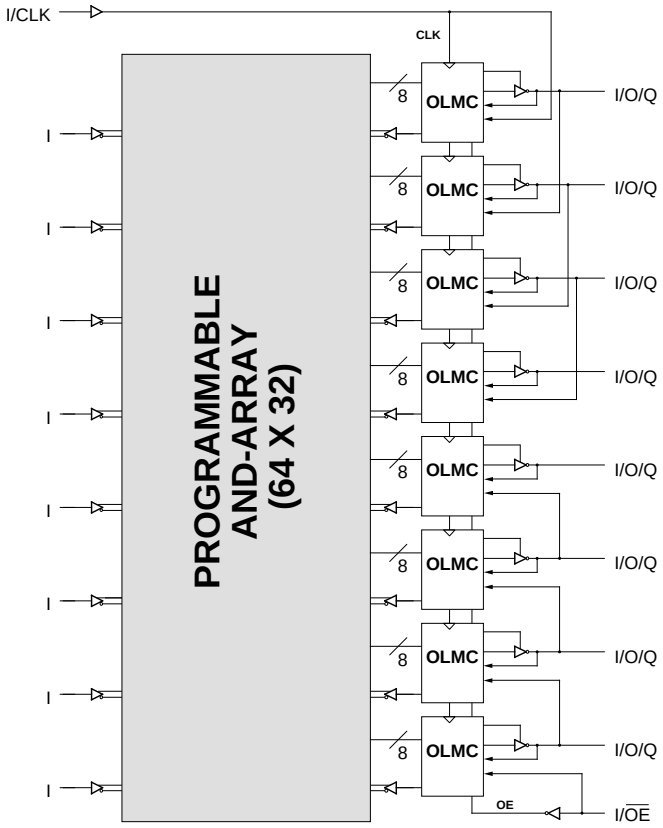
DESCRIPTION

The GAL16V8/883 is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883. This military grade device combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed/power performance available in the 883 qualified PLD market. The GAL16V8C/883, at 7.5ns maximum propagation delay time, is the world's fastest military qualified CMOS PLD.

The generic GAL architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL16V8/883 is capable of emulating all standard 20-pin PAL® devices with full function/fuse map/parametric compatibility.

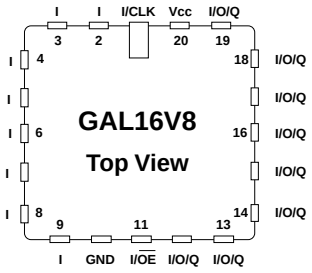
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM

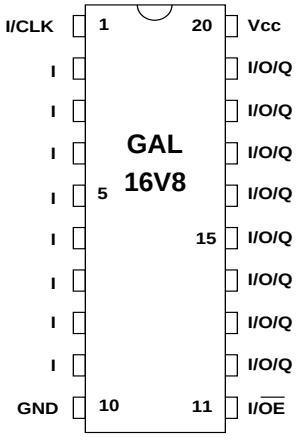


PIN CONFIGURATION

LCC



CERDIP



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Case Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) ..... –55 to 125°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	12	mA
I_{OH}	High Level Output Current			—	—	–2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C		–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L-7	—	75	130	mA

1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	-7		UNITS
			MIN.	MAX.	
tpd	A	Input or I/O to Combinational Output	1	7.5	ns
tco	A	Clock to Output Delay	1	6	ns
tcf[2]	—	Clock to Feedback Delay	—	6	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	7	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	76.9	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	76.9	—	MHz
	A	Maximum Clock Frequency with No Feedback	100	—	MHz
twh	—	Clock Pulse Duration, High	5	—	ns
twl	—	Clock Pulse Duration, Low	5	—	ns
ten	B	Input or I/O to Output Enabled	1	9	ns
	B	$\overline{OE}$ to Output Enabled	1	7	ns
tdis	C	Input or I/O to Output Disabled	1	9	ns
	C	$\overline{OE}$ to Output Disabled	1	7	ns

1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Descriptions section.
3) Refer to fmax Descriptions section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Case Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) ..... –55 to 125°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	L-10[1]	—	—	–100	µA
			L-15/-20/-30	—	—	–10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	12	mA
I_{OH}	High Level Output Current			—	—	–2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C		–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -10/-15/ -20/-30	—	75	130	mA

1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	-10		-15		-20		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinational Output	2	10	3	15	3	20	3	30	ns
tco	A	Clock to Output Delay	1	7	2	12	2	15	2	20	ns
tcf[2]	—	Clock to Feedback Delay	—	7	—	12	—	15	—	20	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	12	—	15	—	25	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	58.8	—	41.6	—	33.3	—	22.2	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	58.8	—	41.6	—	33.3	—	22.2	—	MHz
	A	Maximum Clock Frequency with No Feedback	62.5	—	50	—	41.6	—	33.3	—	MHz
twh	—	Clock Pulse Duration, High	8	—	10	—	12	—	15	—	ns
twl	—	Clock Pulse Duration, Low	8	—	10	—	12	—	15	—	ns
ten	B	Input or I/O to Output Enabled	—	10	—	15	—	20	—	30	ns
	B	$\overline{OE}$ to Output Enabled	—	10	—	15	—	18	—	25	ns
tdis	C	Input or I/O to Output Disabled	—	10	—	15	—	20	—	30	ns
	C	$\overline{OE}$ to Output Disabled	—	10	—	15	—	18	—	25	ns

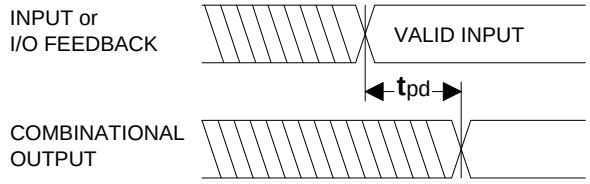
1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Descriptions section.
3) Refer to fmax Descriptions section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

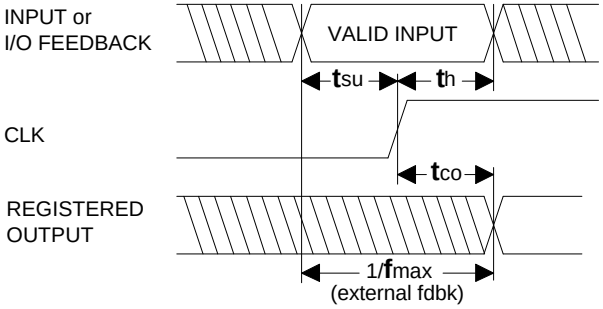
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

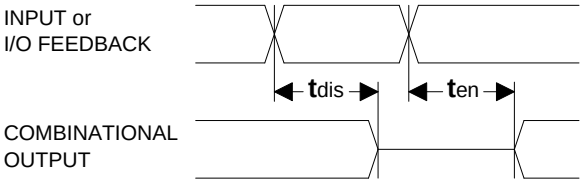
SWITCHING WAVEFORMS



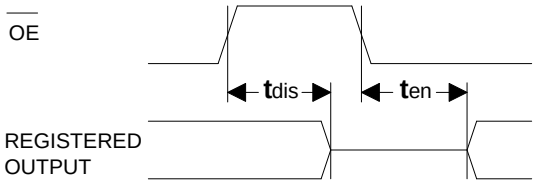
Combinatorial Output



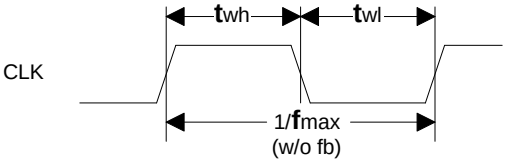
Registered Output



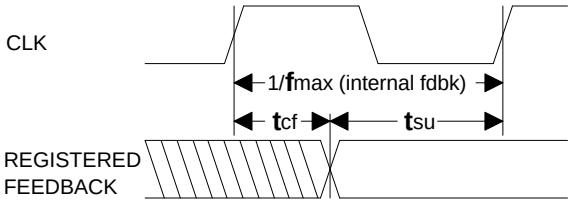
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

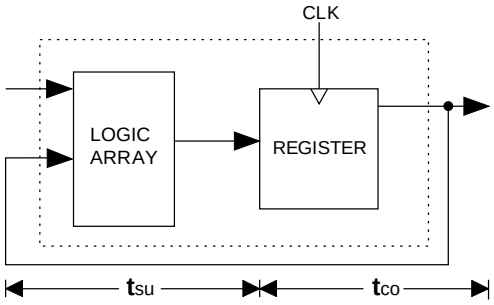


Clock Width



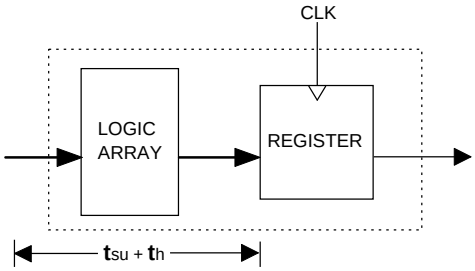
fmax with Feedback

fmax DESCRIPTIONS



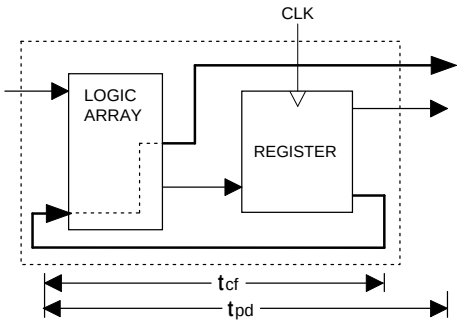
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

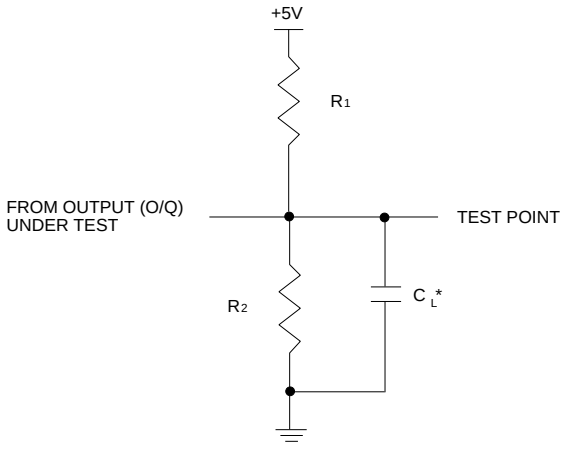
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		390Ω	750Ω	50pF
B	Active High	∞	750Ω	50pF
	Active Low	390Ω	750Ω	50pF
C	Active High	∞	750Ω	5pF
	Active Low	390Ω	750Ω	5pF



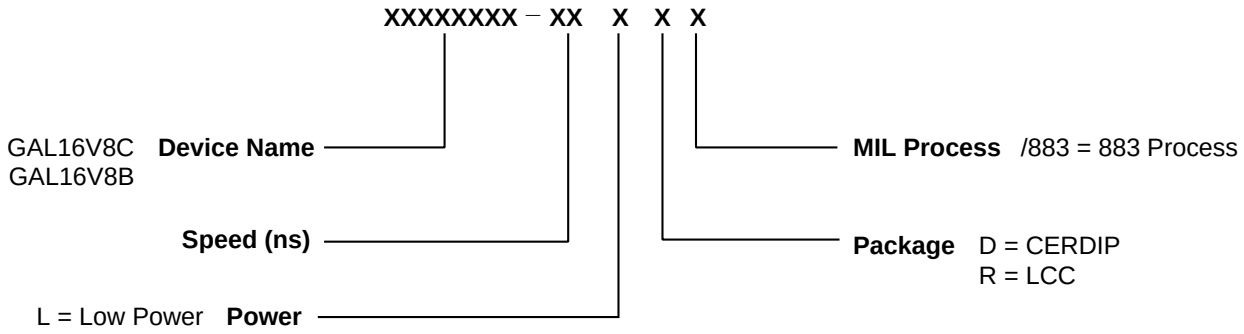
*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL16V8 ORDERING INFORMATION (MIL-STD-883 and SMD)

					Ordering #	
Tpd (ns)	**Tsu (ns)**	**Tco (ns)**	**Icc (mA)**	**Package**	**MIL-STD-883**	**SMD #**
7.5	7	6	130	20-Pin CERDIP	GAL16V8C-7LD/883	5962-8983907RA
			130	20-Pin LCC	GAL16V8C-7LR/883	5962-89839072A
10	10	7	130	20-Pin CERDIP	GAL16V8B-10LD/883	5962-8983904RA
			130	20-Pin LCC	GAL16V8B-10LR/883	5962-89839042A
15	12	12	130	20-Pin CERDIP	GAL16V8B-15LD/883	5962-8983903RA
			130	20-Pin LCC	GAL16V8B-15LR/883	5962-89839032A
20	15	15	130	20-Pin CERDIP	GAL16V8B-20LD/883	5962-8983902RA
			130	20-Pin LCC	GAL16V8B-20LR/883	5962-89839022A
30	25	20	130	20-Pin CERDIP	GAL16V8B-30LD/883	5962-8983901RA

Note: Lattice Semiconductor recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number is recommended.

PART NUMBER DESCRIPTION



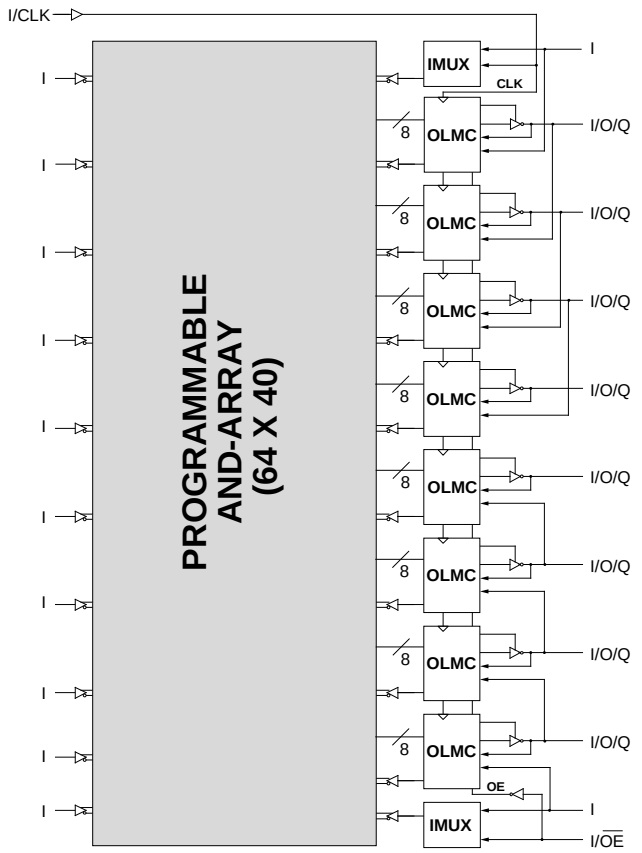
GAL20V8/883

High Performance E²CMOS PLD Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 10 ns Maximum Propagation Delay**
  - **— Fmax = 62.5 MHz**
  - **— 7 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 12 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **50% REDUCTION IN POWER FROM BIPOLAR**
  - **— 75mA Typ Icc on Low Power Device**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Also Emulates 24-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

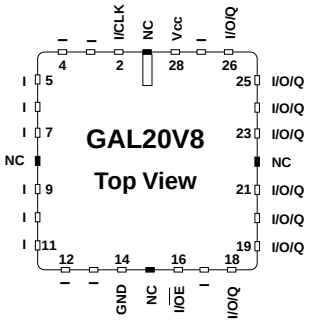
The GAL20V8/883 is a high performance E²CMOS programmable logic devices processed in full compliance to MIL-STD-883. This military grade device combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed/power performance available in the 883 qualified PLD market.

The generic GAL architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20V8/883 is capable of emulating all standard 24-pin PAL® devices with full function/fuse map/parametric compatibility.

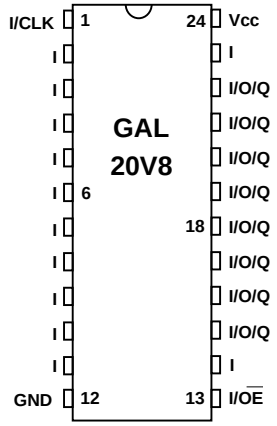
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

PIN CONFIGURATION

LCC



CERDIP



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Case Temperature with
Power Applied ..... –55 to 125°C

1.Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

CaseTemperature (T_C) ..... –55 to 125°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V_{IH} \le V_{IN} \le V_{CC}$		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	12	mA
I_{OH}	High Level Output Current			—	—	–2.0	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C		–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -10/-15/-20	—	75	130	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and TA = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	-10		-15		-20		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinational Output	2	10	2	15	2	20	ns
tco	A	Clock to Output Delay	1	7	1	12	1	15	ns
tcf[2]	—	Clock to Feedback Delay	—	7	—	12	—	15	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	12	—	15	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	58.8	—	41.6	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	58.8	—	41.6	—	33.3	—	MHz
	A	Maximum Clock Frequency with No Feedback	62.5	—	50	—	41.6	—	MHz
twh	—	Clock Pulse Duration, High	8	—	10	—	12	—	ns
twl	—	Clock Pulse Duration, Low	8	—	10	—	12	—	ns
ten	B	Input or I/O to Output Enabled	—	10	—	15	—	20	ns
	B	$\overline{OE}$ to Output Enabled	—	10	—	15	—	18	ns
tdis	C	Input or I/O to Output Disabled	—	10	—	15	—	20	ns
	C	$\overline{OE}$ to Output Disabled	—	10	—	15	—	18	ns

1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Descriptions section.
3) Refer to fmax Descriptions section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Case Temperature with
Power Applied ..... –55 to 125°C

1.Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

CaseTemperature (T_C) ..... –55 to 125°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \le V_{IN} \le V_{CC}$		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	12	mA
I_{OH}	High Level Output Current			—	—	–2.0	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C		–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz Outputs Open	L -15/-20	—	75	130	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and TA = 25 °C

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	-15		-20		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinational Output	3	15	3	20	ns
tco	A	Clock to Output Delay	2	12	2	15	ns
tcf[2]	—	Clock to Feedback Delay	—	12	—	15	ns
tsu	—	Setup Time, Input or Feedback before Clock	12	—	15	—	ns
th	—	Hold Time, Input or Feedback after Clock	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	41.6	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	41.6	—	33.3	—	MHz
	A	Maximum Clock Frequency with No Feedback	50	—	41.6	—	MHz
twh	—	Clock Pulse Duration, High	10	—	12	—	ns
twl	—	Clock Pulse Duration, Low	10	—	12	—	ns
ten	B	Input or I/O to Output Enabled	—	15	—	20	ns
	B	$\overline{OE}$ to Output Enabled	—	15	—	18	ns
tdis	C	Input or I/O to Output Disabled	—	15	—	20	ns
	C	$\overline{OE}$ to Output Disabled	—	15	—	18	ns

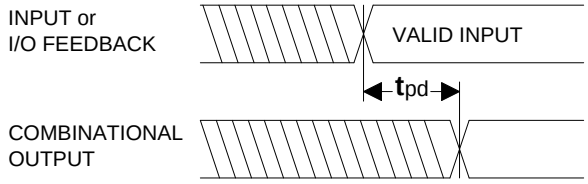
1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Descriptions section.
3) Refer to fmax Descriptions section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

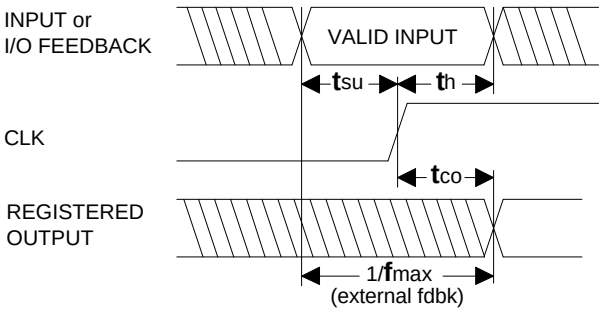
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

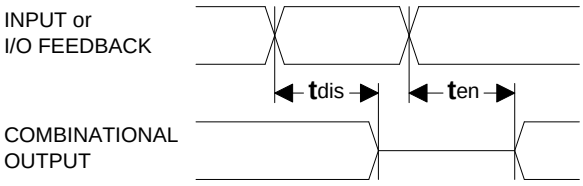
SWITCHING WAVEFORMS



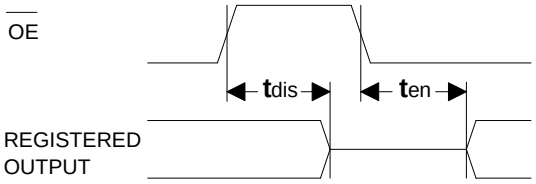
Combinatorial Output



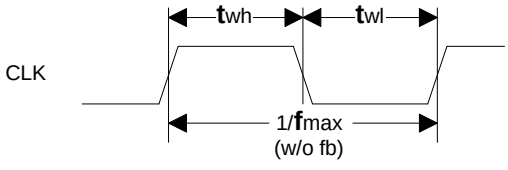
Registered Output



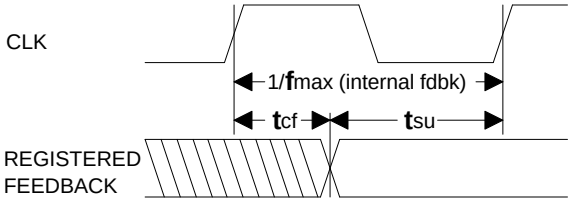
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

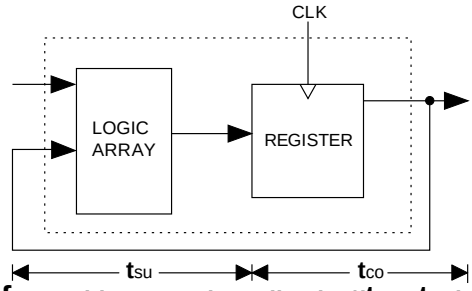


Clock Width



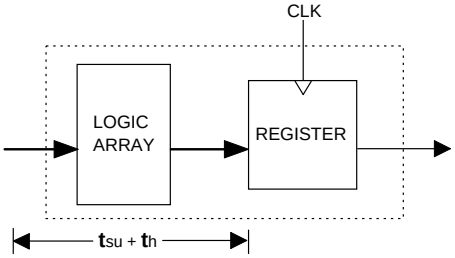
fmax with Feedback

fmax DESCRIPTIONS



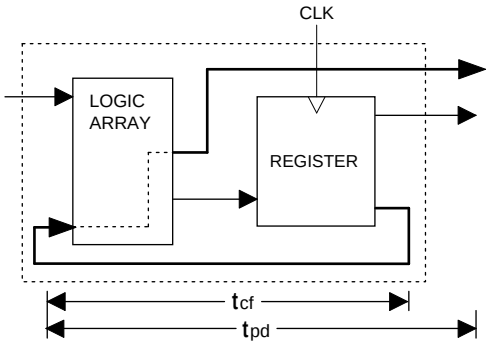
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

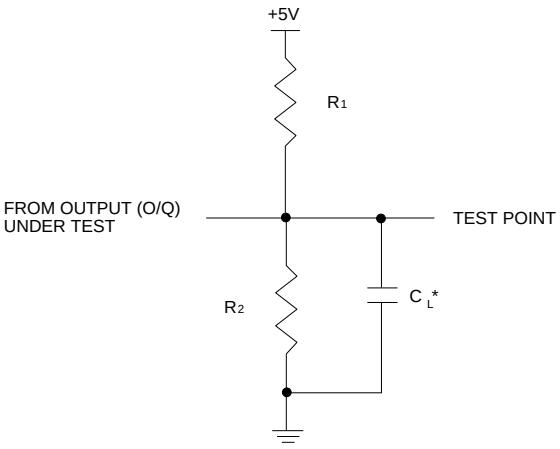
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		390Ω	750Ω	50pF
B	Active High	∞	750Ω	50pF
	Active Low	390Ω	750Ω	50pF
C	Active High	∞	750Ω	5pF
	Active Low	390Ω	750Ω	5pF



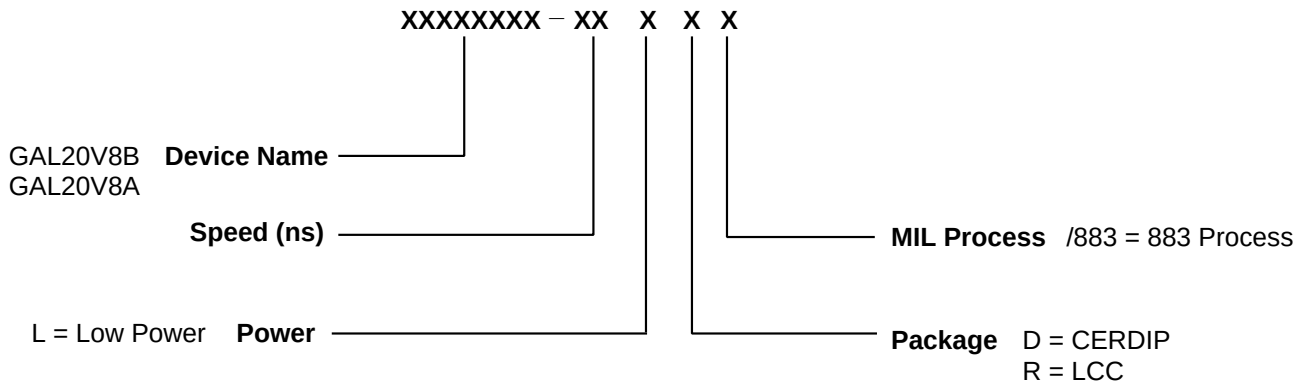
*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL20V8 ORDERING INFORMATION (MIL-STD-883 and SMD)

					Ordering #	
Tpd (ns)	**Tsu (ns)**	**Tco (ns)**	**Icc (mA)**	**Package**	**MIL-STD-883**	**SMD #**
10	10	7	130	24-Pin CERDIP	GAL20V8B-10LD/883	5962-8984004LA
			130	28-Pin LCC	GAL20V8B-10LR/883	5962-89840043A
15	12	12	130	24-Pin CERDIP	GAL20V8B-15LD/883	5962-8984003LA
			130	28-Pin LCC	GAL20V8A-15LR/883	5962-89840033A
20	15	15	130	24-Pin CERDIP	GAL20V8B-20LD/883	5962-8984002LA
			130	28-Pin LCC	GAL20V8A-20LR/883	5962-89840023A

Note: Lattice Semiconductor recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number is recommended.

PART NUMBER DESCRIPTION



GAL22V10/883

High Performance E²CMOS PLD Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 10 ns Maximum Propagation Delay**
  - **— Fmax = 166 MHz**
  - **— 7ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 12 mA Outputs**
  - **— UltraMOS® Advanced CMOS Technology**
- **ACTIVE PULL-UPS ON ALL PINS**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
  - **— Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVCMOS 22V10 Devices**
- **50% REDUCTION IN POWER VERSUS BIPOLAR**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

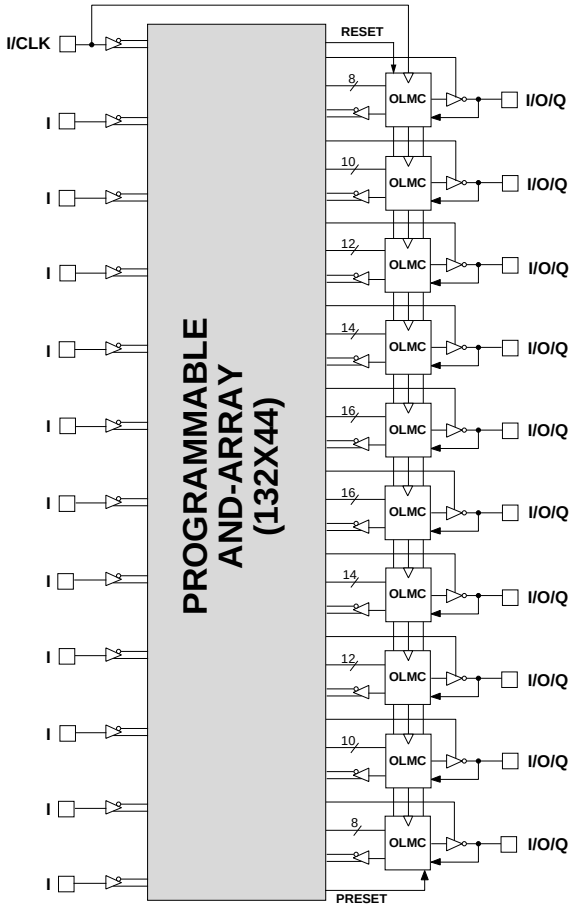
DESCRIPTION

The GAL22V10/883 is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883. This military grade device combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available of any military qualified 22V10 device. CMOS circuitry allows the GAL22V10 to consume much less power when compared to bipolar 22V10 devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

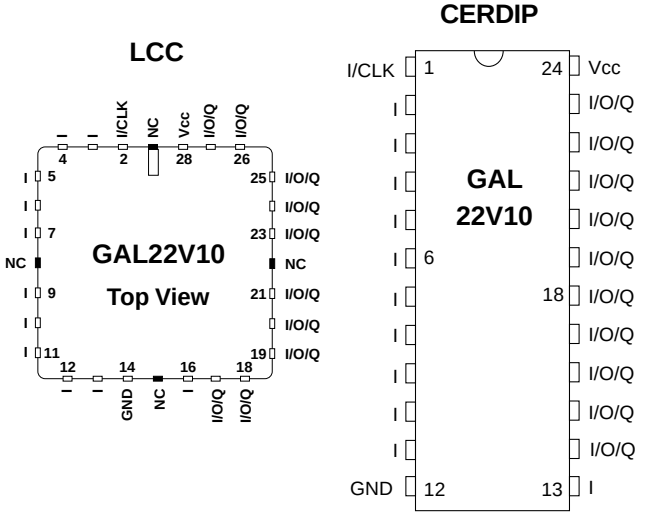
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10 is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor guarantees 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are guaranteed.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037; http://www.latticesemi.com

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Case Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) ..... -55 to 125°C
Supply Voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss - 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	12	mA
I_{OH}	High Level Output Current			—	—	-2.0	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C		-50	—	-135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -10	—	90	150	mA

1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-10		UNITS
			MIN.	MAX.	
tpd	A	Input or I/O to Combinatorial Output	—	10	ns
tco	A	Clock to Output Delay	—	7	ns
tcf[2]	—	Clock to Feedback Delay	—	7	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	6	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	76.9	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	76.9	—	MHz
	A	Maximum Clock Frequency with No Feedback	166	—	MHz
twh	—	Clock Pulse Duration, High	3	—	ns
twl	—	Clock Pulse Duration, Low	3	—	ns
ten	B	Input or I/O to Output Enabled	—	10	ns
tdis	C	Input or I/O to Output Disabled	—	12	ns
tar	A	Input or I/O to Asynchronous Reset of Register	—	12	ns
tarw	—	Asynchronous Reset Pulse Duration	10	—	ns
tarr	—	Asynchronous Reset to Clock Recovery Time	6	—	ns
tspr	—	Synchronous Preset to Clock Recovery Time	10	—	ns

1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Description section.
3) Refer to fmax Description section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +7V
Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Case Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Case Temperature (T_C) ..... -55 to 125°C
Supply Voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss - 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	12	mA
I_{OH}	High Level Output Current			—	—	-2.0	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C		-50	—	-135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -15/-20/-25/-30	—	90	150	mA

1) The leakage current is due to the internal pull-up on all pins. See Input Buffer section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-15		-20		-25		-30		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinatorial Output	—	15	—	20	—	25	—	30	ns
tco	A	Clock to Output Delay	—	8	—	15	—	20	—	20	ns
tcf[2]	—	Clock to Feedback Delay	—	8	—	15	—	20	—	20	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	12	—	17	—	20	—	25	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	50	—	31.2	—	25	—	22	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	50	—	31.2	—	25	—	22	—	MHz
	A	Maximum Clock Frequency with No Feedback	62.5	—	33	—	33	—	25	—	MHz
twh	—	Clock Pulse Duration, High	8	—	15	—	15	—	20	—	ns
twl	—	Clock Pulse Duration, Low	8	—	15	—	15	—	20	—	ns
ten	B	Input or I/O to Output Enabled	—	15	—	20	—	25	—	25	ns
tdis	C	Input or I/O to Output Disabled	—	15	—	20	—	25	—	25	ns
tar	A	Input or I/O to Asynchronous Reset of Register	—	20	—	25	—	30	—	30	ns
tarw	—	Asynchronous Reset Pulse Duration	15	—	20	—	25	—	30	—	ns
tarr	—	Asynchronous Reset to Clock Recovery Time	15	—	20	—	25	—	30	—	ns
tspr	—	Synchronous Preset to Clock Recovery Time	12	—	17	—	20	—	25	—	ns

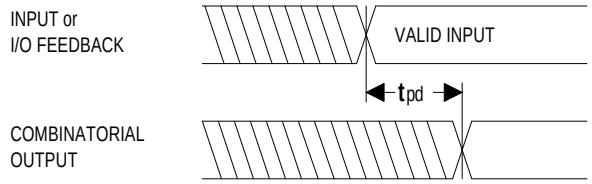
1) Refer to Switching Test Conditions section.
2) Calculated from **f**max with internal feedback. Refer to fmax Description section.
3) Refer to fmax Description section.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

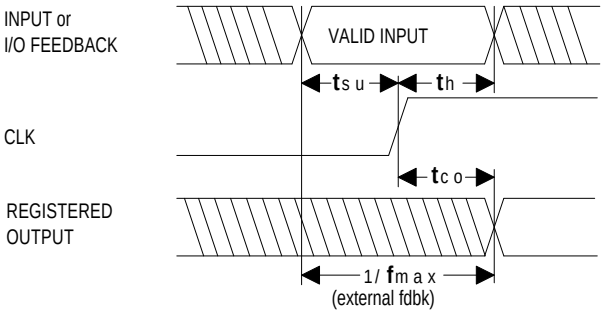
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

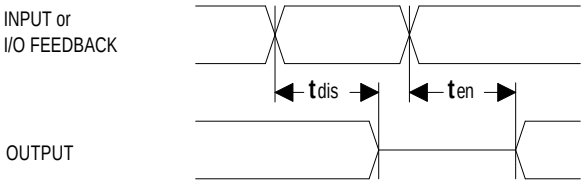
SWITCHING WAVEFORMS



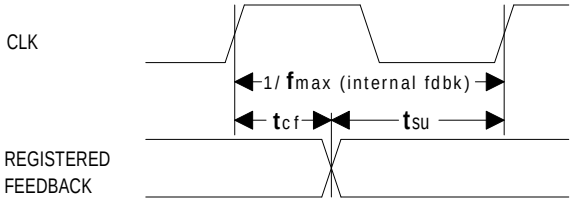
Combinatorial Output



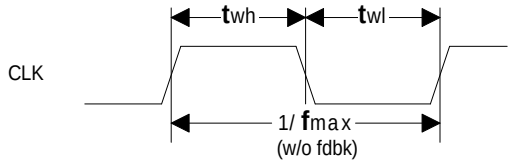
Registered Output



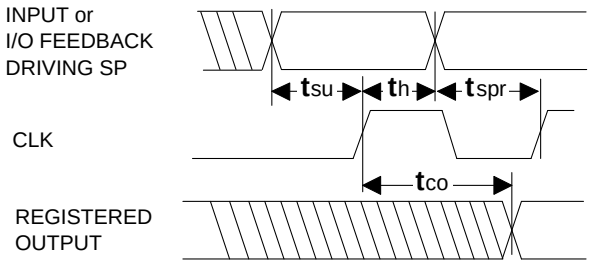
Input or I/O to Output Enable/Disable



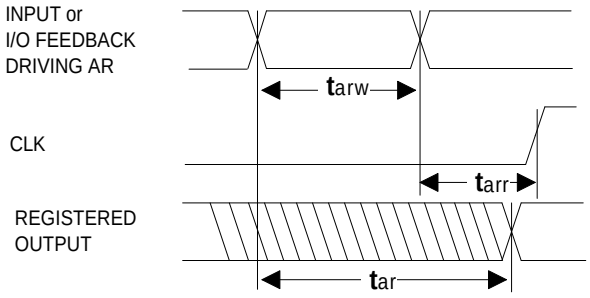
fmax with Feedback



Clock Width

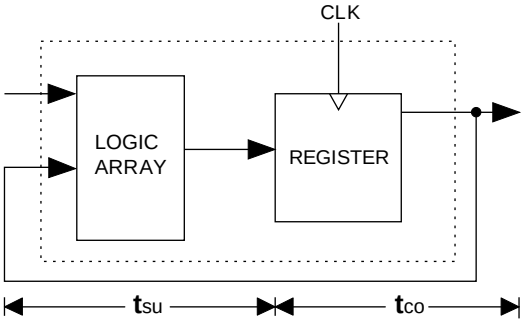


Synchronous Preset



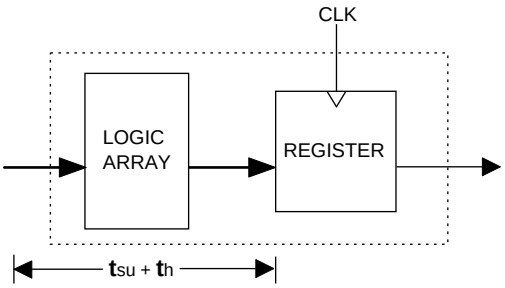
Asynchronous Reset

fmax DESCRIPTIONS



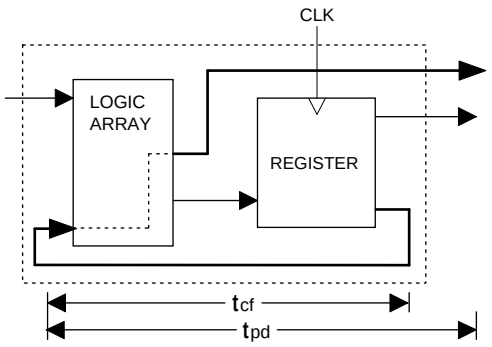
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

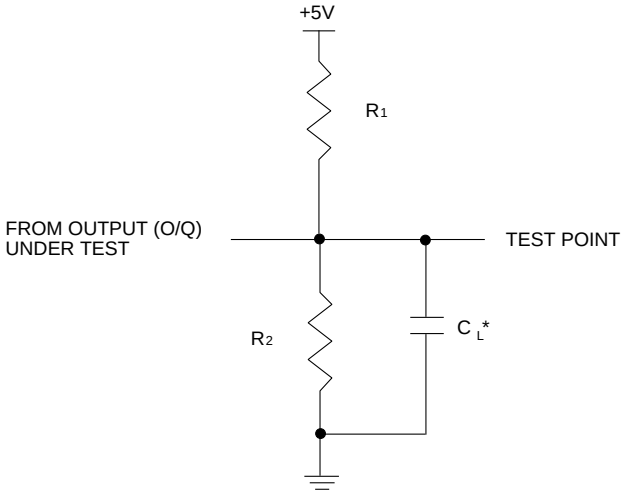
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		390Ω	750Ω	50pF
B	Active High	∞	750Ω	50pF
	Active Low	390Ω	750Ω	50pF
C	Active High	∞	750Ω	5pF
	Active Low	390Ω	750Ω	5pF



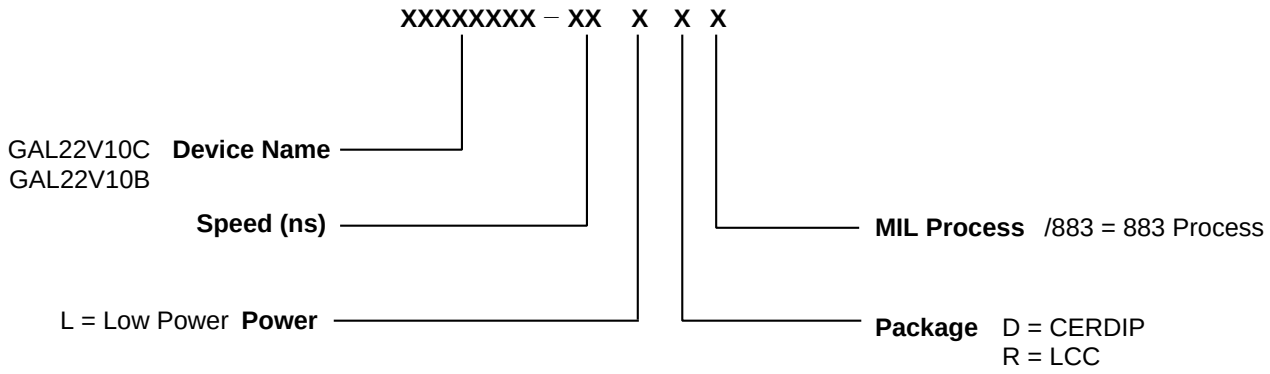
*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL22V10 ORDERING INFORMATION (MIL-STD-883 and SMD)

					Ordering #	
Tpd (ns)	**Tsu (ns)**	**Tco (ns)**	**Icc (mA)**	**Package**	**MIL-STD-883**	**SMD #**
10	6	7	150	24-Pin CERDIP	GAL22V10C-10LD/883	5962-8984106LA
			150	28-Pin LCC	GAL22V10C-10LR/883	5962-89841063A
15	12	8	150	24-Pin CERDIP	GAL22V10B-15LD/883	5962-8984103LA
			150	28-Pin LCC	GAL22V10B-15LR/883	5962-89841033A
20	17	15	150	24-Pin CERDIP	GAL22V10B-20LD/883	5962-8984102LA
			150	28-Pin LCC	GAL22V10B-20LR/883	5962-89841023A
25	20	20	150	24-Pin CERDIP	GAL22V10B-25LD/883	5962-8984104LA
30	25	20	150	24-Pin CERDIP	GAL22V10B-30LD/883	5962-8984101LA

Note: Lattice Semiconductor recognizes the trend in military device procurement towards using SMD compliant devices, as such, ordering by this number is recommended.

PART NUMBER DESCRIPTION



Section 6

Lattice Semiconductor Design Tool Strategy

Introduction

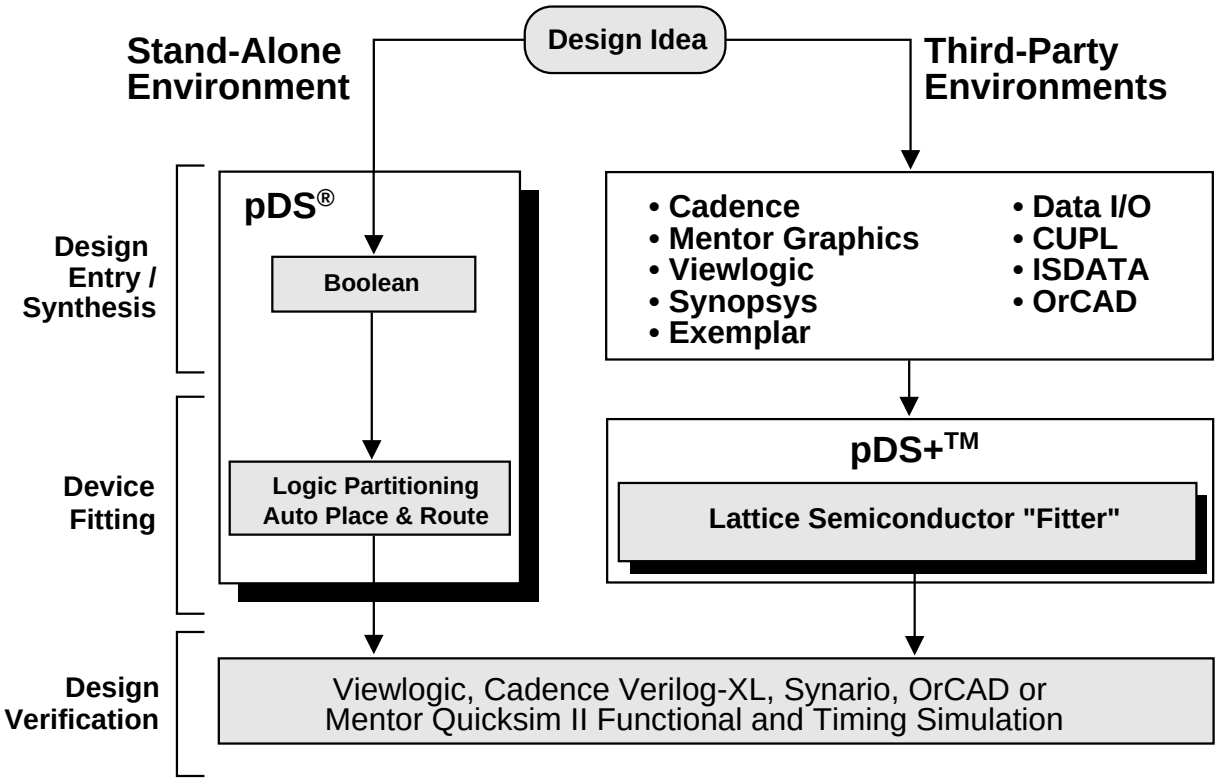
The Lattice Semiconductor Corporation (LSC) design tool strategy for the ispLSI and pLSI families is to support a wide range of design environments. LSC provides both a proprietary PC-based solution (pDS®) as well as third-party compatible CAE tools (pDS+™ Fitters) that run on PC, Sun and Hewlett Packard (HP) workstation platforms.

The LSC pDS pLSI/ispLSI software provides a comprehensive, high-performance, low-cost package for logic development. Developed and supported by LSC, pDS provides an easy-to-use Windows-based graphical interface using a mouse and pull-down menus. Design entry includes Boolean equations, standard and TTL macros. For simulation, timing tables are included as a standard offering. Additionally, pDS interfaces with Viewlogic's Viewsim, OrCAD's VST, and Data I/O's Synario simulation package for full functional and timing simulation. pDS software generates industry standard JEDEC programming files and supports direct download into ispLSI devices.

LSC's pDS+ (pDS Plus) solution supports multiple third-party CAE tools, providing designers with the capability to design in familiar CAE environments. These third-party CAE tools offer schematic capture, hardware description language (such as VHDL), state machine language, Boolean equation, and macro design entry as well as functional and timing simulators for design verification.

LSC's pDS and pDS+ solutions give designers powerful, easy to use, cost-effective design tools to meet their development needs. Each third-party vendor must adhere to strict quality and certification requirements before becoming qualified, thus ensuring superior support.

Figure 1. pDS and pDS+ Design Flows



Lattice Semiconductor Design Tool Strategy

Design Flow

There are three steps in the LSC ispLSI and pLSI design flow: design entry, device fitting (logic partitioning, place and route), and design verification. (See the pDS and pDS+ Design Flow). This section outlines the design flow of the pDS and pDS+ solutions.

pDS

LSC's pDS solution is a comprehensive, self-contained design solution which operates on a PC under Microsoft Windows™. pDS uses familiar ABEL-like Boolean equations, standard macros and a library of TTL macros for design entry, and provides manual partitioning, high speed automatic place and route, and simulation timing tables for design verification. A variety of simulators, such as Viewlogic's Viewsim simulation package, are compatible with pDS for functional and timing simulation.

After the development work has been completed, the design is ready to be programmed into a device. For third-party programming support, the pDS package generates a JEDEC fusemap . Alternatively, the ispLSI devices can be programmed directly from the PC with the LSC isp Engineering Kit.

The pDS development systems are ideal for designers who desire a cost-effective, user friendly approach to ispLSI and pLSI design.

pDS+

The pDS+ solution combines third-party CAE tools for design entry and verification with the LSC pDS+ Fitter for device fitting to offer a powerful and complete development solution. LSC pDS+ Fitters support a broad range of third party design tools, including:

Vendor	Design Tool
Cadence	Concept, Synergy, Verilog-XL, Leapfrog
Data I/O	ABEL, Synario
Exemplar Logic	Galileo Logic Explorer
ISDATA	LOG/iC Classic, LOG/iC 2
Mentor Graphics	Design Architect, Autologic & Autologic II, Quicksim II, Quick-VHDL, System V (Model Tech)
Logical Devices	CUPL
OrCAD	SDT, PLD, VST 386+, Capture for Windows, Simulate for Windows
Synopsys	Design Compiler Expert & Professional, FPGA Compiler, VSS
Viewlogic	PRO Series, Workview Plus, Powerview, Workview Office

The design entry step is typically performed with schematic capture, Boolean equations, state machines, truth tables or a Hardware Description Language (HDL). Once design entry is complete, the design is ready to be implemented into a LSC ispLSI or pLSI device.

The LSC pDS+ Fitter uses architecture-specific algorithms to synthesize a logic description into an ispLSI or pLSI device. Steps in the device fitting process include logic optimization and minimization, automatic logic partitioning, and automatic place and route.

pDS+ also supports design verification. Design verification options include both functional and timing simulation. Various combinations of graphical and text-based functional and timing simulators are supported by third-party CAE vendors.

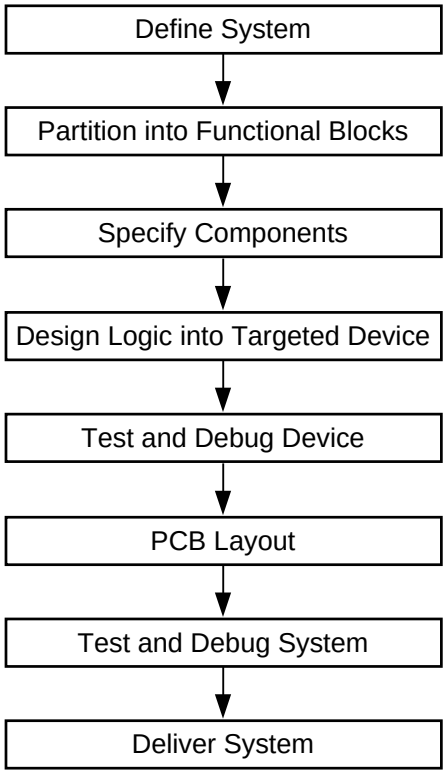
Following design verification, the LSC pDS+ Fitter generates a JEDEC fusemap for device programming. The design can be programmed into a pLSI device using third-party programmers. In addition, the ispLSI devices can be programmed directly from a PC using LSC's isp Engineering Kit, or from dedicated logic designed into the end-system.

System Design Process

Introduction

Conceptually, system definition is the first step in the design process. This involves visualizing the PLD's interaction with the rest of the electronic system and defining a general flow diagram to determine the design's basic sequential behavior. This organizational flow, used to integrate an entire subsystem into high density devices, is described in the following topics and shown in figure 1.

Figure 1. System Design Flow



Partitioning

After completing the conceptual design, the designer partitions the system into modules or functional blocks. These blocks can be a few components or multiple circuit boards with numerous components. The designer organizes these functional blocks to match the capabilities of the devices being targeted, for example, the number of I/O pins, flip-flops and gates needed. The user should also consider the frequency at which the targeted device must operate, the number of clocks required, and the timing relationships of signals (AC specifications).

Specifying Components

After the partitioning is defined, the designer chooses the components which will be used to implement the desired functions. The design should meet the system specifications using the least number of components in order to keep the system cost as low as possible while keeping the system reliability as high as possible.

System specifications calling for low weight, low power and reduced size also drive designers to higher levels of logic integration. These added requirements can adversely affect the design schedule and project completion. The ispLSI and pLSI high-density devices can meet such design requirements while delivering excellent performance. The ispLSI and pLSI family of high-speed, high-density PLDs supported by easy-to-use effective software for fast design implementation and verification.

Design Entry and Optimization

After the functional partitioning and component specifications are completed, the logic necessary to implement the functions is defined block by block. The logic may include standard TTL functions, CMOS logic functions, or functions from a library, such as the Lattice Semiconductor Corporation (LSC) Macro or TTL library. The implementation of logic into a high density device is optimized for the targeted device by the design software. The partitioning also affects the optimization. Optimization can be for speed, utilization or a combination of both.

Logic entry for an LSC high-density device is done with the pLSI/ispLSI Development System (pDS) or with any of the third-party CAE tools supported by LSC's pDS+ Fitters. The pDS software utilizes the Graphical User Interface (GUI) of Microsoft's Windows™ to provide a complete design flow from logic entry to programming ispLSI/pLSI devices within hours. pDS+ Fitters, in conjunction with third-party CAE tools, support textual design entry using a Hardware Description Language (HDL); standard CAE schematic design entry; and/or Boolean, truth table or state machine entry.

Test and Debug

When designing a system, or a portion of a system, it is easier to test and debug pieces or modules rather than the entire system. In this manner, the designer can

confirm module designs, or functional blocks, and find problems earlier in the design cycle.

Logic can be verified by either timing simulation or actual testing of the programmed device. Simulation can be accomplished using a variety of logic simulators. Design errors detected by software simulation can be corrected by the designer before the printed circuit board is laid out and manufactured, which saves time and reduces cost. Board and system level simulation can be accomplished through behavioral simulation using Synopsys Logic Modeling Division models.

Reprogrammable devices allow the designer to test, debug, and modify logic right on the p.c. board. ispLSI and pLSI devices can be reprogrammed multiple times. This reprogrammability further assists the designers by allowing them to temporarily program the devices with diagnostic and design verification logic.

The designer should always attempt to design logic with testability in mind. Testability means different things to different designers. Key guidelines to be aware of are:

- ❑ Large counters should be segmented for quick and easy testing.
- ❑ Logic should be designed for controllability and observability.
- ❑ There should be no floating nets.
- ❑ All nets should be at a known state or are able to be set or reset.

To assist system testability, the ispLSI devices offer preload and verification features. These features allow register contents to be verified without using logic analyzers or other debugging tools.

Printed Circuit Board Layout

Once the logic has been verified, the Printed Circuit Board (PCB) is laid out and manufactured. Since the logic may be changed during design, this phase of the system design is usually executed after the logic has been validated. It is recommended that board design and layout be done after verifying designs using ispLSI and pLSI parts.

System Test and Debug

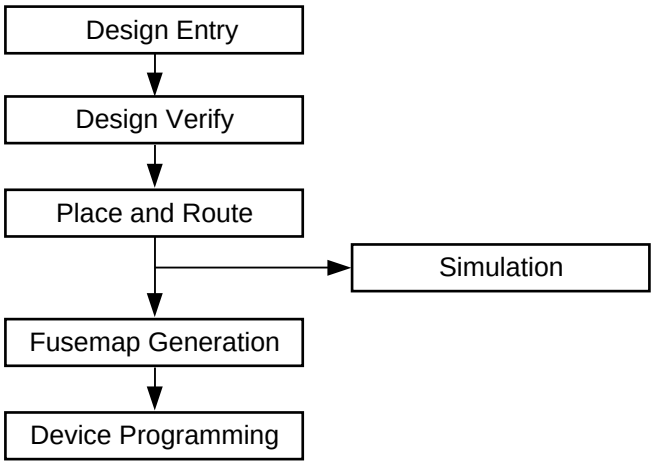
System test and debug is the final stage of the design process. The logic and the PCB are tested as a system and minor enhancements or bug fixes are implemented. Because of the flexibility of the ispLSI and pLSI devices, minor changes can be made without greatly affecting the layout of the PCB or the pinout of the device.

ispLSI and pLSI Design Flow

Introduction

Once the system design has been organized into functional components, and the logic functions which need to be incorporated in the selected components defined, the logic design phase begins. The general design flow is shown in figure 1. An ispLSI or pLSI design may be implemented from a number of design environments: including pLSI/ispLSI Development System (pDS) and numerous third-party CAE tools.

Figure 1. General Design Flow



These design environments offer various levels of design implementation from logic entry through programming the device. They support a variety of user interfaces and entry methods including: MS Windows GUI, Verilog-HDL, VHDL, truth tables, state machines and Boolean equations.

Design Entry

The pDS software allows the user to manually partition the logic to control design fit and performance. Using the MS Windows environment, logic functions are placed into Generic Logic Blocks (GLBs) and I/O Cells. This can be done by using the Edit, Cut, Copy, and Paste functions to enter Boolean equations and/or pre-defined functions from the LSC Macro and TTL libraries.

In addition to Boolean design entry, the pDS+ Fitters (in conjunction with third-party CAE tools) allow high-level descriptions of counters, adders, comparators, etc. High-level languages also support state machines, truth tables and case constructs for behavioral design implementations.

For standard CAE schematic designs, the pDS+ Fitters/third-party CAE tools provide support for graphical and hierarchical logic implementations using the Lattice Semiconductor Corporation (LSC) libraries of primitives and macros. The integrated user interfaces also allow easy integration of system or user-created functions into a hierarchical schematic using a top-down or bottom-up design methodology.

Design Verification

Verification using the pDS software is accomplished in two steps after logic has been placed. First, each cell may be individually verified to ensure that the minimized logic will fit into the GLB architecture. After all GLB and I/O cells are incrementally checked, the entire design is then verified to ensure that all nets have proper sources and destinations.

Because the advanced pDS+ tools perform automatic partitioning, design verification is done at a higher-level (pre-partitioned). For example, in the ABEL environment, the Compile (ahdl2pla) function performs the syntax and design rule checks. After the Compile phase, the Optimize (plaopt) function (optionally) minimizes the design.

In the pDS+Viewlogic environment, pre-partitioned design verification is performed by the Design Analyzer which ensures the logic conforms to the LSC design rules. Other CAE tools may perform these functions differently, but each has been tested for completeness and accuracy.

Partitioning

Partitioning using the pDS software is done by the user as part of the design entry process. The advanced pDS+ tools incorporate LSC's automatic partitioner which accepts converted data from designs entered using the third-party CAE tool of choice. LSC specific attributes for design entry are available to guide the partitioner in order to optimize usage of device features and performance.

Place and Route

All LSC design tools offer automatic place and route. This entails placement of GLB and IOC logic and then routing (or interconnecting) the source signals to their destinations. In the ispLSI and pLSI devices, the Global

Routing Pool (GRP) provides fast interconnects from external inputs and GLB feedbacks to the GLB inputs. The Output Routing Pool (ORP) provides flexible interconnects from GLB outputs to external pins.

Post-Route Simulation

After place and route, a netlist for full timing and function simulation may be passed to the third-party simulator. Many of these simulators offer both textual and graphical input and interfaces. Board and system level simulation models are available from Synopsys Logic Modeling Division.

Documentation

Report files, containing partitioned equations and pin-out information, may be generated for routed or un-routed designs. The pDS software can also generate reports with post-route maximum timing delays. In addition, the design can be exported in a variety of design formats. This supports design interfaces to standard third-party CAE tools.

Device Programming

Programming information is generated on a routed design by the FuseMap Generator for a specific ispLSI and pLSI device. It is an ASCII file written in the JEDEC format.

Two programming methods are used to program the ispLSI and pLSI devices. The first method uses the Device Programming Mode for both types of devices. This method facilitates device programming support from third-party vendors. The second method uses the LSC In-System Programming Mode and applies to the ispLSI family of devices.

Both methods of device programming allow the user to program and read back the fuesmap from the programmed device for verification (if the security cell has not been set).

Figure 2. pDS Design Flow

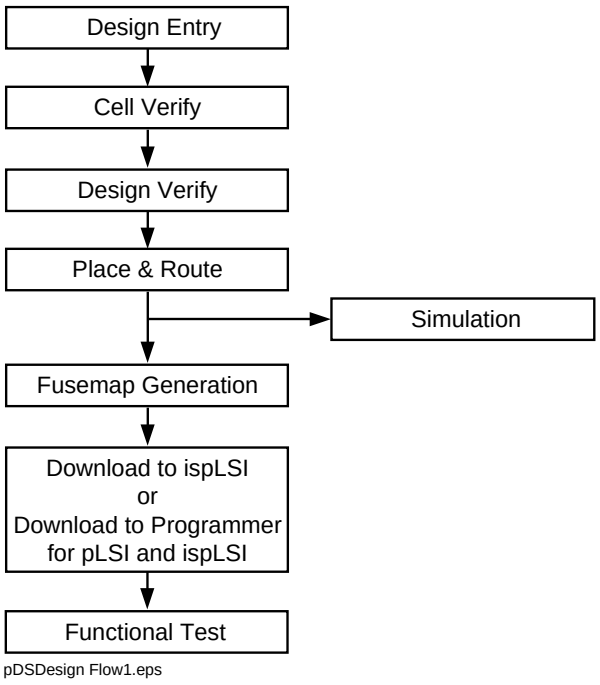
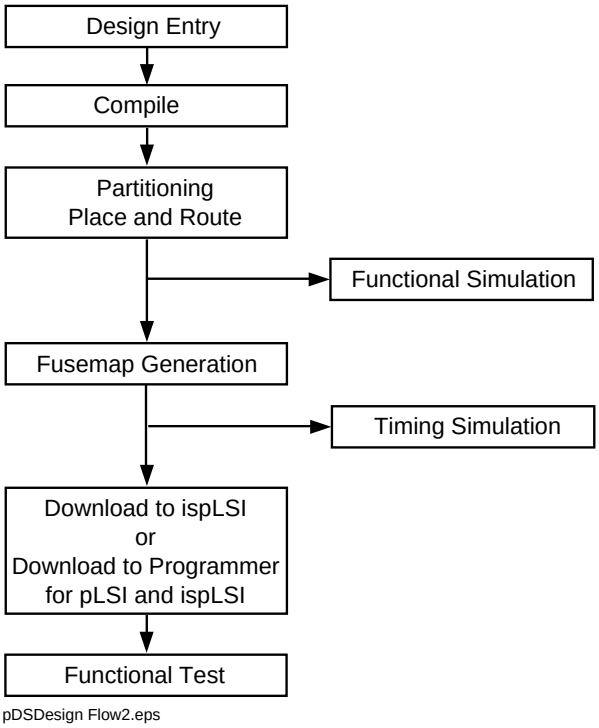


Figure 2a. Typical pDS+ Design Flow



pDS® Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000 and 6000**
- **DESIGN ENTRY WITH EASY-TO-USE WINDOWS™ ENVIRONMENT**
  - **— ABEL-Like Boolean Equation Entry**
  - **— Logic Macro Entry with Over 275 "TTL-Like" Macros and Over 200 TTL Macros**
  - **— Manual Device Partitioning Ensures Tight Control of Performance and Utilization**
- **FAST DESIGN COMPILATION**
  - **— Multi-Level Logic Synthesis**
  - **— Efficient Design Optimization and Minimization**
  - **— "Hands-Free" Automatic Place and Route**
  - **— Predictable Performance**
- **COMPLETE DESIGN VERIFICATION**
  - **— Functional and Timing Simulation Options**
- **INDUSTRY STANDARD JEDEC PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Fuse Map**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download**
  - **— ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **— PC Windows 3.1/Windows 95/ Windows NT**

Introduction

The pDS software is a comprehensive design package for the Lattice Semiconductor Corporation (LSC) ispLSI and pLSI device families giving full design entry and device implementation capabilities under the Windows design environment. The pDS software provides the best solution for high performance designs which require direct control of the logic implementation. It offers designers complete control over the performance and utilization of the device. The pDS software allows designers to quickly move from concept to a programmed logic device.

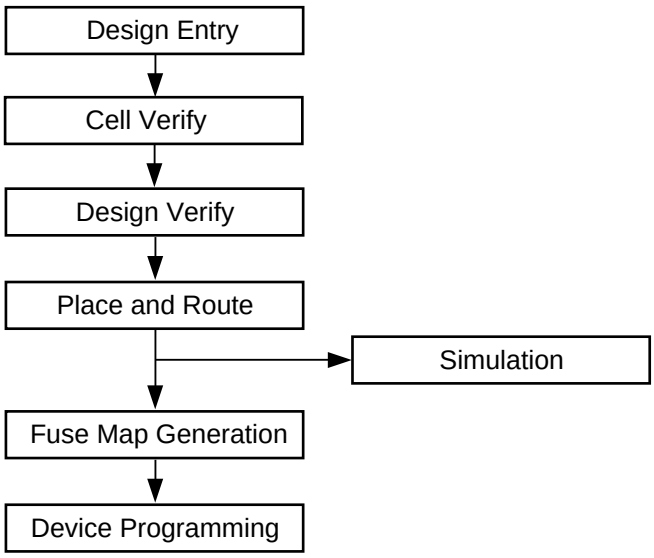
The pDS software also offers simulation options for full functional and timing simulation of designs using a variety of third-party simulators.

pDS Software

Using the pDS software, designs can be defined completely using simple Boolean equations and "TTL-like" or TTL logic macros. Automated design capabilities shorten design cycles allowing designers to explore several design solutions before deciding on the one that provides the best solution.

Designs can be entered in two ways: either through the integrated edit windows within the pDS software, or by using a standard ASCII text editor to create a design file that can be imported into the pDS environment. The Place and Route software automatically places the logic and routes the interconnections. The fuse map program generates a fuse file which can then be downloaded into a device programmer or directly to an ispLSI device (see figure 1).

Figure 1. pDS Design Flow



Design Entry

pDS software offers an easy to use interface as shown in figure 2. Designers can quickly enter the design into GLBs and I/O cells through this interface. An example of an edit window is shown in figure 3. Tables 1, 2 and 3 provide a condensed list of the different operations which are supported in the pDS software.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Figure 2. pDS Software User Interface

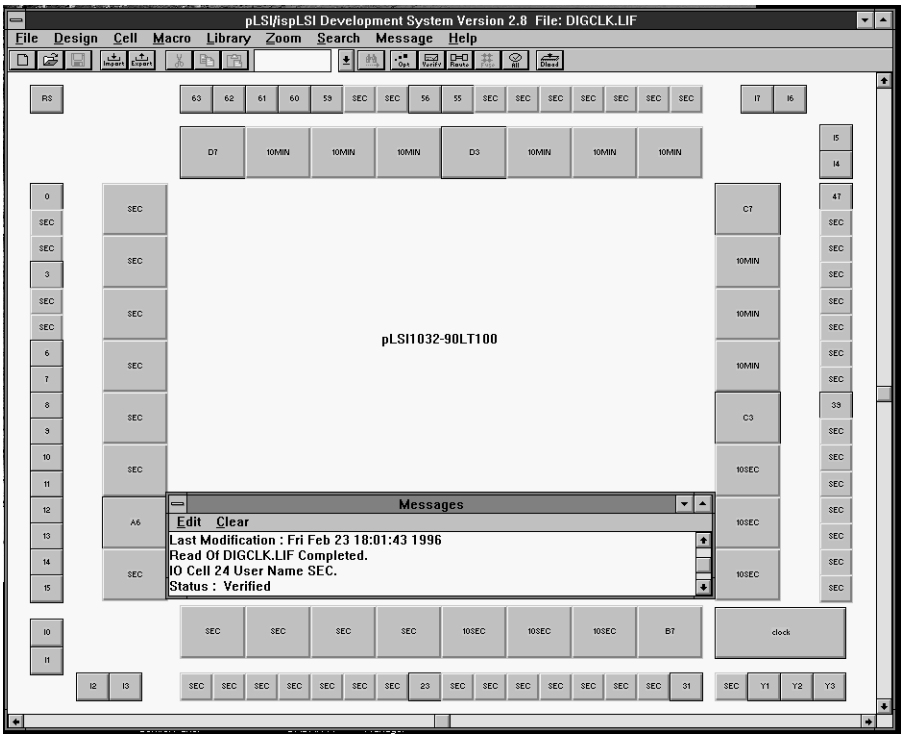


Figure 3. Sample Edit Window Illustrating Boolean Equations and Macros

```
SIGTYPE CO_P OUT;
SIGTYPE C1   REG OUT;
XOR4 (par, D1, D2, D3, D4)
EQUATIONS
     CO_P = CO_0 & CO_1 # CO_2;
     C1   = C1$$  C0;
     C1.CLK = SYSCLK;
END;
```

The following tables show some of the pDS software keywords, operators and dot extensions used.

Table 1. Keywords

Keyword	Description
CONSTANT	Assigns a value to a signal
SET	Assigns a label to a group of signals
SIGTYPE	Assigns specific attributes to a GLB output
CRIT	Used for the 4 product term bypass
XPIN	Identifies external signal in the I/O cell
LOCK	Locks an I/O cell to a pin
EQUATIONS	Beginning of the Boolean description of the logic in a GLB
//	The text that follows is a comment

Table 2. Operators

Operator	Description
=	Assignment
!	Inversion
$$	Hardware exclusive OR
&	AND
#	OR
$	Exclusive OR
!$	Exclusive NOR

Table 3. Dot Extensions

Extension	Description
.D	Identifies the signal as the D input
.Q	Identifies the signal as the Q output
.RE	Identifies the product term reset signal for the GLB
.CLK	Identifies the system clock for the GLB
.PTCLK	Identifies the product term clock for the GLB
.OE	Identifies the output enable signal for the I/O cells within the megablock

The pDS software offers an extensive selection (over 275) of TTL-like macros. These macros enable the design engineer to use familiar pre-defined functions to build a design. Table 4 shows a summary of the TTL macros also available in the pDS software.

Logic Optimization

The pDS software provides extensive design rule checking during the optimization and fitting process. After the design has been checked, the software initiates logic minimization to reduce the number of product terms needed. There are two minimization options:

— Fast Min
— Strong Min

The Fast Min option performs quick minimization to reach the debugging stage sooner. The Strong Min option performs a comprehensive logic minimization to maximize device resource utilization and ensures efficient design implementation. With the Strong Min option, small design changes can generally be performed without expensive PC board rework.

Automatic Place and Route

The pDS software provides an automatic place and route routine which eliminates the need for manual routing and provides a quicker design cycle time. The router automatically generates pinouts based on an optimal design implementation or it can use a user defined pinout.

Incremental place-and-route capability allows last-minute logic updates to be implemented without design pin-out changes.

Post Route Simulation

Complete post route design verification can be peformed using optional third party timing simulators.

Fuse Map Generation

The Lattice Semiconductor fuse map generation module outputs the file containing the fuse pattern used to implement the logic in the device. A security feature offers protection of proprietary designs from unauthorized duplication.

Table 4. Macro Summary

Function Type	Number of Macros	Number of TTL Functions
AND/NAND	20	11
OR/NOR	16	8
XOR/XNOR	4	2
Decoder/Encoder	17	16
AND/OR	8	7
Flip/Flop	28	19
Latch	10	6
Arithmetic	17	16
Counter	22	20
Shift Register	14	14
MUX/DEMUX	15	12
Miscellaneous	14	13

System Requirements

— 486/Pentium IBM Compatible PC
— MS DOS Version 3.3 or Later
— MS Windows Version 3.1 or Later
— MS Windows 95
— MS Windows NT
— 8 MB RAM and 10 MB Hard Disk Space
— Parallel Printer Port for Software Key
— VGA or Higher Resolution Display
— Mouse (Windows Compatible)

Product Ordering Information

Product Code	Description
pDS1101-PC1	pLSI/ispLSI Development System (pDS)
pDS1101-3UP/PC1	pLSI and ispLSI Development System (pDS) 3000 and 6000 Family Upgrade
pDS3302-PC2	Viewlogic Viewsim Timing & Functional Simulator
pDS1102-PC2	Viewlogic Viewsim Simulation Libraries and Interface Files
pDS1170-PC1	OrCAD VS386+ Simulation Libraries and Interface

Annual Maintenance*

pDS1101M-PC1	Maintenance for pDS1101-PC1
pDS1102M-PC2	Maintenance for pDS1102-PC2
pDS1170M-PC1	Maintenance for pDS1170-PC1
pDS3302M-PC2	Maintenance for pDS3302-PC2

*One year of maintenance is provided with every product purchase.

Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

Table 5. Programming Support

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30/A
System General	TURPRO-1

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
1-408-428-6414 (International)
BBS: 1-408-428-6417
FAX: 1-408-944-8450
email: apps@latticesemi.com

pDS+™ ABEL Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000**
- **INTEGRATED DEVELOPMENT ENVIRONMENT FOR MIXED-MODE DESIGN ENTRY**
  - **— ABEL Hardware Description Language (ABEL-HDL) or ABEL VHDL Syntax Support Boolean Equations, Truth Tables and State Machine Entry**
  - **— Graphical, Menu-Driven User Interface**
- **SUPPORTS VIEWLOGIC VIEWPLD™**
- **pDS+ ABEL FITTER**
  - **— Multi-Level Logic Synthesis**
  - **— Efficient Design Optimization and Minimization**
  - **— Automatic Mapping and Device Fitting**
  - **— Automatic Partitioning with High Utilization**
  - **— Predictable Performance**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Device Fuse Map**
- **PLATFORMS SUPPORTED**
  - **— Windows 3.1/Windows 95/Windows NT**
  - **— Sun SPARC 4™ and Above**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download (PC Versions)**
  - **— ispATE™ Board Test Programming Utility**

Introduction

The pDS+ ABEL software from Lattice Semiconductor offers a powerful solution to fit high-density logic designs into Lattice's ispLSI and pLSI devices.

Design entry is made simple by using ABEL software from Data I/O together with the pDS+ ABEL Fitter for design implementation. The ABEL software and pDS+ ABEL Fitter offer high-level, device independent design entry with efficient logic compilation, delivering unprecedented performance for the most complex designs.

Data I/O ABEL

The easy-to-use, menu-driven ABEL software packages provide a complete pre-fit design environment. Using ABEL-HDL from DATA I/O Corporation or ABEL VHDL, complex designs can be quickly and efficiently described using a combination of Boolean Equations, Truth Tables, State Machine syntax or other HDL descriptions. The HDL syntax allows design creation without regard to any specific device dependencies. The built-in functional simulator allows designs to be fully verified before device fitting. The menu driven environment makes design implementation as easy as clicking a mouse button.

pDS+ ABEL Fitter

The pDS+ ABEL Fitter for ispLSI and pLSI devices is completely integrated within the ABEL Software environment. The pDS+ ABEL Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place and route and fusemap generation with optional test vectors, in standard JEDEC format. Extensive top level design control is provided to optimize design implementation for speed and/or high device resource utilization.

Design Optimization & Logic Minimization

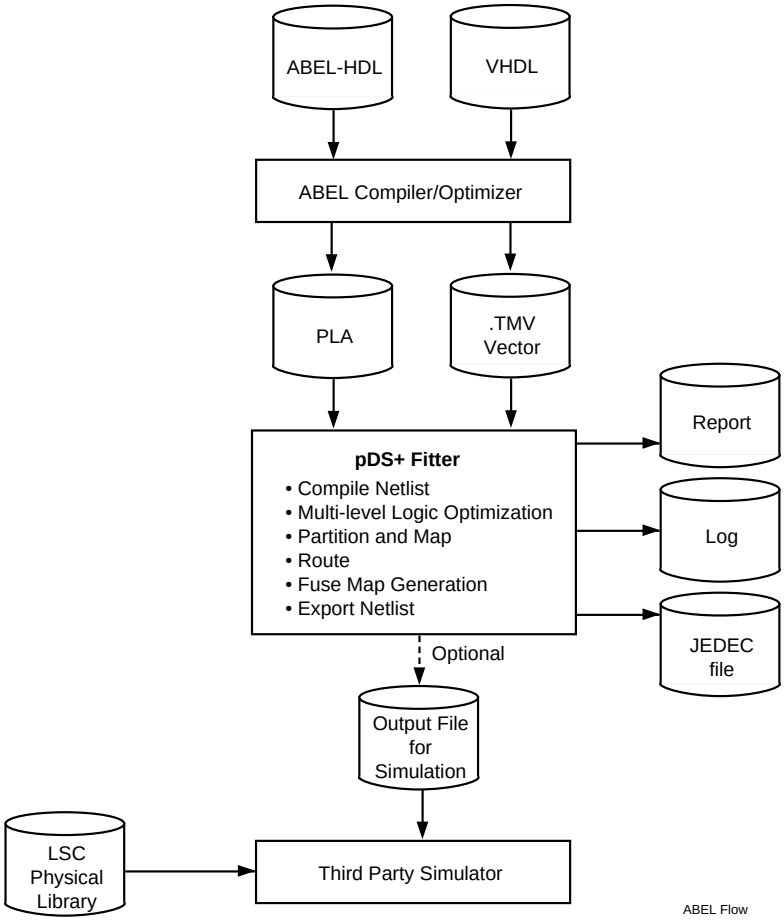
The pDS+ ABEL Fitter uses proprietary algorithms targeted for device specific features. The Fitter optimizes the design thoroughly, utilizing logic minimization, product term sharing and XOR functions whenever possible. In addition, the pDS+ ABEL Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Automatic Partitioning

The pDS+ ABEL Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features such as the hard XOR function and product term sharing. The internal XOR can be utilized for Arithmetic functions, T-Type flip-flops, and on & off set optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the fitter to efficiently use device resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Figure 1. pDS+ ABEL Fully Integrated Design Environment



Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Router optimally interconnects signals between I/O cells and GLBs through the Global Routing Pool (GRP) and Output Routing Pool (ORP). It also performs GLB splitting and GLB output duplication to enhance routing.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation. The result is that small design changes won't cause expensive PC board re-work.

Design Parameter Control

Extensive design parameter control at the design entry level is possible with the pDS+ ABEL Fitter giving the user the option to optimize the design for maximum utilization and speed. Controls are specified using "Property" statements in the ABEL design file. These controls fall into two categories:

- — Fitter Controls
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Controls

Special properties can be passed to the pDS+ ABEL Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization. Here are a few of the powerful features:

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ ABEL Fitter provides a parameter file feature which helps designers eliminate guesswork and optimizes the design for the right device. It allows the user to try a number of design implementation options using the design implementation controls in batch mode. The parameter file instructs the partitioner and the router on how to maximize both device utilization and performance.

The pDS+ ABEL Fitter also provides post-route equations showing exactly how the design is implemented in the selected device.

Fuse Map Generation

The pDS+ ABEL Fitter supports a device fusemap in standard JEDEC format. A security feature gives protection of proprietary designs from unauthorized duplication. The fitter also appends any design test vectors in JEDEC format to the device fusemap thus facilitating a quick, easy functional verification of a programmed device.

Design Verification

The pDS+ ABEL software supports functional simulation of all ispLSI and pLSI designs using the built-in ABEL functional simulator. The simulation test vectors can be combined into the JEDEC file for device testing in a programmer.

Complete post route design verification can also be performed using optional Viewlogic Viewsim, PROsim, or other third party timing simulators. The pDS+ ABEL software generates the output file required for third-party simulation. Simulation libraries are available from Lattice Semiconductor for various PC and Sun-based CAE vendor tools. The Viewlogic PROsim simulator and Synario simulator are available from Lattice Semiconductor for the PC platform.

System Requirements (PC Platform)

- 486/Pentium™ IBM Compatible PC
- Operating System
  - MSDOS Version 4.x or Later
  - Windows 3.1
  - Windows NT
  - Windows 95
- 16 MB RAM with 30MB Hard Disk Space
- ABEL 4.1 or Later
- Parallel Printer Port for Software Key

System Requirements (Sun Platform)

- Sun Sparc 4 and above
- Sun OS Version 4.x
- Open Windows 3.0
- ABEL 4.1 or Later
- 16 MB RAM with 30 MB Hard Disk Space
- 3 Button Mouse

Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88

Programmer Vendor	Model
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High-pin count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2102-PC1	Fitter for DATA I/O ABEL on PC Platform
pDS2102-3UP/PC1	3000 Family Upgrade for pDS2102-3UP/PC1
pDS2102-SN1	Fitter for DATA I/O ABEL on Sun Platform
pDS2102-3UP/SN1	3000 Family Upgrade for pDS2102-3UP/SN1
pDS1102-PC2	Viewlogic Library and Interface for PC
pDS1102-SN1	Viewlogic Library and Interface for Sun
pDS3302-PC2	PROSim Simulator with Libraries
pDS1120-PC1	Synario Libraries and Interface
pDS1170-PC1	OrCAD Simulator Library and Interface
pDS1160-SN1	Cadence Verilog-XL Library and Interface
pDS1150-SN1	Mentor Graphics Quicksim II Library and Interface

Maintenance*

pDS2102M-PC1	Maintenance for pDS2102-PC1
pDS2102M-SN1	Maintenance for pDS2102-SN1
pDS1102M-PC2	Maintenance for pDS1102-PC2
pDS1102M-SN1	Maintenance for pDS1102-SN1
pDS3302M-PC2	Maintenance for pDS3302-PC2
pDS1120M-PC1	Maintenance for pDS1120-PC1
pDS1170M-PC1	Maintenance for pDS1170-PC1
pDS1160M-SN1	Maintenance for pDS1160-SN1
pDS1150M-SN1	Maintenance for pDS1150-SN1

*One year of maintenance is provided with every product purchase.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
1-408-428-6414 (International)
BBS: 1-408-428-6417
FAX: 1-408-944-8450
email: apps@latticesemi.com

pDS+™ Cadence Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000**
- **DESIGN ENTRY USING CADENCE CONCEPT™**
  - **— Schematic-Entry**
  - **— Verilog-HDL and VHDL Entry Using Synergy Synthesis Tool**
  - **— Over 300 "TTL-Like" Macros**
  - **— Design Verification Using Verilog Functional and Timing Simulation**
  - **— Command Line Driven User Interface**
- **LATTICE SEMICONDUCTOR pDS+ CADENCE FITTER**
  - **— Automatic Device Fitter Ensures High Utilization and Performance**
  - **— Efficient Design Optimization & Minimization**
  - **— Automatic Partitioning with High Utilization**
  - **— Extended Route Option for Maximizing Device Performance or Resources**
  - **— Predictable Performance**
- **COMPLETE DESIGN VERIFICATION**
  - **— Verilog-XL™ Logic Simulation**
  - **— Verilog Netlist Used for Functional Simulation**
  - **— Input Files (.vlo and .sdf) for Verilog TIming Simulator Created by Fitter**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Device Fuse Map**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download (PC)**
  - **— ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **— SUN O/S 4.1.3 and Above**

Introduction

The pDS+ Cadence software from Lattice Semiconductor Corporation (LSC) offers a powerful solution to fit high density logic designs into Lattice Semiconductor's ispLSI and pLSI devices.

Design entry is made simple by using Concept software and or Synergy Synthesis from Cadence together with the pDS+ Cadence Fitter for design implementation. The Cadence software offers high-level, device independent design entry with efficient logic compilation, delivering unprecedented performance for the most complex designs.

Cadence Concept

The Cadence Concept schematic entry software allows the user to create designs without regard to any specific device dependencies. Cadence Concept offers features such as automatic symbol generation, cut and paste, unlimited pan and zoom, as well as many other features to help the user reach design verification quickly and easily. The menu-driven environment provides a simplified method of design entry, making use of multi-window operation for schematic, simulator and waveform windows to be opened concurrently. Verilog-HDL and VHDL high level language designs can be synthesized using Cadence's Synergy Synthesis tools. These powerful languages speed the design of both simple and complex logic functions. The design environment also includes the Verilog-XL logic simulator, which allows designs to be fully tested before device programming. Results can also be dynamically back annotated to the schematic window for design verification.

pDS+ Cadence Fitter

The pDS+ Cadence Fitter for ispLSI and pLSI devices is executed as a stand alone program, using the EDIF output from Concept or Synergy as input. The Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place & route and fusemap generation in standard JEDEC format. Timing simulation input files for Verilog are generated by the Fitter when needed by the user. The pDS+ Cadence software comes complete with a library of over 300 TTL-like macros to simplify design entry. Extensive top level design control is provided to optimize design implementation for speed and/or high device resource utilization.

Design Optimization and Logic Minimization

The pDS+ Cadence Fitter uses proprietary algorithms targeted for device specific features. The Fitter optimizes the design thoroughly, utilizing logic minimization, product term sharing and XOR functions wherever necessary. In addition, the pDS+ Cadence Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Figure 1. pDS+ Cadence Design Interface

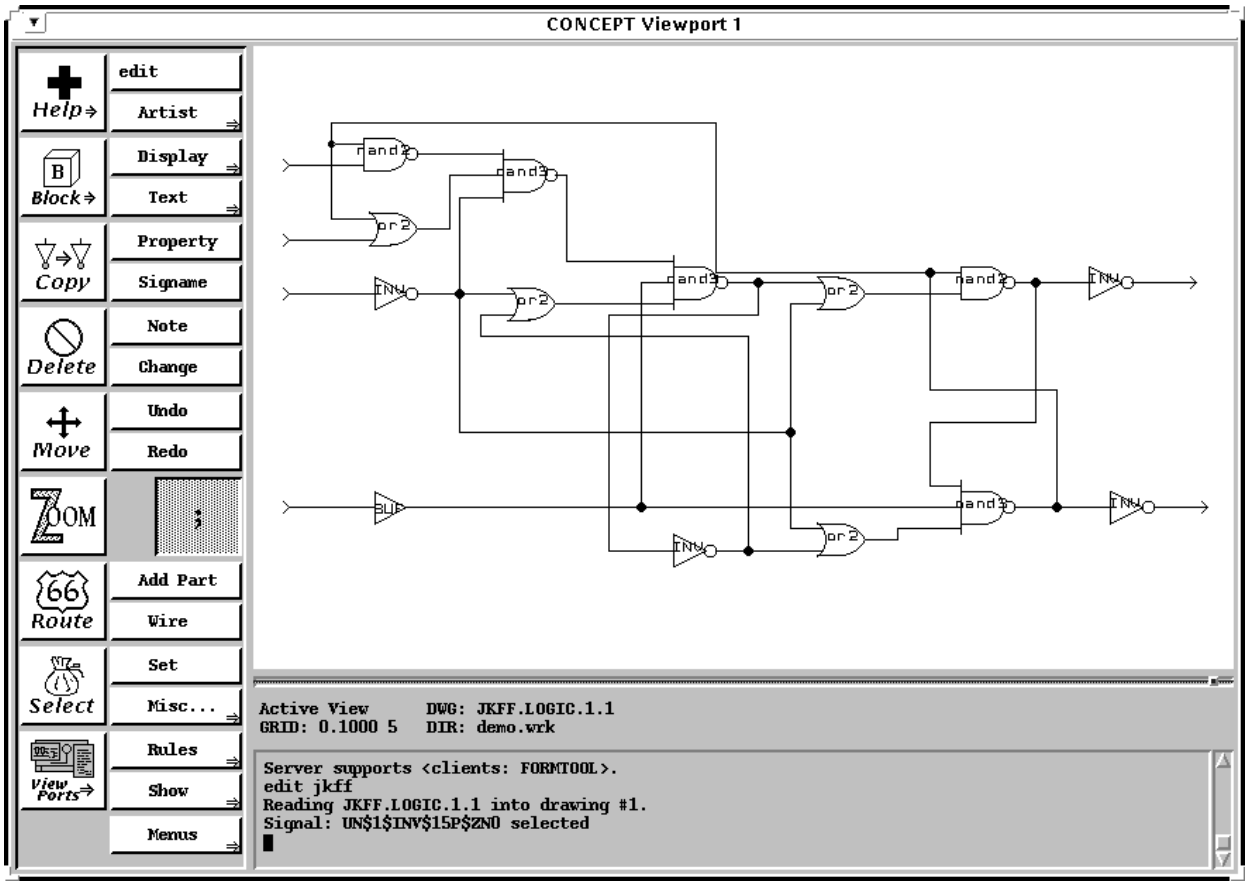
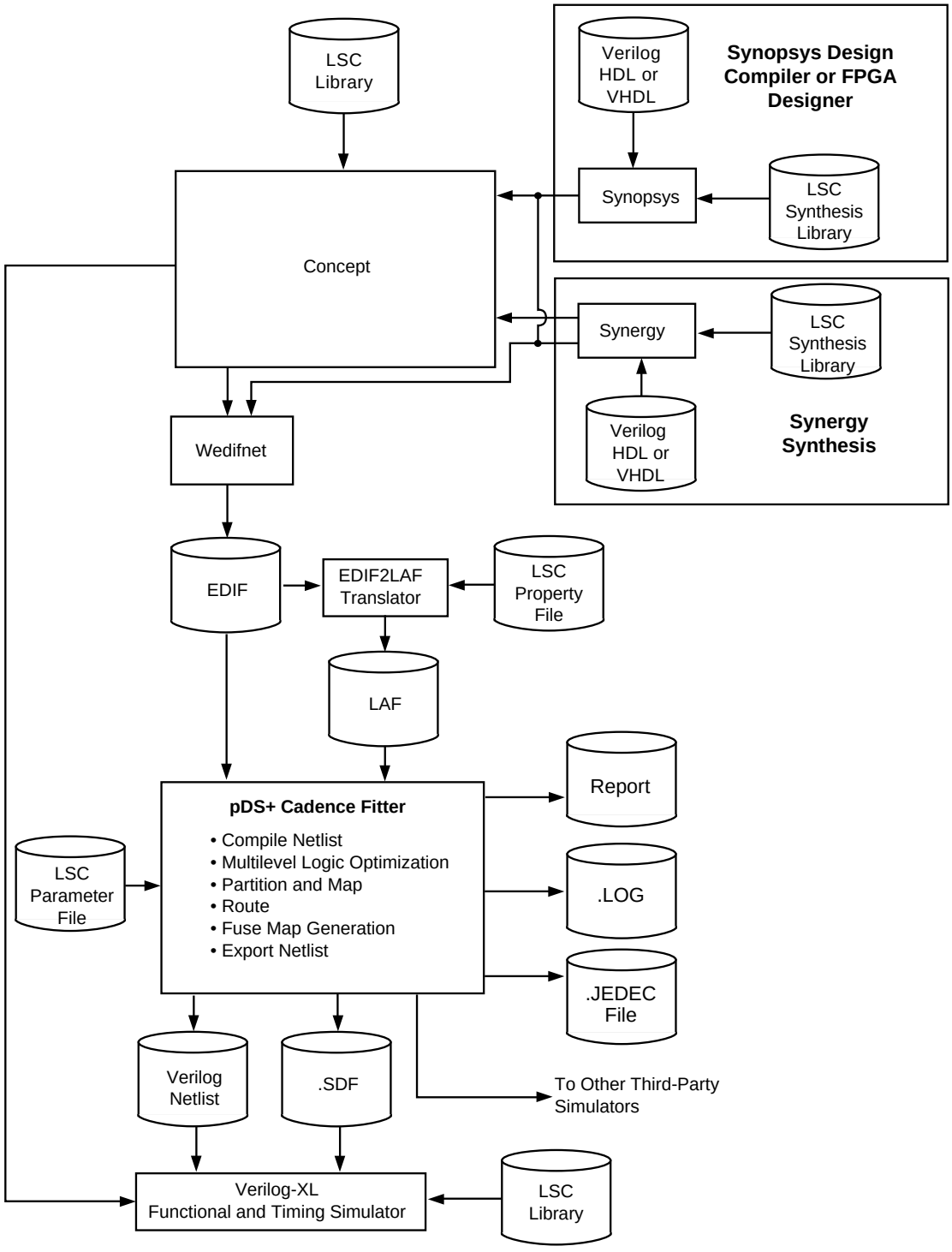


Figure 2. pDS+ Cadence Design Process



Automatic Partitioning

The pDS+ Cadence Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features, such as the hard XOR function and product term sharing. The internal XOR can be utilized for Arithmetic functions, T-Type flip-flops, and on & off set optimization functions. Common sub-expressions are extracted, and unused registers are eliminated. These features combine to maximize device resource utilization and increase design performance.

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation. The result is that small design changes won't cause expensive PC board rework.

Design Parameter Control

Extensive design parameter control at the design entry level is possible with the pDS+ Cadence Fitter giving the user the option to optimize the design for maximum utilization and speed. Controls are specified using “property” statements in the property file or parameter file. The parameter file and property files contain:

- — Fitter Control Options
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+ Cadence Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization. Here are a few of the powerful features:

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following properties specify paths in the design that have special fitting requirements:

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ Cadence Fitter uses a parameter file (.PAR file) feature to help designers optimize the design for the right device. It allows the user to try a number of design implementation options using the design implementation controls in batch mode. The parameter file instructs the partitioner and the router on how to maximize both device utilization and performance.

The pDS+ Cadence Fitter also provides post route equations showing exactly how the design is implemented in the selected device.

Design Verification

The pDS+ Cadence software provides functional and full timing simulation of ispLSI and pLSI designs using Verilog-XL Logic Simulation. Functional simulation is performed before fitting the design with a netlist is created using the Cadence Concept Verilog Netlister (vloglink). Lattice Semiconductor provides Verilog-compatible libraries to perform simulation. For timing simulation, the pDS+ Cadence Fitter generates a Verilog netlist (.vlo file) and Standard Delay Format (.sdf file) file for input to Verilog-XL, which is invoked from the command line. The test fixture file (.cmd) is used as stimulus for simulation.

Fuse Map Generation

The pDS+ Cadence Fitter generates a device fusemap in standard JEDEC format. The fusemap is automatically produced and inserted in the JEDEC file after a successful route. A security feature gives protection of proprietary designs from unauthorized duplication.

System Requirements

Sun Sparc 4 and above

- — Sun OS Version 4.x
- — Open Windows 3.0
- — 16 MB RAM with 30 MB Hard Disk space
- — 3 Button Mouse

Programmer Support

All devices in the ispLSI device family can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can be programmed using third-party PLD programmers. These devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2160-SN1	Fitter for Cadence Concept/ Verilog-XL, includes Libraries
pDS1160-SN1	Cadence Concept Schematic and Verilog Simulation Libraries and Interface
pDS1165-SN1	Cadence Synergy Synthesis Libraries
pDS2160-3UP/SN1	3000 Family Upgrade

Annual Maintenance*

pDS2160M-SN1	Maintenance for pDS2160-SN1
pDS1160M-SN1	Maintenance for pDS1160-SN1
pDS1165M-SN1	Maintainance for pDS1165-SN1

*One year of maintenance is provided with every product purchase.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
1-408-428-6414 (International)
BBS: 1-408-428-6417
FAX: 1-408-944-8450
email: apps@latticesemi.com

pDS+™ Exemplar Software

Features

- **ispLSI® and pLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000 and 6000**
- **DESIGN ENTRY USING EXEMPLAR GALILEO LOGIC EXPLORER**
  - **— VHDL OR VERILOG-HDL Entry**
  - **— Library of Over 300 Macros**
  - **— Command Line Driven User Interface**
- **LATTICE SEMICONDUCTOR pDS+™ EXEMPLAR FITTER**
  - **— Multi-Level Logic Synthesis**
  - **— Efficient Design Optimization and Minimization**
  - **— Automatic Mapping and Device Fitting**
  - **— Automatic Partitioning with High Utilization**
  - **— Predictable Performance**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Device Fuse Map**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download (PC Versions)**
  - **— ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **— PC DOS/Windows 3.1/Windows 95/Windows NT**
  - **— Sun Workstation, SUN O/S 4.1.3 and Above**

Introduction

pDS+ Exemplar software from Lattice Semiconductor Corporation (LSC) offers a powerful logic design solution for Lattice's ispLSI and pLSI families of high density PLDs.

Design entry is made simple by tight integration between Exemplar Logic's Galileo tool set and the pDS+ Exemplar Fitter for design implementation. Lattice Semiconductor's pDS+ Exemplar software offers multi-level design synthesis, automatic place and route, and efficient device utilization, delivering high performance for complex logic designs.

Exemplar's Galileo

Exemplar's Galileo Logic Explorer™ supports the description of more complex designs using standard VHDL and Verilog-HDL constructs for structural, data flow and RTL behavior. The high-level design paradigm supported by Exemplar Logic encompasses three distinct design steps: device-independent specification and simulation; constraint-independent, architecture-specific implementation; and gate-level verification.

Products in the Galileo family supporting Lattice Semiconductor ispLSI and pLSI device design include the Logic Explorer synthesis tool, the Time Explorer tool for timing analysis, schematic viewing, back annotation and the V-System VHDL simulator from Model Technology.

pDS+ Exemplar Fitter

The pDS+ Exemplar Fitter for ispLSI and pLSI devices is executed as a stand-alone program, using the EDIF output from Galileo as input. The pDS+ Fitter provides hands-off design implementation through an intelligent multi-level synthesis algorithm, logic partitioning, automatic place and route and standard JEDEC fuse map generation for device programming. Timing simulation input files for the V-System simulator are generated by the Fitter and are coupled with Lattice Semiconductor's VITAL-compliant VHDL Library as needed by the user.

Macro Library

The Lattice Semiconductor Exemplar Synthesis Libraries contain a library of over 300 high-level functions to simplify design entry. These macros enable the design engineer to use familiar, predefined functions to build a design. Direct instantiation of these functions is provided to enhance device performance and utilization.

Figure 3. Macro Summary

Macro Type	Quantity
AND/NAND	29
OR/NOR	24
XOR/XNOR	12
I/Os	89
Flip-Flops	39
Latches	30
Arithmetic	33
Counters	65
Shift Registers	15
Miscellaneous	45

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Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Figure 1. Exemplar Logic Design Interface

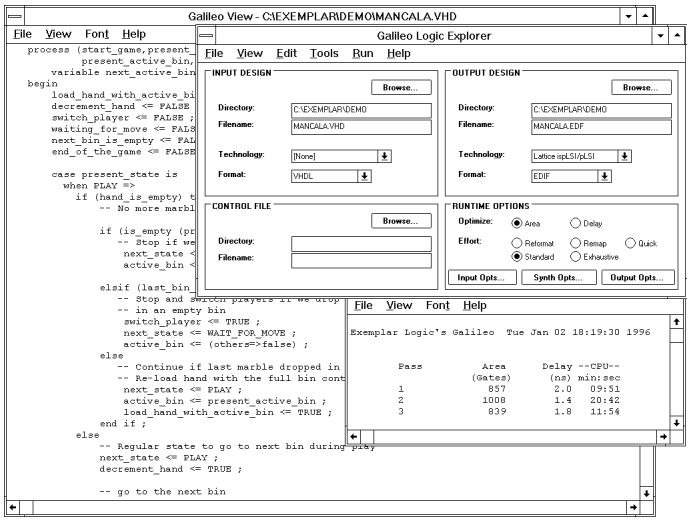
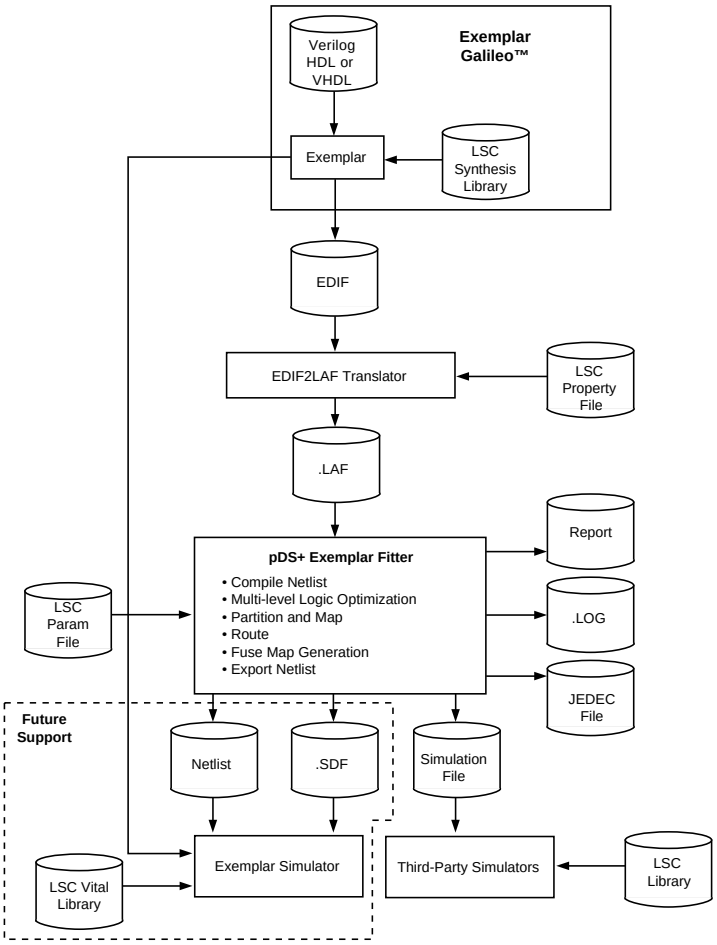


Figure 2. Lattice Semiconductor pDS+ Exemplar Design Flow



Design Optimization & Logic Minimization

The pDS+ Exemplar Fitter uses proprietary algorithms targeted for Lattice Semiconductor's device-specific architectural features. The Fitter optimizes the design thoroughly, utilizing logic minimization, product term sharing and XOR functions wherever possible. In addition, the pDS+ Exemplar Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Automatic Partitioning

The pDS+ Exemplar Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the ispLSI family's features such as the hard XOR and product term sharing. The internal XOR can be utilized for arithmetic functions, T-type flip-flops, and on and off set optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the Fitter to efficiently use device resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation.

Design Parameter Control

The pDS+ Exemplar Fitter offers extensive design control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using "attributes" in the design property and parameter files. The parameter and property files contain:

- — Fitter Control Options
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+Exemplar Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization.

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following properties specify paths in the design that have special fitting requirements:

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ Exemplar Fitter provides the ability to use a parameter file (design.par) feature which helps designers eliminiate guesswork and optimize the designs for the right devices. It allows the user to try a number of design implementation options using all of the fitter control options in a batch mode. The parameter file instructs the partitioner and the router to maximize both device utilization and performance.

Property File

The pDS+ Exemplar Fitter provides the ability to use a property file (design.prp) feature which allows the designer to control the fitter using all of the design attributes available. The property file helps guide the fitter in implementing the design in the best way.

Design Verification

The pDS+ Exemplar Fitter provides a post route design file for optional timing simulation. The pDS+ Exemplar software offers complete post route design verification using optional timing simulators. The pDS+ Exemplar Fitter generates the files required by third-party simulators, and generates a "sim" file which can be used for simulation with behavioral simulation models from Synopsys' Logic Modeling Division.

Fuse Map Generation

pDS+ Exemplar software generates a device fuse map in standard JEDEC format. A security feature offers protection of proprietary designs from unauthorized duplication. The Fitter appends any design test vectors in JEDEC format to the device fusemap, facilitating a quick, easy functional verification of a programmed device.

System Requirements (PC Platform)

- 486/Pentium™ IBM-Compatible PC
- Operating System
  - MSDOS Version 4.x or Later
  - Windows 3.1
  - Windows NT
  - Windows 95
- 16 MB RAM with 30MB Hard Disk Space
- Parallel Printer Port for Software Key

System Requirements (Sun Platform)

- Sun Sparc 4 and above
- Sun OS Version 4.x
- Open Windows 3.0
- 16 MB RAM with 30 MB Hard Disk Space
- 3 Button Mouse

Programmer Support

All devices in the Lattice Semiconductor ispLSI device family can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All Lattice Semiconductor ispLSI and pLSI devices can be programmed using third-party programmers. These devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2110-PC1	pDS+ Exemplar Fitter and Synthesis Library (PC)
pDS2110-SN1	pDS+ Exemplar Fitter and Synthesis Library (Sun)
pDS1110-PC1	Lattice Semiconductor Exemplar Synthesis Library (PC)
pDS1110-SN1	Lattice Semiconductor Exemplar Synthesis Library (Sun)
pDS2110-3UP/PC1	3000 Family Upgrade (PC)
pDS2110-3UP/SN1	3000 Family Upgrade (Sun)
pDS1131-PC1*	Verilog and VITAL Compliant VHDL Simulation Libraries (PC)
pDS1131-SN1*	Verilog and VITAL Compliant VHDL Simulation Libraries (Sun)

* Call factory for availability.

Annual Maintenance**

pDS2110M-PC1	Maintenance for pDS2110-PC1
pDS2110M-SN1	Maintenance for pDS2110-SN1
pDS1110M-PC1	Maintenance for pDS1110-PC1
pDS1110M-SN1	Maintenance for pDS1110-SN1
pDS1131M-PC1	Maintenance for pDS1131-PC1
pDS1131M-SN1	Maintenance for pDS1131-SN1

**One year of maintenance is provided with every product purchase.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic) 1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com

pDS+™ Mentor Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000**
- **DESIGN ENTRY USING MENTOR GRAPHICS DESIGN ARCHITECT SCHEMATIC CAPTURE, AUTOLOGIC AND AUTOLOGIC II SYNTHESIS AND QUICKSIM SIMULATOR**
  - **— VHDL or Verilog-HDL Entry**
  - **— Library of Over 300 Macros for Schematic Capture**
  - **— Functional and Full Timing Simulation**
  - **— Command Line Driven User Interface**
- **LATTICE SEMICONDUCTOR pDS+™ MENTOR FITTER**
  - **— Multi-Level Logic Synthesis**
  - **— Efficient Design Optimization and Minimization**
  - **— Automatic Mapping and Device Fitting**
  - **— Automatic Partitioning with High Utilization**
  - **— Predictable Performance**
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- **PLATFORMS SUPPORTED**
  - **— HP O/S UX 9.X and Above**
  - **— Sun O/S 4.x**

Introduction

pDS+™ Mentor software from Lattice Semiconductor Corporation (LSC) offers a powerful logic design solution for Lattice Semiconductor's ispLSI and pLSI families of high density devices.

Design entry is made simple using the familiar Mentor Graphics' Design Architect schematic capture and/or Autologic synthesis tools and the pDS+ Mentor Fitter for design implementation. Lattice Semiconductor's pDS+ Mentor software offers multi-level design synthesis, automatic place and route, and efficient device utilization, delivering high performance for more complex designs. Once design implementation is complete, the pDS+ Mentor software creates the proper files for full timing simulation using Mentor Graphics' QuickSim II simulator.

Mentor Graphics Tools

Schematic capture can be completed using Mentor Graphics' Design Architect schematic editor and a Lattice Semiconductor library of over 300 macros. For top-down design, use Design Architect to capture the logic design at the architectural, logic and circuit levels. Support is also available for VHDL and Verilog-HDL design synthesis using the Autologic or Autologic II synthesis tools. Autologic synthesis can take complex high-level language or behavioral, datapath or functional descriptions and make them quick and easy. Once the schematic or synthesis netlist has been created, the interface to Lattice Semiconductor's pDS+ Mentor Fitter is through a standard EDIF file. The pDS+ Mentor Fitter also outputs a standard EDIF file for interfacing to the Mentor Graphics QuickSim II simulator. QuickSim II then allows you to accurately perform and integrate full timing simulations. Quick VHDL simulation support is expected 2Q96.

pDS+ Mentor Fitter

Lattice Semiconductor's pDS+ Mentor Fitter for ispLSI and pLSI devices is executed as a stand-alone program, using the EDIF output from Mentor Graphics tools as input. The Lattice Semiconductor Fitter provides hands-off design implementation through an intelligent multi-level synthesis algorithm, logic partitioning, automatic place and route and standard JEDEC fuse map generation for device programming. Timing simulation input files for the QuickSim simulator are generated by the Fitter and are coupled with Lattice Semiconductor's Mentor Graphics simulation library when needed by the user.

Macro Library

The Lattice Semiconductor Mentor Synthesis Libraries include over 300 high-level functions to simplify design entry. These macros enable the design engineer to use familiar, predefined functions to build a design. Direct instantiation of these functions is provided to enhance device performance and utilization.

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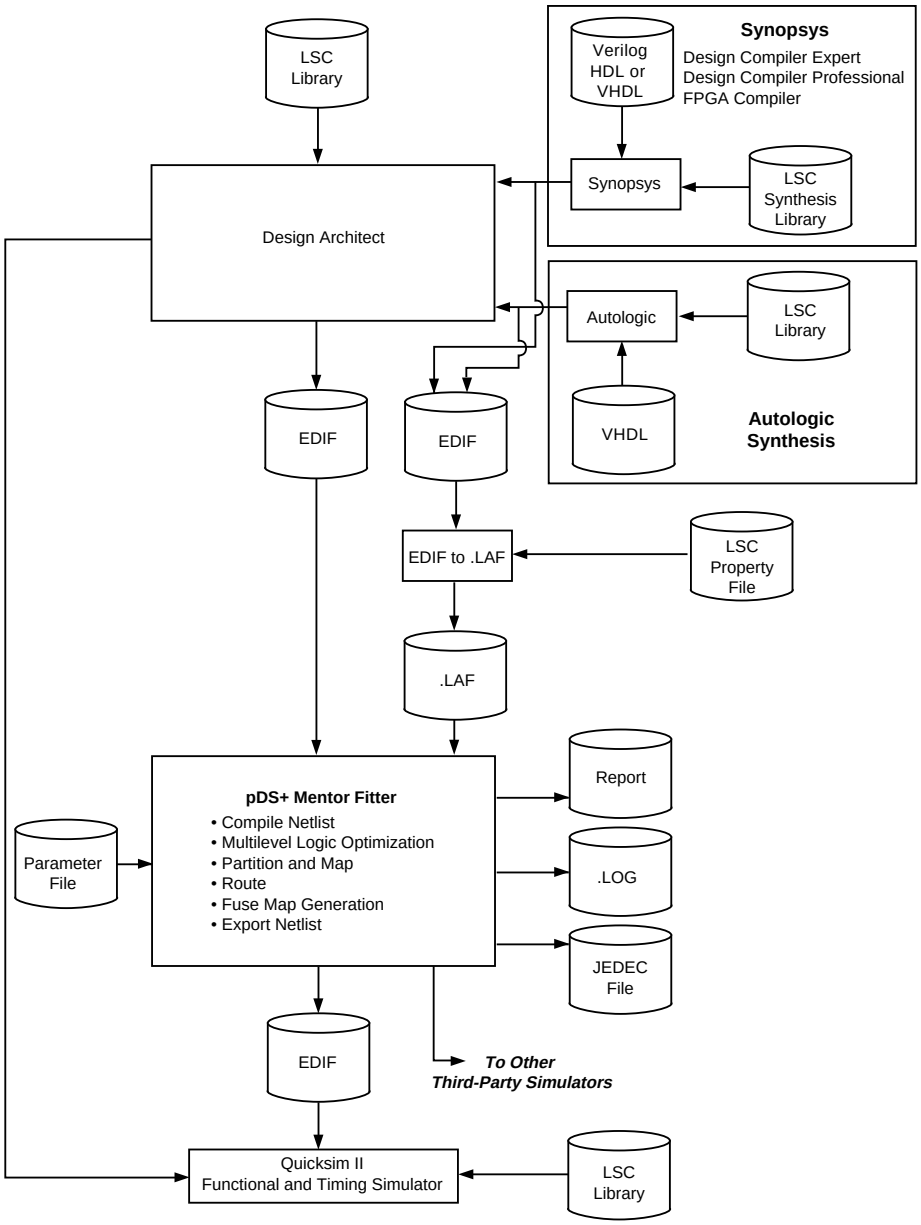
Figure 1. Lattice Semiconductor's pDS+ Mentor Design Flow



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The pDS+ Mentor Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the ispLSI family's features such as the hard XOR and product term sharing. The internal XOR can be utilized for arithmetic functions, T-type flip-flops, and on and off set optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the Fitter to efficiently use device resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

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Design Parameter Control

The pDS+ Mentor Fitter offers extensive design control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using “attributes” in the design property and parameter files. The parameter and property files contain:

- — Fitter Control Options
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+ Mentor Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization.

Feature	Description
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PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
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MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
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Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
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CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following properties specify paths in the design that have special fitting requirements:

Feature	Description
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SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ Mentor Fitter provides the ability to use a parameter file (design.par) feature which helps designers eliminiate guesswork and optimize the designs for the right devices. It allows the user to try a number of design implementation options using all of the fitter control options in a batch mode. The parameter file instructs the partitioner and the router to maximize both device utilization and performance.

Property File

The pDS+ Mentor Fitter provides the ability to use a property file (design.prp) feature which allows the designer to control the fitter using all of the design attributes available. The property file helps guide the fitter in implementing the design in the best way.

Design Verification

The pDS+ Mentor Fitter provides a post route design file for optional timing simulation. The pDS+ Mentor software offers complete post route design verification using optional timing simulators. The pDS+ Mentor Fitter generates the files required for third-party simulation with behavioral simulation models from Logic Modeling.

Fuse Map Generation

pDS+ Mentor software generates a device fuse map in standard JEDEC format. A security feature offers protection of proprietary designs from unauthorized duplication. The Fitter appends any design test vectors in JEDEC format to the device fusemap, facilitating a quick, easy functional verification of a programmed device.

System Requirements (Sun Platform)

— Sun Sparc 4 and above
— Sun OS Version 4.x
— Open Windows 3.0
— 16 MB RAM with 30 MB Hard Disk Space
— Three-Button Mouse

System Requirements (HP Platform)

— HP 700 Workstation and Above
— HP O/S UX9.x and Above
— 16 MB RAM and 30 MB Hard Disk Space
— Three-Button Mouse

Programmer Support

All devices in the Lattice Semiconductor ispLSI device family can be programmed while installed on the target circuit board. In-system programming can be performed using a DOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test. All Lattice Semiconductor ispLSI and pLSI devices can be programmed using third-party programmers. These devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2150-HP1	pDS+ Mentor Fitter and Libraries (HP)
pDS2150-SN1	pDS+ Mentor Fitter and Libraries (Sun)
pDS2150-3UP/HP1	pDS2150 3000 Family Upgrade (HP)
pDS2150-3UP/SN1	pDS2150 3000 Family Upgrade (Sun)
pDS1150-HP1	Mentor Libraries and Interface (HP)
pDS1150-SN1	Mentor Libraries and Interface (Sun)
pDS1155-HP1	Mentor Autologic Synthesis Library (HP)
pDS1155-SN1	Mentor Autologic Synthesis Library (Sun)

Annual Maintenance*

pDS2150M-HP1	Maintenance for pDS2150-HP1
pDS2150M-SN1	Maintenance for pDS2150-SN1
pDS1150M-HP1	Maintenance for pDS1150-HP1
pDS1150M-SN1	Maintenance for pDS1150-SN1
pDS1155M-HP1	Maintenance for pDS1155-HP1
pDS1155M-SN1	Maintenance for pDS1155-SN1

*One year of maintenance is provided with every product purchase.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic) 1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com

pDS+™ OrCAD Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000**
- **SUPPORTS OrCAD SDT 386+ OR CAPTURE FOR WINDOWS DEVELOPMENT ENVIRONMENT FOR DESIGN ENTRY**
  - **— Schematic Entry**
  - **— Over 300 "TTL-Like" Macros**
  - **— Graphical, Menu-Driven Interface**
  - **— Command Line Driven User Interface**
- **SUPPORTS OrCAD PLD 386+ DESIGN ENVIRONMENT FOR BOOLEAN DESIGN ENTRY**
- **LATTICE SEMICONDUCTOR pDS+ OrCAD FITTER**
  - **— Multi-Level Logic Synthesis**
  - **— Efficient Design Optimization and Minimization**
  - **— Automatic Mapping and Device Fitting**
  - **— Automatic Partitioning with High Utilization**
  - **— Predictable Performance**
- **COMPLETE DESIGN VERIFICATION**
  - **— Using OrCAD's VST 386+ Simulator or Simulate for Windows**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Device Fuse Map**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download**
  - **— ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **— PC DOS/WIndows 3.1/Windows 95/Windows NT**

Introduction

The pDS+ OrCAD Software from Lattice Semiconductor Corporation (LSC) offers a powerful solution to fit high density logic designs into Lattice Semiconductor's ispLSI and pLSI devices.

Design entry, simulation, and implementation are made simple using tools such as Capture for Windows from OrCAD (see figure 1). The OrCAD software and pDS+ Fitter support high level, device independent design entry together with efficient logic compilation, delivering the most complex designs in the shortest time possible.

OrCAD Software

OrCAD supports schematic entry using its Schematic Design Tools (SDT 386+) or Capture for Windows v6.1 software (see figure 2). The OrCAD capture tools work with Lattice Semiconductor's library of over 300 TTL-like macros to let you create designs without regard to any specific device dependencies. They offer advanced features such as cut and paste, unlimited zoom and pan functions, automatic symbol generation as well as many other features to streamline and speed-up the design and verification process. OrCAD also supports schematic/Boolean Equation entry using the PLD 386+ tool. Schematics, using an OrCAD primitive library, can be incorporated and processed by the PLD 386+ tool. A PLD 386+ file for Boolean Equation entry (using OrCAD HDL) can be generated and processed. The ESP environment also supports optional timing simulation, using the OrCAD Verification and Simulation software, so designs can be fully simulated before device programming. The menu-driven environment makes design implementation as easy as a single click of the mouse button. Results can also be dynamically back annotated to the schematic for design verification.

pDS+ OrCAD Fitter

The pDS+ OrCAD Fitter for ispLSI and pLSI devices is executed as a standalone program, using the OrCAD EDIF output from capture tools or the PLA output from PLD 386+ as an input. Figure 3 shows the design flow for pDS+ OrCAD. The design flow is as follows:

— Create a design using either Capture or PLD 386+.

— Perform a pre-route simulation utilizing the OrCad simulator.

— Create either an EDIF file or a PLA file.

— Compile either your EDIF or PLA file with the pDS+ OrCAD fitter to generate a .ifo and .dba file for simulation and JEDEC, LOG and report files for programming and device debug.

— Perform a post-route simulation in OrCAD using the Lattice Semiconductor timing simulation library and OrCAD's simulator.

— Program the selected device.

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Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Figure 1. OrCAD Capture for Windows

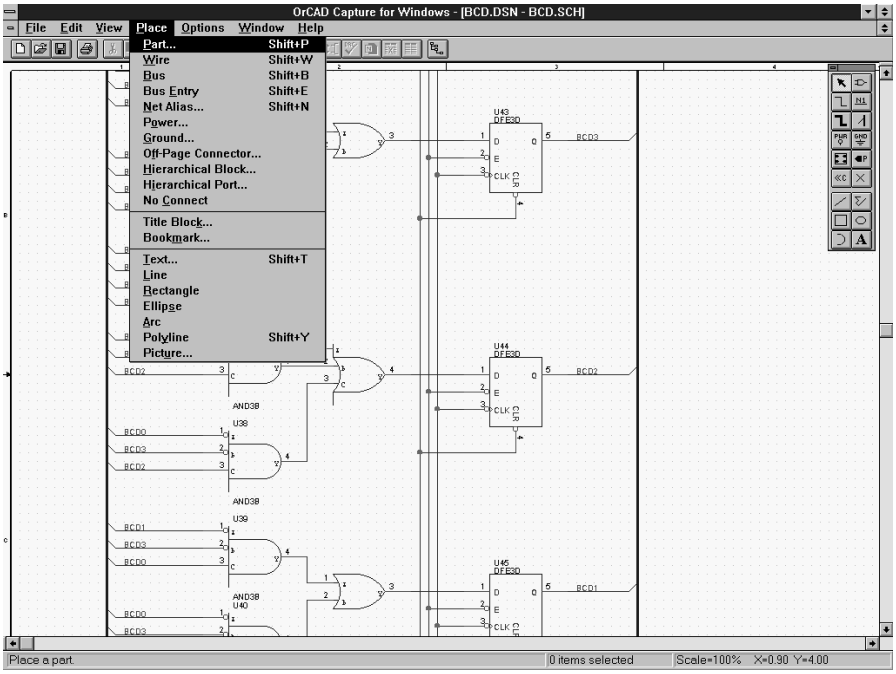


Figure 2. OrCAD SDT 386+ Environment

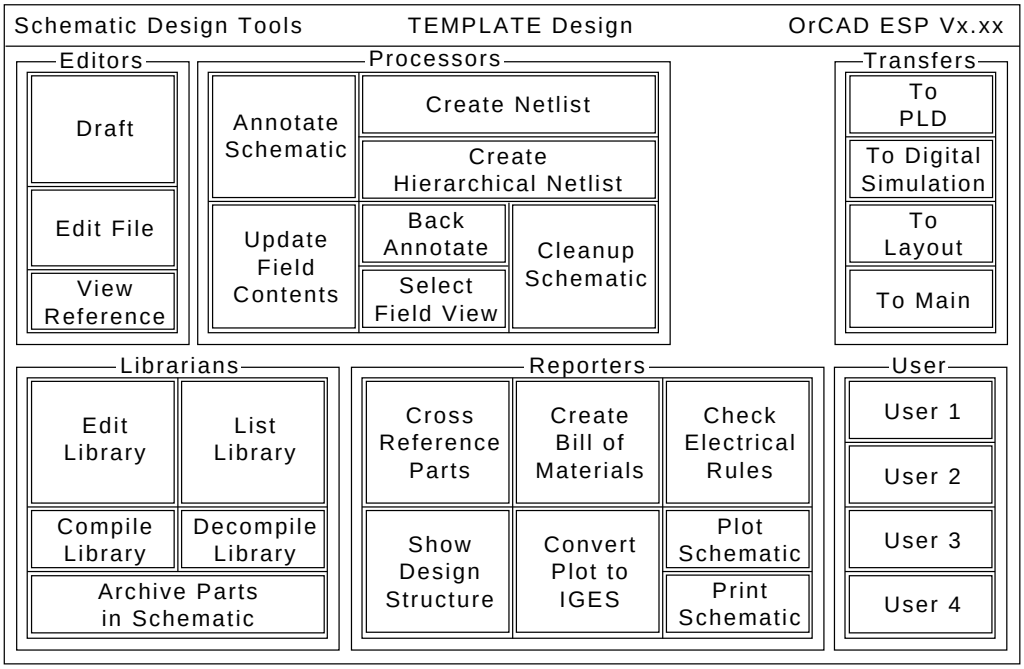
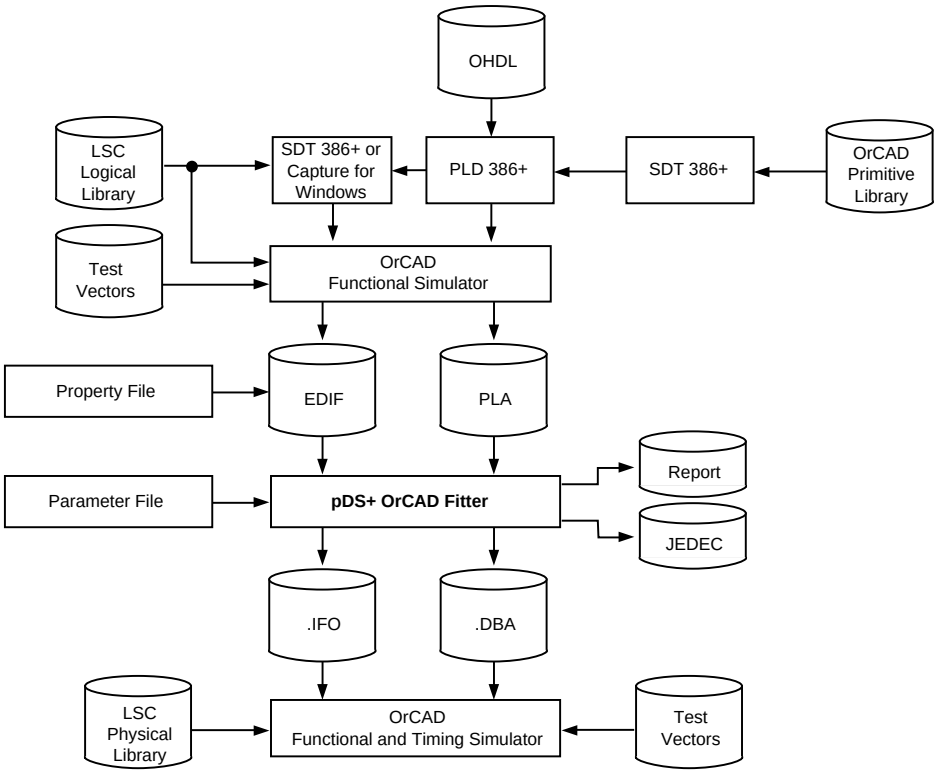


Figure 3. pDS+ OrCAD Design Flow



The pDS+ OrCAD Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place and route and fusemap generation for programming.

pDS+ OrCAD Macro Library

The pDS+ OrCAD software offers an extensive selection of over 300 TTL-like macros. These macros enable the design engineer to use familiar predefined functions to build a design. Table 1 shows a summary of the available macros in the pDS+ software.

Table 1. Macro Summary

Macro Type	Quantity
AND/NAND	29
OR/NOR	24
XOR/XNOR	12
I/Os	89
Flip-Flops	39
Latches	30
Arithmetic	33
Counters	65
Shift Registers	15
Miscellaneous	45

Design Optimization and Logic Minimization

The pDS+ OrCAD Fitter uses proprietary logic synthesis algorithms targeted for device-specific features. The fitter performs a thorough design optimization, utilizing logic minimization, product term sharing and XOR functions wherever necessary. In addition, the pDS+ OrCAD Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Automatic Partitioning

The pDS+ OrCAD Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features such as the hard XOR and product term sharing. The internal XOR can be utilized for arithmetic functions, T-Type flip-flops, and on and offset optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the Fitter to efficiently use device resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation.

Design Parameter Control

The pDS+ OrCAD Fitter offers extensive design parameter control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using “Attributes” in the ESP or Capture for Windows design environment or in property and parameter files. These controls fall into two categories:

- — Fitter Controls
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+ OrCAD Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization. Here are a few of the powerful features:

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.

Feature	Description
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following properties specify paths in the design that have special fitting requirements:

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ OrCAD Fitter provides the ability to use a parameter file (design.par) feature which helps designers eliminate guesswork and optimize the designs for the right devices. It allows the user to try a number of design implementation options using all of the fitter control options in a batch mode. The parameter file instructs the partitioner and the router to maximize both device utilization and performance and helps speed the design process.

Property File

The pDS+ OrCAD Fitter also accepts a property file (design.prp) which allows the designer to assign specific features to signal and nets using all of the design attributes available. The property file helps guide the fitter in implementing the design in the most efficient way.

Design Verification

The pDS+ OrCAD Fitter also provides a post route design file for optional timing simulation. The pDS+ OrCAD software offers complete post route design verification using the optional OrCAD timing simulator. The pDS+ OrCAD Fitter generates the files required for simulation, and generates a "sim" file which can be used with behavioral simulation models from Synopsys Logic Modeling Division.

Fuse Map Generation

The pDS+ OrCAD software generates a device fuse map in standard JEDEC format. A security feature offers protection of proprietary designs from unauthorized duplication. The Fitter also appends any design test vectors in JEDEC format to the device fusemap thus facilitating a quick, easy functional verification of a programmed device.

System Requirements (PC Platform)

- 486/Pentium™ IBM Compatible PC
- Operating System
  - MSDOS Version 4.x or Later
  - Windows 3.1
  - Windows NT
  - Windows 95
- 16 MB RAM with 30MB Hard Disk Space
- Parallel Printer Port for Software Key

Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2170-PC1	pDS+ OrCAD Fitter & Libraries (PC)
pDS1170-PC1	OrCAD Library & Interface (PC)
pDS2170-3UP/PC1	3000 Family Support for pDS+ OrCAD Fitter

Annual Maintenance*

pDS2170M-PC1	Maintenance for pDS2170-PC1
pDS1170M-PC1	Maintenance for pDS1170-PC1

*One year of maintenance is provided with every product purchase.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic) 1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com

pDS+™ Synario Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT TOOLS**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000**
  - **— Supports Lattice Semiconductor ispGAL® and GAL® Design-In**
- **DESIGN ENTRY USING DATA I/O'S SYNARIO**
  - **— ABEL-HDL Entry**
  - **— Schematic Capture**
  - **— Tightly Integrated User Interface**
- **LATTICE SEMICONDUCTOR pDS+™ SYNARIO FITTER**
  - **— Multi-Level Logic Synthesis**
  - **— Efficient Design Optimization and Minimization**
  - **— Automatic Mapping and Device Fitting**
  - **— Automatic Partitioning with High Utilization**
  - **— Predictable Performance**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Device Fuse Map**
- **IN-SYSTEM PROGRAMMING**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download**
  - **— ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **— PC Windows 3.1 and Above**

Introduction

pDS+ Synario software from Lattice Semiconductor offers a powerful logic design solution for Lattice Semiconductor's ispLSI and pLSI families of high density PLDs. The ISP Synario System, Syn-Entry ISP and Syn-Sim ISP software products support Lattice Semiconductor's ispLSI and pLSI 1000, 2000 and 3000 high density families, as well as its ispGAL and GAL devices. Coupling these powerful tools with Lattice Semiconductor's pDS+ Synario Fitter provides tightly integrated front-to-back design capability.

The complete ISP Synario System supports smaller ispLSI and pLSI high density devices (up to and including the ispLSI and pLSI 2096), ispGAL and GAL devices with complete schematic or language design entry, fitting and functional simulation. Lattice Semiconductor's pDS+ Synario software offers multi-level design synthesis, automatic place and route and efficient device utilization, delivering high performance, even for more complex designs.

ISP Synario System

The Lattice Semiconductor ISP Synario System contains everything needed to design and program with Lattice Semiconductor ispLSI devices. The full version of Data I/O's Synario-Entry tools for schematic capture and ABEL-HDL language logic design, a functional simulator and Data I/O's Project Navigator for easy design and logic debugging are included. The ISP Synario System supports high density design for Lattice Semiconductor's ispLSI and pLSI 1016, 1024, 2032, 2064 and 2096 devices. The tools included also support the full range of Lattice Semiconductor's industry standard ispGAL and GAL devices, including the ispGAL22V10, GAL16V8, GAL20V8 and GAL6001 devices, and others. In addition, the ISP Synario System includes device samples of the ispLSI 2032, isp GAL22V10 and ispGDS™, as well as an ispDOWNLOAD™ Cable to download designs to the PC board.

Project Navigator

Data I/O's Synario Project Navigator contains detailed, built-in knowledge of the Lattice Semiconductor design flow. The Project Navigator knows the processing status of all portions of the design. If the design is changed and the netlist regenerated, Project Navigator changes only the necessary items, since it knows that other parts of the design are current. Processing options are intelligently defaulted and detailed device-specific help is available for each step.

Synario-Entry

All of Data I/O's Synario products are Windows-based and easy to use. For example, highlight a net and the net is highlighted throughout the design hierarchy. Run a rules check and errors appear in a box. Click on an error and the system jumps to the schematic or text containing the error. The Synario-Entry tool is designed to allow you to describe even the most complex designs using familiar language constructs or by capturing the logic schematic using a library of Data I/O logic primitives. Synario Behavioral Entry with hierarchical support also allows

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Figure 1. Synario Design Interface

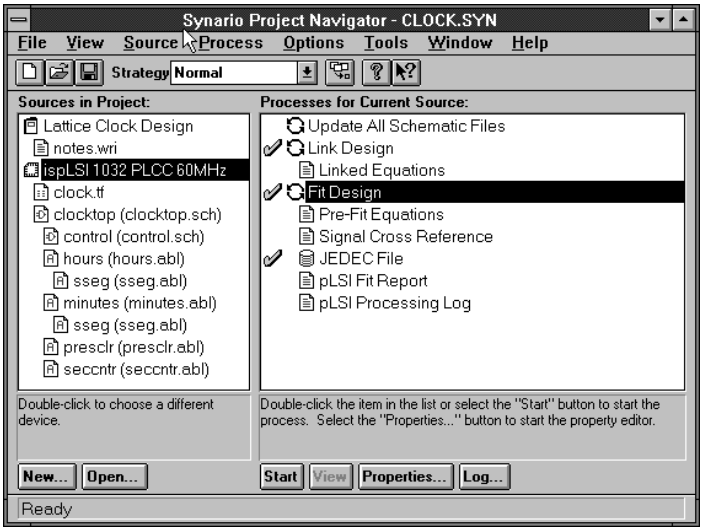
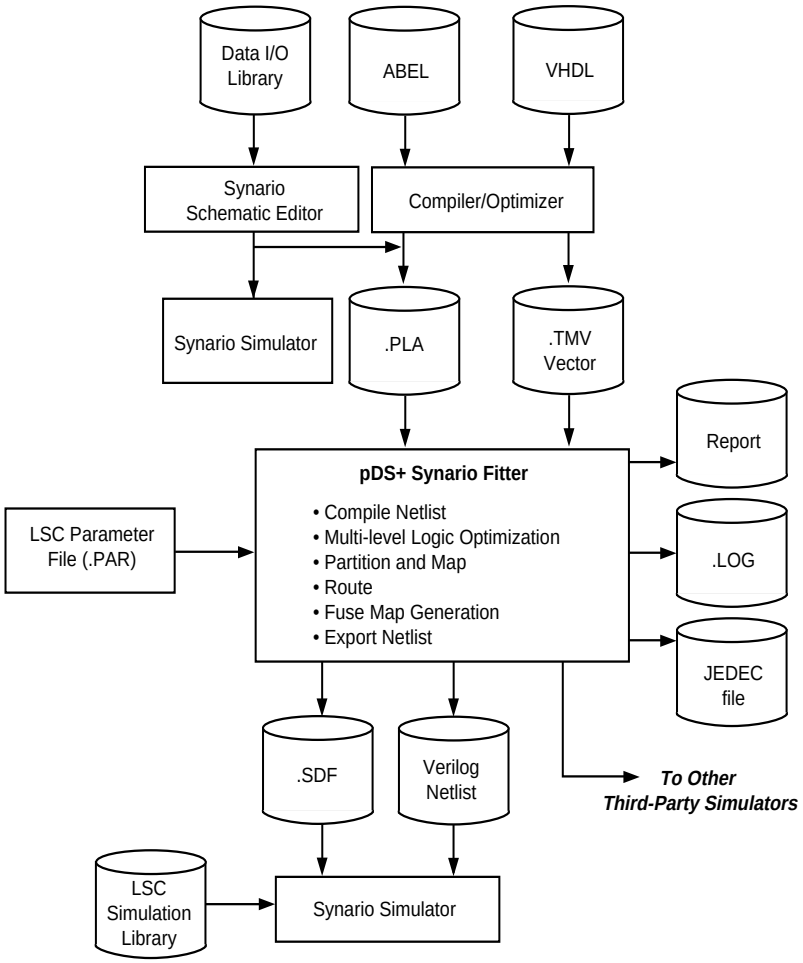


Figure 2. Lattice Semiconductor pDS+ Synario Design Flow



device-specific logic synthesis compatible with ABEL-HDL for easy retargeting of existing low density designs to high density Lattice Semiconductor ispLSI and pLSI architectures. Commonly referred to as Syn-Entry, a Lattice Semiconductor-only version of this tool — Syn-Entry ISP — is available directly from Lattice Semiconductor.

Synario Simulator

Data I/O's Synario-Simulator uses Synario source files to complete functional simulations quickly. After pDS+ Synario completes the fitting task, a compatible netlist and standard delay format (SDF) file are created for full delay-annotated timing simulations. The waveform viewer allows the user to display waveforms in a logic analyzer-like format. The Simulator's waveform viewer and the schematic communicate with one another. Once a simulation has run, the values beneath the cursor are displayed on the associated schematic nets. Simulation results are tied back to the source file when possible to save interpretation time and speed the debug process. Just like Syn-Entry, a Lattice Semiconductor-only version, Syn-Sim ISP, is also available.

pDS+ Synario Fitter

Lattice Semiconductor's pDS+ Synario Fitter for ispLSI and pLSI devices is tightly integrated within the Synario environment and the Project Navigator, using the PLA output from Synario as input. The Lattice Semiconductor Fitter provides hands-off design implementation through an intelligent multi-level synthesis algorithm, logic partitioning, automatic place and route and standard JEDEC fuse map generation for device programming. Timing simulation input files for the Synario simulator are generated by the Fitter and can be coupled with Lattice Semiconductor's Synario Simulation Library by the user as needed.

Design Optimization & Logic Minimization

The pDS+ Synario Fitter uses proprietary algorithms targeted for Lattice Semiconductor's powerful device-specific architectural features. The Fitter optimizes the design thoroughly, using logic minimization, product term sharing and XOR functions wherever possible. In addition, the pDS+ Synario Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Design Parameter Control

The pDS+ Synario Fitter offers extensive design control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using "attributes" in the design property and parameter files. These controls fall into two categories:

- — Fitter Controls
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+Synario Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization.

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
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FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following properties specify paths in the design that have special fitting requirements:

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
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Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ Synario Fitter provides the ability to use a parameter file (design.par) feature which helps designers eliminiate guesswork and optimize the designs for the right devices. It allows the user to try a number of design implementation options using all of the fitter control options in a batch mode. The parameter file instructs the partitioner and the router to maximize both device utilization and performance.

Property File

The pDS+ Synario Fitter provides the ability to use a property file (design.prp) feature which allows the designer to control the fitter using all of the design attributes available. The property file helps guide the fitter in implementing the design in the best way.

Design Verification

The pDS+ Synario Fitter provides a post route design file for optional timing simulation. The pDS+ Synario software offers complete post route design verification using optional timing simulators. The pDS+ Synario Fitter generates the files required for third-party simulation, and generates a "sim" file which can be used for simulation with behavioral simulation models from Synopsys' Logic Modeling Division.

Fuse Map Generation

pDS+ Synario software generates a device fuse map in standard JEDEC format. A security feature offers protection of proprietary designs from unauthorized duplication. The Fitter appends any design test vectors in JEDEC format to the device fusemap, facilitating a quick, easy functional verification of a programmed device.

System Requirements (PC Platform)

- 486/Pentium™ IBM Compatible PC
- Operating System
  - MSDOS Version 4.x or Later
  - Windows 3.1
  - Windows NT
  - Windows 95
- 16 MB RAM with 30MB Hard Disk Space
- ABEL 4.1 or Later
- Parallel Printer Port for Software Key

Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2120-PC1	pDS+ Synario Fitter and Libraries
pDS2120-3UP/PC1	pDS2120 3000 Family Upgrade
pDS1120-PC1	Synario Library and Interface
pDS1401-PC1	Syn-Entry ISP
pDS3402-PC1	Syn-Sim ISP
ISP-SYN	ISP Synario System
Annual Maintenance*	
pDS2120M-PC1	Maintenance for pDS2120-PC1
pDS1120M-PC1	Maintenance for pDS1120-PC1
pDS1401M-PC1	Maintenance for pDS1401-PC1
pDS3402M-PC1	Maintenance for pDS3402-PC1

*One year of maintenance is provided with every product purchase, except ISP-SYN.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic) 1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com

pDS+™ Synopsys Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000**
- **SUPPORTS SYNOPSYS DESIGN COMPILER AND FPGA COMPILER TOOLS**
  - **— Lattice Semiconductor Corporation (LSC) Synopsys Technology Library for Synthesis**
- **DESIGN ENTRY USING VHDL OR VERILOG-HDL**
  - **— High-Level Language Entry**
  - **— Optimized Functions for Direct Instantiation**
  - **— Direct Path to pDS+ Synopsys Fitter**
- **LATTICE SEMICONDUCTOR pDS+™ SYNOPSYS FITTER**
  - **— Automated Device Fitter Ensures High Utilization and Performance**
  - **— Efficient Design Optimization and Minimization**
  - **— Automatic Partitioning with High Utilization**
  - **— Export Verilog and SDF for Verilog Simulation**
  - **— Export Wire File for Viewsim Simulation**
- **SUPPORTS CADENCE CONCEPT, VIEWLOGIC VIEWDRAW, AND MENTOR GRAPHICS DESIGN ARCHITECT SCHEMATIC CAPTURE TOOLS**
  - **— Design Import via Synopsys-Generated EDIF Design Netlist**
  - **— Design Property Entry Using Viewlogic, Cadence Concept or Mentor Graphics Tools**
- **DESIGN VERIFICATION WITH POPULAR THIRD PARTY SIMULATORS**
  - **— Verilog-XL™ Simulation from Cadence**
  - **— Viewsim Simulation from Viewlogic**
  - **— Quicksim II From Mentor Graphics**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Fuse Map**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download (PC)**
  - **— ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **— Sun O/S 4.x**
  - **— HP O/S UX 9.x and Above**

Introduction

The pDS+ Synopsys Fitter and Libraries from Lattice Semiconductor offer a powerful solution to fit high density logic designs into Lattice's ispLSI and pLSI devices.

Synopsys offers synthesis tools, called Design Compiler and FPGA Compiler, which use Verilog HDL or VHDL input formats for design entry. The Synopsys Synthesis Libraries support both Design Compiler and FPGA Compiler design environments.

Design entry is made simple by using device independent Verilog HDL or VHDL design languages. These designs are then synthesized by the Design Compiler or the FPGA Compiler, using Synopsys synthesis libraries, into an EDIF netlist.

A direct path from Synopsys into the pDS+ Synopsys fitter, using an EDIF netlist with an attribute file for fitter and design controls can also be used or the EDIF netlist/ schematic can be imported into Cadence Concept, Viewlogic, or Mentor Graphics schematic environments. For more details, refer to the Design Flows section of this datasheet.

pDS+ Synopsys Fitter

The pDS+ Synopsys Fitter for ispLSI and pLSI devices is executed as a standalone program, using the EDIF output from Synopsys, Cadence Concept, Mentor Graphics Design Architect or wire files from Viewlogic as input. The pDS+ Synopsys Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place & route and fusemap generation in standard JEDEC format. Timing simulation input files for Verilog XL, Quicksim II or Viewsim are generated by the Fitter when requested by the user.

Design Optimization and Logic Minimization

The pDS+ Synopsys Fitter uses proprietary logic synthesis algorithms targeted for device-specific features. The fitter performs a thorough design optimization, utilizing logic minimization, product term sharing and XOR functions wherever necessary. In addition, the pDS+ Synopsys Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

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Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

pDS+ Synopsys Macro Library

The Synopsys Synthesis Libraries come complete with a library of over 300 high level functions to simplify design entry. These macros enable the design engineer to use familiar predefined functions to build a design. Direct instantiation of these functions is provided to enhance device performance and utilization.

Figure 3. Macro Summary

Macro Type	Quantity
AND/NAND	29
OR/NOR	24
XOR/XNOR	12
I/Os	89
Flip-Flops	39
Latches	30
Arithmetic	33
Counters	65
Shift Registers	15
Miscellaneous	45

Automatic Partitioning

The pDS+ Synopsys Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features such as the hard XOR and product term sharing. The internal XOR can be utilized for Arithmetic functions, T-Type flip-flops, and on & off set optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the Fitter to efficiently use device resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation. The result is that small design changes won't cause expensive PC board rework.

Design Parameter Control

The pDS+ Synopsys Fitter offers extensive design control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using "Attributes" in the design property and parameter files. These controls fall into two categories:

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  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+ Synopsys Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization.

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Design implementation controls are used for changing such design parameters as security and pull-ups. Some of the implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following properties specify paths in the design that have special fitting requirements:

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ Synopsys Fitter provides the ability to use a parameter file (design.par) feature which helps designers eliminate guesswork and optimize the designs for the right devices. It allows the user to try a number of design implementation options using all of the fitter control options in a batch mode. The parameter file instructs the partitioner and the router to maximize both device utilization and performance.

Figure 1. pDS+ Synopsys Design Flow

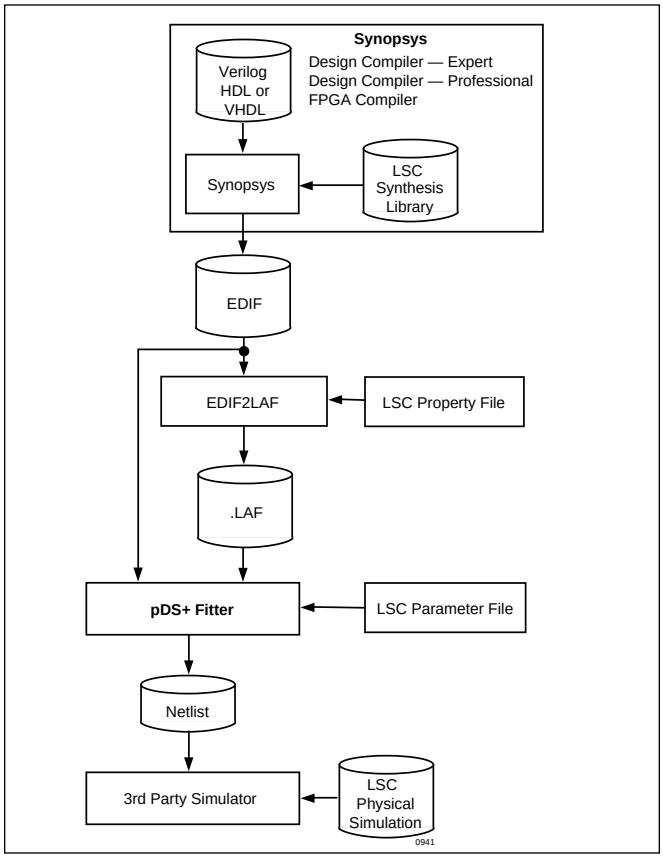
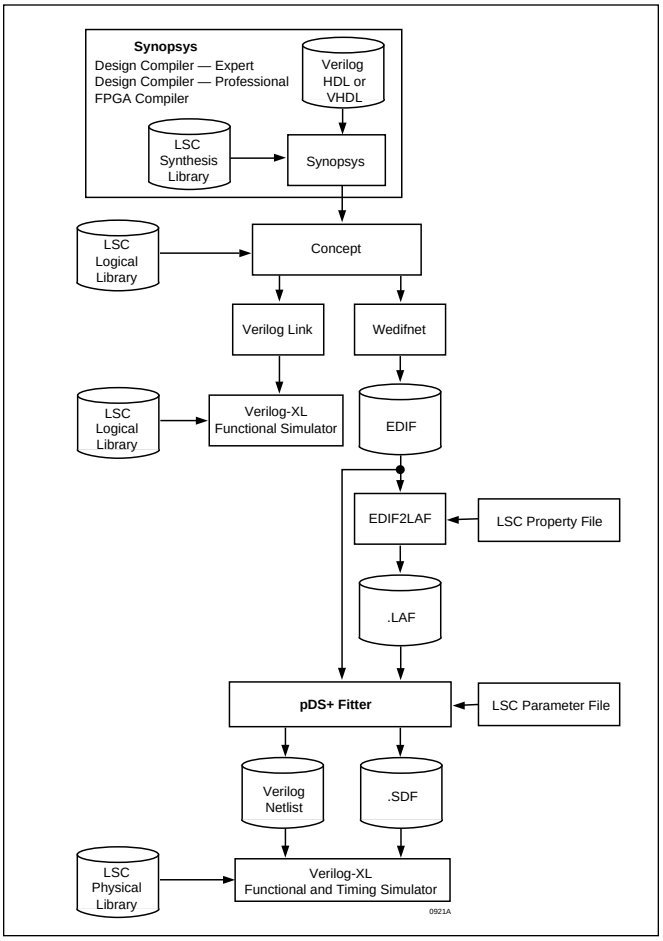


Figure 2. pDS+ Cadence Flow with Synopsys Option



Property File

The pDS+ Synopsys Fitter also accepts a property file (design.prp) which allows the designer to assign specific features to signals and nets using all of the design attributes available. The property file helps guide the fitter in implementing the design in the best way.

Design Verification

The pDS+ Synopsys Fitter provides a post route design file for optional timing simulation. The pDS+ Synopsys software offers complete post route design verification using optional timing simulators. The pDS+ Synopsys Fitter generates the files required for third-party simulation, and generates a “sim” file which can be used for simulaton with behavioral simulation models from Synopsys Logic Modeling Division.

Fusemap Generation

The pDS+ Synopsys software generates a device fuse map in standard JEDEC format. A security feature offers protection of proprietary designs from unauthorized duplication. The Fitter also appends any design test vectors in JEDEC format to the device fusemap thus facilitating a quick, easy functional verification of a programmed device.

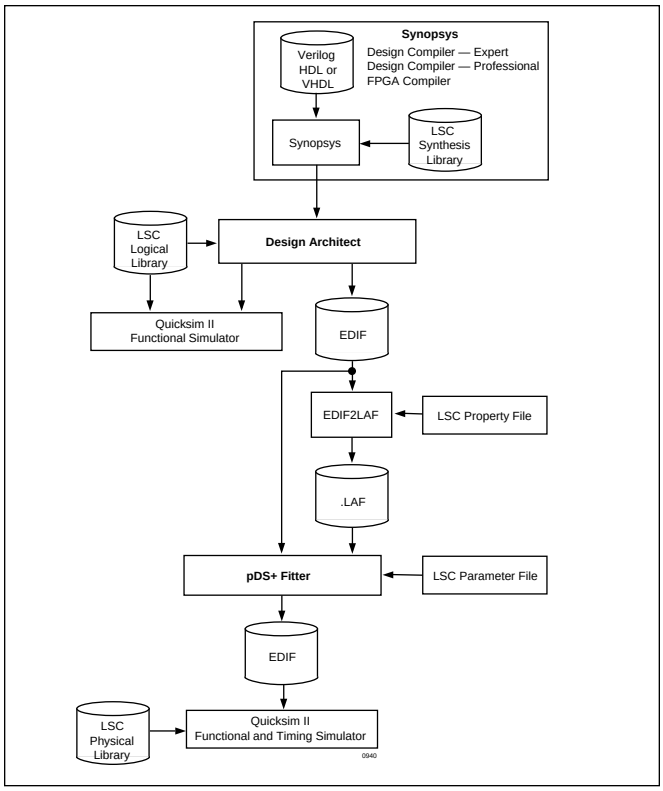
Design Flows

pDS+ Synopsys Design Flow

Designers can compile designs described in VHDL or Verilog HDL using Synopsys Design Compiler or FPGA Compiler and the Lattice Synopsys Synthesis Libraries. The EDIF netlist file from Synopsys can be read directly by the pDS+ Synopsys Fitter. If a property file (design.prp) exists, the EDIF2LAF translator must be run before the fitter is executed.

Design attributes and fitter control options can also be added to the design.par file.

Figure 3. pDS+ Mentor Graphics Design Flow with Synopsys Option



The EDIF output can then be read by the pDS+ Synopsys Fitter where the design is automatically partitioned, routed and a JEDEC file for device programming is generated (see figure 1).

pDS+ Cadence Design Flow with Synopsys Option

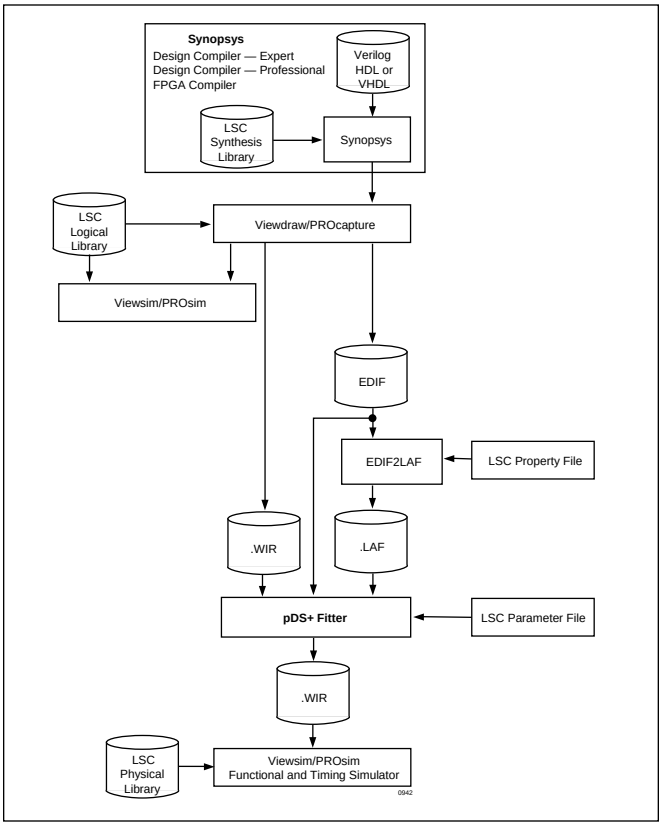
Designers can compile designs described in VHDL or Verilog HDL using Synopsys Design Compiler or FPGA Compiler and the LSC Synopsys Synthesis Libraries. The EDIF netlist file or schematic file from Synopsys can be read into Concept, the Cadence schematic capture tool. Design attributes and fitter control options can be added in the schematic. The EDIF output from Concept can then be read by the pDS+ Cadence Fitter where the design is automatically partitioned, routed and a JEDEC file for device programming is generated.

Verilog-XL simulation library can be used to do both pre and post route simulation (see figure 2).

pDS+ Mentor Graphics Design Flow with Synopsys Option

Designers can compile designs described in VHDL or Verilog HDL using Synopsys Design Compiler or FPGA Compiler and the LSC Synopsys Synthesis Libraries. Designs described in VHDL can also be compiled with the LSC Autologic Synthesis library.

Figure 4. pDS+ Viewlogic Design Flow with Synopsys Option



The Mentor Graphics Design Architect (DA) can read the design database from the Synopsys synthesis tools.

The EDIF output from DA can then be read by the pDS+ Mentor Fitter where the design is automatically partitioned, routed and a JEDEC file for device programming is generated.

Quicksim II simulation libraries can be used to do both pre and post route simulations (see figure 3).

pDS+ Viewlogic Design Flow with Synopsys Option

Designers can compile designs described in VHDL or Verilog HDL with Synopsys and the LSC Synopsys Synthesis Libraries. The EDIF netlist file or schematic file from Synopsys can be read into Viewdraw, the Viewlogic schematic capture tool. Design attributes and fitter control options can be added in the schematic. The .WIR file from Viewdraw can then be read by the pDS+ Viewlogic

Fitter where the design is automatically partitioned, routed and a JEDEC file for device programming is generated.

Pre and post route simulations can be performed using Viewsim (see figure 4).

System Requirements (Sun Platform)

— Sun Sparc 4 and above
— Sun OS Version 4.x
— Open Windows 3.0
— 16 MB RAM with 30 MB Hard Disk Space
— Three-Button Mouse

System Requirements (HP Platform)

— HP 700 Workstation and Above
— HP O/S UX9.X and Above
— 16 MB RAM and 30 MB Hard Disk Space
— Three-Button Mouse

Programmer Support

All devices in the Lattice Semiconductor ispLSI device family can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE equipment during final board test. All LSC ispLSI and pLSI devices can be programmed using third-party programmers. These devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS1102-SN1	Viewlogic Viewsim and Viewdraw Libraries and Interface Files
pDS1140-HP1	Lattice Semiconductor Synopsys Synthesis Libraries (HP)
pDS1140-SN1	Lattice Synopsys Synthesis Libraries
pDS1150-HP	Mentor Interface Kit (HP)
pDS1150-SN1	Mentor Interface Kit (Sun)
pDS1160-SN1	Cadence Libraries and Interface
pDS2101-SN1	pDS+ Viewlogic Fitter
pDS2101-3UP/SN1	3000 Family Upgrade for pDS+ Viewlogic Fitter
pDS2140-HP1	pDS+ Synopsys Fitter (HP)
pDS2140-3UP/HP1	3000 Family Upgrade for pDS+ Synopsys Fitter (HP)
pDS2140-SN1	pDS+ Synopsys Fitter and Libraries
pDS2140-3UP/SN1	3000 Family Upgrade for pDS+ Synopsys Fitter
pDS2150-HP1	pDS+ Mentor Fitter and Libraries (HP)
pDS2150-SN1	pDS+ Mentor Fitter and Libraries
pDS2150-3UP/HP1	3000 Family Upgrade for pDS+ Mentor Fitter
pDS2150-3UP/SN1	3000 Family Upgrade for pDS+ Mentor Fitter
pDS2160-SN1	pDS+ Cadence Fitter and Libraries
pDS2160-3UP/SN1	3000 Family Upgrade for pDS+ Cadence Fitter

Annual Maintenance**

pDS1102M-SN1	Maintenance for pDS1102-SN1
pDS1140M-HP1	Maintenance for pDS1140-HP1
pDS1140M-SN1	Maintenance for pDS1140-SN1
pDS1150M-HP1	Maintenance for pDS1150-HP1
pDS1150M-SN1	Maintenance for pDS1150-SN1
pDS1160M-SN1	Maintenance for pDS1160-SN1
pDS2101M-SN1	Maintenance for pDS2101-SN1
pDS2140M-HP1	Maintenance for pDS2140-HP1
pDS2140M-SN1	Maintenance for pDS2140-SN1
pDS2150M-HP1	Maintenance for pDS2150-HP1
pDS2150M-SN1	Maintenance for pDS2150-SN1
pDS2160M-SN1	Maintenance for pDS2160-SN1

**One year of maintenance is provided with every product purchase.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic) 1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com

pDS+™ Viewlogic Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000**
- **INTEGRATED PRO SERIES™, WORKVIEW PLUS™ AND POWERVIEW™ DEVELOPMENT ENVIRONMENT FOR DESIGN ENTRY**
  - **— Schematic Entry**
  - **— Synthesis VHDL Language Entry**
  - **— Over 300 "TTL-Like" Macros**
  - **— Graphical, Menu-Driven User Interface**
  - **— Command Line-Driven User Interface**
- **LATTICE SEMICONDUCTOR pDS+ VIEWLOGIC FITTER**
  - **— Multi-Level Logic Synthesis**
  - **— Efficient Design Optimization and Minimization**
  - **— Automatic Mapping and Device Fitting**
  - **— Automatic Partitioning with High Utilization**
  - **— Predictable Performance**
- **COMPLETE DESIGN VERIFICATION**
  - **— Using Viewsim™/PROsim™ Timing SImulator**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Device Fuse Map**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download (PC Versions)**
  - **— ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **— PC Windows 3.1/Windows 95/Windows NT**
  - **— Sun O/S 4.x**
  - **— Sun Solaris 2 O/S 2.3 and Above**

Introduction

The pDS+ Viewlogic Software from Lattice Semiconductor Corporation (LSC) offers a powerful solution to fit high density logic designs into Lattice Semiconductor Corporation's (LSC) ispLSI and pLSI devices.

Design entry and implementation is made simple using the software environments from Viewlogic Corporation. The pDS+ Viewlogic software supports high level, device independent design entry together with efficient logic compilation, delivering the most complex designs in the shortest time possible.

Viewlogic Software

Viewlogic supports schematic entry using Workview Plus or Powerview (Viewdraw) or PRO Series PROcapture software. Viewdraw/PROcapture works with a library of over 300 TTL-like macros to let you create designs without regard to any specific device dependencies. Viewdraw/PROcapture offer advanced features such as cut and paste, unlimited zoom and pan functions, automatic symbol generation as well as many other features to streamline and speed-up the design and verification process. Optional Viewsynthesis/PROsynthesis software supports VHDL language entry as well. The integrated design environment supports optional timing simulators, Viewsim/PROsim, so designs can be fully simulated before device programming. The Menu-driven environment makes design implementations as easy as a single click of the mouse button. The pDS+ Viewlogic design environment also offers the user multi-window operation, allowing schematic, simulator and waveform (Viewwave/PROwave) windows to be opened concurrently. Results can also be dynamically back annotated to the schematic for design verification.

The Viewwave/PROwave software are graphical editors for creating simulation input stimulus as well as analyzing waveforms. This graphical editor/analyzer also increases designer productivity through its speed and ease-of-use. Workview Office™ software support is scheduled. Contact Lattice Semiconductor for availability.

pDS+ Viewlogic Fitter

The pDS+ Viewlogic Fitter for ispLSI and pLSI devices is completely integrated within the Viewlogic environment. The pDS+ Viewlogic Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place and route and fusemap generation. Extensive top level design control is provided for design implementation optimized for speed and/or high device resource utilization.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

pDS+ Viewlogic Macro Library

The pDS+ Viewlogic software offers an extensive selection (over 300) of TTL-like macros. These macros enable the design engineer to use familiar predefined functions to build a design. Table 1 shows a summary of the available macros in the pDS+ software.

Table 1. Macro Summary

Macro Type	Quantity
AND/NAND	29
OR/NOR	24
XOR/XNOR	12
I/Os	89
Flip-Flops	39
Latches	30
Arithmetic	33
Counters	65
Shift Registers	15
Miscellaneous	45

Design Optimization and Logic Minimization

The pDS+ Viewlogic Fitter uses proprietary logic synthesis algorithms targeted for device-specific features. The fitter performs a thorough design optimization, utilizing logic minimization, product term sharing and XOR functions wherever necessary. In addition, the pDS+ Viewlogic Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Automatic Partitioning

The pDS+ Viewlogic Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features such as the hard XOR and product term sharing. The internal XOR can be utilized for Arithmetic functions, T-Type flip-flops, and on & off set optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the Fitter to efficiently use device

Figure 1. pDS+ Viewlogic PC Design Interface

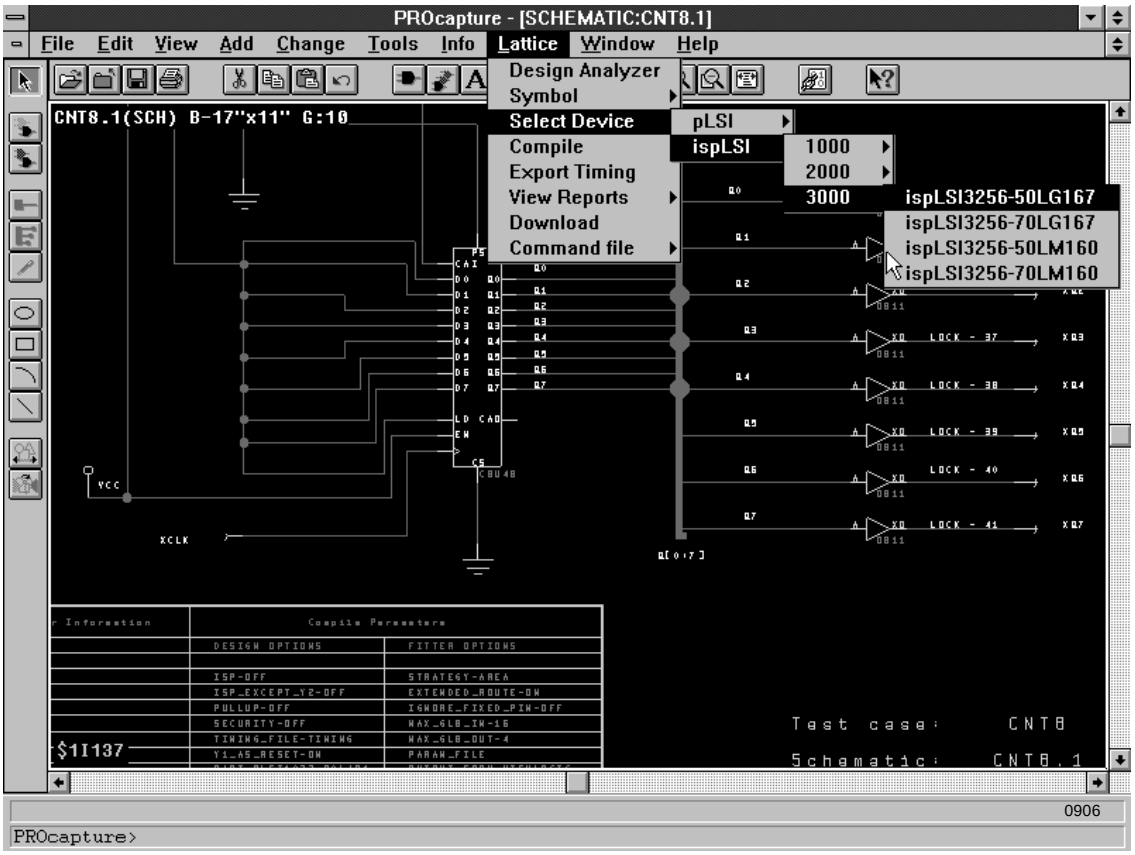


Figure 2. pDS+ Viewlogic Integrated Design Environment

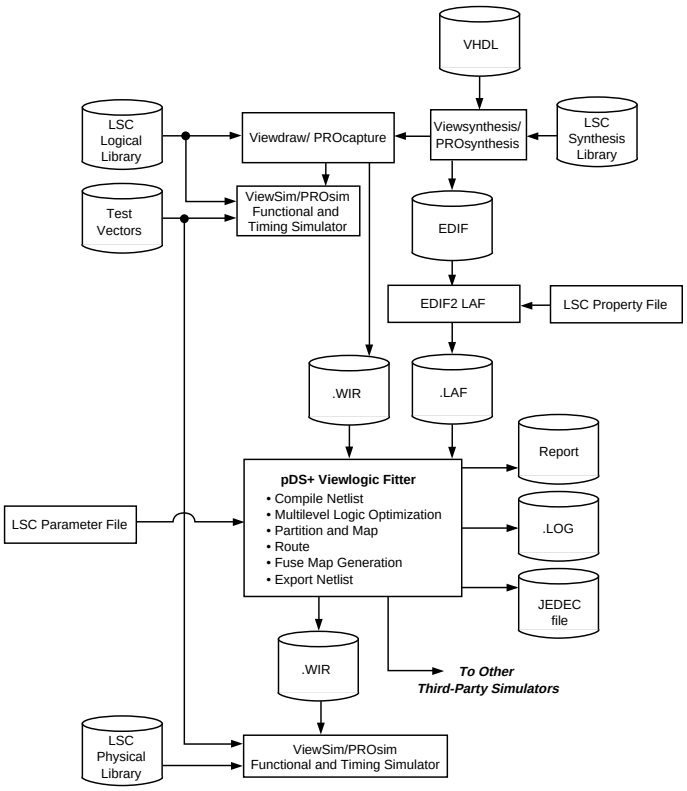
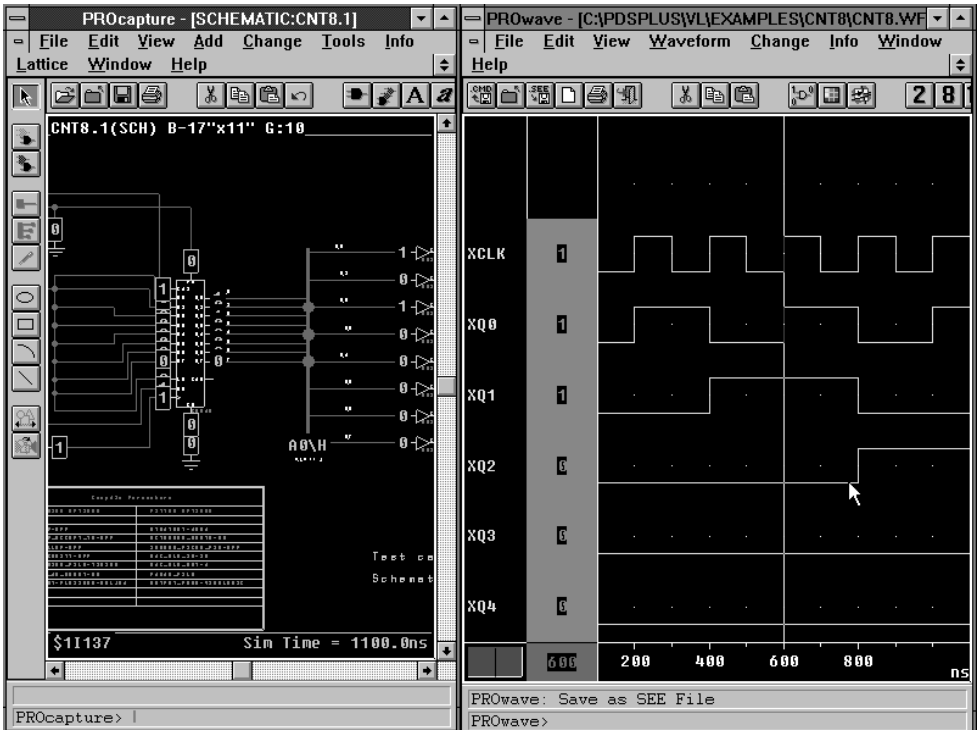


Figure 3. Viewlogic Multi-Window Design Environment



resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation. The result is that small design changes won't cause expensive PC board re-work.

Design Parameter Control

The pDS+ Viewlogic Fitter offers extensive design parameter control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using "Attributes" in the Viewdraw/PROcapture design file. These controls fall into two categories:

- — Fitter Controls
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+ Viewlogic Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization. Here are a few of the powerful features:

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following properties specify paths in the design that have special fitting requirements:

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ Viewlogic Fitter provides a parameter file feature which helps designers eliminate the guesswork and optimizes the design for the right device. It allows the user to try a number of design implementation options using all of the design implementation controls in a batch mode. The parameter file instructs the partitioner and the router to maximize both device utilization and performance.

Property File

The pDS+ Viewlogic Fitter also accepts a property file (design.prp) which allows the designer to assign specific features to signals and nets using all of the design attributes available. The property file helps guide the fitter in implementing the design in the best way.

Design Verification

The pDS+ Viewlogic software offers complete post route design verification using the optional Viewsim/PROsim timing simulators. The pDS+ Viewlogic Fitter generates the "sim" file which can be used with the Viewsim/PROsim simulators, or other design platforms with behavioral simulation models from Synopsys Logic Modeling Division. The Viewlogic simulation libraries and the PROsim simulator are available from Lattice Semiconductor.

Fuse Map Generation

The pDS+ Viewlogic software generates a device fusemap in standard JEDEC format. A security feature offers protection of proprietary designs from unauthorized duplication JEDEC format to the device fusemap thus facilitating a quick, easy functional verification of a programmed device.

System Requirements (PC Platform)

- 486/Pentium IBM Compatible PC
- MS DOS Version 3.3 or Later
- Windows 3.1 or Later
- 16 MB RAM with 30 MB Hard Disk Space
- Serial Port for Mouse
- 3 Button Mouse (Mouse Systems Compatible)
- Parallel Printer Port for Software Key
- Workview Plus 4.3 or later
- PROseries 6.0 or later

System Requirements (Sun Platform)

- Sun Sparc 4
- Sun O/S Version 4.x or Solaris 2.3 or Later
- Open Windows 3.0
- Powerview 5.1 or Later
- 16 MB RAM with 30 MB Hard Disk Space
- 3 Button Mouse

Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS1102-PC2	Viewlogic Viewsim/PROsim and Viewdraw/PROcapture Libraries and Interface Files (Direct Viewlogic Customers on the PC)
pDS1102-SN1	Viewlogic Viewsim/PROsim and Viewdraw/PROcapture Libraries and Interface Files (Direct Viewlogic Customers on the Sun)
pDS1102-SN2	Viewlogic Viewsim/PROsim and Viewdraw/PROcapture Libraries and Interface Files (Direct Viewlogic Customers on the Sun)
pDS1103-PC2	Viewlogic Viewsim/PROsim and Viewdraw/PROcapture Software Upgrade, Libraries, and Interface Files (Viewlogic Software from Other FPGA Suppliers on the PC)
pDS1104-PC2	Viewlogic Viewsim/PROsim and Viewdraw/PROcapture Software Upgrade, Libraries, and Interface Files (Viewlogic Software from Xilinx on the PC)
pDS1105-PC2	Viewlogic Viewsynthesis/ PROsynthesis Library (PC)
pDS1105-SN1	Viewlogic Viewsynthesis/ PROsynthesis Library (Sun)
pDS1301-PC2	Viewlogic PROcapture Schematic Editor
pDS2101-PC2	pDS+ Viewlogic Fitter for PC
pDS2101-SN1	pDS+ Viewlogic Fitter for Sun
pDS2101-SN2	pDS+ Viewlogic Fitter for Solaris 2 O/S
pDS2101-3UP/SN1	3000 Family Upgrade for pDS2101-3UP/SN1
pDS2101-3UP/PC2	3000 Family Upgrade for pDS2101-3UP/PC2

pDS3302A-PC2	pDS+ Viewlogic PROsim Functional and Timing Simulator (PC) for PROcapture Users
pDS3302-PC2	pDS+ Viewlogic PROsim Functional and Timing Simulator (PC) for Simulation Only Users
pDS3305A-PC2	Viewlogic PROsynthesis VHDL Synthesis Tools

Annual Maintenance*

pDS1102M-PC2	Maintenance for pDS1102-PC2
pDS1102M-SN1	Maintenance for pDS1102-SN1
pDS1102M-SN2	Maintenance for pDS1102-SN2
pDS1103M-PC2	Maintenance for pDS1103-PC2
pDS1104M-PC2	Maintenance for pDS1104-PC2
pDS1105M-PC2	Maintenance for pDS1105-PC2
pDS1105M-SN1	Maintenance for pDS1105-SN1
pDS1301M-PC2	Maintenance for pDS1301-PC2
pDS2101M-PC2	Maintenance for pDS2101-PC2
pDS2101M-SN1	Maintenance for pDS2101-SN1
pDS2101M-SN2	Maintenance for pDS2101-SN2
pDS3302M-PC2	Maintenance for pDS3302-PC2 or pDS3302A-PC2
pDS3305AM-PC2	Maintenance for pDS3305A-PC2

*One year of maintenance is provided with every product purchase.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic) 1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com

pDS+™ LOG/iC Software

Features

- **pLSI® AND ispLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000**
- **DESIGN ENTRY USING ISDATA LOG/iC CLASSIC OR LOG/iC2**
  - **— Design Verification Using LOG/iC Functional Simulation**
  - **— Lattice Semiconductor Fitter for Design Synthesis**
  - **— Optional Timing Simulation**
- **INTEGRATED DEVELOPMENT ENVIRONMENT FOR MIXED-MODE DESIGN ENTRY**
  - **— ISDATA LOG/iC Syntax, Including Boolean Equations, Truth Tables and State Machines, Optional VHDL, Schematics or Graphical State Machine Entry**
  - **— Graphical, Menu-Driven User Interface**
- **LATTICE SEMICONDUCTOR pDS+ LOG/iC FITTER**
  - **— Multi-Level Logic Synthesis**
  - **— Efficient Design Optimization and Minimization**
  - **— Automatic Mapping and Device Fitting**
  - **— Automatic Partitioning with High Utilization**
  - **— Predictable Performance**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Device Fuse Map**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download**
  - **— ispATE™ Board Test Programming Utility**
- **PLATFORMS SUPPORTED**
  - **— PC Windows 3.1**

Introduction

The pDS+ LOG/iC software from Lattice Semiconductor Corporation (LSC) offers a powerful solution to fit high density logic designs into ispLSI and pLSI devices.

Design entry is made simple by using LOG/iC Classic or LOG/iC2 software from ISDATA GmbH together with the pDS+ LOG/iC Fitter for design implementation. The pDS+ LOG/iC software combines high-level, device independent design entry with efficient logic compilation, delivering unprecedented performance for the most complex designs.

ISDATA LOG/iC

The easy to use, menu-driven ISDATA software package provides a complete design environment (see figure 1). Using the LOG/iC program, complex designs can be quickly and efficiently described using a combination of Boolean Equations, Truth Tables, State Machine syntax or schematics. The LOG/iC syntax creates designs without regard to any specific device dependencies. The built-in functional simulator allows designs to be fully verified before device fitting. The menu driven environment makes design implementation simple to use.

pDS+ LOG/iC Fitter

The pDS+ LOG/iC Fitter for ispLSI and pLSI devices is completely integrated within the LOG/iC software environment. The Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place & route and fusemap generation with optional test vectors in standard JEDEC format. Extensive top level design control is provided to optimize design implementation for speed and/or high device resource utilization.

Design Optimization and Logic Minimization

The pDS+ LOG/iC Fitter uses proprietary algorithms targeted for device specific features. The Fitter optimizes the design thoroughly, compressing multiple level logic into two level logic, and utilizing logic minimization, product term sharing and XOR functions wherever necessary. In addition, the pDS+ LOG/iC Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

Automatic Partitioning

The pDS+ LOG/iC Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features, such as the hard XOR function and product term sharing. The internal XOR can be utilized for arithmetic functions, and T-Type flip-flops. Common sub-expressions are extracted, and unused registers are eliminated. These features combine to maximize device resource utilization and increase design performance.

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Figure 1. pDS+ LOG/iC Design Interface

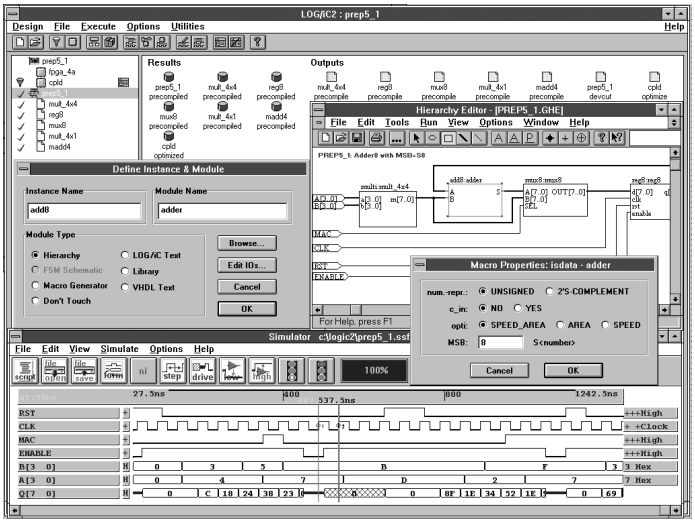
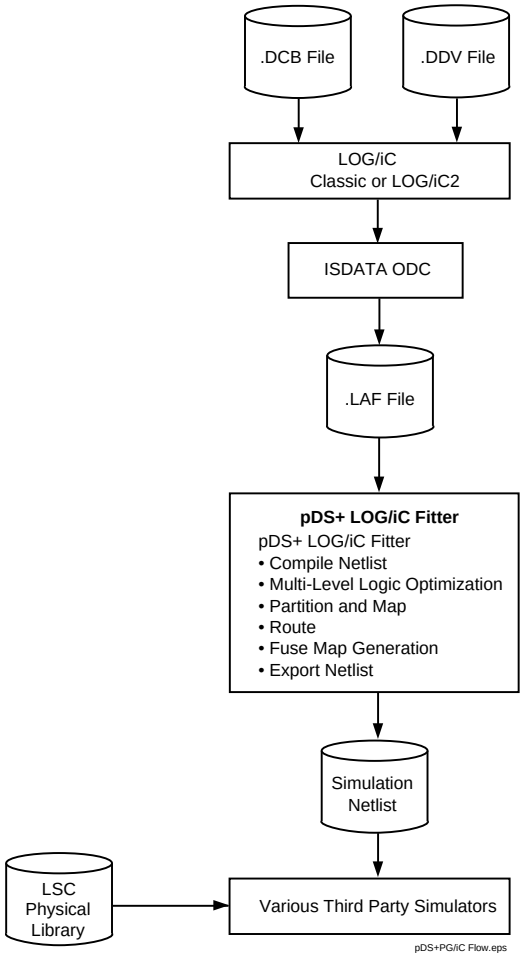


Figure 2. pDS+ LOG/iC Fully Integrated Design Environment



Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or incorporates user assigned pinouts.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation. The result is small design changes don't result in expensive PC board rework.

Design Parameter Control

The pDS+ LOG/iC Fitter offers extensive design control at the design entry level, letting the user optimize the design for maximum utilization and/or speed. All of the controls are specified using "attributes" in the design property and parameter files. These controls fall into two categories:

- — Fitter Controls
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Control Options

Special properties can be passed to the pDS+ LOG/iC Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization.

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

pDS+ LOG/iC Design implementation controls are used for changing such design parameters as security, pull-ups etc. Some of the implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These attributes control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

The following attributes specify paths in the design that have special fitting requirements:

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ LOG/iC Fitter uses a parameter file (.PAR file) feature, which is created by the entries in the .DDV file to help designers optimize the design for the right device. The parameter file instructs the partitioner and the router on how to maximize both device utilization and performance.

Property File

The pDS+ LOG/iC Fitter also accepts a property file (design.prp) which allows the designer to assign specific features to signals and nets using all of the design attributes available. The property file helps guide the fitter in implementing the design in the best way.

The pDS+ LOG/iC Fitter provides post route equations showing exactly how the design is implemented in the selected device. Optional functional simulation is also available for detailed preroute simulation of designs using the VERIFIER section of the LOG/iC menu.

Design Verification

The pDS+ LOG/iC software provides functional simulation of ispLSI and pLSI designs using the optional LOG/iC Functional Design Verifier (FDV).

Complete post route timing simulation is also available using simulators such as OrCAD's VST 386+ and Viewlogic. Timing libraries, sold separately, are required.

Fuse Map Generation

The pDS+ LOG/iC Fitter generates a device fuse map in standard JEDEC format. The fuse map is automatically produced and inserted in the JEDEC file after a successful route. A security feature gives protection of proprietary designs from unauthorized duplication.

System Requirements

486/Pentium IBM Compatible PC

- — Windows 3.1
- — 16 MB RAM with 20MB Hard Disk Space
- — 3 1/2" Floppy Disk Drive
- — ISDATA's LOG/iC Classic or LOG/iC2
- — Parallel Printer Port for Software Key
- — EGA Graphics Monitor or higher

Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High pin-count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2103-PC1	pDS+ Logic Fitter
pDS2103-3UP/PC1	3000 Family Upgrade
pDS3302-PC2	Viewlogic PROsim Simulator
pDS1102-PC2	Viewsim Library
pDS1170-PC1	OrCAD Library
pDS1131-PC1	Verilog and VHDL Sim Library

Annual Maintenance*

pDS1102M-PC2	Maintenance for pDS1102-PC2
pDS1170M-PC1	Maintenance for pDS1170-PC1
pDS1131M-PC1	Maintenance for pDS1131-PC1
pDS2103M-PC1	Maintenance for pDS2103-PC1
pDS3302M-PC2	Maintenance for pDS3302-PC2

*One year of maintenance is provided with every product purchase.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
1-408-428-6414 (International)
BBS: 1-408-428-6417
FAX: 1-408-944-8450
email: apps@latticesemi.com

ISP™ Synario System

Complete Development System: Design Entry, Functional Simulation, Hardware and Device Samples

Includes

- **SOFTWARE**
  - **— Data I/O's Synario Entry and Functional Simulation Software**
  - **— pDS+™ Synario Fitter for ispLSI® and pLSI® Devices**
  - **— ispGDS™ (Generic Digital Switch) Compiler Software**
  - **— ISP™ Programming Software**
- **SAMPLES**
  - **— ispLSI 2032 Device in 44-Pin PLCC Package**
  - **— ispGAL22V10 Device in 28-Pin PLCC Package**
  - **— ispGDS14 Device in 20-pin PLCC Package**
- **HARDWARE**
  - **— ispDOWNLOAD™ Cable**

Features

- **Easy-to-Use Kit Contains Everything Needed for In-System Programmable™ Device Design-in**
- **Data I/O's Synario Software — Schematic Entry, ABEL HDL Entry, Functional Simulator with Waveform Viewer, Synario Project Navigator**
- **Supports LSC's ispLSI 1016, 1024, 2032, 2064 and 2096 Devices — the Industry's Fastest High Density Programmable Devices at up to 154 MHz**
- **Supports All Lattice Semiconductor GAL Architectures including the ispGAL22V10**
- **Supports ISP Generic Digital Switch for Applications such as Software Driven Hardware Configuration and Multiple DIP Switch Replacement**
- **Keyless for Easy Portability**

Introduction

The Lattice Semiconductor ISP Synario System contains everything needed to design and program with Lattice Semiconductor ispLSI and GAL devices. The full version of Data I/O's Synario-Entry tools for schematic capture and ABEL-HDL language logic design, a functional simulator and Data I/O's Project Navigator for easy design and logic debugging are included. The ISP Synario System supports high density design for Lattice Semiconductor's ispLSI and pLSI 1016, 1024, 2032, 2064 and 2096 devices. The tools included also support the full range of Lattice Semiconductor's industry standard ispGAL and GAL devices, including the ispGAL22V10, GAL16V8, GAL20V8 and GAL6001 devices, and others. In addition, the ISP Synario System includes device samples of the ispLSI 2032, isp GAL22V10 and ispGDS™, as well as an ispDOWNLOAD™ Cable to download designs to the PC board.

In-System Programmability (ISP)

ISP is a LSC innovation that enables device programming and reprogramming on the printer circuit board at 5 volts. There are several advantages to in-system programmability: 1) It accelerates board- and system-level debug and enables you to define your board layout earlier in the design process; 2) ISP eliminates bent leads caused by extra handling and socket insertions made during the device programming process; 3) Systems incorporating ISP are reconfigurable with the devices already soldered to the printed circuit board, minimizing board rework expense; and 4) Field upgrades become easy by downloading a new configuration file to the end equipment via floppy disk or modem.

Synario Entry and pDS+ Fitter

The ISP Synario System contains a full featured version of Data I/O's Synario Entry tools for schematic capture and ABEL-HDL language logic design. The Synario Entry tool also includes a functional simulator with waveform viewer and Data I/O's powerful Project Navigator for easy design and logic debugging. Mixed-mode design entry is made easy with this system using schematics and powerful high level equations, truth tables, and state machine syntax in a single device design. Synario's powerful design features and versatile libraries are all presented in a user friendly Windows™ based environment that makes design even easier. The Synario Project Navigator is a design manager that organizes source files and presents an easy to follow processing checklist.

Tightly integrated with Synario, Lattice's pDS+ Synario Fitter features multi-level logic synthesis, automatic partitioning and mapping, design optimization for higher performance and better device utilization, and programming file creation.

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ispLSI and pLSI Device Support

Available in speed grades from 5.5ns to 20ns t_{PD} and 154MHz to 60MHz Fmax, the ispLSI 1000 and 2000 family devices supported by this system represent the fastest and most innovative architectures in the CPLD industry. And best of all, they offer Lattice ISP technology.

ispGAL, GAL and ispGDS Device Support

The ispGAL22V10 is the industry's only in-system programmable 22V10 device and offers speeds up to 7.5ns maximum propagation delay. The logic functionality, fuse map, and AC and DC parameters of the ispGAL22V10 are fully compatible with standard bipolar and CMOS 22V10 devices. The 28-pin PLCC package provides the same functional pinout as the standard 22V10 by using the four no-connect pins on the 28-pin PLCC package for the ISP interface signals. The Lattice GAL device architectures supported include the 16V8, 16V8Z, 16LV8, 16LV8Z, 16VP8, 18V10, 20V8, 20LV8Z, 20RA10, 20VP8, 20XV10, 22LV10, 22V10, 26CV12, 6001, and 6002. Lattice's ispGDS family is a unique in-system programmable switch device with dual banks of I/O switches where any I/O switch in one bank can be driven by any I/O switch in the other bank. Lattice's ispGDS family consists of the ispGDS14, ispGDS18 and ispGDS22 devices.

ISP Daisy Chain Download and ispCODE

ISP Daisy Chain Download software is a comprehensive design download package for the LSC ISP device families. The ISP Daisy Chain software provides an efficient method of programming LSC devices using JEDEC files generated from any compatible software tool. This complete device programming tool helps you to quickly and easily program devices with your designs, supporting both the Microsoft Windows and DOS environments.

The ISP Daisy Chain Download software includes:

- — Support for the Microsoft Windows 3.1 design environment
- — Support for the DOS environment
- — JEDEC file conversion to the ispSTREAM™ for download directly from your system to a device
- — Detection and identification of as many as 30 devices in a daisy chain
- — Single ISP device programming
- — Multiple ISP device daisy chain programming
- — Easy set-up menus for multiple ports
- — Simple device configuration menus

ispCODE software includes ANSI C source routines for In-System Programming. ispCODE makes it easier to implement ISP technology programming using an embedded system microprocessor or ATE final test equipment.

Product Ordering Information

Product Code	Description
ISP-SYN	ISP Synario System

isp™ Starter Kit

Starter Software, Hardware, Datasheets and Samples for the ispLSI®, ispGAL® and ispGDS™ Families

Includes

- **SOFTWARE**
  - **— ispStarter™ Design Development System for ispLSI 1016/E and 2032 Device Design**
  - **— ispGDS™ (Generic Digital Switch) Compiler and Download Software**
  - **— ispCODE™ ANSI C Source Programming Routines**
  - **— ISP Daisy Chain Download Software**
  - **— Lattice Semiconductor Corporation (LSC) Data Book**
  - **— LSC ISP Manual**
- **SAMPLES**
  - **— ispLSI 2032 Device in 44-Pin PLCC Package**
  - **— ispGAL22V10 Device in 28-Pin PLCC Package**
  - **— ispGDS14 Device in 20-Pin PLCC Package**
- **HARDWARE**
  - **— ispDOWNLOAD™ Cable**

Features

- **Easy-to-Use Kit Contains Everything Needed for In-System Programmable™ Device Design-in**
- **Supports LSC's ispLSI 1016/E and 2032 Devices — the Industry's Fastest High Density Programmable Devices at up to 154 MHz**
- **Supports Industry Standard 22V10 Architecture Coupled with LSC's Innovative In-System Programmable Design Capability**
- **Supports ISP Generic Digital Switch for Applications such as Software Driven Hardware Configuration and Multiple DIP Switch Replacement**
- **E^2CMOS Technology**

Introduction

The ispStarter Kit is designed to make Lattice Semiconductor's innovative In-System Programmable device technology available in a single, complete package. The ispStarter Kit contains all the software, hardware, device samples, and information you need to begin designing with LSC's ISP products. The ispLSI devices are the fastest High Density Programmable Logic devices in the industry, at 154 MHz, as certified by PREP™ Benchmarks. LSC's 7.5ns ispGAL22V10 device has all the advantages of In-System Programmability and maintains the familiar 22V10 architecture and 28-pin PLCC pinout. The ispGDS is a unique family of devices that offers the ability to configure its programmable switch matrix to connect signals arbitrarily between two banks of I/O pins or to force pins to fixed high or low logic states.

In-System Programmability (ISP)

ISP is a LSC innovation that enables device programming and reprogramming on the printer circuit board at 5 volts. There are several advantages to in-system programmability: 1) It accelerates board- and system-level debug and enables you to define your board layout earlier in the design process; 2) ISP eliminates bent leads caused by extra handling and socket insertions made during the device programming process; 3) Systems incorporating ISP are reconfigurable with the devices already soldered to the printed circuit board, minimizing board rework expense; and 4) Field upgrades become easy by downloading a new configuration file to the end equipment via floppy disk or modem.

ispLSI 2032 and ispStarter Software

The ispLSI 2032 device is a fast, high density programmable logic device containing 32 logic registers, 32 Universal I/O pins, two dedicated input pins, three dedicated clock input pins, and a programmable Global Routing Pool (GRP). The basic logic element of the device is the Generic Logic Block (GLB) which has 18 inputs, a programmable AND/OR/XOR array, and four outputs that may be configured as either combinatorial or registered. LSC's ispStarter Design Software is a high performance development environment that runs on IBM compatible 386/486/Pentium PCs. The software has a friendly, efficient, Microsoft Windows Interface which supports familiar Boolean equation entry and includes libraries of over 300 complex macros. The ispStarter software features automatic logic Place and Route for quick design implementation.

ispGAL22V10 and Download Software

The ispGAL22V10 is the industry's first in-system programmable 22V10 device and offers a fast 7.5ns maximum propagation delay time. The generic architecture provides maximum flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The logic

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functionality, fusemap, and AC and DC parameters of the ispGAL22V10 are fully compatible with standard bipolar and CMOS 22V10 devices. The 28-pin PLCC package provides the same functional pinout as the standard 22V10 by using the four "No Connect" pins on the 28-pin PLCC for the ISP interface signals.

Designs for the ispGAL22V10 can be compiled by any logic compiler supporting the 22V10 architecture.

ispGDS Compiler

The Lattice Semiconductor ispGDS family is an ideal solution for reconfiguring system signal routing and replacing DIP switches used for feature selection. Each I/O cell can be configured as an input, an inverting or noninverting output, or a fixed TTL high or low output. Any I/O pin in the bank can be driven by any I/O pin in the opposite bank. A single input can also drive one or more outputs in the opposite bank, allowing a signal, such as a clock, to be distributed to multiple destinations on the board.

The ispGDS Compiler software is a simple text entry and compilation design tool that produces a standard JEDEC file for device programming.

ISP Daisy Chain Download and ispCODE

ISP Daisy Chain Download software is a comprehensive design download package for the LSC ISP device families. The ISP Daisy Chain software provides an efficient method of programming LSC devices using JEDEC files generated from any compatible software tool. This complete device programming tool helps you to quickly and easily program devices with your designs, supporting both the Microsoft Windows and DOS environments.

The ISP Daisy Chain Download software includes:

- — Support for the Microsoft Windows 3.1 design environment
- — Support for the DOS environment
- — JEDEC file conversion to the ispSTREAM™ for download directly from your system to a device
- — Detection and identification of as many as 30 devices in a daisy chain
- — Single ISP device programming
- — Multiple ISP device daisy chain programming
- — Easy set-up menus for multiple ports
- — Simple device configuration menus

ispCODE software includes ANSI C source routines for In-System Programming. ispCODE makes it easier to implement ISP technology programming using an embedded system microprocessor or ATE final test equipment.

Ordering Information

Part Number	Description
isp-SK2	LSC ispStarter Kit

ispCODE™ Software

Source Code for In-System Programming of the ispLSI®, ispGAL® and ispGDS™ Families

Features

- **C-LANGUAGE SOURCE CODE FOR IN-SYSTEM PROGRAMMING OF THE ispLSI®, ispGAL® and ispGDS™ FAMILIES**
  - **— Simplifies In-System Programming**
  - **— Pre-Defined Routines for Common Programming Functions**
  - **— Extensively Commented Code Provides Complete Reference**
  - **— Easy Modification Saves Valuable Time**
  - **— Supports Programming of Multiple ispLSI Devices on Individual Boards**
- **ACCEPTS PROGRAMMING FILES FROM pLSI® AND ispLSI® DEVELOPMENT SYSTEM**
  - **— Supports pDS® and pDS+™ Software**
  - **— Supports ispLSI 1000/E, 2000, 3000 and 6000 Families**
- **PORTABLE TO ANY HARDWARE PLATFORM**
  - **— Adaptable to Any Hardware Interface**
  - **— UNIX Systems, PCs, Testers, Embedded Systems**
  - **— ANSI-Standard C for Portability**
- **GENERATES ispSTREAM™ FORMAT FOR GREATER EFFICIENCY**
  - **— Bit-packed File Format for Storing JEDEC Fuse Map**
  - **— Requires Less Than 1/8 the Storage Space of a Standard JEDEC File**
  - **— Ideal for Use in Embedded Systems**
  - **— Includes Checksum To Assure Data Integrity**
- **USER ELECTRONIC SIGNATURE (UES) SUPPORTED**
  - **— Provides Data Storage Area In Device**
  - **— Facilitates User Identification of Program for Secured Devices**
  - **— Automatic Counter Records Number of Programming Cycles**

Introduction

The ispCODE software from Lattice Semiconductor Corporation (LSC) is designed to facilitate in-system programming of ISP devices on customer-specific hardware platforms. The ispCODE works with Lattice Semiconductor's pDS and pDS+ software to give users a powerful, fully integrated tool kit for developing logic designs and programming ISP devices "on-the-fly."

After completion of the logic design and creation of a JEDEC file by the pDS or pDS+ software (see figure 1), in-system programming can be accomplished on customer-specific hardware: UNIX systems, PCs, testers, embedded systems (see figure 2). The ispCODE software package supplies specific routines, with extensively commented code, for incorporation into user application programs. These routines provide users with flexible, easy-to-use program modules which support the programming of a single device or multiple devices on a board.

ispCODE Software

The ispCODE software consists of source files containing routines for performing all the functions needed to control the programming of Lattice Semiconductor in-system programmable devices. These routines are provided as fully-commented source code for easy inclusion with any software written in the industry-standard C language. These source code routines were designed from the ground up to be easily portable to any system that has an ANSI-standard C compiler. The majority of the code is completely independent of the hardware platform and rarely requires modification. All hardware dependent portions of the code are related to how the output ports are driven. The code supports the programming of multiple ISP devices in a daisy chain configuration.

A compiled version of the ispCODE is provided to demonstrate how to use the ispCODE 'C' source routines. The compiled code, TURBO.EXE, programs the device(s) through the PC parallel port. By making small changes to the hardware-specific source file and recompiling the 'C' routine, a command utility like TURBO.EXE can be created. Furthermore, the 'C' routines on the .EXE file can be integrated into user interface routines which can be customized for the end application.

The example program and the hardware-specific code are written to run on IBM PC or compatible microcomputers. The example program uses the standard PC parallel printer port to provide the interface to the device's in-system programming pins (see figure 3). The pinout is compatible with the isp Engineering Kit Model 100.

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Customizing ispCODE

ispCODE is intended to help customize the ISP programming process if the standard Lattice Semiconductor IBM-PC compatible software is unable to meet specific application needs. Some examples of non-standard needs are:

- Using a platform other than the parallel port of an IBM-PC
- Using a customized user interface
- Using the UES feature of ISP devices for board serialization (adding serial numbers to the UES, uniquely identifying the board).

If programming using the standard PC parallel port, Lattice Semiconductor recommends the use of either the Windows or DOS based download software. ISP Daisy Chain Download is provided with all new pDS and pDS+ shipments and software updates.

The files that follow are available as part of the ispCODE set:

DOS File Name	Descriptions
dld2isp.exe	Converts JEDEC files to ispSTREAM format
express.exe	Command line programming utility
ispcode.c	C source code
lattice.h	Header file for use in ispcode.c
readme.txt	A text file with information updated since this manual
turbo.exe	Compiled ispcode.c

Design Flow Using ispCODE

ispCODE reads the Lattice Semiconductor Bitstream file (ispSTREAM™) format instead of directly using JEDEC files. *dld2isp.exe* accepts a DLD file and converts the JEDEC files listed in the DLD file to a single Bitstream file. The DLD file is the file that defines the device ordering, device type, and JEDEC files for a daisy chain configuration of ISP devices. The Bitstream file should be created on a PC and transferred to the ISP device programming platform.

Figure 1. Using the ispCODE Software

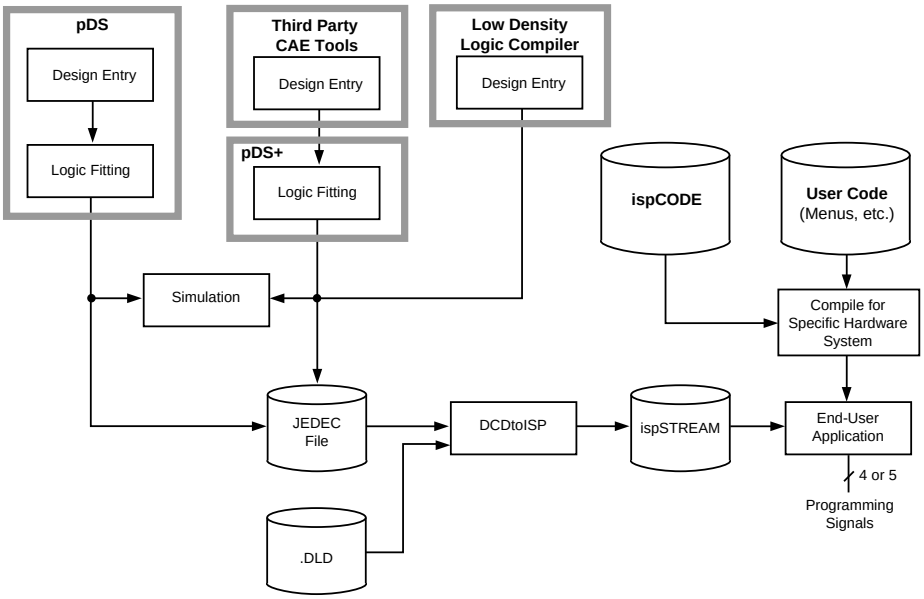


Figure 2. Configuring an ispLSI Device from an On-board Microprocessor

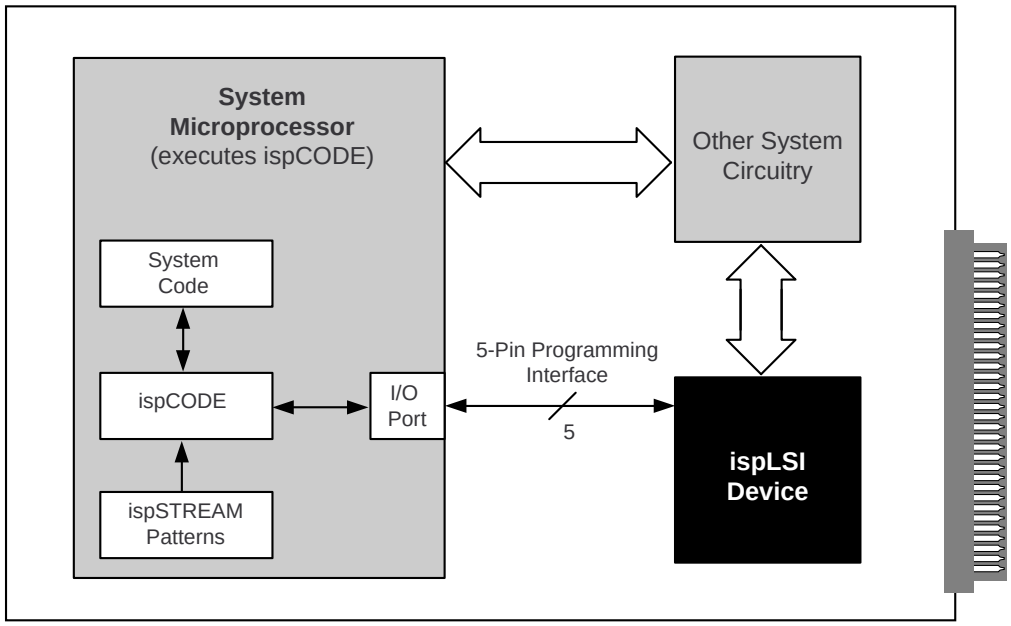
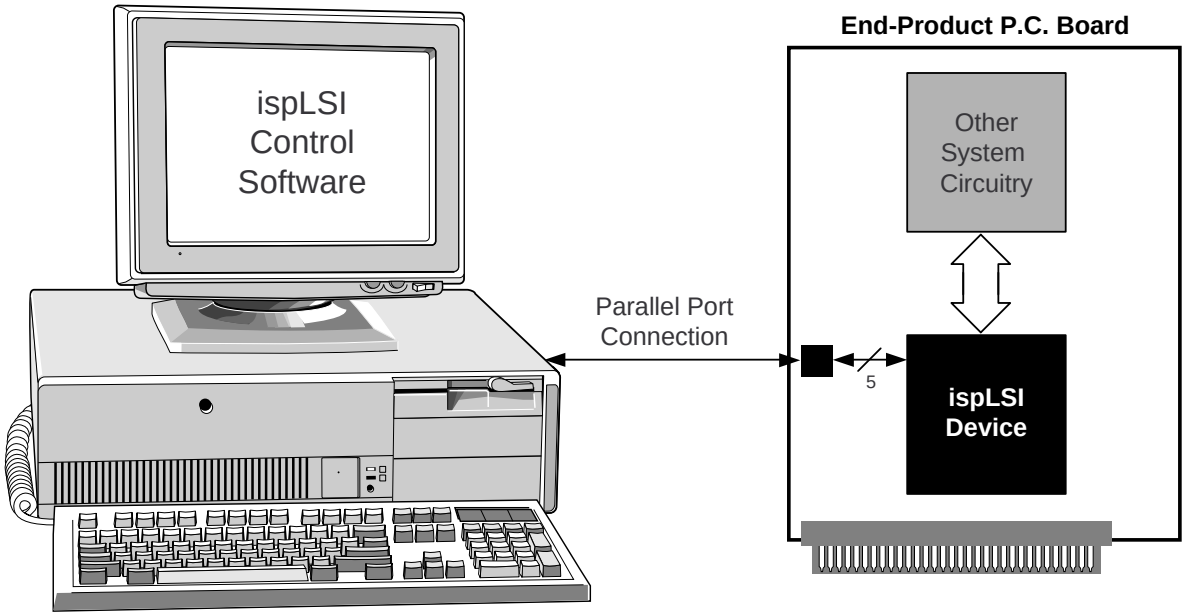


Figure 3. Configuring an ispLSI Device from a Remote System



If performing ISP programming debugging, Lattice Semiconductor recommends the use of the evaluation/design download option of the Windows or DOS based download software. If a command line version is needed, then *express.exe* supports all the same operations as the evaluation/design download of the Windows or DOS based download.

The DLD file format is the Lattice Semiconductor standard approach to defining the configuration of a daisy chain. The format of the file is straightforward: each line contains the device type, followed by an operation code, followed by a JEDEC file name. An example is shown below:

```
GDS22     PV   GDS22.jed
1016      PV   1016.jed
22V10     PV   22v10.jed
1032      PV   1032.jed
```

The previous DLD file is illustrated in Figure 4.

This file can be created manually with an ASCII text editor, or automatically with Lattice Semiconductor download software. The following rules apply when creating the DLD file:

1. The lines in the DLD file correspond to the position of the device in the chain with the first device (the device whose SDI is connected to the hardware programming port) corresponding to the first line in the file.
2. The maximum number of devices supported in a daisy chain is currently set to 60 in all Lattice Semiconductor download tools.
3. Only the following set of operations can be used in the DLD file when using *dld2isp.exe* to generate the ispSTREAM file (.isp file) for ispCODE V3.02.

Operation	Description
PV	Program and verify
PU	Program and verify with UES data from sources other than the JEDEC files
V	Verify only
NOP	No operation, by-pass device

4. The valid device names are currently:

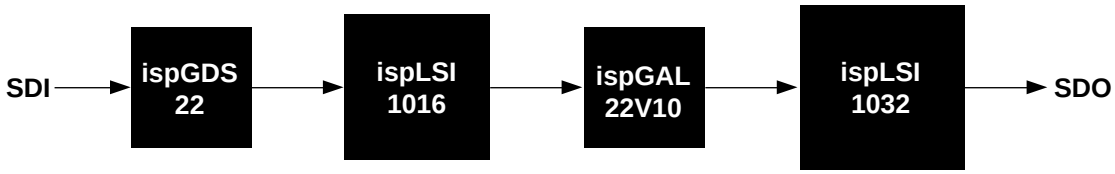
GDS14	1024	2032
GDS18	1032	2064
GDS22	1032E	2096
22V10	1048	2128
1016	1048C	3256
1016E	1048E	

To generate the ispSTREAM file, at the DOS prompt type: **dld2isp** *design_name.dld.*

The ispSTREAM file generated will be *design_name.isp.*

If the daisy chain is too large, *dld2isp.exe* displays the message “Not Enough PC Memory”. Lattice Semiconductor can supply, upon request, a *dld2isp.exe* that uses extended memory or it is possible to use a multiple DLD strategy. The multiple DLD approach requires breaking the programming operation into two or more Bitstream files, and programming different sets of devices with each Bitstream file. Using the NOP code to skip devices is the easiest way. If two Bitstream files are needed, then create two DLD files. In the first DLD file, insert NOP’s for the first set of devices in the original DLD file and in the second DLD file, insert NOP’s for the second set of devices. The first Bitstream file will only program the

Figure 4. ISP Daisy Chain



second set of devices (since the first set is NOP), and the second Bitstream file will only program the first set of devices.

The "PU" operation is available only from ispCODE version 3.01 or later. This operation allows customization of the powerful UES feature of ispLSI devices for specific applications and manufacturing flows. This field causes ispCODE to save the UES information in **char *ues**, a string that contains all the device UES information. The following shows the procedure to customize the UES:

1. Use the PU code in the DLD file for each device that will have its UES changed

2. Modify the **program_ues** routine to modify the UES with the desired value.

The **char *ues** contains the UES string that was read from the devices prior to their erasure. The UES will be written back out to the devices during the **program_ues** routine. If changes to the UES are desired, then change it at a point in the code prior to the *printf* statement in the first few lines of that routine.

Using the UES

The UES is a user-defined section of bits in the Lattice Semiconductor device that can store any sort of information, such as a board serial number or device version number. The UES is normally part of the device JEDEC file. Although the JEDEC file is an ASCII text file that can be edited with a text editor, Lattice Semiconductor recommends the use of the UES editor in the Lattice Semiconductor Windows or DOS based download software. Using the download software to edit the JEDEC file insures that any necessary corrections to the pattern and transmission checksums will be made (the UES of the ispGDS devices and ispGAL devices is included in the pattern checksum calculation, but not for ispLSI devices).

There are considerations when manually adding the checksum. The JEDEC standard allows UES data to be entered in ASCII, HEX, and binary formats and inserted directly after the pattern checksum. A text editor can be used to edit the JEDEC files directly. Please note that while the pattern checksum is not affected, the transmission checksum will be incorrect. The transmission checksum should be changed to 0000 to comply with JEDEC standard. For example:

•UES in ASCII Format

```
CXXXX*
UA UES IN ASCII*
<etx>0000
```

•UES in HEX Format

```
CXXXX*
UH01234567890ABCDEF*
<etx>0000
```

•UES in Binary Format

```
CXXXX*
U010100010*
<etx>0000
```

•This is a JEDEC compatible fuse file.

```
<stx>
DESIGN NAME:GAL61-3.lif
PART NAME  :ispLSI1048-70LQ
CREATED BY :PDS+ FUSEGEN Version 2.2
CREATED DATE:Wed Dec 22 14:23:20 1995
*QP120
*QF57600
*G0
*F0
*L00000
11......
........
11......
*CD079
uaA_MSG   <- Insert the U field here.
<etx>0000
```

Command Line Programming Utility

express.exe is a DOS command line utility that allows sequential daisy chain programming of devices. It does not support parallel programming. A standard DLD file must be created before running *express.exe*. Proper usage with all the available switches for *express.exe* can be seen by running it from the DOS prompt. The basic usage is:

express [*drive:*][*path*] *dld_filename*

The operations supported by *express.exe* are:

Operation	Description
PV	Program and verify
V	Verify only
NOP	No operation, by-pass device
C	Calculate the pattern checksum of the device
E	Erase the device only
RS	Read the pattern and UES from the device and save it in a JEDEC file.

ispCODE Source Code

Version 3 of ispCODE is set of C routines to read a Bitstream file and program a chain of ISP devices simultaneously. Since all the complex work is done by *dld2isp.exe* when the Bitstream file is created, the resulting ispCODE is relatively simple. Most of the code is a state machine which parses the Bitstream file. This state machine portion should not be modified. The only portions of ispCODE that can be modified safely are the routine to read and write from the parallel port and the routine to implement timing.

ispCODE uses the standard routines **inp** and **outp** to read from and write to the port. To redirect the I/O to a different address, create routines similar to the **inp** and **outp** routines, then link them to ispCODE. One way to do this is to make a global search and replace of "inp" and "outp" with the new I/O routine names. By renaming "inp" and "outp" to these new names, all I/O will be redirected through the new functions.

If modifying the timing routine, it is critical to meet the minimum pulse requirements specified for the different ISP devices. ispCODE calls a single routine, **pulse_width**, whenever a delay needs to be made. This routine is passed an argument that indicates the number of milliseconds to wait. Modification may be needed for this to work in a non-PC environment. It is important that the modified version of **pulse_width** guarantees that the wait period is at least as long as the argument specified. It is not critical if the pulse width is exceeded by a few hundred milliseconds. A lot of the calibration procedures the routine runs through is used to compensate for the problems that occur when running as a DOS window from Windows. If not running as a DOS window is, it may be possible to simplify the timing procedures. Of course, it is critical to insure that the minimum pulse width times are met, regardless of the method used. If minimum pulse widths are not met, device programming may not be reliable. Note that none of these routines guarantee that a pulse width will not be exceeded. If running as a DOS window or Windows application, the routine can be interrupted by another task, and the pulse time may be larger than specified.

The Borland compiler supplies a DOS routine called **delay** that is accurate to within 1 ms. The **pulse_width** code can instead be replaced with a call to **delay PROVIDING** that the application is never run as a DOS window. Lattice Semiconductor has measured the **delay** function and proven it does not work reliably when used in an application that is running as a DOS window. It is possible to put a check in one's code to help insure it is not run as a DOS window. When running as a DOS window under Windows 3.1, the environmental variable "windir" is set (as lowercase) by Windows. Therefore, by using getenv("windir") to see if the code is running as a DOS window, it is possible to insure that **delay** is not used in that case.

If running only under the Windows environment, Windows 3.1 provides the multimedia services to give high resolution timing under Windows. If compiling as a Windows application, then include the "mmsystem.h" header file, and implement a delay function like this:

```
start_time=time(NULL);
      // get starting time in seconds
timeBeginPeriod(1);
      // set to one millisecond
current_time=timeGetTime();
      // get the current value
         while((timeGetTime()-
current_time)<delay_time){NULL;
      // hog cpu time until finished}
timeEndPeriod(1);
      // free up this timer
```

A somewhat more complicated way of controlling timing when running as a DOS window is to use the Virtual Timer Devices(VTD) services available from Windows. Note that this procedure will not work when running strictly as a DOS application. Again, one can use the getenv("windir") approach explained above to see if the program is running as a DOS or DOS window application. A 32-bit time count, incremented every millisecond, is available from the VTD services by using an assembly routine like the following:

```
.MODEL large
        .DATA
vtd_addr        DD 0
        .CODE
        .386
        PUBLIC _read_timer_doswin

_read_timer_doswin     PROC

;
; this routine avoids the problems with
Windows virtualizing
; the timer ports. Instead, this routine
uses the VTD to get a 32
; timer value.
;
```

```
       mov ax, 1684h                    ;
get VTD address
       mov bx, 5h
       int 2fh
       mov word ptr [vtd_addr],di       ;
save the address
       mov word ptr [vtd_addr+2],es
       mov ax, 0101h                    ;
get current system
                                        ;
time in ms
       call DWORD PTR [vtd_addr]

       ;
       ; return the values in eax in dx,
ax
       ;

       mov edx, eax
       shr edx, 16                      ;
return 32 bit time count
       ret

_read_timer_doswin       ENDP
       END
```

An example C program that uses this routine is shown below:

```
#include <stdio.h>
#include <dos.h>
void delay(unsigned int);
extern "C" unsigned long int
read_timer_doswin(void);

// use extern to prevent name mangling,
if C++ compiler used

main (){
int i;

// generate an 80ms square wave on the
parallel port

     for(i=0;i<=1000;i++){
          outportb(0x378,0xff);
          delay(80);
          outportb(0x378,0x00);
          delay(80);
     }
}
```

```
void delay(unsigned int wait_ms){
unsigned long int start,stop;
     start=read_timer_doswin();
     printf("%lu\n",start);
     while (read_timer_doswin()-start <
wait_ms){
          NULL;
     }
}
```

Devices Supported

The ispCODE library of routines will support all LSC in-system programmable devices. As new devices are developed and released, the ispCODE library will be updated to include them.

Hardware Requirements

The ispCODE routines are designed to be portable to any hardware platform with an ANSI C compiler available. The code is written such that accessing the pins of the Lattice device is done by writing to a memory or I/O port address.

In addition to driving the pins, a method of controlling timing in the millisecond range is required. The best approach for this is a hardware-based method, such as a timer chip that can be read. Most micro controllers have a timer built in, and most other systems have some way of keeping time that may be used. The ispCODE source files include an example of reading the timer chip on a PC to accurately time the programming pulses.

ispCODE Ordering Information

A copy of the ispCODE is included with all LSC Fitter purchases.

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic) 1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com

isp™ Engineering Kit Model 100

Features

- **SUPPORTS ALL ispLSI® 1000, 2000, 3000 AND 6000 FAMILY MEMBERS**
- **STAND-ALONE DEVICE PROGRAMMER**
- **DOWNLOAD DIRECTLY TO AN ISP™ DEVICE ON A SYSTEM BOARD**
  - **Only 5 Control/Data Pins Needed**
- **QUICK DEVICE PROGRAMMING**
- **INEXPENSIVE, SMALL AND COMPACT**
  - **Eliminates Need For Expensive, Remote Programmer**
- **EXCELLENT FOR PROTOTYPING NEW DESIGNS**
  - **Not Intended For Production Programming**
- **EASY TO USE**
- **CONNECTS DIRECTLY TO PARALLEL PRINTER PORT OF HOST PC**

Description

The isp Engineering Kit Model 100 provides designers a quick and inexpensive means of evaluating and prototyping new designs using Lattice Semiconductor Corporation (LSC) in-system programmable Large Scale Integration (ispLSI) devices. This Kit is designed for engineering purposes only and is not intended for production use. The Kit programs devices from the parallel printer port of a host PC using the Lattice Semiconductor's pLSI/ispLSI Development System (pDS®) or pLSI/ispLSI Development System Plus (pDS+™) design tools. By connecting a system cable (included) from a host PC to isp Engineering Kit, or connecting from the host PC to the target device on the system board, a JEDEC file can be easily downloaded into the ispLSI device(s).

Components

The isp Engineering Kit Model 100 consists of two primary components, each sold separately:

— Universal Programming Module (UPM)

— Socket Adapters

The adapters plug into the UPM base. The adapter provides the appropriate PLCC, PQFP, TQFP, or QFP socket for a particular ispLSI device package.

isp Engineering Kit - Model 100

UPM Description

The Model 100 Universal Programming Module is designed to support all package types available from LSC. It consists of the following components:

— Universal Programming Module Base Unit

— Power Supply Converter (110VAC/9VDC @ 200mA)

- Included for North America and Asia Only

— 25-Pin Parallel Port Adapter

— 6' Universal Programming Module Download Cable with Modular Phone connectors (RJ45) on both ends

— 6' System Download Cable with a Modular Phone connector on one end and a AMP 1-87499-3 connector on other end

The connection between the host PC and the UPM base unit is shown in figure 1.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Electrical Characteristics

Power Supply

AC Input Voltage:	110 VAC
DC Output Voltage:	9 VDC @ 200mA

UPM Physical Characteristics

Length:	3.75 inches
Width:	2.625 inches
Depth:	1.375 inchs

Download Cables

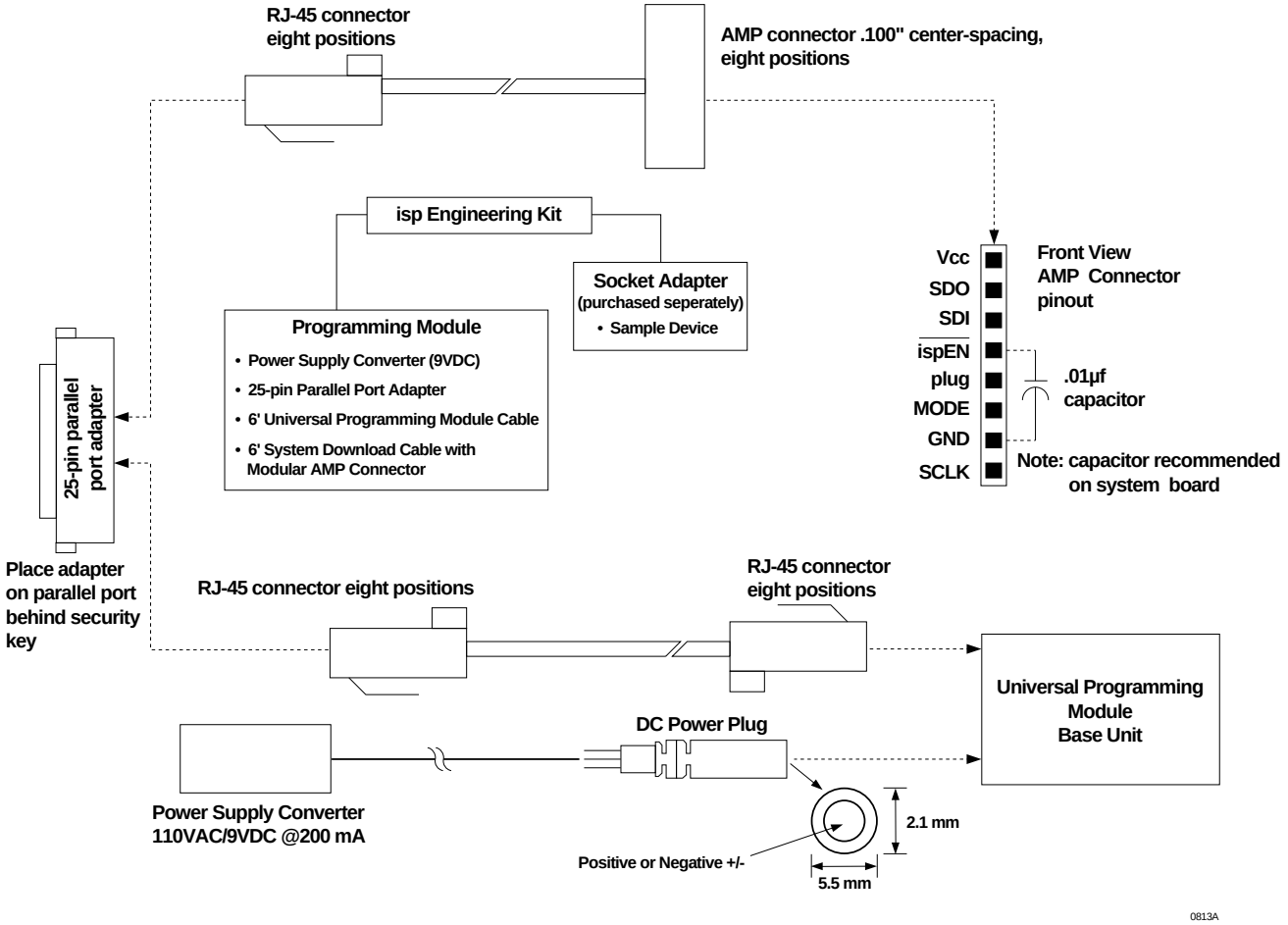
Download Cable with RJ-45 Phone Connectors on Both Ends

Length:	6.0 feet (192.8 cm)
Connectors:	RJ-45 with eight positions

System Download Cable with RJ-45 Phone and AMP 1-87499-3 Connectors

Length:	6.0 feet (192.8 cm)
Connectors:	RJ-45 with eight positions AMP single in-line 0.100 “ center spacing 8 positions

Figure 1. Universal Programming Module Description



Product Ordering Information

Product Code	Description
pDS4102-PM	isp Engineering Kit Model 100 for the PC:
	UPM programming module, (2) 8 wire Download cables, AC/DC Power Supply Converter, 25-Pin Parallel Port Adapter
pDS4102E-PM	ISP Engineering Kit Model 100 for the PC (European Model)
pDS4102-J44	44-pin PLCC socket adapter, (1) ispLSI 1016 Engineering Sample
pDS4102-T44	44-pin TQFP socket adapter, (1) ispLSI 1016 Engineering Sample
pDS4102-J68	68-pin PLCC socket adapter, (1) ispLSI 1024 Engineering Sample
pDS4102-J84	84-pin PLCC socket adapter, (1) ispLSI 1032 Engineering Sample
pDS4102-T100	100-pin TQFP socket adapter, (1) ispLSI 1032 Engineering Sample
pDS4102-Q120	120-pin PQFP socket adapter, (1) ispLSI 1048 Engineering Sample
pDS4102-Q128	128-pin PQFP socket adapter, (1) ispLSI 1048E Engineering Sample
pDS4102-M160	160-pin MQFP socket adapter, (1) ispLSI 3256 Engineering Sample

ISP Daisy Chain Download Software

Features

- **LATTICE SEMICONDUCTOR CORPORATION (LSC) SOFTWARE FOR IN-SYSTEM PROGRAMMING (ISP™)**
- **SUPPORTS ALL LSC ISP DEVICES**
- **JEDEC FILE CONVERSION TO ispSTREAM™ FOR DOWNLOAD VIA ispDOWNLOAD™ CABLE DIRECTLY FROM A PC TO A DEVICE**
- **DETECTION AND IDENTIFICATION OF AS MANY AS 30 DEVICES IN A DAISY CHAIN**
- **MULTIPLE LSC ISP DEVICE PROGRAMMING IN PARALLEL (TURBO) MODE**
- **USER ELECTRONIC SIGNATURE (UES) PROGRAMMING**
- **SECURITY FUSE SUPPORT**
- **EASY-TO-USE DEVICE CONFIGURATION MENUS WITH FUNCTIONS FOR PROGRAM, VERIFY, CHECKSUM, ERASE AND READ AND SAVE**
- **BOTH DOS AND WINDOWS VERSIONS INCLUDED IN EVERY PACKAGE**

Introduction

ISP Daisy Chain Download software is a comprehensive, programmable device download package for all LSC In-System Programmable™ device families. ISP Daisy Chain Download software provides an efficient method for programming LSC ISP devices from the logic design JEDEC file generated by any LSC Fitter or compiler tool. ISP Daisy Chain Download software allows you to quickly and easily program devices using specific commands like Program and Verify. ISP Daisy Chain Download software programs ISP devices on a printed circuit board (or in-system) quickly and easily. Most importantly, devices can be programmed again and again, depending on your system needs.

In-System Programmability

ISP is an LSC innovation that enables device programming and reprogramming on the printed circuit board at 5 volts. There are several advantages to in-system programmability: 1) It accelerates board- and system-level debug and enables you to define your board layout earlier in the design process; 2) ISP eliminates bent leads caused by extra handling and socket insertions made during the device programming process; 3) Systems incorporating ISP are reconfigurable with the devices already soldered to the printed circuit board, minimizing board rework expense; and 4) Field upgrades become easy by downloading a new configuration file to the end equipment via floppy disk or modem.

Figure 1 illustrates a typical block diagram of multiple LSC ISP devices cascaded together for ISP programming.

ISP Daisy Chain Download for Windows

When you invoke the download program, the ISP Daisy Chain Download software window appears. Use the drop-down windows or the toolbar icons to perform the various functions required to configure and download for ISP programming. Figure 2 shows the ISP Daisy Chain Download for Windows main menu.

A convenient menu banner and command icons make it easy to execute all the operations available with ISP Daisy Chain Download software. Included are File, Configuration, Command, Help, Turbo and UES drop-down menu options and/or command icons. The software automatically creates a .dld configuration file which may be stored and edited as desired.

Up to 30 devices may be selected for programming using the New Configuration window. JEDEC file names must be specified for each device programmed in a given configuration. Easy-to-use menus allow for the selection of devices and programming operations with the click of a mouse. Programming operations include Program and Verify, Verify, Checksum, Erase, No Operation, and Read and Save. Once the configuration is complete, a status window provides immediate results relating to the operation.

ISP Daisy Chain Download for DOS

The DOS version of ISP Daisy Chain Download software performs generally the same functions as the Windows

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Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Figure 1. Multiple Lattice Semiconductor ISP Devices Cascaded for ISP Programming

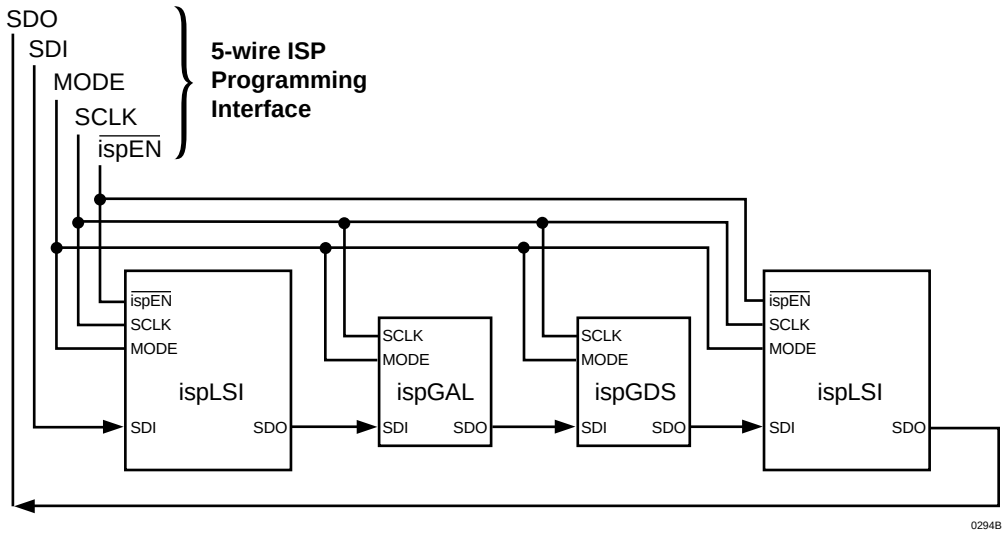


Figure 2. ISP Daisy Chain Download Main Menu (Windows)

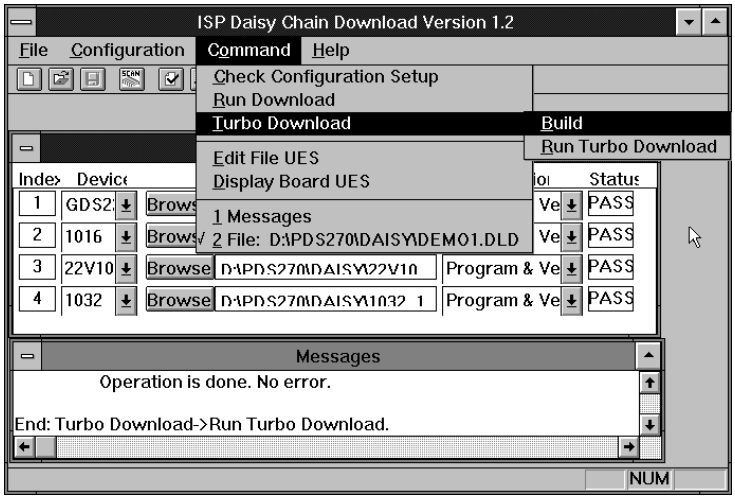
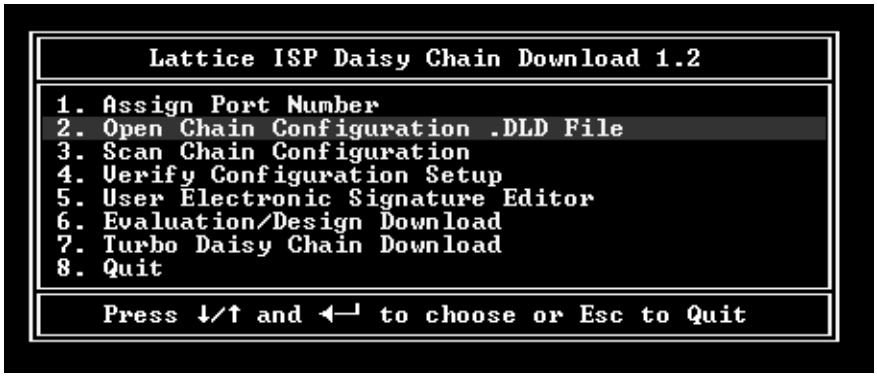


Figure 3. ISP Daisy Chain Download Main Menu (DOS)



version. When the DOS version is launched from the project working directory, the main menu appears on the screen (see Figure 3). The menu items allow you to assign the parallel port for programming and to perform functions such as opening a configuration file.

Use any text editor to generate or edit a configuration (.dld) file for device programming. The .dld file contains the ISP device type, desired programming function and the full path to the device JEDEC file(s).

ISP Turbo Download

LSC has patented the way the ispSTREAM is read from the JEDEC files and sent to the daisy chain. You must have a daisy chain configuration to use Turbo Download.

From the .dld file, the ispSTREAM is created and turbo programming may be performed. With ISP Turbo Download, you can program any number of devices in the time it takes to program a single device in the chain. An example can be illustrated in a chain of three devices with programming times of ten, seven and seven seconds, respectively. Serially, the programming time would be 24 seconds for all three devices. ISP Turbo Download programs all three devices in parallel in a total of ten seconds. The more devices chained together, the more time is saved.

Both the Windows and DOS versions of ISP Daisy Chain Download software have Turbo Download capabilities.

UES Programming

A new feature allows the user to edit and/or read the User Electronic Signature (UES) data in the JEDEC file. The Windows version allows you to set the UES in ASCII format, while the DOS version provides both ASCII and Hexadecimal UES access.

The UES is a reprogrammable memory area within each device used to identify the device logic revision and other functions. For instance, the UES may include user ID codes, revision numbers, pattern identification codes or inventory control codes.

Hardware Requirements

- IBM PC-AT 486 or compatible
- One serial port
- One parallel port
- 1 MB RAM
- EGA/VGA display (VGA is recommended)
- 3-1/2" floppy disk drive
- Mouse, Microsoft Windows compatible
- DOS and Windows versions of ISP Daisy Chain Download software occupy 500KB of disk space

Product Ordering Information

ISP Daisy Chain Download software is included with every LSC ispStarter™ Kit, ISP Synario System, pDS® and pDS+™ Fitter (PC only).

Warranty Service

- 90-day warranty on disk media

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic) 1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com

ispDOWNLOAD™ Cable

Download Cable for In-System Programming of the ispLSI®, ispGAL® and ispGDS™ Families of Devices

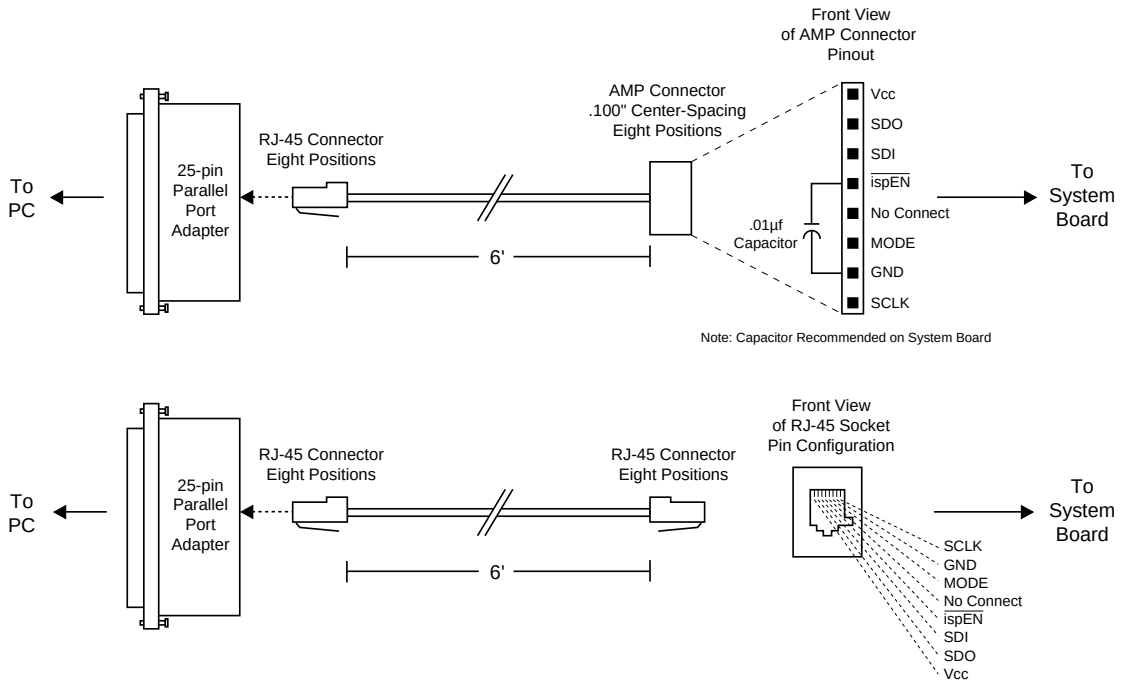
Features

- **CABLE AND PARALLEL PORT ADAPTER FACILITATE IN-SYSTEM PROGRAMMING OF ISP FAMILY OF DEVICES**
  - **— Simplifies In-System Programming**
  - **— Ideal for Design Prototyping and Debugging**
- **SUPPORTS ALL ISP® FAMILIES**
  - **— ispLSI™ Families (1000/E, 2000, 3000 and 6000)**
  - **— ispGAL® Family**
  - **— ispGDS™ Family**
- **EASY-TO-USE CONNECTORS**
  - **— 25-Pin Adapter Connects to PC Parallel Printer Port**
  - **— Two 6' Cables Offer PC Board Interface Options:**
    - **RJ-45 Connector**
    - **AMP Connector (8 Position, .100 Inch Center Spacing)**

Introduction

The ispDOWNLOAD Cable is designed to facilitate in-system programming of all Lattice Semiconductor Corporation (LSC) ISP devices on a printed circuit board directly from the parallel port of a PC. With In-System Programmiability™, hardware functions can be programmed and modified in real-time on the system board to give additional product features, shorten system design and debug cycle time, enhance product manufacturability and simplify field upgrades. After completion of the logic design and creation of a JEDEC file by a logic compiler such as the pDS®, pDS+™ Fitter or ispGDS Compiler software, Lattice Semiconductor's ISP Daisy Chain Download software programs devices on the end-product PC board by generating programming signals directly from the parallel port of a PC which then pass through the ispDOWNLOAD Cable to the device. With this cable and a connector on the PC board, no additional components are required to program a device. The ISP Daisy Chain Download software automatically generates the appropriate ISP command, programming address and data from the JEDEC fuse map information. ISP Daisy Chain Download software is included with all LSC pDS and pDS+ Fitter products.

Figure 1. ispDOWNLOAD Cable Offers Two Types of In-System Programming Interfaces



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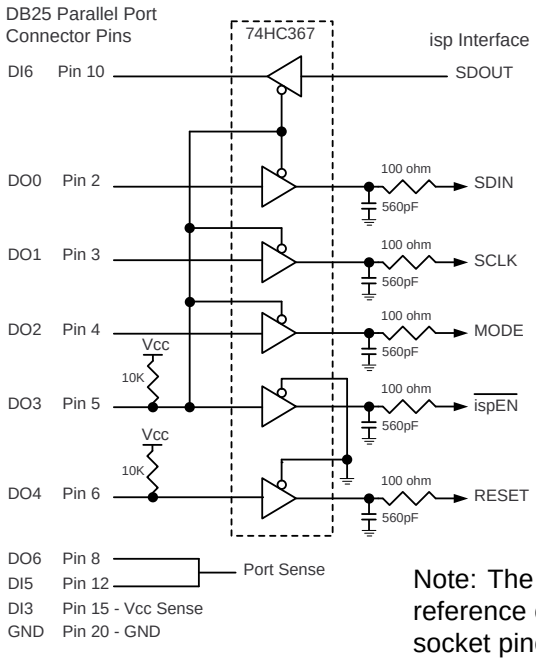
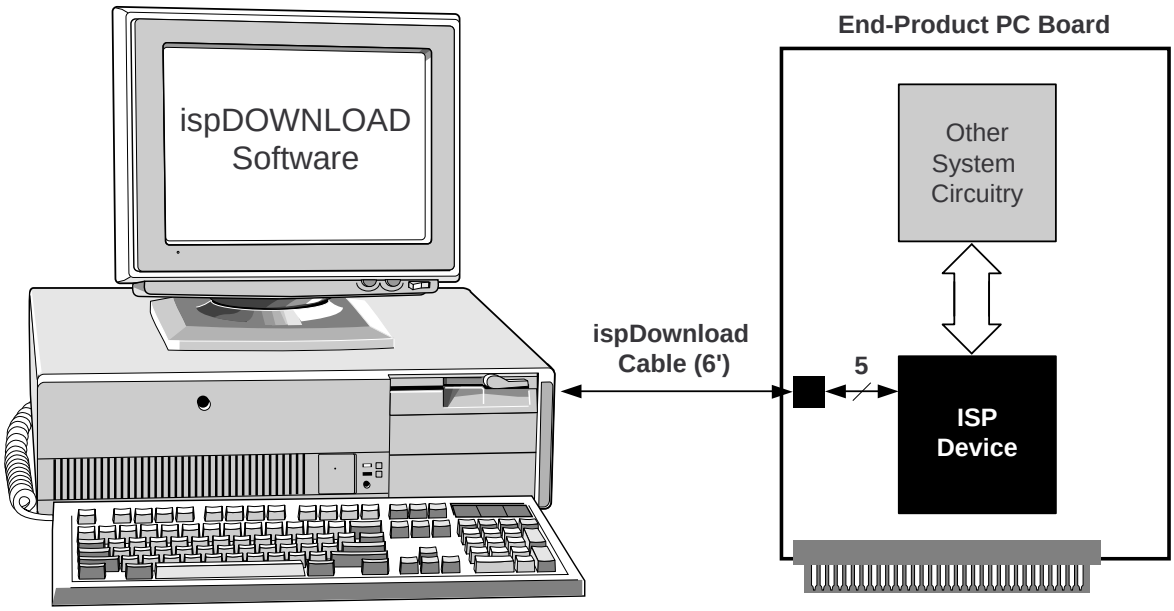
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

Figure 2. PC Parallel Port Connector



Note: The pin numbers in this diagram are for reference only. Do not use pin numbers as the socket pinout for board layout.

Figure 3. Configuring In-System Programming from a Remote System



Product Ordering Information

Product Code	Description
pDS4102-DL	ispDOWNLOAD Cable (For PC Only) Contains: Two 6' Cables with RJ45 and AMP Connectors, Parallel Port Adapter, Documentation

ispATE™ Software

Vector Creation Utility for In-System Programming of ISP™ Devices on Automatic Test Equipment

Features

- **TEST VECTOR CREATION UTILITY FOR IN-SYSTEM PROGRAMMING OF ISP DEVICES USING AUTOMATIC TEST EQUIPMENT (ATE)**
  - **— Simplifies In-System Programming on a Tester**
  - **— Generates Programming or Programming/ Verification Vectors**
- **SUPPORTS POPULAR AUTOMATIC TEST EQUIPMENT**
  - **— Teradyne Z1800 Series of Board Testers**
  - **— GenRad GR228X Series of Board Testers**
  - **— Hewlett-Packard HP3065 and HP3070 Families of Board Testers**
  - **— Additional Tester Support Planned**
- **PROGRAMMING OF SINGLE OR MULTIPLE ISP DEVICES IN A DAISY CHAIN PROGRAMMING CONFIGURATION**
  - **— Single Set of ISP Programming Signals Programs Multiple Devices**
  - **— Only TTL-Level Signals Needed to Program ISP Devices**
- **WINDOWS AND DOS VERSIONS FOR PC**
  - **— Windows Version Provides Windows User Interface and On-Line Help**
  - **— DOS Version Accepts Command Line Entry of Test Vector Parameters**
- **ACCEPTS PROGRAMMING FILES FROM LATTICE SEMICONDUCTOR'S DEVELOPMENT SYSTEMS**
  - **— Supports pDS® and pDS+™ Software**
  - **— Converts JEDEC or ispSTREAM™ Files into ISP Programming Vectors**
  - **— Supports ispGAL22V10, ispGDS, and ispLSI 1000/E, 2000, 3000 and 6000 Families**
- **ISP DEVICES SIMPLIFY MANUFACTURING FLOW**
  - **— Eliminate Stand-Alone Device Programming**
  - **— Eliminate Unnecessary Device Handling**
  - **— Eliminate Inventory Headaches**
  - **— Eliminate Incorrect Device Placement on the PCB**
- **ISP DEVICES ENHANCE BOARD LEVEL TESTABILITY**
  - **— Program Lattice Semiconductor ISP Devices On-Board with "Temporary" Test Patterns/Exercise Enhanced Test Functions/Re-Pattern ISP Devices with "Production" Patterns**

Introduction

Programming standard programmable logic devices (PLDs) is very time consuming using a stand-alone device programmer. Stand-alone programming adds costly steps to the production flow, as well as inventory headaches. By using your ATE equipment to program Lattice Semiconductor's revolutionary in-system programmable (ISP) PLDs, you can simply solder blank ISP devices onto your board like any standard component and eliminate special PLD production flows.

You can also enhance the testability of your product by developing custom logic configurations for your ISP devices specifically to enhance board test. The ISP devices can be subsequently reconfigured for their normal system functions after initial board test has been completed.

All Lattice Semiconductor Corporation (LSC) ISP devices can be easily programmed by using four or five TTL-level signals, referred to as the ISP interface. The ISP programming instructions control the serial downloading and programming of the ISP devices. Since this interface uses standard TTL-signals (no "supervoltages" required), it can easily be driven by an ATE tester.

The ispATE utility fits into the overall ISP implementation flow for programming LSC ISP devices using ATE as shown in Figure 1. One or more JEDEC files are created by LSC's pDS (proprietary) or pDS+ Fitter (third-party) development systems. These JEDEC files are then read by the ispATE utility and converted into programming vectors using the ATE's test vector format. The ATE then applies these vectors to the ISP interface pins to program or verify the ISP devices as part of the board test program.

The ispATE utility also supports the LSC daisy chain programming configuration, which allows one or more ISP devices to be programmed in a serial daisy chain through a single set of ISP programming signals.

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ispATE Overview

ispATE creates ATE-compatible programming test vectors. Both DOS command line and DOS shell menu versions of ispATE are available. The ispATE utility converts one or more JEDEC files into a series of test vectors compatible with either HP or Teradyne board testers. When the ATE drives the ISP interface of the ISP devices with the test-vector series, the ATE will program the ISP devices. Note that these vectors are not "functional test" vectors: their only purpose is to program the ISP devices with the JEDEC file contents.

Multiple ISP devices can be programmed through a single ISP interface (see Figure 2) if they are daisy chained together (see also the ISP Architecture and Programming section of this Data Book). The ispATE utility also supports ATE programming through this interface. To do so, the user must construct a configuration file, which lists the device type, order, and JEDEC file name, to determine the proper sequence of programming vectors. The configuration file is in an ISP Daisy Chain Download configuration file (.dld) format.

ISP Daisy Chain Download Configuration File (.dld)

The syntax of the ISP Daisy Chain Download format configuration file (.dld) is similar to the ispCODE configuration file. The device type (the number only) is followed by the operation to perform (this is ignored by ispATE) and the JEDEC (.jed) file name. Note that a .dld configuration file does not support reading a Bitstream (.isp) file.

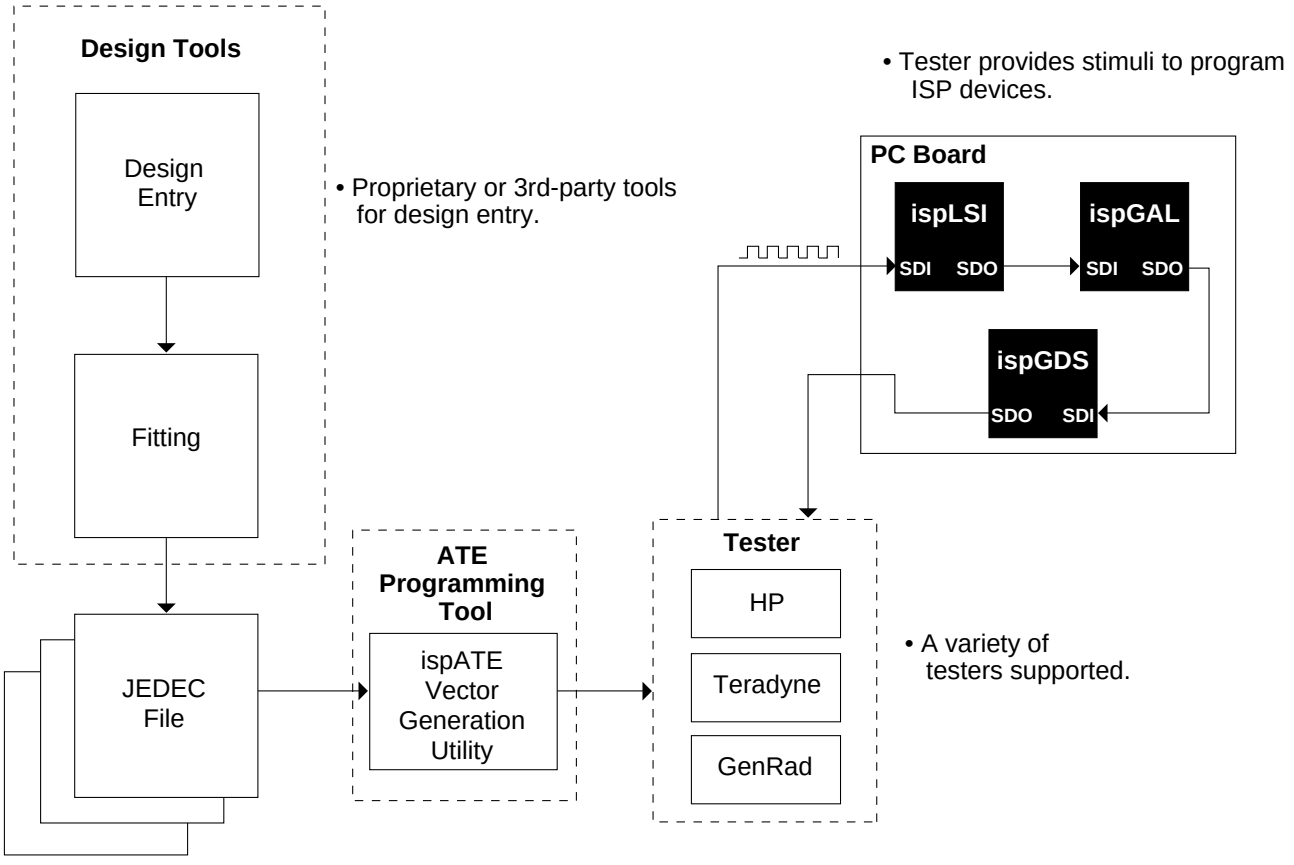
For example:

```
1024     V      1024F.JED
1016     PV     LAGO_16.JED
1032     V      1032HA.JED
1048C    PV     ADD16A.JED
```

Operation options are program (P) and verify (V).

The first device in the list is the device whose SDI pin is connected to the ISP programming hardware interface, i.e. devices are listed "first" to "last" in the chain.

Figure 1. ISP Implementation Flow Using ispATE



DOS Version of ispATE

The DOS version of ispATE accepts command line entry of test vector parameters. If you invoke ispATE without any parameters, ispATE will display a help message listing the available options, like the example in listing 1.

The DOS dialog box interface of ispATE provides the same capability as the DOS command line version (see Figure 3). It also provides on-line help for a more detailed explanation of the parameters.

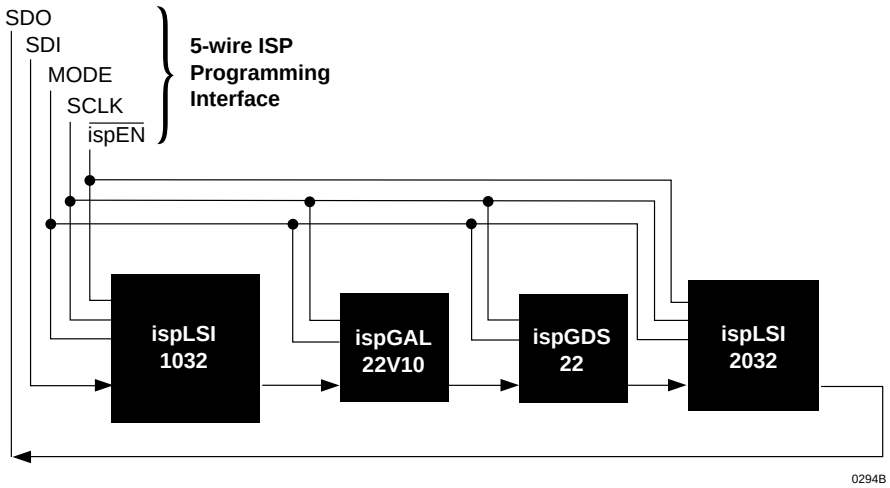
Example Output

The vector files produced by both the DOS and Windows versions of ispATE are in ASCII format, with one vector per line. Examples of the HP-PCF format, Teradyne Table Format and GenRad Table Format are shown below:

HP-PCF Format

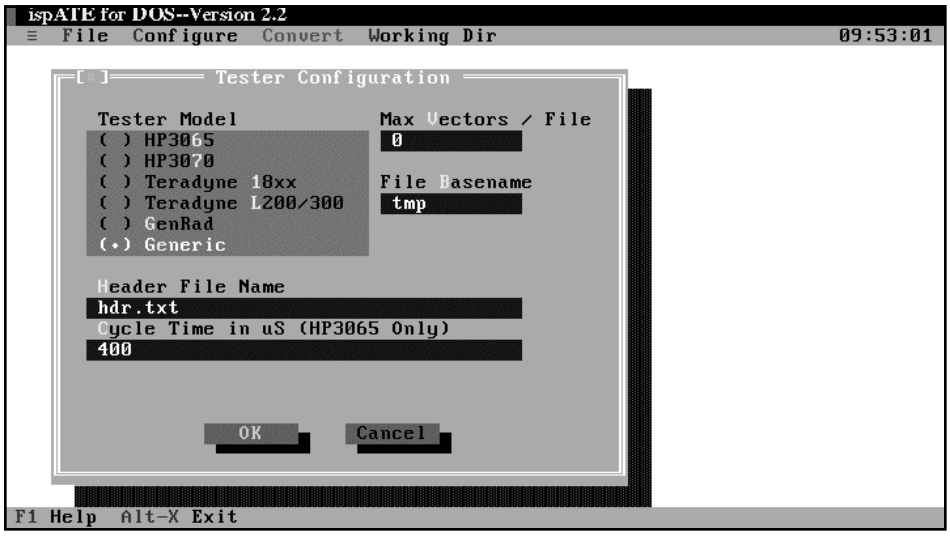
As an example, the HP-PCF test-vector format is shown in the listing below. Line 1 in the listing is an example of

Figure 2. Daisy Chain ISP Programming Configuration Example



Note: The ispLSI 1032 would be the first device in the chain description for a .DLD configuration file.

Figure 3. ispATE Vector Creation Utility, DOS Version



a test vector. The value of every pin in the ISP interface is defined in this line as a one (1), zero (0), or don't care (X). The tester will read this line and apply the indicated values. Not shown in this example is a mapping statement, which defines how the columns correspond to the ISP interface. In this example, the signals are mapped from left to right as $\overline{\text{ispEN}}$, MODE, SCLK, SDI and SDO.

```
“0000X”
“0100X”
“0101X”
! Vector 70
“0111X”
“0101X”
“0100X”
“0000X”
“0000X”
“0010X”
“0000X”
end pcf
wait 300m
pcf
“0000X”
“0100X”
“0101X”
! Vector 80
end pcf
wait 500u
pcf
“0111X”
“0101X”
“0100X”
“0000X”
“0000X”
“0100X”
end pcf
wait 500u
pcf
“0110X”
“0100X”
“0000X”
“0000X”
```

Teradyne Format

The listing below is a section from a Teradyne Table format vector file. An “X” indicates a "don't care" state for a pin, an “L” indicates that the pin should be driven to a 0, and an “H” indicates that the pin should be driven to a 1.

The order of the signals is 10 ms Delay, 1 ms Delay, $\overline{\text{ispEN}}$, MODE, SCLK, SDI and SDO.

```
LLLHHHX;
LLLHLHX;
LLLHLLX;
LLLLLLX;
LLLLLLX;
LLLLHLX;
LLLLLLX;
 ‘Waiting 300 milliseconds
 ‘Pulse the 10ms delay 1shot
Begin REPEAT 30;
HL——X;
LL——X;
End REPEAT;
LLLLLLX;
LLLHLLX;
 ‘ Vector 100
LLLHLHX;
```

Listing 1. ispATE help message listing available options.

```
USAGE       :  ispATE config_file tester num_vectors vec_file header
config_file :  ISP Daisy Chain Download format .dld file.
tester      :  HP3070
               HP3065
               Ter1800 (Teradyne Z1800 series)
               Generic
num_vectors :  The upper limit on how many vectors to use per file 0 for no limit.
vec_file    :  Name of the file(s) to contain the generated vectors
               Just enter the base name – the converter will add the rest
               For example, foo becomes foo01.pcf,foo02.pcf, ...
header      :  The name of the text file to paste at the start of each vector file
```

```
 'Pulse the 1ms delay 1shot
Begin REPEAT 1;
LH——X;
LL——X;
End REPEAT;
LLLHHHX;
LLLHLHX;
LLLHLLX;
LLLLLLX;
LLLLLLX;
LLLHLLX;
 'Pulse the 1ms delay 1shot
Begin REPEAT 1;
LH——X;
LL——X;
End REPEAT;
LLLHHLX;
LLLHLLX;
LLLLLLX;
 ' Vector 110
LLLLLLX;
```

GenRad Format

The listing below is a section from the GenRad Table. An "X" indicates a "don't care", 0 and 1 indicates the logic low and high respectively, and a "C" indicates a clock pulse. The order of the signals are the same as the previous two format as follows: $\overline{\text{ispEN}}$, MODE, SCLK, SDI, and SDO.

```
00C0X
0000X
0100X
0101X
0111X
0101X
0100X
0000X
0000X
0010X
0000X
+wait 300m
0000X
0100X
0101X
+wait 500u
0111X
0101X
0100X
0000X
0000X
0100X
+wait 500u
0110X
0100X
0000X
0000X
0100X
0101X
0111X
0101X
```

Partitioning Vectors into Individual Files

A large number of vectors are required for programming an ISP device, especially if you are programming and verifying the larger devices in the ispLSI families. You may find that your ATE requires that you partition the files into multiple file sets, due to the number of vectors and limitations imposed by the amount of available tester memory. The ispATE tool supports this by allowing you to enter a maximum number of vectors to be included in any one file.

Hardware Considerations

Maintaining Signal Values between Vector Files

Since the vector files may need to be split for ATE processing, it is critical that the ATE not inadvertently change the state of the ISP clock pin (SCLK) between files. The software will insure that the last vector of a file will have the SCLK pin held low. If the ATE allows the pins to float while the next file is being loaded, the SCLK pin should have a pull-down resistor connected to it to insure that the clock does not glitch and put the ISP device into an invalid state.

ISP Interface

Lattice Semiconductor also recommends that the ISP interface signals be held at their inactive state when not being driven by the tester. You can simply add pull-down resistors to the ISP interface programming fixture to accomplish this.

Timing

When you program LSC ISP devices, you must insure that the specified erase, programming, and verification times are met by the ATE (these timing parameters are specified in the LSC Data Book and data sheets for the appropriate devices). The ispATE utility will implement these programming delays in different ways, depending on your tester manufacturer and model (see vector file

examples on previous page). However, you must insure that if you change the vector cycle time (for HP), or make one-shot delay changes (for Teradyne), that you will not violate the timing specifications that ispATE used when originally creating the vector file. Since these issues are model dependent, they are discussed in detail below.

HP

ispATE currently supports two families of HP ATE board testers (the HP3070 and the HP3065). The 3070 testers support delays by using a "WAIT" statement. For example, if "WAIT 80 ms" appears in the PCF vector file, then the ATE will wait 80 ms at that point.

The 3065 testers do not support the wait statement, so ispATE will use repeat loops to implement the required delays. ispATE assumes a 1 MHz test-vector rate, so if you later decide to change the cycle time, it is critical that you update the timing loops as well. Lattice Semiconductor also provides an AWK utility called FIXCYCLE to update repeat loop counters for other vector cycle times. This utility is included with ispATE and is available as a DOS executable called FIXCYCLE.EXE, and as an AWK source file called FIXCYCLE.AWK if you need to run the conversion on a UNIX platform.

Teradyne Z1800

Since the Teradyne Z1800 family of board testers does not support timing through repeat loops, accurate timing requires the introduction of external delay "one-shots" to the test fixture. ispATE assumes that there will be a 10 ms and a 1 ms one-shot present in the test fixture, and generates strobe signals to trigger the one-shots to create the desired delays. Teradyne has built a custom test-fixture board for ISP programming which generates accurate delay pulses; contact Teradyne Applications Engineering at (510) 932-6900 for further information.

GenRad GR228X

LSC ispATE software generates a generic vector format for GenRad testers. The generic vector files must be converted to a specific GenRad Tester format by using the utilities provided by GenRad. The "+wait" statements are converted by the GenRad utility to properly time the ISP programming and verification pulse widths. Contact GenRad Inc. at (508) 287-7000 to obtain the GenRad utilities.

Optimizing for Programming Speed

Programming ISP devices can take several seconds per device. To minimize the programming time, ispATE programs the devices in the chain in parallel and uses the minimum test vector set.

Skipping Bulk Erase Verification Vectors

If you generate both programming and verification vectors, approximately one-third of the total number of vectors will be devoted to verification, or reading back of the device contents. Since verification has a 1 ms delay between rows, as opposed to the 80 ms delay for programming rows, verification vectors do not consume two thirds of the total amount of programming time. To reduce programming time, depending on your application, verification may be eliminated. You may be performing functional test of the board, which would make this verification step redundant. In this case, you can tell ispATE to generate vectors for programming only.

How to Obtain ispATE

The ispATE vector-creation utility is provided free of charge by Lattice Semiconductor. You can download it from the LSC BBS at (503) 693-0215. The file name is ispate.zip. The DOS version is included in the zip file, along with useful utilties.

Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic) 1-503-693-0201 (International)
BBS:	1-503-693-0215
FAX:	1-503-681-3037
email:	gal@latticesemi.com
Teradyne	1-510-932-6900
GenRad	1-508-287-7000
HP	1-800-452-4844

ispLSI and pLSI Design Tool Selector Guide

Lattice Semiconductor pLSI and ispLSI Development System (pDS) Environment		What You Have or Need from a Third-Party Vendor	What You Need From Lattice Semiconductor	Lattice Semiconductor PC Part Numbers	Lattice Semiconductor Sun Part Numbers
ispStarter Kit		N/A	ispStarter Kit (ispLSI 1016 & 2032)	isp-SK2	N/A
Boolean Entry and Fitting		N/A	pDS	pDS1101-PC1	N/A
3000 Family Device Support Option*		N/A	pDS 3000 Upgrade	pDS1101-3UP/PC1	N/A
Simulation Options*	Viewlogic	N/A	PROsim Simulator Including Libraries	pDS3302-PC2	N/A
	Viewlogic	PROsim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A
	Viewlogic	PROsim Simulator from Actel or Other Vendor	PROsim Upgrade Including Libraries	pDS1103-PC2	N/A
	Viewlogic	PROsim Simulator from Xilinx	PROsim Upgrade Including Libraries	pDS1104-PC2	N/A
	Viewlogic	Workview PLUS ViewSim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A
	OrCAD	VST 386+ or Simulation for Windows Simulator	OrCAD Library and Interface	pDS1170-PC1	N/A
	Verilog	OVI-Compliant Verilog Simulator	Verilog Library	pDS1131-PC1	N/A
	VHDL	Vital-Compliant VHDL Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	N/A

Lattice Semiconductor pDS+ ABEL Environment		What You Have or Need from a Third-Party Vendor	What You Need From Lattice Semiconductor	Lattice Semiconductor PC Part Numbers	Lattice Semiconductor Sun Part Numbers
PLD Compiler and Fitting		ABEL Compiler	pDS+ ABEL Fitter	pDS2102-PC1	pDS2102-SN1
3000 Family Device Support Option**		N/A	pDS+ ABEL 3000 Upgrade	pDS2102-3UP/PC1	pDS2102-3UP/SN1
Simulation Options**	Viewlogic	N/A	PROsim Simulator Including Libraries	pDS3302-PC2	N/A
	Viewlogic	PROsim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A
	Viewlogic	PROsim Simulator from Actel or Other Vendor	PROsim Upgrade Including Libraries	pDS1103-PC2	N/A
	Viewlogic	PROsim Simulator from Xilinx	PROsim Upgrade Including Libraries	pDS1104-PC2	N/A
	Viewlogic	Workview PLUS ViewSim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A
	Viewlogic	Powerview ViewSim Simulator	Viewlogic Library and Interface	N/A	pDS1102-SN1
	OrCAD	VST 386+ or Simulation for Windows Simulator	OrCAD Library and Interface	pDS1170-PC1	N/A
	Synario	Synario Verilog Simulator	Synario Library and Interface	pDS1120-PC1	N/A
	Cadence	Cadence Verilog-XL Simulator	Cadence Library and Interface	N/A	pDS1160-SN1
	VHDL	Vital-Compliant VHDL Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	pDS1131-SN1

* Lattice Semiconductor pDS Software is required with any of these options.
** The appropriate third-party front end tools and the Lattice Semiconductor pDS+ Fitter are required with any of these options.
*** pDS3302A should be purchased in conjunction with pDS1301-PC2.

Lattice Semiconductor pDS+ Cadence Environment		What You Have or Need from a Third-Party Vendor	What You Need From Lattice Semiconductor	Lattice Semiconductor PC Part Numbers	Lattice Semiconductor Sun Part Numbers
Capture, Simulation, and Fitting		Concept Schematic Editor Verilog-XL Simulator	pDS+ Cadence Fitter (Includes Concept Schematic Library and Verilog-XL Simulation Library)	N/A	pDS2160-SN1
Synthesis, Simulation, and Fitting		Synergy Synthesis Tool Verilog-XL Simulator Verilog-XL Simulator (Optional)	pDS+ Cadence Fitter (Includes Concept Schematic Library and Verilog-XL Simulation Library)	N/A	pDS2160-SN1
			Cadence Synergy Library	N/A	pDS1165-SN1
3000 Family Device Support Option**		N/A	pDS+ Cadence 3000 Upgrade	N/A	pDS2160-3UP/SN1
Simulation Options**	Cadence Verilog	Verilog-XL Simulator	Cadence Library and Interface	N/A	pDS1160-SN1
	Cadence VHDL	Leapfrog Simulator	Verilog and VHDL Simulation Libraries	N/A	pDS1131-SN1

Lattice Semiconductor pDS+ Exemplar Environment		What You Have or Need from a Third-Party Vendor	What You Need From Lattice Semiconductor	Lattice Semiconductor PC Part Numbers	Lattice Semiconductor Sun Part Numbers
VHDL or Verilog-HDL Synthesis and Fitting		Logic Explorer, Antares (Exemplar) Galileo	pDS+ Exemplar Fitter Including Libraries	pDS2110-PC1	pDS2110-SN1
3000 Family Device Support Option**		N/A	pDS+ Exemplar 3000/6000 Upgrade	pDS2110-3UP/PC1	pDS2115-3UP/SN1
Simulation Options**	Viewlogic	N/A	PROsim Simulator Including Libraries	pDS3302-PC2 or pDS3302A-PC2***	N/A
	Viewlogic	PROsim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A
	Viewlogic	PROsim Simulator from Actel or Other Vendor	PROsim Upgrade Including Libraries	pDS1103-PC2	N/A
	Viewlogic	PROsim Simulator from Xilinx	PROsim Upgrade Including Libraries	pDS1104-PC2	N/A
	Viewlogic	Workview PLUS ViewSim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A
	Viewlogic	Powerview ViewSim Simulator	Viewlogic Library and Interface	N/A	pDS1102-SN1
	OrCAD	VST 386+ or Simulation for Windows Simulator	OrCAD Library and Interface	pDS1170-PC1	N/A
	Verilog	OVI-Compliant Verilog Simulator	Verilog Library	pDS1121-PC1	N/A
	Cadence	Cadence Verilog Simulator	Cadence Library and Interface	N/A	pDS1160-SN1
	Vantage	Speedwave VHDL Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	pDS1131-SN1
	VHDL	Vital-Compliant VHDL Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	pDS1131-SN1
	Antares (Model Tech)	System V Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	pDS1131-SN1

** The appropriate third-party front end tools and the Lattice Semiconductor pDS+ Fitter are required with any of these options.
*** pDS3302A should be purchased in conjunction with pDS1301-PC2.

Lattice Semiconductor pDS+ CUPL Environment		What You Have or Need from a Third-Party Vendor	What You Need From Lattice Semiconductor	Lattice Semiconductor PC Part Numbers	Lattice Semiconductor Sun Part Numbers
PLD Compiler and Fitting		CUPL Compiler	pDS+ CUPL Fitter	pDS2190-PC1	N/A
3000 Family Device Support Option**		N/A	pDS+ CUPL 3000 Upgrade	pDS2190-3UP/PC1	N/A
Simulation Options**	Viewlogic	N/A	PROsim Simulator Including Libraries	pDS3302-PC2	N/A
	Viewlogic	PROsim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A
	Viewlogic	PROsim Simulator from Actel or Other Vendor	PROsim Upgrade Including Libraries	pDS1103-PC2	N/A
	Viewlogic	PROsim Simulator from Xilinx	PROsim Upgrade Including Libraries	pDS1104-PC2	N/A
	Viewlogic	Workview PLUS ViewSim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A
	OrCAD	VST 386+ or Simulation for Windows Simulator	OrCAD Library and Interface	pDS1170-PC1	N/A
	Verilog	OVI-Compliant Verilog Simulator	Verilog Library	pDS1131-PC1	N/A
	VHDL	Vital-Compliant VHDL Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	N/A

Lattice Semiconductor pDS+ LOG/iC Environment		What You Have or Need from a Third-Party Vendor	What You Need From Lattice Semiconductor	Lattice Semiconductor PC Part Numbers	Lattice Semiconductor Sun Part Numbers
PLD Compiler and Fitting		LOG/iC PLUS or Perfect Compiler and ODS	pDS+ LOG/iC Fitter	pDS2103-PC1	N/A
3000 Family Device Support Option**		N/A	pDS+ LOG/iC 3000 Upgrade	pDS2103-3UP/PC1	N/A
Simulation Options**	Viewlogic	N/A	PROsim Simulator Including Libraries	pDS3302-PC2	N/A
	Viewlogic	PROsim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A
	Viewlogic	PROsim Simulator from Actel or Other Vendor	PROsim Upgrade Including Libraries	pDS1103-PC2	N/A
	Viewlogic	PROsim Simulator from Xilinx	PROsim Upgrade Including Libraries	pDS1104-PC2	N/A
	Viewlogic	Workview PLUS ViewSim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A
	OrCAD	VST 386+ or Simulation for Windows Simulator	OrCAD Library and Interface	pDS1170-PC1	N/A
	Verilog	OVI-Compliant Verilog Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	N/A
	VHDL	Vital-Compliant VHDL Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	N/A

** The appropriate third-party front end tools and the Lattice Semiconductor pDS+ Fitter are required with any of these options.
*** pDS3302A should be purchased in conjunction with pDS1301-PC2.

Lattice Semiconductor pDS+ Mentor Environment		What You Have or Need from a Third-Party Vendor	What You Need From Lattice Semiconductor	Lattice Semiconductor HP Part Numbers	Lattice Semiconductor Sun Part Numbers
Capture, Simulation, and Fitting		Design Architect Schematic Editor Quicksim II Simulator	pDS+ Mentor Fitter (Includes Design Architect Schematic Library and Quicksim II Simulation Library)	pDS2150-HP1	pDS2150-SN1
Synthesis, Simulation, and Fitting		Autologic Synthesis Tool Quicksim II Simulator	pDS+ Mentor Fitter (Includes Design Architect Schematic Library and Quicksim II Simulation Library)	pDS2150-HP1	pDS2150-SN1
			Mentor Autologic Library	pDS1155-HP1	pDS1155-SN1
3000 Family Device Support Option**		N/A	pDS+ Mentor 3000 Upgrade	pDS2150-3UP/HP1	pDS2150-3UP/SN1
Simulation Options**	Mentor	Quicksim II Simulator	Mentor Library and Interface	pDS1150-HP1	pDS1150-SN1
	Cadence	Verilog-XL Simulator	Cadence Library and Interface	N/A	pDS1160-SN1
	VHDL	Quick VHDL Simulator or System V Simulator from Antares	Verilog and VHDL Simulation Libraries	pDS1131-HP1	pDS1131-SN1

Lattice Semiconductor pDS+ OrCAD Environment		What You Have or Need from a Third-Party Vendor	What You Need From Lattice Semiconductor	Lattice Semiconductor PC Part Numbers	Lattice Semiconductor Sun Part Numbers
Capture, Simulation, and Fitting		SDT 386+ or Capture for Windows Schematic Editor VST386+ Simulation for Windows Simulator	pDS+ OrCAD Fitter (Includes Lattice Semiconductor's OrCAD Schematic Capture Libraries and Simulation Libraries)	pDS2170-PC1	N/A
PLD Compiler, Simulation, and Fitting		PLD 386+ PLD Compiler VST386+ Simulator	pDS+ OrCAD Fitter (Includes Lattice Semiconductor's OrCAD Schematic Capture Libraries and Simulation Libraries)	pDS2170-PC1	N/A
3000 Family Device Support Option**		N/A	pDS+ OrCAD 3000 Upgrade	pDS2170-3UP/PC1	N/A
Simulation Options**	Viewlogic	N/A	PROsim Simulator Including Libraries	pDS3302-PC2	N/A
	Viewlogic	PROsim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A
	Viewlogic	PROsim Simulator from Actel or Other Vendor	PROsim Upgrade Including Libraries	pDS1103-PC2	N/A
	Viewlogic	PROsim Simulator from Xilinx	PROsim Upgrade Including Libraries	pDS1104-PC2	N/A
	Viewlogic	Workview PLUS ViewSim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A
	OrCAD	VST 386+ or Simulation for Windows Simulator	OrCAD Libraries and Interface	pDS1170-PC1	N/A
	Verilog	OVI-Compliant Verilog Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	N/A
	VHDL	Vital-Compliant VHDL Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	N/A

** The appropriate third-party front end tools and the Lattice Semiconductor pDS+ Fitter are required with any of these options.
*** pDS3302A should be purchased in conjunction with pDS1301-PC2.

Lattice Semiconductor pDS+ Synario Environment		What You Have or Need from a Third-Party Vendor	What You Need From Lattice Semiconductor	Lattice Semiconductor PC Part Numbers	Lattice Semiconductor Sun Part Numbers
GAL Compiler (Capture and ABEL Entry)		None	ISP Synario System	ISP-SYN	N/A
Capture, ABEL Entry Functional Simulation and Fitting (Up to 96 Macrocells)		None	ISP Synario System	ISP-SYN	N/A
Capture, ABEL Entry and Fitting		None	ISP Synario Entry	pDS1401-PC1	N/A
			pDS+ Synario Fitter Including Libraries	pDS2120-PC1	N/A
Capture, Simulation and Fitting		Synario Schematic Editor (Syn-Entry)	pDS+ Synario Fitter (Includes Lattice Semiconductor's Synario Device Kit)	pDS2120-PC1	N/A
Capture, Simulation, GAL Compiler, and Fitting		Synario Schematic Editor and ABEL Compiler (Syn-Entry)	pDS+ Synario Fitter (Includes Lattice Semiconductor's Synario Device Kit)	pDS2120-PC1	N/A
3000 Family Device Support Option**		N/A	pDS+ Synario 3000 Upgrade	pDS2120-3UP/PC1	N/A
Simulation Options**	Synario	None	ISP Synario Simulator	pDS3402-PC1	N/A
	Viewlogic	None	PROsim Simulator Including Libraries	pDS3302-PC2	N/A
	Viewlogic	PROsim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A
	Viewlogic	PROsim Simulator from Actel or Other Vendor	PROsim Upgrade Including Libraries	pDS1103-PC2	N/A
	Viewlogic	PROsim Simulator from Xilinx	PROsim Upgrade Including Libraries	pDS1104-PC2	N/A
	Viewlogic	Workview PLUS ViewSim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A
	OrCAD	VST 386+ or Simulation for Windows Simulator	OrCAD Library and Interface	pDS1170-PC1	N/A
	Synario	Synario Verilog Simulator	Synario Device Kit	pDS1120-PC1	N/A
	Verilog	OVI-Compliant VHDL Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	N/A
	VHDL	Vital-Compliant VHDL Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	N/A

** The appropriate third-party front end tools and the Lattice Semiconductor pDS+ Fitter are required with any of these options.
*** pDS3302A should be purchased in conjunction with pDS1301-PC2.

Lattice Semiconductor pDS+ Synopsys Environment		What You Have or Need from a Third-Party Vendor	What You Need From Lattice Semiconductor	Lattice Semiconductor HP Part Numbers	Lattice Semiconductor Sun Part Numbers
Synthesis and Fitting		Design Compiler-Expert Synthesis Tool	pDS+ Synopsys Fitter (Includes Lattice Semiconductor Synopsys Synthesis Libraries)	pDS2140-HP1	pDS2140-SN1
Synthesis and Fitting		Design Compiler-Professional Synthesis Tool	pDS+ Synopsys Fitter (Includes Lattice Semiconductor Synopsys Synthesis Libraries)	pDS2140-HP1	pDS2140-SN1
Synthesis and Fitting		FPGA Compiler Synthesis Tool	pDS+ Synopsys Fitter (Includes Lattice Semiconductor Synopsys Synthesis Libraries)	pDS2140-HP1	pDS2140-SN1
3000 Family Device Support Option**		N/A	pDS+ Synopsys 3000 Upgrade	pDS2140-3UP/HP1	pDS2140-3UP/SN1
Simulation Options**	Synopsys	VSS Simulator	Verilog and VHDL Simulation Libraries	pDS1131-HP1	pDS1131-SN1
	Viewlogic	Powerview ViewSim Simulator	Viewlogic Library and Interface	N/A	pDS1102-SN1
	Mentor	Quicksim II Simulator	Mentor Library and Interface	pDS1150-HP1	pDS1150-SN1
	Cadence	Verilog-XL Simulator	Cadence Library and Interface	N/A	pDS1160-SN1
	Verilog	OVI-Compliant Verilog Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	N/A
	VHDL	Vital-Compliant VHDL Simulator	Verilog and VHDL SImulation Libraries	pDS1131-HP1	pDS1131-SN1

Synopsys Synthesis in Other Third-Party/Lattice Semiconductor pDS+ Environments	What You Have or Need from a Third-Party Vendor	What You Need From Lattice Semiconductor	Lattice Semiconductor HP Part Numbers	Lattice Semiconductor Sun Part Numbers
Synthesis and Fitting in the Cadence Environment	Any Synopsys Synthesis Tool and Cadence Concept Schematic Editor Cadence Concept Schematic Editor	pDS+ Cadence Fitter	N/A	pDS2160-SN1
		Lattice Semiconductor Synopsys Synthesis Libraries	N/A	pDS1140-SN1
Synthesis and Fitting in the Mentor Environment	Any Synopsys Synthesis Tool and Mentor Design Architect Schematic Editor	pDS+ Mentor Fitter	pDS2150-HP1	pDS2150-SN1
		Lattice Semiconductor Synopsys Synthesis Libraries	pDS1140-HP1	pDS1140-SN1
Synthesis and Fitting in the Viewlogic Environment	Any Synopsys Synthesis Tool and Viewlogic ViewDraw Schematic Editor	pDS+ Viewlogic Fitter	N/A	pDS2101-SN1
		Lattice Semiconductor Viewlogic Library and Interface	N/A	pDS1102-SN1
		Lattice Semiconductor Synopsys Synthesis Libraries	N/A	pDS1140-SN1

** The appropriate third-party front end tools and the Lattice Semiconductor pDS+ Fitter are required with any of these options.
*** pDS3302A should be purchased in conjunction with pDS1301-PC2.

Lattice Semiconductor pDS+ Viewlogic Environment		What You Have or Need from a Third-Party Vendor	What You Need From Lattice Semiconductor	Lattice Semiconductor PC Part Numbers	Lattice Semiconductor Sun Part Numbers	Sun Solaris 2 O/S
Capture and Fitting		None	pDS+ Viewlogic Fitter	pDS2101-PC2	N/A	N/A
			PROcapture Schematic Editor	pDS1301-PC2	N/A	N/A
VHDL Synthesis and Fitting		None	pDS+ Viewlogic Fitter	pDS2101-PC2	N/A	N/A
			PROsynthesis Synthesis Tool	pDS3305A-PC2	N/A	N/A
			PROcapture Schematic Editor (Required in Synthesis Flow)	pDS1301-PC2	N/A	N/A
Capture and Fitting		PROcapture or ViewDraw Schematic Editor	pDS+ Viewlogic Fitter	pDS2101-PC2	pDS2101-SN1	pDS2101-SN2
			Viewlogic Library and Interface	pDS1102-PC2	pDS1102-SN1	pDS1102-SN2
VHDL Synthesis and Fitting		PROcapture or ViewDraw Schematic Editor and PROsynthesis or ViewSynthesis Synthesis Tool	pDS+ Viewlogic Fitter	pDS2101-PC2	pDS2101-SN1	pDS2101-SN2
			Viewlogic Synthesis Library	pDS1105-PC2	pDS1105-SN1	pDS1105-SN1
			Viewlogic Library and Interface	pDS1102-PC2	pDS1102-SN1	pDS1102-SN2
PLD Compiler and Fitting		ViewPLD Compiler	pDS+ ABEL Fitter	pDS2102-PC1	pDS2102-SN1	N/A
3000 Family Device Support Option**		N/A	pDS+ Viewlogic 3000 Upgrade	pDS2101-3UP/PC2	pDS2101-3UP/SN1	pDS2101-3UP/SN1
Simulation Options**	Viewlogic	N/A	PROsim Simulator Including Libraries	pDS3302-PC2 or pDS3302A-PC2***	N/A	N/A
	Viewlogic	PROsim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A	N/A
	Viewlogic	PROsim Simulator from Actel or Other Vendor	PROsim Upgrade Including Libraries	pDS1103-PC2	N/A	N/A
	Viewlogic	PROsim Simulator from Xilinx	PROsim Upgrade Including Libraries	pDS1104-PC2	N/A	N/A
	Viewlogic	Workview PLUS ViewSim Simulator	Viewlogic Library and Interface	pDS1102-PC2	N/A	N/A
	Viewlogic	Powerview ViewSim Simulator	Viewlogic Library and Interface	N/A	pDS1102-SN1	pDS1102-SN2
	OrCAD	VST 386+ or Simulation for Windows Simulator	OrCAD Library and Interface	pDS1170-PC1	N/A	N/A
	Verilog	OVI-Compliant Verilog Simulator	Verilog Library	pDS1131-PC1	pDS1131-SN1	N/A
	Cadence	Cadence Verilog Simulator	Cadence Library and Interface	N/A	pDS1160-SN1	N/A
	Vantage	Speedwave VHDL Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	pDS1131-SN1	N/A
	VHDL	Vital-Compliant VHDL Simulator	Verilog and VHDL Simulation Libraries	pDS1131-PC1	pDS1131-SN1	N/A

** The appropriate third-party front end tools and the Lattice Semiconductor pDS+ Fitter are required with any of these options.
*** pDS3302A should be purchased in conjunction with pDS1301-PC2.

GAL Development Support

Lattice Semiconductor Corporation (LSC) recommends the use of qualified programming equipment when programming LSC devices. Lattice Semiconductor works with several programming manufacturers to insure that there is cost effective equipment available. We have approved programmers in each of the following catagories:

- Low Cost GAL Only Programmers
- Mid Range 28-pin Programmers
- Full Universal Programmers
- Production Programming Equipment

LSC conducts a very stringent qualification procedure, which includes a complete evaluation of the programming, verification and load algorithms; verification of critical pulse widths and voltage levels, along with a complete yield analysis. The result is the best programming yields in the industry and a guarantee of 100% programming yields to customers using qualified programming equipment. Below are the third-party programmers which are qualified to program LSC devices.

For a current listing of LSC qualified programmers, please call LSC's Literature Distribution Department (Tel: 503-693-0287; FAX: 503-681-3037).

For compiler support, the following vendors provide design tools which support Lattice Semiconductor devices.

Qualified Programmers

Vendor	Programmer
Data I/O	Autosite
	Unisite
	3900
	2900
	29B
	60A/H
Logical Devices	Allpro 88
	Allpro 40
Stag	System 3000
	ZL30B & ZL30A
	Quasar-U84 & Quasar-U40
System General	TURPRO-1 & TURPRO-1/FX
	SGUP-85A
SMS Microcomputer	Sprint Expert
	Sprint Plus
BP-Microsystems	BP-1200
	PLD-1128 & CP-1128
	PLD-1100
Advin	Pilot-U84 & Pilot-U40
	Pilot-GL & Pilot-GCE

Logic Development Tools

Vendor	Logic Compiler
Accel Technology	Tango PLD
Cadence	PIC Designer Composer
	PIC Designer Concept
Data I/O	ABEL
ISDATA	LOG/iC Classic or LOG/iC 2
Lattice Semiconductor (Data I/O)	ISP Synario System
Logical Devices	CUPL
Mentor Graphics	PLSynthesis II
Minc	PLDesigner-XL
OrCAD	OrCAD PLD 386+
Omation	Schema-PLD
Viewlogic	ViewPLD
Data I/O	Synario

Programmer Development Tools Vendors

Accel Technologies
6825 Flanders Dr.
San Diego, CA 92121
TEL: 1-800-488-0680
TEL: (619) 554-1000
FAX: (619) 554-1019

Advin Systems
1050-L Duane Ave
Sunnyvale, CA 94086
TEL: 1-800-627-2456
TEL: (408) 243-7000
FAX: (408) 736-2503

BP Microsystems
1000 N Post Oak Road
Houston, TX 77055-7237
TEL: 1-800-225-2102
TEL: (713) 688-4600
FAX: (713) 688-0902
BBS: (713) 688-9283

Cadence Design Systems
555 River Oaks Parkway
San Jose, CA 95134
TEL: (408) 943-1234
FAX: (408) 943-0513

Data I/O/Synario Design Automation
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
TEL: 1-800-247-5700
TEL: 1-800-426-1045
TEL: (206) 881-6444
FAX: (206) 882-1043

In Europe, contact:
Data I/O Corp.
TEL: +31 (0) 20-6622866

In Japan, contact:
Data I/O Corp.
TEL: (03) 432-6991

ISDATA GmbH5
Daimlerstraße 51
76185 Karlsruhe
Germany
TEL: 0721-751087
FAX: 0721-752634

Logical Devices
130 Capital Drive
Golden, CO 80401
TEL: 1-800-315-7766
TEL: (303) 279-6868
FAX: (303) 279-6869

Mentor Graphics
8005 S.W. Boeckman Rd.
Wilsonville, OR 97070
TEL: (503) 685-7000
FAX: (503) 685-1204

Minc Incorporated
6755 Earl Dr.
Colorado Springs, CO 80918
TEL: (719) 590-1155
FAX: (719) 590-7330

OrCAD Systems Corp.
9300 S.W. Nimbus Drive
Beaverton, OR 97008
TEL: (503) 671-9500
FAX: (503) 671-9501

SMS Micro Systems
IM Grund 15
D-88239 Wangen
Germany
TEL: (49) 7522-9728-21
FAX: (49) 7522-9728-50

Stag Microsystems
Silver Court
Watchmead
Welwyn Garden City
Herts AL7 1LT
England
TEL: 44-1707-332-148
FAX: 44-1707-371-503

In the U.S., contact:
Devices, Inc.
710 Lakeway, Suite 265
Sunnyvale, CA 94086
TEL: (408) 735-7824
FAX: (408) 735-7828

System General
3 Fl., No. 1, Alley 8, Lane 45
Bao Shing Rd.
Shin Dian
Taipei, Taiwan R.O.C.
TEL: 886-2-9173005
FAX: 886-2-9111283

In the U.S., contact:
System General
1603A South Main Street
Milpitas, CA 95035
TEL: 1-800-967-4776
TEL: (408) 263-6667
FAX: (408) 262-9220
BBS: (408) 262-6438

Viewlogic Systems
293 Boston Post Rd. West
Marlboro, MA 01752
TEL: (508) 480-0881
FAX: (508) 480-0882

ispGDS Compiler Support

Introduction

To simplify the development of ispGDS designs, Lattice Semiconductor offers an ispGDS assembler named "GASM" which processes the input ASCII files to generate the JEDEC compatible fusemap files required for the ispGDS devices. ispGDS assembler software is available at no cost from the Lattice Semiconductor BBS at 503-693-0215 under GDSPKG.ZIP file. This software is also available on diskette by calling the Lattice Semiconductor Hotline at 1-800-327-8425 (FASTGAL) For design engineers familiar with standard third-party compiler software packages, ABEL from Data I/O and CUPL from Logical Devices also support all ispGDS devices.

Using the ispGDS Compiler

The compiler will accept an ASCII text file containing the ispGDS programming instructions, and will create JEDEC and .DOC files. Once a JEDEC file has been created, the ispGDS device can be programmed by either downloading the JEDEC file to a programmer, or by using the ispGDS Download utility to program the device using the parallel port of an IBM compatible PC.

Compiler Syntax

The basic compiler syntax supports inserting comments, title, device type, pin assignments and input/output assignments. The ispGDS compiler source file comment lines are denoted with quote marks at the beginning of the comment lines. The title is defined with the key word "title = ". Any text following the "title =" key word that are within single quotes are defined to be the title of the design. Similarly, the device type is defined by the key word "device =" followed by the three valid device types -- ispgds22, ispgds18, ispgds14. The compiler syntax also allows the user to assign pin names by typing in a 10 character pin name followed by at least a single space, the "pin" key word and the pin number. This pin assignment is optional since the compiler syntax allows the user to use the "pin" key word and the pin number directly in the input/output assignments.

The output pins are assigned on the left side of the equation and the input pins are assigned on the right side of the equation. To assign an output pin to either high or low, simply assign "H" or "L" respectively on the right side of the equation. If you need to assign an input pin to multiple output pins, use one line for each assignment, as shown in the following example. In the example below, pin 28 is an input that is routed to three outputs — pin 1, pin 2 and pin 3. Further, each output's polarity can be individually defined. The example shows pin 3 as an active low polarity whereas pin 1 and pin 2 are defined to be active high polarity. An example source file is appended at the end of this document.

```
 pin 1 = pin 28
 pin 2 = pin 28
!pin 3 = pin 28
```

Assembling a File

To use the assembler, create an ASCII ispGDS source file, then invoke the assembler from the DOS command line. For example: `gasm <test.gds>`

where test.gds is the name of the ispGDS source file. GASM will create a JEDEC file with the same base name, and a .JED extension, like "test.jed," and a doc file with a .DOC extension, like "test.doc."

Programming the ispGDS

You can either program the ispGDS using a JEDEC file output from the GASM assembler, or by using the GDS_PROG routines included in the GDSPKG software package. To program the ispGDS using a programmer, follow these steps:

1. Create an ASCII ispGDS source file
2. Assemble the ispGDS file using the ispGDS assembler (GASM).
3. Download the JEDEC file created by the assembler to the programmer and program the device. The JEDEC file will have the same name as your ispGDS source file, but will have a .JED extension (for example, "test.jed").

Alternatively, you may want to program the ispGDS devices either through the parallel port of an IBM compatible PC, or through some custom hardware configuration. The routines included in the ispGDS compiler software package are configured to use the PC parallel port for programming. If you want to use a custom hardware configuration, read through the comments in GDS_PROG for information on which routines need to be modified. If you are programming using the PC, you will

need an ispDOWNLOAD™ Cable and ISP programming interface signals on the circuit board which will plug into the printer port on your PC.

To program using the parallel port of the PC, follow these steps:

1. Create an ASCII ispGDS source file
2. Assemble the ispGDS file using the ispGDS assembler (GASM)
3. Convert the JEDEC file to ispSTREAM format by running JEDTOISP. See the documentation on JEDTOISP for further information.
4. Run GDS _PROG to program the device using the PC parallel port.

ispGDS Source Format

The following text is an example of an ispGDS source file.

```
"This is a comment (line begins with quote mark)
title = 'DIP SWITCH REPLACEMENT CONFIGURATION'

" the ispgds device type (ispgds22, ispgds18, ispgds14)
device = ispgds22

" pin names are defined as follows

pin_name  pin 28

" pin 1 is an output connected to pin 28
pin 1 = pin_name
pin 2 = pin 27

" pin 3 is another output connected to pin 28

pin 3 = pin 28

" pin 5 is always high
pin 5 = h

"pin 6 is always low
pin 6 = l
pin 8 = pin 22

"! defines the inverted output for pin 9
!pin 9 = pin 20

pin 10 = pin 19
pin 12 = pin 17
pin 13 = pin 16
pin 14 = pin 15
```

Notes

If you get an error regarding "pin 0", you may have duplicated an output pin assignment (by assigning different input signals to the same output pin). Refer to the line number in the assembler error message to locate the source of the problem.

Section 7

Quality Assurance Program

Introduction

Lattice Semiconductor Corporation (LSC) views quality assurance as a corporate responsibility and an integral part of all operational activities. LSC's Quality Assurance organization is independent from Manufacturing and has direct access to top management, assuring sufficient authority is afforded to quality issues.

LSC's quality program is in full compliance to the quality assurance requirements of MIL-I-38535B Appendix C and all inspection system requirements of MIL-I-45208. LSC is also fully certified to the ISO 9001 standard.

Reliability

All new products, processes and vendors must pass predefined evaluations before receiving initial qualification release. Major changes to products, processes or vendors require additional qualificaton before implementation. To assure continuing conformance to reliability goals, an ongoing monitor program is maintained on all products.

In-Process Control

Qualified product must be manufactured under strict quality controls that start with regulated procurement and documented inspection plans for all incoming materials. Sample testing and in-line monitoring as well as statistical process control charts provide constant feedback at each critical step of the manufacturing process.

Calibration

All equipment involved in determining product conformance to specifications through inspection, measurement or testing must be of the required accuracy. Equipment is calibrated and maintained on a defined interval against a nationally recognized standard. In addition, equipment must exhibit a suitable indicator showing calibration status as well as safeguards to disallow unauthorized adjustments.

Training

Key manufacturing personnel must complete a formal training program and obtain certification for each operation before they are allowed to perform activities affecting quality. Methods and records identifying the type and extent of training are maintained and recertification required on a yearly basis.

Subcontractor Control

All subcontracted manufacturing operations must be performed by sources exhibiting a quality program commensurate to that of Lattice Semiconductor. Key suppliers are audited at least once a year to monitor their compliance to LSC's quality initiatives and goals. Incoming inspection is performed to provide feedback and continuous improvement of subcontractor performance with the main objective being to control quality at the source. Communications and in-line data are continuously exchanged to allow real-time monitoring of subcontractor manufacturing operations.

Document Control

Every product and process must have adequate written documentation released and available at the point of use before production begins. All information related to the definition, manufacturing, testing and support of LSC products or services shall be maintained and controlled. Initial release as well as subsequent changes must be properly reviewed and approved before implemented.

Nonconforming Material

Material found to be nonconforming to specified requirements is identified, segregated, analyzed and dispositioned per documented procedures. Records are maintained denoting the nature of the discrepancy as well as the final disposition. All dispositions involve the applicable engineering section and Quality Assurance. Where applicable, the root cause of the discrepancy will be identified and a corrective action implemented using the CAR (Corrective Action Request) form.

Failure Analysis

Failure modes discovered during qualification testing, inspections, customer returns or in-process screening are processed through LSC's Failure Analysis group to determine the cause or relevancy of the failure. Verified failure modes are documented and corrective action initiated as required to eliminate the root cause.

Corrective/Preventive Action

All operational functions utilize a documented corrective action system coordinated, recorded and monitored by Quality Assurance. The system is designed to provide for proactive problem identification and resolution in a timely manner. Inputs include vendor, internal and customer related problems. Emphasis is placed on effective elimination of the root cause to prevent recurrence of the problem.

Management is responsible for ensuring that employees have sufficiently well defined responsibilities, authority and organizational freedom to identify potential quality related problems as well as initiate and implement solutions.

Self Audit

Internal self audits of the entire quality and delivery system are performed per written procedures and to a predefined schedule. The functional audits evaluate actual method to written procedure. The results of these audits are documented on a checklist and any discrepancies are brought to the attention of personnel responsible for the audited area. Deficiencies require corrective actions must be initiated and subsequently verified as to deployment and effectiveness. A periodic review of these functional audit results and corrective actions is performed by Quality Assurance.

Procurement

All direct materials and services affecting quality or reliability of end product must be purchased from qualified sources. Selection of these critical suppliers is based upon one of more of the following: quality system audits, product qualification testing, correlation studies, incoming inspection and demonstrated ability. A qualified supplier list is maintained by Quality Assurance and used by Purchasing to control procurement. Each purchase order must specify the applicable controlling requirements for all such direct materials or services.

Qualification Program

Introduction

Lattice Semiconductor Corporation (LSC) has an intensive qualification program for examining and testing new products, processes, and vendors in order to insure the highest levels of quality. LSC's Quality and Reliability Group is responsible for defining and implementing this qualification program.

The following table outlines the steps which must be performed before a new product, package or process is released. The requirements listed below are general guidelines. Detailed information on Lattice's qualification process is available to customers upon request.

Qualification Requirements

Test	Duration		
	New Product	New Wafer Process	New Package
125° C Operating Lifetest (5.25V)	1,000 Hours	1,000 Hours	1,000 Hours[1]
150° C Biased Retention Bake (5.25V)	1,000 Hours	1,000 Hours	1,000 Hours[1]
Endurance Cycling	10,000 Cycles	10,000 Cycles	N/A
ESD (CDM, HBM, MM)	End of Test	End of Test	N/A
Latch-Up Immunity	End of Test	End of Test	N/A
Temperature Cycling (-65 to 150° C)	1,000 Cycles	1,000 Cycles	1,000 Cycles
Biased 85/85 (5V)	N/A	1,000 Hours	1,000 Hours
Autoclave (121° C, 15psig)	N/A	168 Hours	168 Hours
Solderability	N/A	N/A	End of Test
Physical Dimensions	N/A	N/A	End of Test

1. Required for new assembly technologies only.

Qualification Program

Reliability Monitor Program

The Reliability Monitor Program provides for a periodic reliability monitor of LSC products. The program assures that all Lattice products comply on a continuing basis with established reliability and quality levels.

The Reliability Monitor Program is designed to monitor all fab and assembly facilities as well as each process technology in production. A summary of the program test and sampling plan is shown below.

Short Term Process Monitor (Bi-Weekly)

Test	# of Samples	Duration
125° C Operating Lifetest (6.50V)	70	160 Hours
150° C Biased Retention Bake (5.25V)	70	160 Hours
Autoclave (121° C, 15psig)	35	160 Hours
Temperature Cycling (-65 to 150° C)	35	250 Cycles

Long Term Process Monitor (Monthly)

Test	# of Samples	Duration
125° C Operating Lifetest (6.00V)	100	1000 Hours
150° C Biased Retention Bake (5.25V)	150	1000 Hours

Ongoing Package Monitor (Monthly)

Test	# of Samples	Duration
Temperature Cycling (-65 to 150° C)	50	1000 Cycles
85° C / 85% RH	75	1000 Hours

E^2CMOS Testability Improves Quality

Introduction

The inherent testability of Lattice Semiconductor's E^2CMOS PLDs significantly improves their quality and reliability. By using electrically erasable EEPROM technology to produce GAL, pLSI and ispLSI devices, Lattice Semiconductor Corporation (LSC) is able to perform 100% AC/DC, functional, and parametric testing of every single device. In order to achieve the highest quality levels, LSC programs and tests each device repeatedly throughout the manufacturing process.

Actual Test vs. Simulated Test

Why is "actual test" so significant? PLDs, unlike most other semiconductor devices, have a programmable element that determines the final device functionality and AC/DC performance. These programmable elements can be fabricated from metal link fuses, programmable diodes or transistors, volatile static RAM cells, UV EPROM cells or electrically erasable EEPROM cells. Each of these technologies carries a different variability of programming success and a variance in the impact of the programming success on the performance and reliability of the device.

The most common programmable elements are the metal fuse, EPROM cell and EEPROM cell. Of these element types, only the EEPROM cell can be thoroughly tested by the manufacturer prior to shipment to an end user OEM.

EEPROM Allows Actual Test

Each of the technologies identified above can be programmed. In this manner they are all the same. The differences become apparent when the erase times are analyzed. Metal link and One-Time Programmable (OTP) devices cannot be erased. UV EPROM devices can be erased, however the time required is 20-30 minutes (in an expensive windowed package). EEPROM devices, on the other hand, offer instant erasability on the order of 50 ms (thousandth's of a second). The advantage of this instant erase for manufacturing test is significant. Instant erase allows instant re-patterning for additional testing.

EEPROM technology has been used for PLD manufacturing by LSC for more than a decade. LSC refers to their high performance EEPROM technology as E^2CMOS technology. Extensive reliability studies of the technology have been performed with industry-wide acceptance, including the military.

Other Methods Are Imprecise

All PLD devices must be tested to some degree to validate functionality and performance. Technologies that are not erasable or require lengthy erase times severely constrain the test flexibility. Since the normal "user" programmable elements cannot be programmed during manufacture (all elements must be available for end-user programming) the manufacturers of one-time programmable PLDs resort to using simulated and correlated performance of test rows, test columns and phantom or dummy-test arrays. At best, this is a statistical measure of the actual device performance. One need only look at the "normal" programming yield fallout of 0.5 to 3% or the "acceptable" post-programming test vector and board yield fallout of 0.5 to 2% to know that this correlation is weak. The quality systems of today are measuring defects in parts per million (PPM). A six sigma program requires less than 3.4 PPM, four orders of magnitude less than that achievable with non-testable PLDs.

Actual Matrix Patterning

The unique capability of E^2CMOS devices to be instantly electrically erased allows these devices to be patterned multiple times during LSC's manufacturing test. Normal array cells in the programmable matrix are patterned, erased and tested again and again. The test rows or columns, phantom arrays, etc., that are used with other technologies are not necessary with E^2CMOS devices. Programmability of every cell is checked dozens of times.

Historically, the checking of a successful programming operation consisted of no more than a pass/fail verification step. This digital, go/no go check is not adequate to assure that the cell is programmed properly with sufficient margin to guarantee long-term reliable performance of the device. LSC E^2CMOS devices are processed through a proprietary cell verification step that consists of an analog measure (to millivolt accuracy) of the actual cell threshold. This capability is used for extensive reliability and quality measurements and testing.

Worst Case AC/DC Testing

A PLD does not have a defined function until the engineer patterns the device with his custom pattern. The manufacturer, when considering the testing of a PLD, must consider the hundreds of different architecture and functional variations that can be created by the end user. Each configuration of architecture brings on a different set of worst case pattern and stimulus conditions. Quick application of a series of worst case patterns that cover

all of the permutations of input combinations, array load and switching, and output configuration is required.

E²CMOS devices offer instant erasability to address this reconfiguration and test problem. Testing each additional worst case configuration takes fractions of a second, allowing multiple patterns to be checked to assure performance to rated speeds. The final result is a device with defects reduced from PPH (parts per hundred) to PPM (parts per million).

ISO 9000 Program

Introduction

Lattice Semiconductor Corporation (LSC) is the first major PLD manufacturer to complete ISO 9000 registration. LSC Quality Systems have been certified, and the company is registered to the ISO 9000 standard. LSC certification is for ISO 9001, the most comprehensive of the various ISO 9000 levels, covering the design, manufacturing, sales, and service functions.

ISO 9000 Certification

Certification to the ISO 9000 standard provides a recognized and standardized basis for the continued development of the quality and reliability of LSC products. This certification assures LSC's customers that its Quality Systems are well organized and embody a "Quality First" philosophy. It also reaffirms LSC's promise to provide its customers with the highest quality and most reliable products in the industry.

What is ISO 9000?

The ISO 9000 series is an international version of British Standard BS 5750, intended to define the quality management systems for a wide range of an organization's activities. The standard was initiated by the British Standards Institution, which over the last 80 years has certified over 9,000 Quality Systems. Today, both the CEN (European Committee for Standardization), which is commissioned to coordinate quality standards in Europe and remove potential trade restrictions within and outside the European Community, and the USA Standard ANSI/ASQC have adopted the ISO 9000 series.

Four quality standards make up the ISO 9000 series: ISO 9004, ISO 9003, ISO 9002, and ISO 9001. ISO 9004 is an informational document containing guidelines for Quality Management and Quality Systems. ISO 9003 guarantees quality in a product's final testing and inspection. ISO 9002 confirms quality in the production and installation of a product. ISO 9001 assures quality in a product's design, development, production, and installation. ISO 9001 is composed of 20 system sections, including the ISO 9002 and ISO 9003 subsets. Lattice Semiconductor is certified to the most comprehensive quality standard of the series, ISO 9001, and registered with the American Society for Quality Control's Registration Accreditation Board.

Lattice Semiconductor: First PLD Supplier to Achieve ISO 9000 Certification

Notes

Section 8

ISP™ Architecture and Programming

Introduction

This section describes how to program Lattice Semiconductor Corporation's (LSC) ISP devices once the JEDEC standard fuse map file has been generated. It is divided into two subsections. The first subsection "Getting Started Fast" is intended to give the reader enough ISP hardware information to easily implement LSC's ISP solutions using the LSC ISP tools, which are briefly described at the end of this section. The second subsection "ISP Expert" gives more details on low-level, device-specific programming algorithms. Since these algorithms are transparently handled by LSC's programming tools, the second subsection is intended for those readers who want a thorough understanding of the programming procedures, which would be required for any custom implementation of ISP.

Subsection I — Getting Started Fast

ISP Interface
ISP State Machine Operation
ISP Device Programming Configurations
Hardware Considerations
Hardware Programming Tools
ISP Programming Software
Programming Times
User Electronic Signature (UES)

Subsection II — ISP Expert

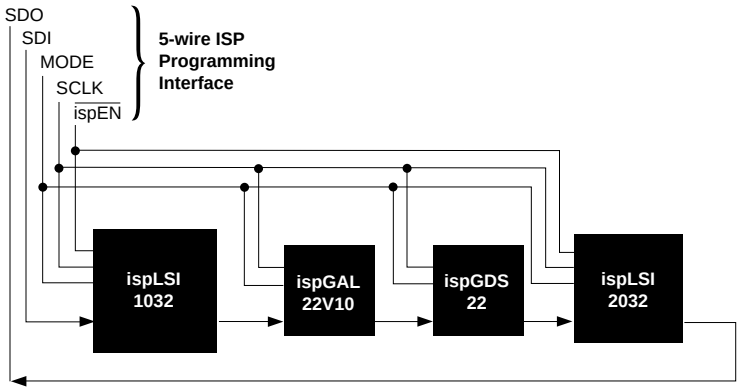
ispLSI Programming Details
Boundary Scan (ispLSI 3000 and 6000 Families)
ispGDS Programming Details
ispGAL Programming Details
ISP Daisy Chain Details

In-System Programming (ISP) Interface

Programming LSC's ispLSI, ispGAL, and ispGDS devices is based on a simple serial ISP programming interface (Figure 1). The basic elements of the ISP programming interface are the mode control (MODE), serial data in (SDI), serial data out (SDO), and serial clock (SCLK) inputs, as well as a three-state programming control state machine integrated into each ISP device. LSC's ISP devices utilize nonvolatile E^2CMOS technology and require only five-volt, TTL-level programming signals from the ISP interface for in-system programming. The internal three-state state machine, which determines whether the device is in the normal operation state or in the programming states, is controlled by the four ISP programming pins. MODE and SDI furnish control inputs to the state machine, SDI and SDO make up the programming data inputs and outputs to and from an internal shift register, and SCLK provides the clock. ispLSI devices use a fifth programming pin, $\overline{\text{ispEN}}$, to multiplex the functions of the SDI, SDO, SCLK, and MODE pins between ISP functions during programming and user-defined logic functions during normal PLD operation.

The internal state machine controls the sequence of programming operations such as identifying the ISP device, shifting in the appropriate data and commands, controlling the internal programming pulse widths to ensure proper programming voltage margins, and erasing the device. Programming consists of shifting the logic implementation stored in a JEDEC file into the device serially through the SDI pin along with the appropriate address and commands, programming the data into the

Figure 1. Multiple ISP Device Programming Interface



E^2CMOS logic elements, and shifting the data from the logic array out through the SDO pin for verification.

ISP Programming Pins

The programming pins used to program Lattice devices are each described in detail in this section. Figure 2 shows the ispLSI 1032 84-Pin PLCC device pinout.

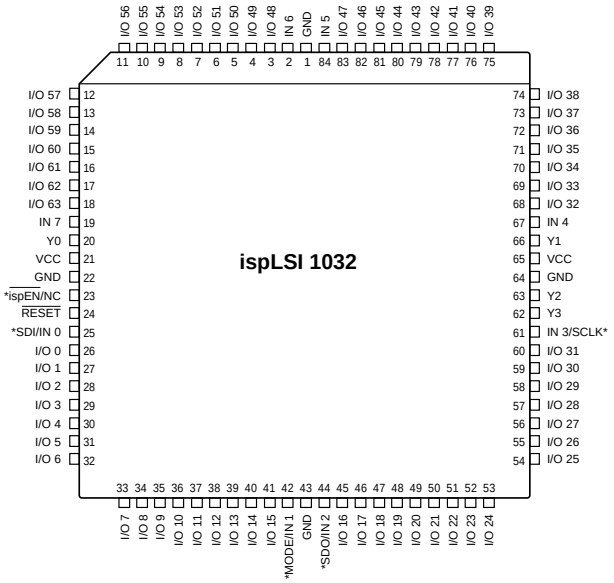
The Serial Data In (SDI) pin performs two different functions. First, it acts as the data input to the serial shift register built inside each ISP device. Second, it functions as one of the two control pins for the programming state machine. Because of this dual role, the function of SDI is controlled by the MODE pin. When MODE is low, SDI becomes the serial input to the shift register, and when MODE is high, SDI becomes a control signal for the programming state machine. Internally, the SDI signal is multiplexed to various shift registers in the device. The different shift instructions of the state machine determine which of these shift registers receives input from SDI.

The MODE signal, combined with the SDI signal, controls the programming state machine, as described in the "ISP State Machine Operation" section which follows.

The Serial Clock (SCLK) pin provides the serial shift register with a clock. SCLK is used to clock the internal serial shift registers and clock the ISP state machine between states. State changes and shifting data in are performed on low-to-high transitions. When MODE is high, SCLK controls the programming state machine, and when MODE is low, SCLK acts as a shift register clock to shift data in or out or to start an operation. When shifting data out, the data is available and valid on SDO only after a subsequent high-to-low transition of SCLK.

The Serial Data Out (SDO) pin is connected to the output of the internal serial shift registers. As previously stated, the selection of which shift register to output is determined by the ISP state machine's shift instruction. When

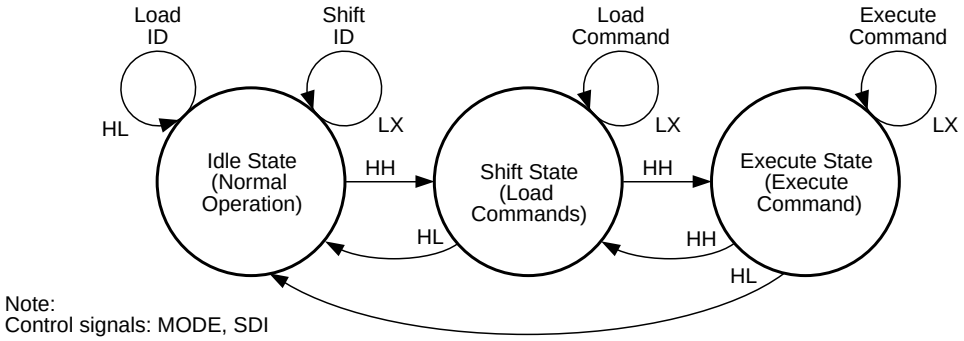
Figure 2. ispLSI 1032 84-Pin PLCC Pinout Diagram



MODE is driven high, SDO connects directly to SDI, bypassing the device's shift registers.

The $\overline{\text{ispEN}}$ pin, only utilized on the ispLSI devices, determines which mode the device is in, namely *Edit Mode* (ISP programming mode) or *Normal Mode* (normal device operation mode). When $\overline{\text{ispEN}}$ is driven low on an ispLSI device, the device I/O pins are put into a high impedance state (by internal active pull-up resistors equivalent to 100KΩ) and the device enters Edit Mode.

Figure 3. Programming State Machine



ISP State Machine Operation

The programming state machine controls which mode the device is in, and provides the means to read and write data to the device (Figure 3). Four ISP programming pins are used to load and unload data, and to control the state machine. The three states defined in the state machine diagram are the IDLE State, SHIFT State, and EXECUTE State. Instruction codes, which are shifted into the device in the SHIFT state, control which instruction is to be executed in the EXECUTE state. In the SHIFT and EXECUTE states, all the I/O pins are 3-stated. To transition between states, MODE is held high, SDI is set to the appropriate level, and SCLK is clocked. The ispGAL22V10 and ispGDS devices, unlike ispLSI devices which employ an $\overline{\text{ispEN}}$ input pin, rely on the state machine to put the device I/O pins in a high impedance state. The IDLE state puts the ispGAL and ispGDS devices into Normal Mode, and the remaining two states put the devices into ISP programming mode, which places the device I/O pins in the high impedance state.

Idle/ID State

The Idle/ID state is the first state activated when the device enters the Edit Mode (ISP programming mode). The state machine is in the Idle/ID state when the device is idle, in the Edit Mode, or when the user needs to read the device identification (each ISP device type is assigned a unique identification code. See the "ISP Expert" section). The eight-bit device identification is loaded into the shift register by driving MODE high, SDI low, and clocking the ISP state machine with SCLK. Once the ID is loaded, it is read out serially by driving MODE low. Notice that when the device ID is read serially, SDI can either be high or low (called "don't care") and the state machine needs only seven clocks to read out eight bits of device ID. The default state for the control signals is MODE high and SDI low. State transition to the Command Shift State occurs when both MODE and SDI are high while the ISP state machine gets a clock transition. As with most shift registers, the Least Significant Bit (LSB) of the ID gets shifted out from SDO first.

Command Shift State

This state is strictly used for shifting instructions into the state machine. The entire instruction sets for the ispLSI, ispGDS, and ispGAL devices are listed in the "ISP Expert" section. When MODE is low and SDI is "don't care" in the Command Shift State, SCLK shifts the instruction into the state machine. Once the instruction is shifted into the state machine, the state machine must transition to the Execute State to execute the instruction. Driving both MODE and SDI high and applying the clock transfers the state machine from the Command Shift State to the Execute State. If needed, the state machine can move from the Command Shift State to the Idle/ID State by driving MODE high and SDI low.

Execute State

In the Execute State, the state machine executes instructions that are loaded into the device in the Command Shift State. For some instructions, the state machine requires more than one clock to execute the command. An example of this multiple clock requirement is the address or data shift instruction. The number of clock pulses required for these instructions depends on the device shift register sizes. When executing instructions such as Program, Verify, or Bulk Erase, the necessary timing requirements must be followed to make sure that the commands are executed properly. For specific timing information refer to the appropriate data sheets.

To execute a command, MODE is driven low and SDI is "don't care." For multiple clock instructions, the control signals must remain in the same state throughout the duration of the execution. MODE high and SDI high will take the state machine back to the Command Shift State and MODE high and SDI low will take the state machine to the Idle/ID State.

ISP Device Programming Configurations

Serial Daisy Chain

Advantages

One of the main advantages of daisy chained ISP programming is the simplified hardware interface. The number of ISP devices that can be connected to the same serial interface is limited only by the signal drive capability of the ISP programming control logic. One serial daisy chain is capable of providing the necessary programming interface, minimizing the hardware overhead for in-system programming. Software controls generated from PCs, microcontrollers, and test equipment can program and reconfigure ISP devices during various board-level design, test, and manufacturing stages.

Programming Configuration

As shown previously in Figure 1, all the MODE, SCLK, and $\overline{\text{ispEN}}$ (if using ispLSI devices) pins of the ISP devices are connected to the ISP interface, and the first device's SDO is connected to the second device's SDI, and each following SDO to the SDI of the next ISP device. This configuration allows a large string of ISP devices to be programmed, in-system, in a serial daisy chain.

Parallel

For low-density ISP devices daisy chain programming is the most common configuration, but for high-density devices, with multiplexed programming and logic pins controlled by $\overline{\text{ispEN}}$, other programming configurations are also common. ISP devices can be programmed in one of two parallel configurations. The first parallel configuration, called Dedicated ISP Pins, dedicates all ISP programming pins to programming. The second parallel configuration, called Parallel Multiplex below, is mainly used for ispLSI devices. In this configuration, the functions of the ISP programming pins can be multiplexed between acting as programming pins and acting as inputs for normal logic functions.

Dedicated ISP Pins

Figure 4 illustrates one configuration for programming multiple ISP devices, where the ISP programming pins (MODE, SDI, SDO, and SCLK) are dedicated to programming functions. Although this scheme precludes the use of the ISP programming control signal pins as separate dedicated inputs for system logic functions on ispLSI devices, it is the easiest to implement. Each of the four programming control signal pins in each ISP device is connected (i.e. SDI of the ispLSI 1032 is connected to SDI of the ispLSI 1048 and SDI of the ispLSI 1016; MODE of the ispLSI 1032 is connected to MODE of the ispLSI 1048 and MODE of the ispLSI 1016; etc.). With this scheme, the $\overline{\text{ispEN}}$ signal for each ispLSI device is enabled ($\overline{\text{ispEN}}$ low) separately, and one device is placed in Edit (ISP programming) Mode at a time. With one device in Edit Mode, the other devices will be in Normal Mode and can continue to perform normal system logic functions. $\overline{\text{ispEN}}$ is the only programming interface signal that cannot be used for general logic functions.

Parallel Multiplex

Figure 5 illustrates a multiplexing scheme which allows the user to control the ISP programming through multiple independent $\overline{\text{ispEN}}$ signals for the ispLSI devices. The multiple $\overline{\text{ispEN}}$ signals not only control the $\overline{\text{ispEN}}$ inputs of the ispLSI devices, but also act as the control signals for multiplexing the functional and ISP programming signals. This scheme differs from the previous one in that the ISP programming signals are not dedicated to programming. Instead, the ISP programming signals MODE, SDI and SCLK function as inputs for both normal functional mode and the ISP programming mode. SDO, however, functions as an input in normal functional mode and as an output in ISP programming mode. Figure 5 also shows the difference in controlling these different programming signals. Please note that when multiplexing the programming interface signals, the input driving the SDO pin must be 3-stated during programming to avoid signal contention. As previously stated, the ISP programming pins on the ispGAL and ispGDS devices are dedicated to ISP programming, so this configuration is not utilized often for the ispGAL and ispGDS devices. The concept can be modified to multiplex the MODE pin instead of the $\overline{\text{ispEN}}$ pin and becomes useful in some ispGAL and ispGDS applications.

Figure 4. Dedicated ISP Pins Configuration

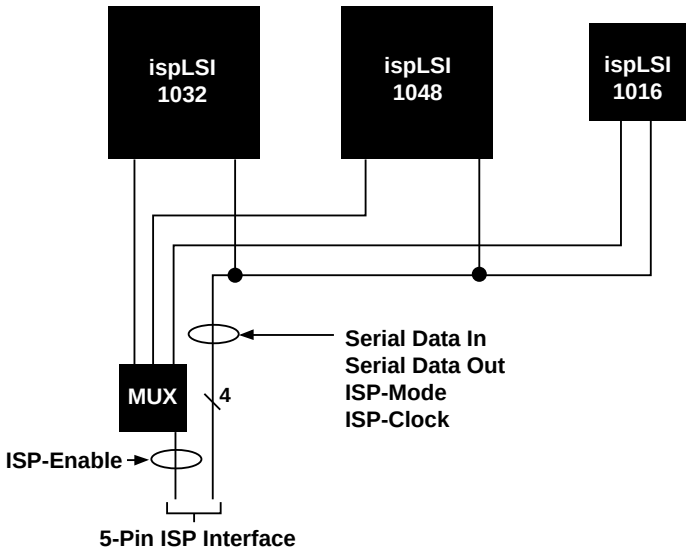
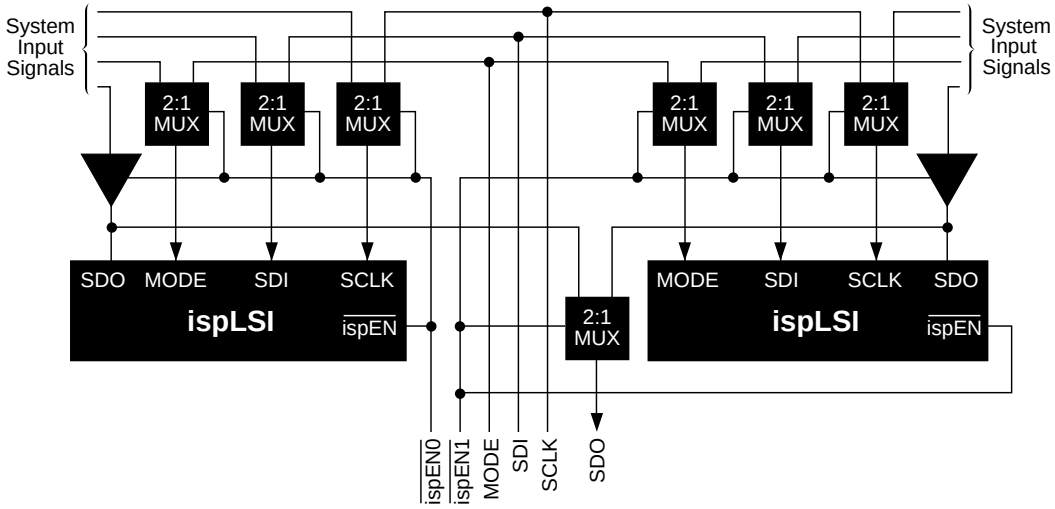


Figure 5. Parallel Multiplex Configuration



Hardware Considerations

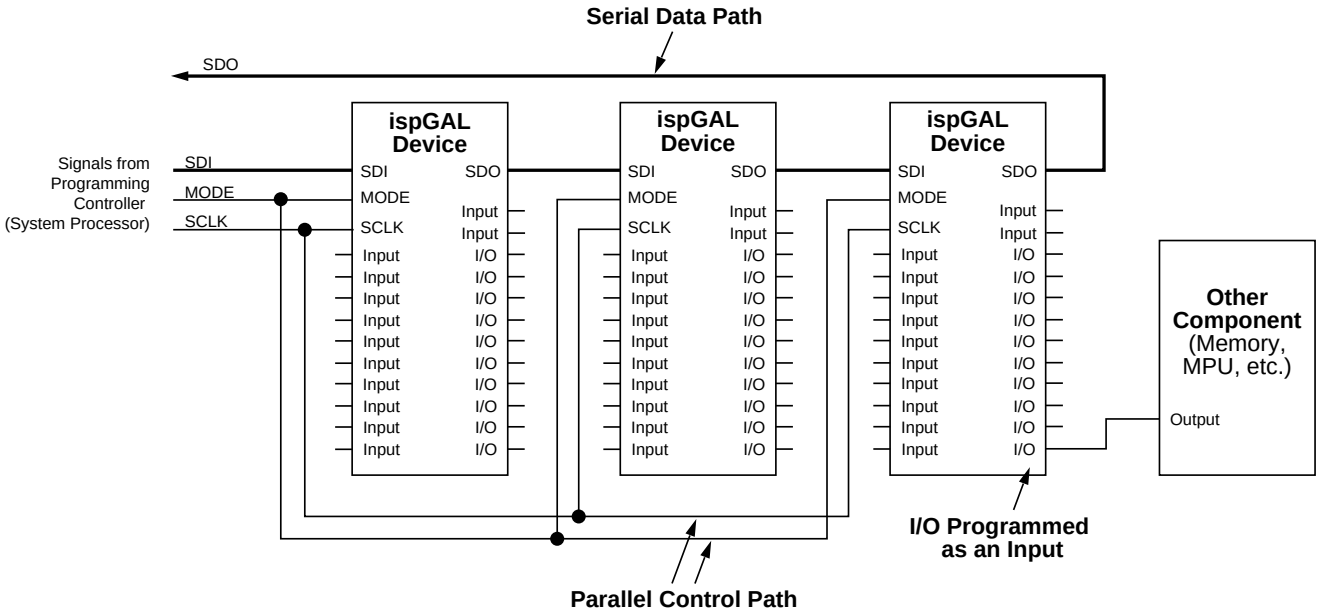
Lattice Semiconductor's In-System Programmable (ISP) technology makes the use of Programmable Logic incredibly simple. Using ISP, multiple devices can be programmed using a single serial daisy chain programming loop. However, as with any high performance semiconductor component, systems must be designed to insure good signal integrity without signal conflicts between components. By doing so, reliable operation can be obtained over a wide range of operating conditions. This section discusses some basic programming hardware issues which should be considered when implementing a system using ISP.

All ISP programming specifications such as the programming cycle and data retention are guaranteed when programming ISP devices over the commercial temperature range (0 to 70° C). It is critical that the programming and bulk erase pulse width specifications are met by the programming platform to insure proper in-system programming. LSC's ISP Daisy Chain Download and ispCODE software insures that these specifications are met when using a PC programming platform.

When using the ispDOWNLOAD cable in a daisy chained configuration, LSC recommends using a maximum of eight ISP devices in a single chain. This is to insure proper programming signal integrity (pulse width, shape, etc.) at the ISP devices. The eight devices can be any combination of ispLSI, ispGAL, and ispGDS devices arranged in any order. The recommended number of devices is based on a typical system board environment with proper signal terminations and typical trace lengths. The actual number of devices that can be programmed in a serial chain may vary according to the system board environment. When using more than eight devices, additional buffering of the ISP programming signals is recommended. Alternatively, multiple programming loops can be employed which are electrically isolated from one another.

I/O pins on ISP devices may be defined as inputs once the devices are programmed. As a result, they typically will be driven by the outputs of other components once mounted on the board. Care must be taken to ensure that I/O pins are not enabled prematurely during programming. To do so when the device is partially programmed can cause contention with other signal drivers since I/O pins destined to be configured as inputs may not be 3-stated yet. This conflict can cause improper device programming and potential damage (Figure 6).

Figure 6. ISP Serial Daisy Chain



All ISP devices are shipped from Lattice Semiconductor with a fuse pattern that will put all I/O pins in the high impedance state prior to programming. The output 3-state is controlled by the $\overline{\text{ispEN}}$ signal on the ispLSI devices. For the ispGAL and ispGDS devices, the output 3-state is controlled by the programming state machine (Shift and Execute states 3-state the devices). When implementing custom ISP programming code, it is important for the ispGAL and ispGDS that the ISP state machine be kept within the Shift and Execute states until the completion of programming. This procedure keeps the partially programmed device or devices from conflicting with other components on the board.

ISP programming signal default states must be maintained during normal device operation. The $\overline{\text{ispEN}}$ pin on the ispLSI devices has an internal pull-up to place the devices in normal functional mode when the pin is not driven externally. The ispGAL22V10B and ispGDS devices' MODE or SDI signals must be tied low through a 1.2KΩ pull-down resistor during normal functional mode. It is not acceptable to let these pins float during normal operation. However, the ispGAL22V10C devices provide an internal pull-down on SDI to maintain socket compatibility with the standard 22V10 in the PLCC package. In addition, it is recommended that the ispDOWNLOAD cable have its $\overline{\text{ispEN}}$ signal tied to a decoupling capacitor (.01μF) to ground on the system board.

Hardware Programming Tools

isp Engineering Kit

Lattice Semiconductor provides a PC-based (Model 100) isp Engineering Kit. The isp Engineering Kit functions as a stand-alone device programmer for prototyping.

isp Engineering Kit Model 100

The isp Engineering Kit Model 100 provides designers with a quick and inexpensive means of evaluating and prototyping new designs using LSC ispLSI devices. This kit is designed for engineering purposes only and is not intended for production use. The kit programs devices from the parallel printer port of a host PC using the LSC pDS or pDS+ PC-based designs tools. By connecting a system cable (included) from the host PC to the isp Engineering Kit, or connecting from the host PC to the target device on the system board, a JEDEC file can be easily downloaded into the ispLSI device(s) (Figure 7).

ispDOWNLOAD™ Cable

The ispDOWNLOAD Cable product is designed to facilitate in-system programming of all LSC ISP devices on a printed circuit board directly from the parallel port of a PC. After completion of the logic design and creation of a JEDEC file by a logic compiler such as the pDS, pDS+ Fitter or ispGDS Compiler software, LSC's ISP Daisy Chain Download Software programs devices on the end-product PC board by generating programming signals directly from the parallel port of a PC which then pass through the ispDOWNLOAD Cable to the device. With this cable and a connector on the PC board, no additional components are required to program a device (Figure 8).

Figure 7. ispEngineering Kit Model 100

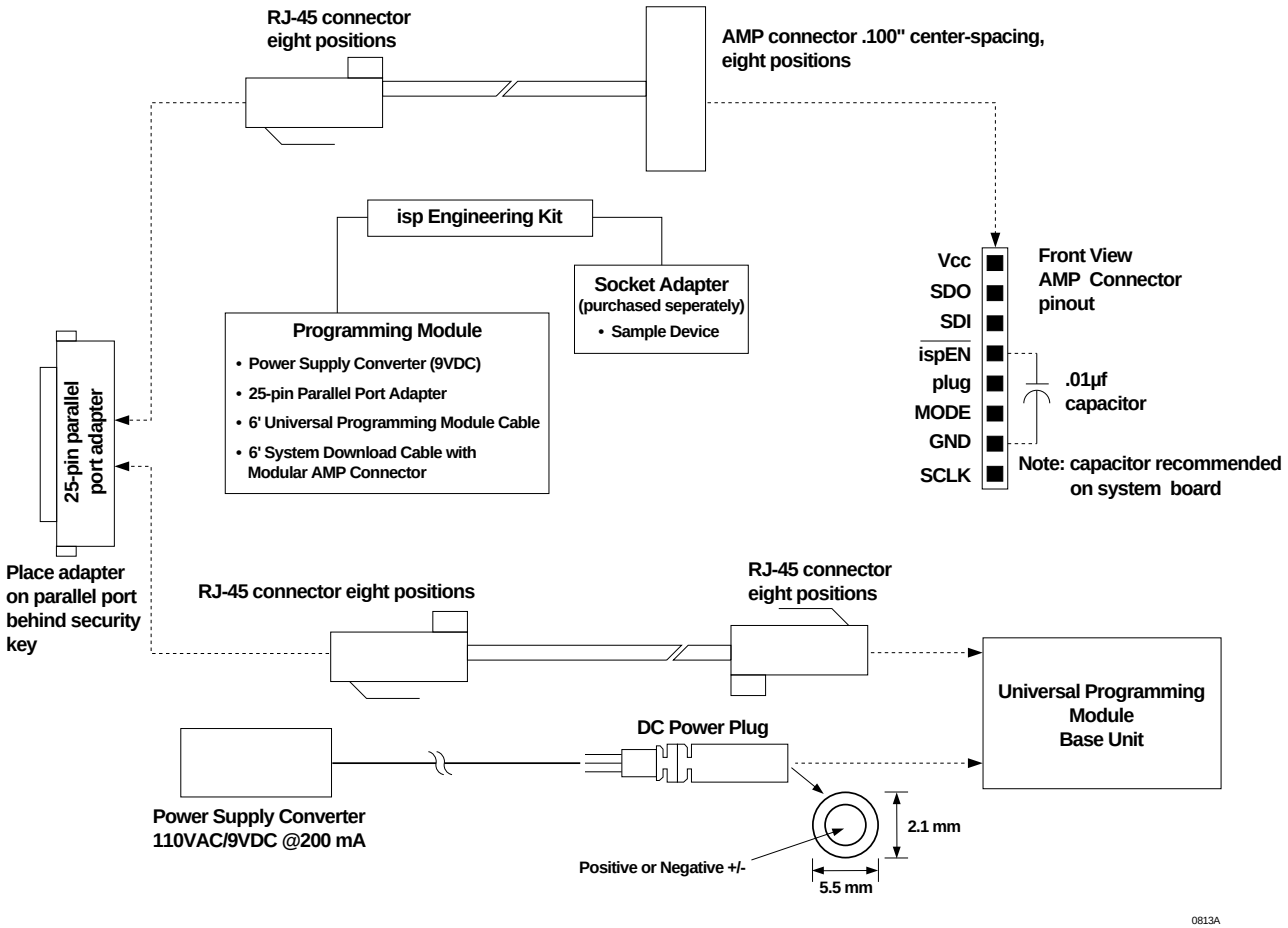
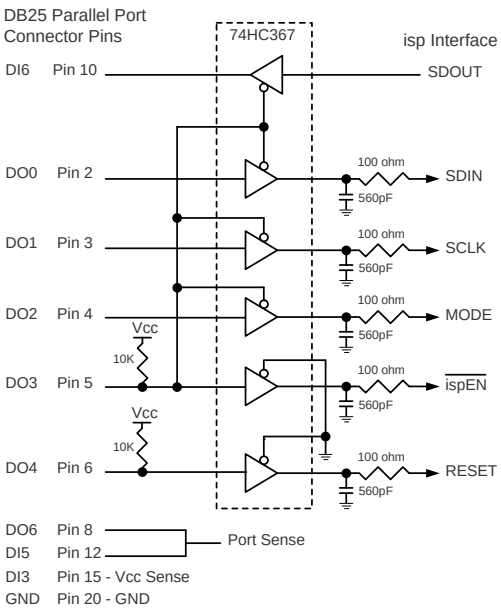
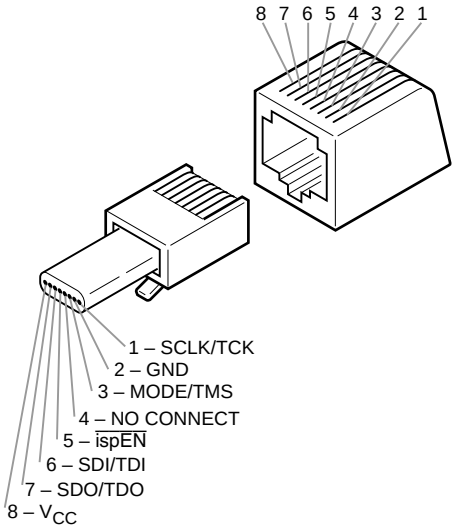


Figure 8. ispDOWNLOAD Cable





Note: The pin numbers in Figure 8 are for reference only. Do not use pin numbers as the socket pinout for board layout.

ispStarter Kits

The ispStarter Kits are designed to make Lattice Semiconductor's innovative in-system programmable device technology available in a single, complete package. The isp Starter Kits contain all the software, hardware, device samples, and information you need to begin designing with ISP products.

The ispStarter Kits include pDS Starter logic development software for ispLSI 1016 and ispLSI 2032 devices, ispGDS compiler software, ispCODE, ISP Daisy Chain Download software, an ispLSI 2032, an ispGAL22V10B, an ispGDS14, and an ispDOWNLOAD Cable.

ISP Synario System

Another complete development tool option, containing all the software, hardware, device samples and information required for ISP design is the ISP Synario System.

The ISP Synario System is based on the popular Synario Entry tool from Data I/O and a version of LSC's pDS+ Synario Fitter supporting ispLSI and pLSI devices up to 1024/2096 device densities. Designs may be entered via Synario Schematic Capture or using ABEL-HDL. Functional Simulation, Project Navigator and the LS Fitter are included, along with the ispGDS Compiler, CODE, ISP Daisy Chain Download software and ispDOWNLOAD Cables. Device samples include the ispLSI 2032, ispGAL22V10B and an ispGDS 14 device. In addition, the ISP Synario System includes GAL compiler support for all LSC GAL devices.

ISP Programming Software

Introduction

Once the JEDEC file has been generated for a given design, the design information, which is stored in the JEDEC file, must be downloaded into the proper device. The download method depends on the hardware available and the design stage. For example, you might program the system with ISP devices during prototyping using a PC. Then, when the system goes to full production, you can use ATE for programming. Finally, if field upgrades are necessary, you can use the system's embedded microprocessor to reprogram the ISP devices. Table 1 summarizes the download methods supported by Lattice Semiconductor.

ispCODE

ispCODE is C-source code that facilitates in-system programming of LSC ISP devices on UNIX systems, PCs, testers and embedded systems. The ispCODE software supplies specific routines, with extensively commented code, for incorporation into user application programs. This software is available from Lattice Semiconductor. For a more thorough description of ispCODE, please refer to the ispCODE Software data sheet in this Data Book.

Table 1. ISP Programming Platform and Download Methods

Programming Platform	Download Methods
PC	ISP Daisy Chain Download ispCODE C Source Routines
Workstation	ispCODE C Source Routines
Embedded Processor	ispCODE Executed by Microprocessor
ATE	ispATE
Third-Party Programmer	Standard JEDEC File Download

ISP Daisy Chain Download

ISP Daisy Chain Download software supports programming of all LSC ISP devices in a serial daisy chain programming configuration in a PC environment. Two varieties of this software exist: one for a Windows environment, the other for a DOS environment. This software is available from Lattice Semiconductor. For a more thorough description of the ISP Daisy Chain Download software, please refer to the ISP Daisy Chain Download software data sheet in this Data Book.

ispATE™

LSC's ispATE is a test-vector creation utility that facilitates programming of LSC ISP devices on HP, Teradyne and GenRad testers. ispATE converts a standard JEDEC file into a programming vector template that can be easily incorporated into a product's printed circuit board functional test program.

ISP Programming Times

The ISP programming times can be approximated by the number of rows that are required to program on a given device and the programming pulse width. Assuming that the overhead of shifting data and other miscellaneous functions are an order of magnitude smaller in time duration and therefore negligible, the total programming time ranges can be calculated .

Calculating Programming Times

ISP programming times can be approximated by the number of rows that are required to program on a given device and the programming pulse width. Assuming that the overhead of shifting data and other miscellaneous functions are several orders of magnitude smaller in time duration and therefore negligible, the total programming time ranges can be calculated using this equation:

$$tpt = asrl * dr * tpwp \text{ (minimum)}$$

where:

tpt: total programming time, ISP devices
asrl: address SR length, from table 8, or
ispGDS = 11
ispGAL22V10 = 44
dr: number of data registers,
ispGDS and ispGAL22V10 = 1
all other ISP devices = 2
tpwp: programming pulse width time,
see tables 5, 6, 7 or 11

Example ispLSI 1016-90 total programming time:

$$tpt = 96 * 2 * 40 \text{ ms} = 7.68 \text{ sec}$$

User Electronic Signature (UES)

The Lattice Semiconductor ispGAL, ispGDS, and ispLSI families can ease problems associated with document control and device traceability, thanks to a feature called the User Electronic Signature (UES).

The UES is basically a user's "notepad" provided in electrically erasable (E^2) cells on each ispGAL, ispGDS, and ispLSI device. The UES consists of an extra row that is appended to the programmable array and allocated for data storage. The physical size of the UES varies by device type. Table 2 indicates the various sizes of the UES.

In the course of system development and production, the proliferation of PLD architectures and patterns can be

Table 2. UES Sizes

Device	UES Size (bits)
ispGAL 22V10	64
ispGDS	32
ispLSI 1016/E	80
ispLSI 1024/E	120
ispLSI 1032/E	160
ispLSI 1048/C/E	240
ispLSI 2032/LV	40
ispLSI 2064	80
ispLSI 2096	120
ispLSI 2128	160
ispLSI 3192	240
ispLSI 3256	160
ispLSI 6192	160

Table 3. ispLSI Device ID Codes

Device	MSB LSB
ispLSI 1016	00000001
ispLSI 1016E	00001011
ispLSI 1024	00000010
ispLSI 1024E	00001100
ispLSI 1032	00000011
ispLSI 1032E	00001101
ispLSI 1048	00000100
ispLSI 1048C	00000101
ispLSI 1048E	00001110
ispLSI 2032	00010101
ispLSI 2064	00010010
ispLSI 2096	00010011
ispLSI 2128	00010100
ispLSI 3192	00100001
ispLSI 3256	00100010
ispLSI 6192	00110010

significant. To further complicate the record-keeping process, design changes often occur, especially in the early stages of product development. The task of maintaining which pattern goes into what device for which socket becomes exceedingly difficult. Once a manufacturing flow has been set, it becomes important to "label" each PLD with pertinent manufacturing information, which is beneficial in the event of a customer problem or return.

LSC incorporated the UES to store such design and manufacturing data as the manufacturer's ID, programming date, programmer make, pattern code, checksum, PCB location, revision number, and/or product flow. This assists users with the complex chore of record maintenance and product flow control. In practice, the UES can be used for any of a number of ID functions.

Within the various bits available for UES data storage, users may find it helpful to define specific fields to make better use of the available storage. A field may use only one bit (or all bits), and can store a wide variety of information. The possibilities for these fields are endless, and their definition is completely up to the user.

Even with the device's security feature enabled, the UES can still be read. With a pattern code stored in the UES, the user can always identify which pattern has been used in a given device. As a second safety feature, when a device is erased and re-patterned, the UES row is automatically erased. This prevents any situation in which an old UES might be associated with a new pattern.

It is the user's responsibility to update the UES when reprogramming. It should be noted that UES information will be included in the checksum reading for ispGAL and ispGDS devices. Therefore, on these two device types, when the UES is modified the checksum will also change. For ispLSI devices, UES is supported through the use of U-field in the JEDEC file which does not affect the checksum.

The UES may be accessed (read or write) through one of three methods. First, most third-party programmers support the UES option for the ispGAL and ispGDS devices through the programmer's user interface, so programming or verifying the UES is as simple as programming or verifying any other array. Second, the UES may be embedded within the JEDEC file or the ISP Daisy Chain Download software by selecting the proper fuse locations in the fuse map for ispGAL and ispGDS devices or in the U-field for the ispLSI devices. Third, the UES can be written or read using Lattice's ispCODE software. Further information on using ispCODE software to program the UES can be found in the ispCODE software data sheet in this Data Book.

ispLSI Programming Details

The following sections describe the programmable state machine instruction set, timing parameters, device layout and programming algorithms as they apply to ispLSI devices in general. Table 3 lists the eight-bit device IDs for all the ispLSI devices.

Table 4 lists the instructions that can be loaded into the state machine in the Command Shift State and then executed in the Execute State. Notice that the device identification is read during the Idle/ID State, and this operation does not require an instruction.

While it is possible to erase the individual arrays of the device, it is recommended that the entire device be erased (UBE) and programmed in one operation. This Bulk Erase operation should precede every programming cycle as an initialization.

When a device is secured by programming the security cell (PRGMSC), the on-chip verify and load circuitry is disabled. The device should be secured as the last procedure, after all the device verifications have been completed. The only way to erase the security cell is to perform a bulk erase (UBE) on the device.

Table 4. ispLSI Programming State Machine Instruction Set

Instruction	Operation	Description
00000	NOP	No operation performed.
00001	ADDSHFT	Address Register Shift: Shifts address into the address shift register from SDIN.
00010	DATASHFT	Data Register Shift: Shifts data into or out of the data serial shift register.
00011	UBE	User Bulk Erase: Erase the entire device.
10000	ERALL	Erase the entire device, including the UES (User Electronic Signature)
00100	GRPBE	Global Routing Pool Bulk Erase: Bulk erases the GRP array only.
00101	GLBBE	Generic Logic Block Bulk Erase: Bulk erases the GLB array only.
00110	ARCHBE	Architecture Bulk Erase: Bulk erases the architecture array and I/O configuration only.
00111	PRGMH	Program High Order Bits: The data in the Data shift register is programmed into the addressed row's high order bits.
01000	PRGML	Program Low Order Bits: The data in the Data shift register is programmed into the addressed row's low order bits.
01001	PRGMSC	Program Security Cell: Programs the security cell of the device.
01010	VER/LDH	Verify/Load High Order Bits: Load the data from the selected row's high order bits into the Data shift register for verification.
01011	VER/LDL	Verify/Load Low Order Bits: Load the data from the selected row's low order bits into the Data shift register for verification.
01110	FLOWTHRU	Flow Through: Bypasses all the internal shift registers and SDOUT becomes the same as SDIN.
10010	VE/LDH	Verify Erase/Load High Order Bits: Load the data from the selected row's high order bits into the Data shift register for erased verification.
10011	VE/LDL	Verify Erase/Load Low Order Bits: Load the data from the selected row's low order bits into the Data shift register for erased verification.
01111	PROGUES	Program UES.
10001	VERUES	Verify UES.

In addition to the two programming and erasing specifications, the following timing specifications must be met:

t_{ispen} - Specifies the time it takes to get into the ISP mode after $\overline{ispEN}$ is activated. Or, the time it takes to come out
t_{ispdis} from the ISP mode after $\overline{ispEN}$ becomes inactive.

t_{su} - Set up time of the control signals before SCLK. Or, the set up time of input signals against other control signals (if applicable).

t_h - Hold time of the control signal after SCLK. It also applies to the same input signals from the set up time.

t_{clkl} - Minimum clock pulse width, low.

t_{clkh} - Minimum clock pulse width, high.

t_{pwv} - Verify or read pulse width. The minimum time requirement from the rising clock edge of a verify/load instruction execution to the next rising clock edge (Figure 9).

t_{rst} - Power on reset timing requirement. t_{rst} must elapse after power up before any operations are performed on the device.

ispLSI Programming Voltage/Timing Specifications and Waveforms

Table 5. ISP Programming Voltage/Timing Specifications (ispLSI 1000E, 2000, 3000 and 6000 Families)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage			4.75	5.0	5.25	V
I_{CCP}	Programming Supply Current			–	50	100	mA
V_{IHP}	Input Voltage High	$\overline{ispEN}$ = Low		2.0	–	V_{CCP}	V
V_{ILP}	Input Voltage Low			0.0	–	0.8	V
I_{IP}	Input Current			–	100	200	µA
V_{OHP}	Output Voltage High	I_{OH} = -3.2 mA		2.4	–	V_{CCP}	V
V_{OLP}	Output Voltage Low	I_{OL} = 5 mA		0.0	–	0.5	V
t_r, t_f	Input Rise and Fall			–	–	0.1	µs
t_{ispen}	$\overline{ispEN}$ to Output 3-State Enabled			–	–	10	µs
t_{ispdis}	$\overline{ispEN}$ to Output 3-State Disabled			–	–	10	µs
t_{su1}	Setup Time, isp State Machine			0.1	–	–	µs
t_{su2}	Setup Time, Program and Erase Cycle*			200	–	–	µs
t_{co}	Clock to Output			–	–	0.1	µs
t_h	Hold Time			0.1	–	–	µs
t_{clkh}, t_{clkl}	Clock Pulse Width, High and Low			0.5	–	–	µs
t_{pwv}	Verify Pulse Width			20	–	–	µs
t_{pwp}	Programming Pulse Width			80	–	160	ms
t_{bew}	Bulk Erase Pulse Width			200	–	–	ms
t_{rst}	Reset Time from Valid V_{CCP}	Rise Time < 50 µs	1000E, 2000	45	–	–	µs
			3000, 6000	100	–	–	µs

Table 2 - 0029isp-2000

Figure 9. Timing Waveforms for In-System Programming (ispLSI 1000E, 2000, 3000 and 6000 Families)

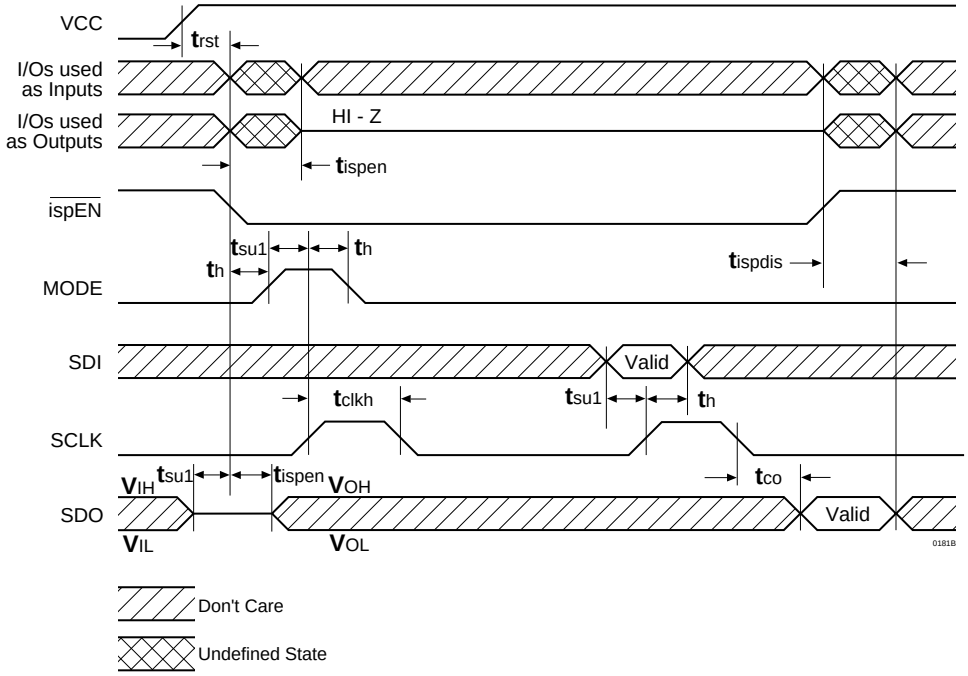


Figure 10. Program, Verify and Bulk Erase Waveforms (ispLSI 1000E, 2000, 3000 and 6000 Families)

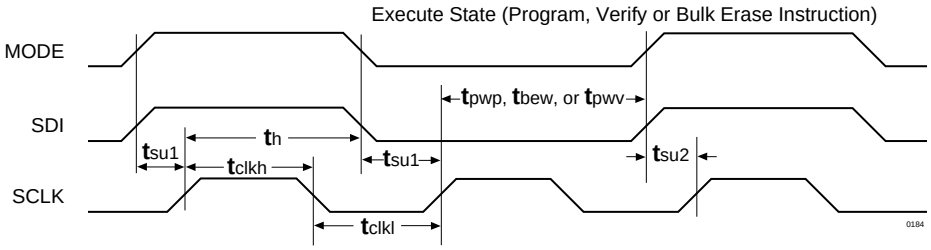


Table 6. ISP Programming Voltage/Timing Specifications (ispLSI 1000 Family)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage		4.75	5	5.25	V
I_{CCP}	Programming Supply Current		–	50	100	mA
V_{IHP}	Input Voltage High	$\overline{ispEN}$ = Low	2.0	–	V_{CCP}	V
V_{ILP}	Input Voltage Low		0	–	0.8	V
I_{IP}	Input Current		–	100	200	µA
V_{OHP}	Output Voltage High	I_{OH} = -3.2 mA	2.4	–	V_{CCP}	V
V_{OLP}	Output Voltage Low	I_{OL} = 5 mA	0	–	0.5	V
t_r, t_f	Input Rise and Fall		–	–	0.1	µs
t_{ispen}	$\overline{ispEN}$ to Output 3-State Enabled		–	2	10	µs
t_{ispdis}	$\overline{ispEN}$ to Output 3-State Disabled		–	2	10	µs
t_{su}	Setup Time		0.1	0.5	–	µs
t_{co}	Clock to Output		0.1	0.5	–	µs
t_h	Hold Time		0.1	0.5	–	µs
t_{clkh}, t_{clkl}	Clock Pulse Width, High and Low		0.5	1	–	µs
t_{pwv}	Verify Pulse Width		20	30	–	µs
t_{pwp}	Programming Pulse Width		40	–	100	ms
t_{bew}	Bulk Erase Pulse Width		200	–	–	ms
t_{rst}	Reset Time From Valid V_{CCP}		45	–	–	µs

1. ISP Programming is guaranteed for T_A = 0˚C to 70˚C Operation only.

Table 2- 0029 isp-C

Figure 11. Timing Waveforms for In-System Programming (ispLSI 1000 Family)

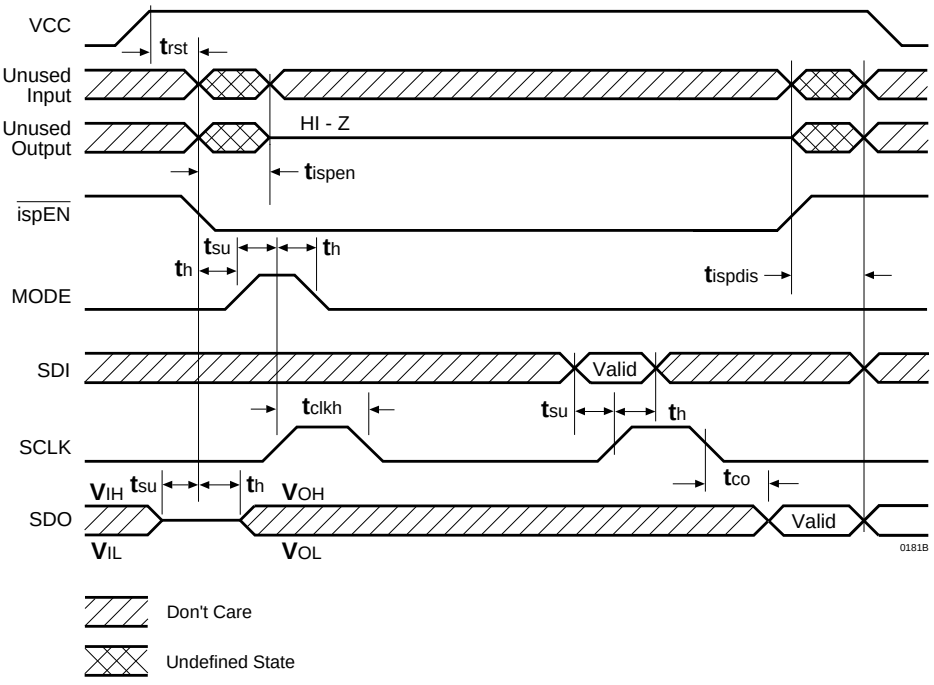


Figure 12. Program, Verify and Bulk Erase Waveforms (ispLSI 1000 Family)

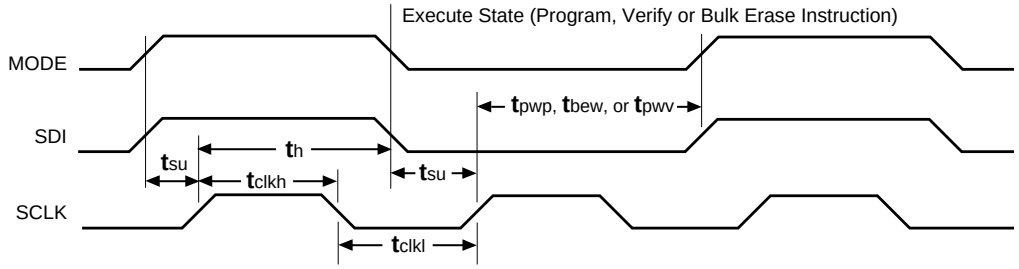
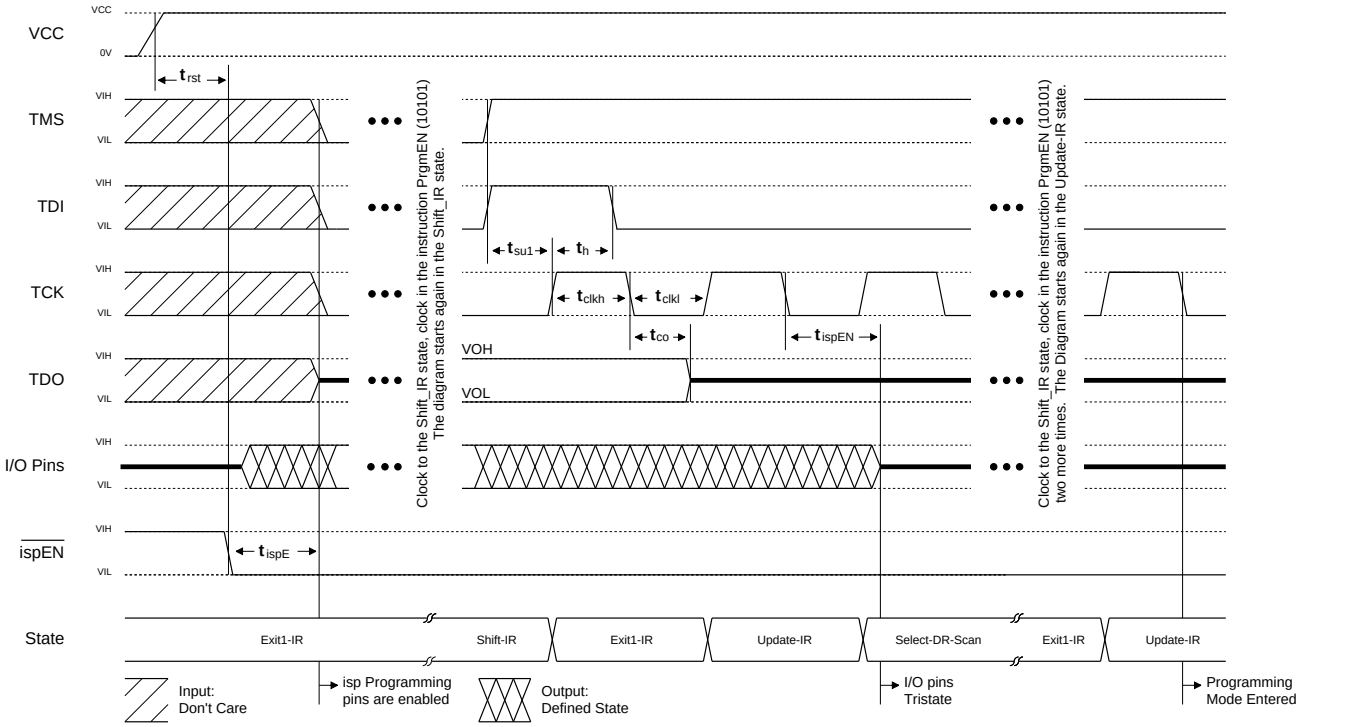


Table 7. ISP Programming Voltage/Timing Specifications (ispLSI 2032LV)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage		3.0	3.3	3.6	V
I_{CCP}	Programming Supply Current		–	50	100	mA
V_{IHP}	Input Voltage High	$\overline{ispEN}$ = Low	2.0	–	V_{CCP}	V
V_{ILP}	Input Voltage Low		0.0	–	0.8	V
I_{IP}	Input Current		–	100	200	µA
V_{OHP}	Output Voltage High	I_{OH} = -3.2 mA	2.4	–	V_{CCP}	V
V_{OLP}	Output Voltage Low	I_{OL} = 5 mA	0.0	–	0.5	V
t_r, t_f	Input Rise and Fall		–	–	0.1	µs
t_{dft}	TDI to TDO Delay with Flowthru Command		–	–	100	ns
t_{ispE}	$\overline{ispEN}$ to Programming Pins Enabled		–	–	1.0	µs
t_{ispD}	$\overline{ispEN}$ to Programming Pins Disabled		–	–	1.0	µs
t_{ispEN}	Program Enable Command to I/O 3-State Enabled		–	–	10	µs
t_{ispDIS}	Program Enable Command to I/O 3-State Disabled		–	–	10	µs
t_{su_1}	Clock Setup Time		100	–	–	ns
t_{su_2}	Program Setup Time		200	–	–	µs
t_{co}	Clock to Output		–	–	80	ns
t_h	Hold Time		10	–	–	ns
t_{clkh}, t_{clkl}	Clock Pulse Width, High and Low		100	–	–	ns
t_{pwv}	Verify Pulse Width		30	–	–	µs
t_{pwp}	Programming Pulse Width		80	–	–	ms
t_{bew}	Bulk Erase Pulse Width $_{CCP}$		200	–	–	ms
t_{rst}	Reset Time from Valid V		1	–	–	µs

Table 2 - 0029isp-2032

Figure 13. Timing Waveforms for Entering the Programming Mode (ispLSI 2032LV)



ENT_TIM.AI

Figure 14. Timing Waveforms for Exiting the Programming Mode (ispLSI 2032LV)

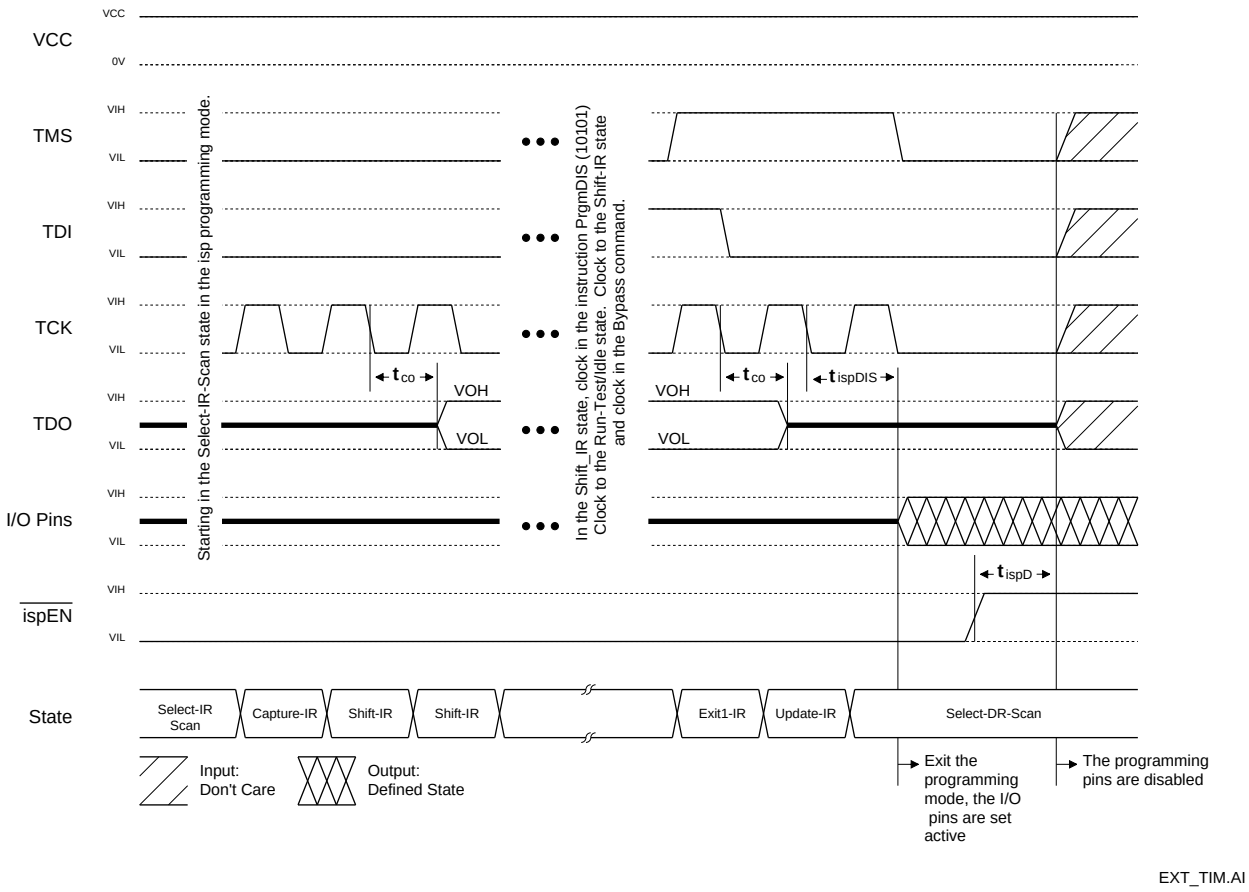
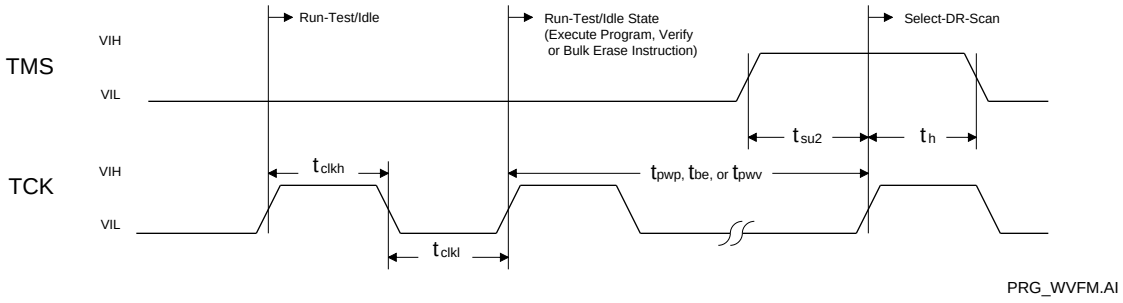


Figure 15. Program, Verify and Bulk Erase Waveform (ispLSI 2032LV)



Device Layout

To translate the JEDEC format programming file into the serial data stream format for programming ispLSI devices, it is necessary to know the physical device layout and programming architecture. Two main factors determine how the translation must be implemented: the length of the address shift register and the length of the data shift register. The length of the address shift register indicates how many rows of data are to be programmed into the device. The length of the Data shift register indicates how many bits are to be programmed in each row. Both registers operate on a First In First Out (FIFO) basis, where the Least Significant Bit (LSB) of the data or address is shifted in first and the Most Significant Bit (MSB) of the data or address is shifted in last. For the Data shift register, the low order bits and the high order bits are separately shifted in.

Each ispLSI device has a predefined number of address rows and data bits needed to access its E^2CMOS cells during programming. The data bits span the columns of the E^2 array. From this information, the number of programming cells (or fuses) are determined. Table 8 highlights the address and data shift register (SR) sizes for currently available ispLSI devices. The JEDEC file for these ispLSI devices will reflect the number of cells (fuses) seen in Table 8. The total number of cells becomes critical if the programming patterns are to be stored in an on-board memory storage of limited capacity such as EPROM or PROM.

The L-fields in the JEDEC programming file indicate the link or fuse numbers of the device. The first cell of the device is indicated by cell number L00000. L-fields of subsequent lines are optional. From this reference cell location, all other cell locations are determined by relative position. A zero (0) in the cell location indicates that the E^2 cell in that particular location is programmed (or has a logic connection intact). A one (1) in the cell location indicates that the cell is erased (equivalent to an open connection). The logic compiler software automatically generates this JEDEC standard programming file after the design has been fit into the device.

Timing

When programming ispLSI devices, there are several critical timing parameters that must be met to ensure proper programming. The two most critical parameters are the programming pulse width (t_{pwp}) and the bulk erase pulse width (t_{bew}). These pulse widths determine the programming and erasing times of the E^2 cells. The following figures and tables show these critical program and erase timing specifications.

Fuse Map to Device Conversion

While the ispCODE software takes care of this detail, it is important to understand how the JEDEC fuse map is mapped onto the physical ispLSI device during programming. The physical layout of the fuse pattern begins with Address Row 0 and ends with the maximum Address Row N and is determined by the length of the Address SR as described in Table 8. Spanning the Address Rows are the outputs of the High-Order Data SR and Low-Order Data SR, as described in Table 9. Programming fuses on a given row are enabled by a “1” within the Address Shift Register for the appropriate row and the use of state machine instructions that selectively operate on the High-Order Data SR or the Low-Order Data SR. For example, the PRGMH instruction programs the High-Order data bits within the device for the selected Address Row and the PRGML instruction programs the Low-Order data bits (Table 4 lists the ISP state machine instructions). Referring to Figure 16, the starting cell (L00000) of the JEDEC fuse map shifts into the device at the physical location corresponding to Address Row 0, High-Order Data SR bit 0. The "n" and "m" in the figure refer to the Address SR length and the Data SR length, respectively, of the device (Table 8). A series of sequential shifts eventually results in the last cell location (Total # of Cells - 1) of the JEDEC fuse map shifting into Address Row (n-1), Low-Order Data SR bit (m-1) on the actual device.

The ispCODE Software routines make use of a bit packed data format, called ispSTREAM™, to transfer data between the JEDEC fuse map and the physical device locations. The binary ispSTREAM format uses one bit to represent the state of each of the programmable cells, instead of the byte value used in an ASCII JEDEC file.

Table 8. ispLSI Address and Data Shift Register and Total Cell Summary

Device	Address SR Length	Data SR Length/Address	Total Number of Cells
ispLSI 1016/E	96/110	160/160	15,360/17,600
ispLSI 1024/E	102/122	240/240	24,480/29,280
ispLSI 1032/E	108/134	320/320	34,560/42,880
ispLSI 1048/C/E	120/155/158	480/480/480	57,600/74,400/75,840
ispLSI 2032	102	80	8,160
ispLSI 2064	118	160	18,880
ispLSI 2096	134	240	32,160
ispLSI 2128	150	320	48,000
ispLSI 3192	216	480	103,680
ispLSI 3256	180	676	121,680
ispLSI 6192	180	600	108,000

Table 9. Summary of ispLSI Data Shift Register Bits

Device	High Order Data SR LSB	High Order Data SR MSB	Low Order Data SR LSB	Low Order Data SR MSB	Data SR Size (Bits)
ispLSI 1016/E	0	79	80	159	160
ispLSI 1024/E	0	119	120	239	240
ispLSI 1032/E	0	159	160	319	320
ispLSI 1048/C/E	0	239	240	479	480
ispLSI 2032	0	39	40	79	80
ispLSI 2064	0	79	80	159	160
ispLSI 2096	0	119	120	239	240
ispLSI 2128	0	159	160	319	320
ispLSI 3192	0	239	240	479	480
ispLSI 3256	0	337	338	675	676
ispLSI 6192	0	299	300	599	600

Considering the additional characters present in a JEDEC file, this adds up to a space savings of more than a factor of eight. In addition, the ispSTREAM does not require any parsing; the bits are simply read from the file and shifted into the device. As only 1922 bytes are required to store the pattern for an ispLSI 1016 device, multiple patterns can be stored in a small amount of memory. The JEDEC fuse map can be translated into ispSTREAM format using the dld2isp.exe program.

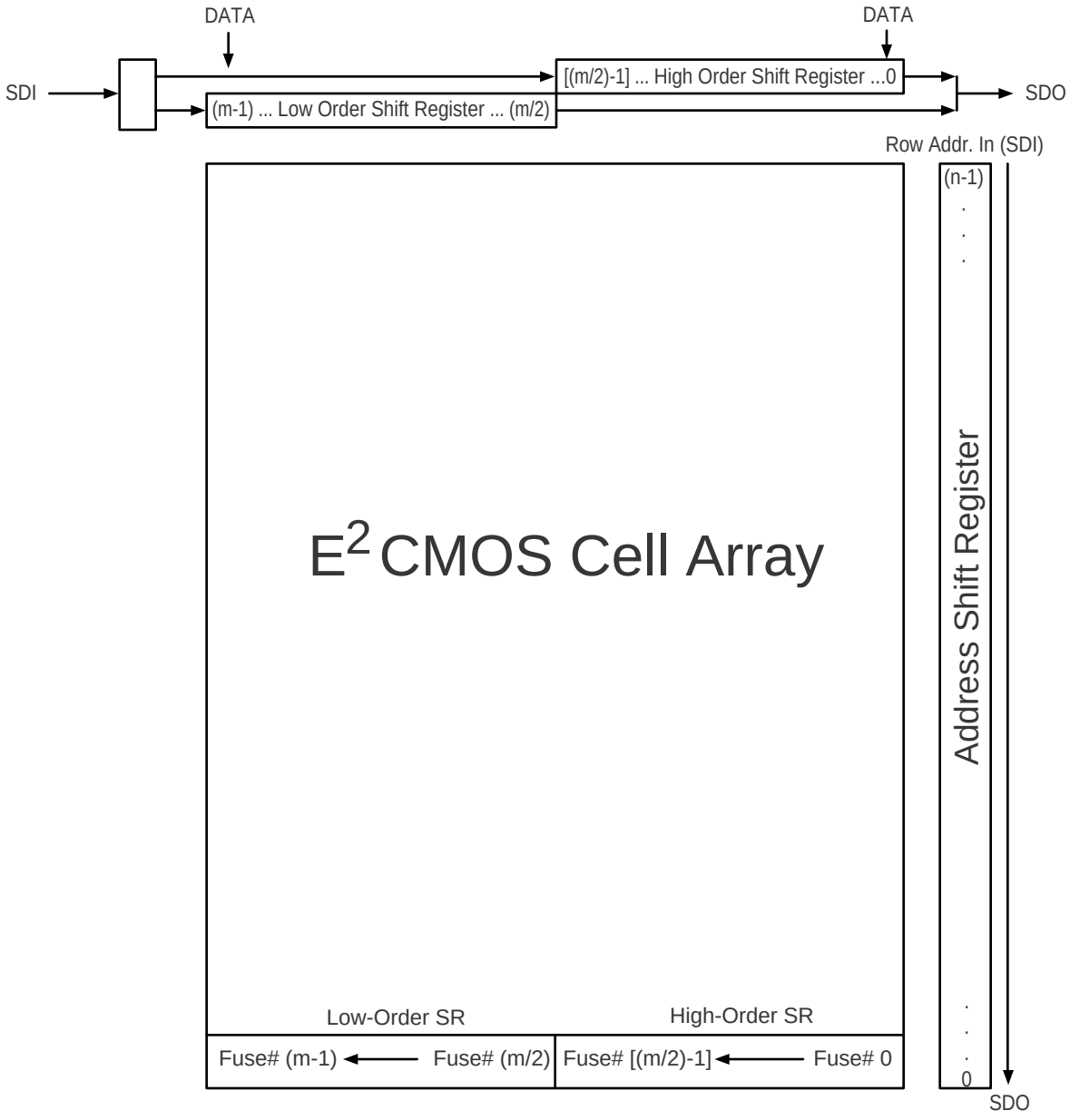
Algorithms

Command Stream

The first step in programming an ispLSI device is to determine the device type to be programmed. This is ascertained by reading the eight-bit ID of every device. By keeping SDI to a known level (either high or low), the ID shift can be terminated when a sequence of eight ones or eight zeros is read. From the device ID, the serial bit stream for programming can be arranged. A typical programming sequence is listed below:

1) ADDSHFT command shift
2) Execute ADDSHFT command
3) Shift address
4) DATASHFT command shift
5) Execute DATASHFT command
6) Shift high order data
7) PRGMH command shift

Figure 16. ispLSI Device to Fuse Map Translation



8) Execute PRGMH

9) DATASHFT command shift

10) Execute DATASHFT command

11) Shift low order data

12) PRGML command shift

13) Execute PRGML

14) Repeat from 1) until all rows are programmed

Boundary Scan

The Lattice Semiconductor ispLSI 3000 and 6000 families of devices supports the IEEE 1149.1 Boundary Scan specifications. The following sections explain in detail how to interface to the devices through the Test Access Port (TAP), how the boundary scan registers are implemented within the devices, and the boundary scan instructions that are supported by the ispLSI and pLSI 3000 and 6000 families.

Test Access Port (TAP)

The test access port of the boundary scan is accessed through six interface signals: TDI, TDO, SCLK, BSCAN, TMS, TRST. These interface signals have two functions in the case of the ispLSI 3000 and 6000 families; they serve as both the Boundary Scan interface and in-system programming interface signals. For the pLSI 3000 and 6000 families, the six interface signals are only used for the boundary scan TAP interface. Table 10 describes the interface signals.

The above mentioned six signals are dedicated for Boundary Scan use for the pLSI devices. As ISP programming is accomplished through the same pins, five of the six signals have both Boundary Scan interface and ISP functions on the ispLSI devices. $\overline{\text{TRST}}$ is the only signal that does not have a dual function. It is used only to reset the TAP controller state machine. The sequencing of test routines are governed by the TAP controller state machine. The state machine uses the TMS and TCK signals as its inputs to sequence the states. Figure 17 is the IEEE1149.1 specified state machine. The condition for the state transition is the state of the TMS input condition before TCK within a given state. The timing diagram is also shown in Figure 17.

The main features of the TAP controller state machine include Test-Logic-Reset state to reset the controller and the Run-Test states. Two main components of the Run-Test states are Data Register (DR) control states and Instruction Register (IR) control states. Both of these register control states are organized in a similar manner. The user can capture the registers, shift the register string, or update the registers. Capturing the DRs simply loads the DR with the data from the corresponding functional input, output, or I/O pins. The IR capture, on the other hand, loads the IRs with the previously executed instruction bits. Shift register states serially shift the DR and IR. In the case of DR shift, the data is shifted according to the order of the inputs, outputs, and I/Os defined in the Boundary Scan section of each device data sheet. The IRs are shifted out from the least significant bit

Table 10. ispLSI and pLSI 3000 and 6000 Family Boundary Scan Interface Signals

pLSI	ispLSI	Pin Function Description
BSCAN	BSCAN/$\overline{\text{ispEN}}$	Active high signal on this pin selects the Boundary Scan function while active low signal selects the ISP function on the ispLSI devices. Internal pullup on this pin drives the signal high when the external pin is not driven.
TCK	TCK/SCLK	Test Clock function for Boundary Scan and serial clock for the the ISP function.
TMS	TMS/MODE	Test Mode Select for Boundary Scan and MODE control for the ISP function.
TDI	TDI/SDI	Test Data Input for Boundary Scan and Serial Data Input for the ISP function. Functions as a serial data input pin for both interfaces.
$\overline{\text{TRST}}$	$\overline{\text{TRST}}$	Test Reset Input is an asynchronous signal to initialize the TAP controller to the Test-Logic-Reset state.
TDO	TDO/SDO	Test Data Output for Boundary Scan and Serial Data Output for the ISP function. Functions as a serial data output pin for both interfaces.

Figure 17a. TAP Controller State Machine

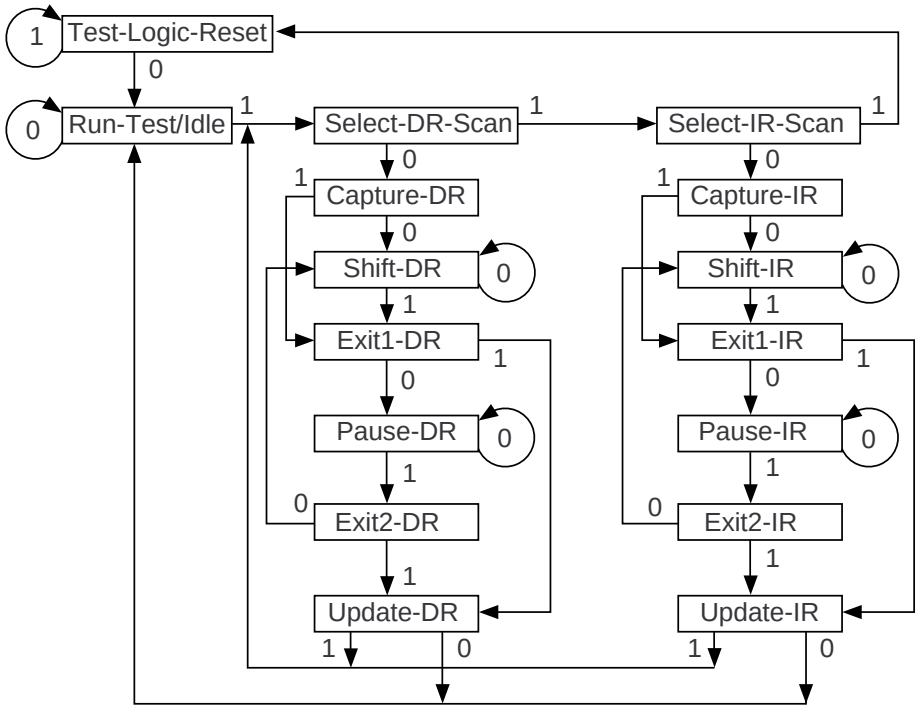
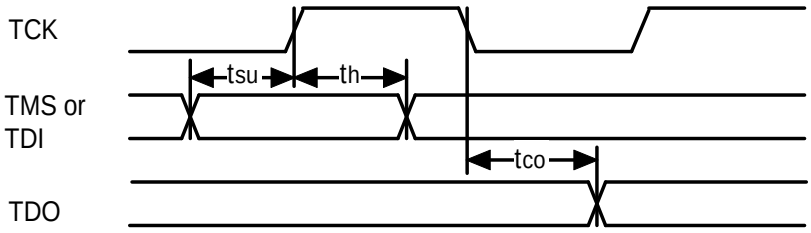


Figure 17b. TAP Controller Timing Diagram



first. During update register states, the DRs update the latches to drive the external pins and the IRs update the instruction bits with the instruction that is to be executed.

Boundary Scan Registers

In order to support Boundary Scan, three types of data registers are defined for the ispLSI and pLSI devices — I/O cell registers, input cell registers and output cell registers (6000 family only). The main purpose of these registers is to capture test data from the appropriate signals and shift data to either drive the test pins or examine captured test data.

Figure 18 describes the register for the I/O cell. The I/O cell, by definition, must have three components: one register component captures the output enable (OE) signal, the second component captures the output data, and the third captures the input data. These components make up the three registers that are part of the shift register string for each of the I/O pins. Only parts of the I/O cell registers will have valid data when I/O pins are configured as input-only or output-only, thus the test routines must be able to monitor the appropriate register bits. The update registers are used mainly to store data that is to be driven onto the I/O pins. The multiplexer controls are driven by the signal from the TAP controller at appropriate states.

The function of an input cell register is much simpler than that of an I/O cell. Figure 19 illustrates the single input register cell. The purpose of the Input cell is to capture the input test data and shift the data out of the shift register string.

Boundary Scan Instructions

Lattice ispLSI and pLSI devices support the three mandatory instructions defined by the Boundary Scan definition. The following paragraphs describe each of the instructions and its instruction code. A two-bit shift register is defined within the devices to implement the Instruction shift register.

The SAMPLE/PRELOAD (Instruction Code - 10*/11100) instruction is used to sample the pins that are to be tested. During the Capture-DR state, while executing this instruction, the DRs are loaded with the state of the pins which can then be examined after shifting the data through TDO. The PRELOAD part of this instruction is simply loading the DRs during Shift-DR state with the desired condition for each of the pins.

The EXTEST (Instruction Code - 00*/00000) instruction drives the external pins with the previously updated values from the DR during the Update-DR state.

The BYPASS (Instruction Code - 11*/11111) instruction is used to bypass any device that is not accessed during any part of the test. The definition of the BYPASS instruction allows TDI not to be driven during the Shift-IR state. In order to shift in the correct instruction code, the TDI pin has an internal pull-up to drive logic high. A bypassed boundary scan device has a single bypass register as shown in Figure 20.

*3256 only.

Figure 18. Boundary Scan I/O Cell

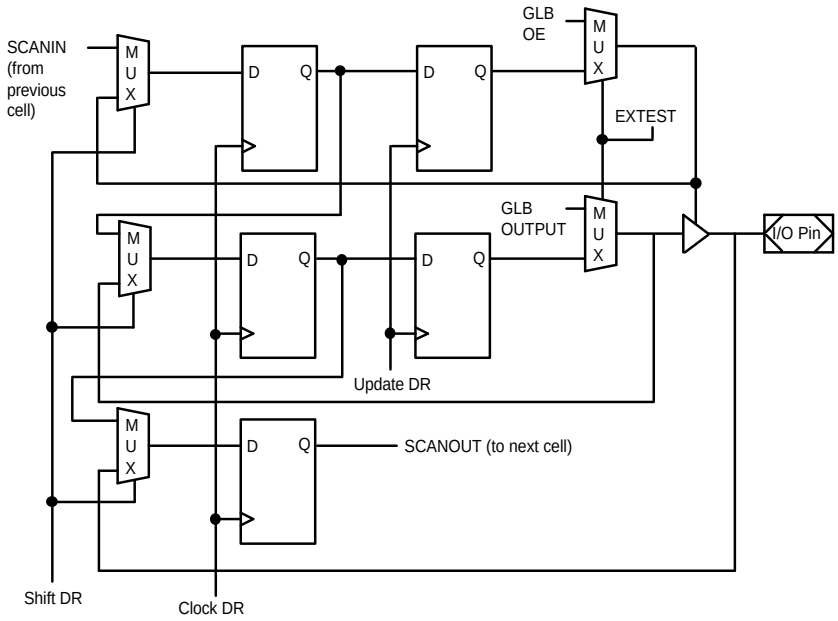


Figure 19. Boundary Scan Input Cell

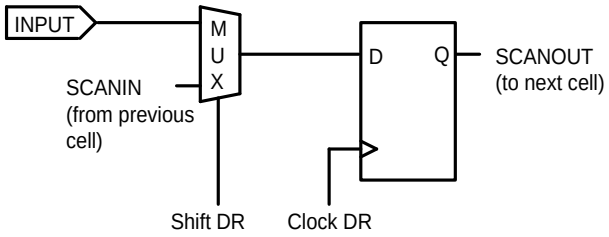
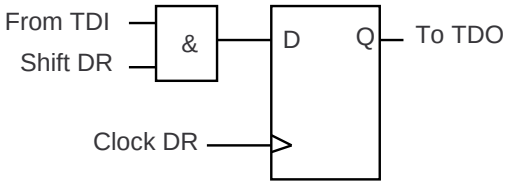


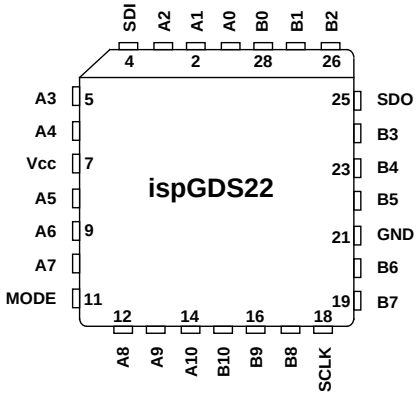
Figure 20. Bypass Register



ispGDS Programming Details

The following sections describe the state machine instruction set, timing parameters, device layout, and programming algorithms as they apply to ispGDS devices in general. Figure 21 shows the ispGDS22 28-pin device pinout.

Figure 21. ispGDS22 28-Pin PLCC Pinout Diagram



Shift Registers

The ispGDS devices have three shift registers, the Device ID shift register, the Instruction shift register and the Data shift register. All shift registers operate on a First In First Out (FIFO) basis, and are chosen by which state the programming state machine is in.

The Device ID shift register is only accessible in the IDLE state. It is eight bits long, and is only used to shift out the device ID. The ispGDS device IDs are 70-72 (hex) (Table 11). The Instruction shift register is only accessible in the SHIFT state. It is five bits long, and is only used to shift the Instruction Codes into the device. The Device ID and Instruction shift registers expect the LSB to be shifted in first. The Data shift register is 24 bits long, and is used to shift all addresses and data into or out of the device. The Data shift register is only accessible in the EXECUTE state when executing a SHIFT_DATA instruction (Table 11).

To program an ispGDS device, data is read from a serial bit stream and shifted into the shift registers. Twenty-four bits are read at a time, shifted into the device, and then a programming operation is performed. The exact sequence, and the methods for converting a JEDEC map into a serial bit stream are explained in the ispGDS Internal Architecture section.

Timing

Programming the ispGDS devices properly requires that a number of timing specifications be met. The specifications relating to programming and erasing the E^2CMOS cells are the most critical. In addition to a minimum pulse width, there is also a maximum timing specification. Refer to the ispGDS programming mode timing specifications in Table 12 for the timing requirements. Timing diagrams for the programming mode specifications are shown in Figures 22, 23, and 24.

Table 11. ispGDS Programming State Machine Instruction Set

Instruction	Operation	Description
00000	NOP	No operation performed.
00010	SHIFT_DATA	Clocks data into, or out of, the Data Shift Register.
00011	BULK_ERASE	Erases the entire device.
00101	ERASE_ARRAY	Erases everything except the Architecture rows.
00110	ERASE_ARCH	Erases the Architecture rows only.
00111	PROGRAM	Programs the Shift Register data into the addressed row.
01010	VERIFY	Load data from the selected row into the Serial Shift Register.
01110	FLOWTHRU	Disables the Shift Register (SDI=SDO).

Figure 22. Programming Mode Timing (ispGDS and ispGAL22V10 Families)

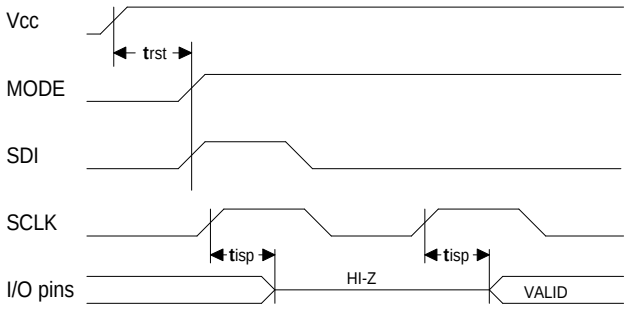


Figure 23. Shift Register Timing (ispGDS and ispGAL22V10 Families)

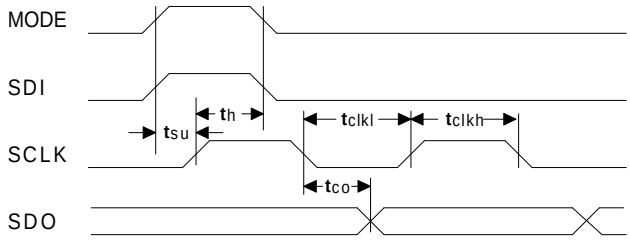


Figure 24. Program, Verify, and Erase Timing (ispGDS and ispGAL22V10 Families)

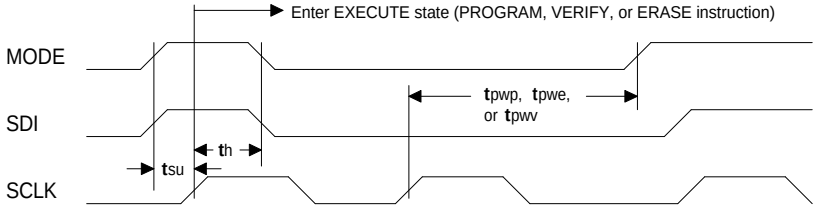


Table 12. Programming Mode Timing Specifications (ispGAL22V10 and ispGDS Families)

Param.	Description		Min.	Max.	Unit
trst	Time from power-up of device to any progamming operation.		1	—	µs
tisp	Time from leaving IDLE state to I/O pins tri-state, or entering IDLE state to I/O pins active.		—	10	µs
tsu	Setup time, from either MODE or SDI to rising edge of SCLK.		100	—	ns
th	Hold time, from rising edge of SCLK to MODE or SDI changing level.		100	—	ns
tco	Time from falling edge of SCLK to data out on SDO.	ispGAL22V10	—	210	ns
		ispGDS	—	150	ns
tclkh	Clock pulse width of SCLK while high.		0.5	—	µs
tclkl	Clock pulse width of SCLK while low.		0.5	—	µs
tpwp	Time for a programming operation.		40	100	ms
tpwe	Time for an erase operation.		200	—	ms
tpwv	Time for a verify operation.		5	—	µs

ispGDS Internal Architecture

This section covers the details of constructing the ispSTREAM format. Only 49 bytes are required to store the pattern for an ispGDS device. If you are using the supplied software tools, a conversion utility (complete with source code) is included to convert an industry-standard JEDEC file to ispSTREAM format. All of the Lattice software routines read and write this ispSTREAM.

The ispGDS devices are composed of two basic architectural components (Figure 25). The first component consists of three rows of architectural information, which contain the three bits that control the function of each I/O cell. The rows are 24 bits long, providing one bit for each I/O cell (the ispGDS18 and ispGDS14 do not use all of the bits). The second component contains the cell data for the switch matrix area of the device and the User Electronic Signature (UES) data area. There are two UES rows of 24 bits each, and 11 switch matrix rows of 24 bits each.

Figure 25. ispGDS Architecture

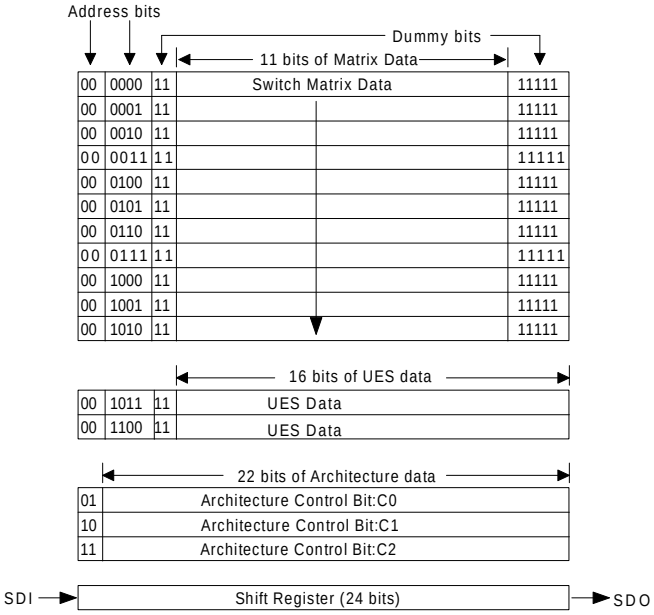
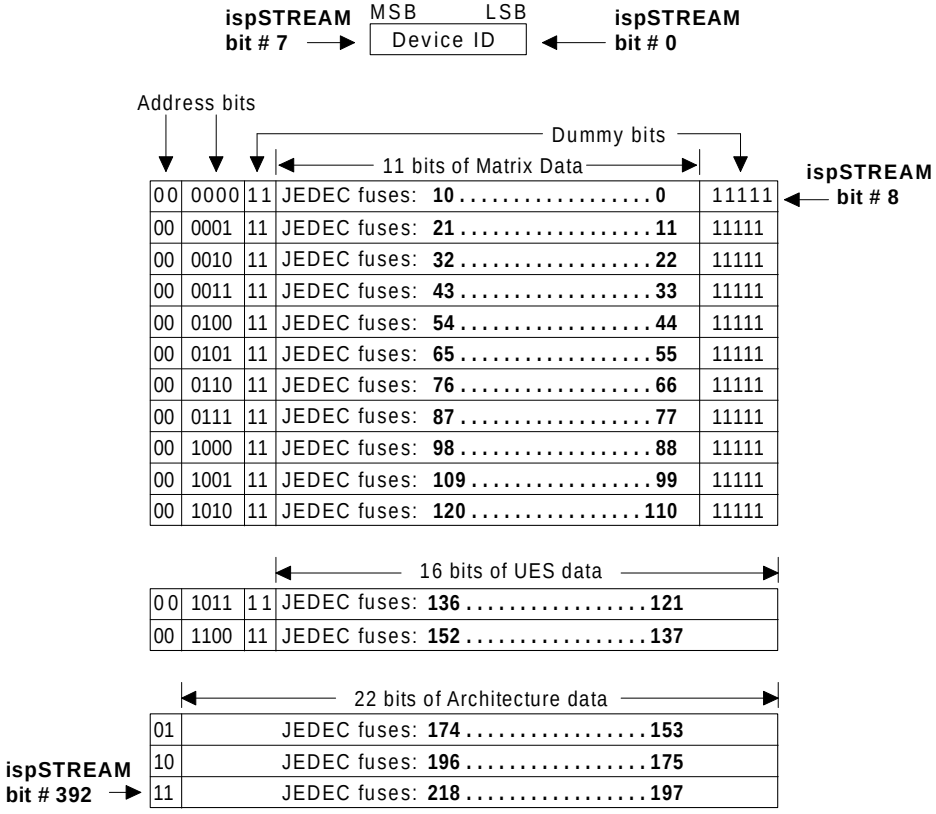


Figure 26. ispGDS ispSTREAM Format



Although the shift register lengths are 24 bits long, it is not composed entirely of data area. In the architectural section, two bits are used for addressing. In the matrix/ UES area, six bits are used for addressing. In the switch matrix area, there are only 11 bits of actual data, and seven dummy bits which exist only to make the shift registers the same length. These seven bits are read as a one, or a logic High on SDO. For the UES, there are 16 bits of actual data in each row and two dummy bits.

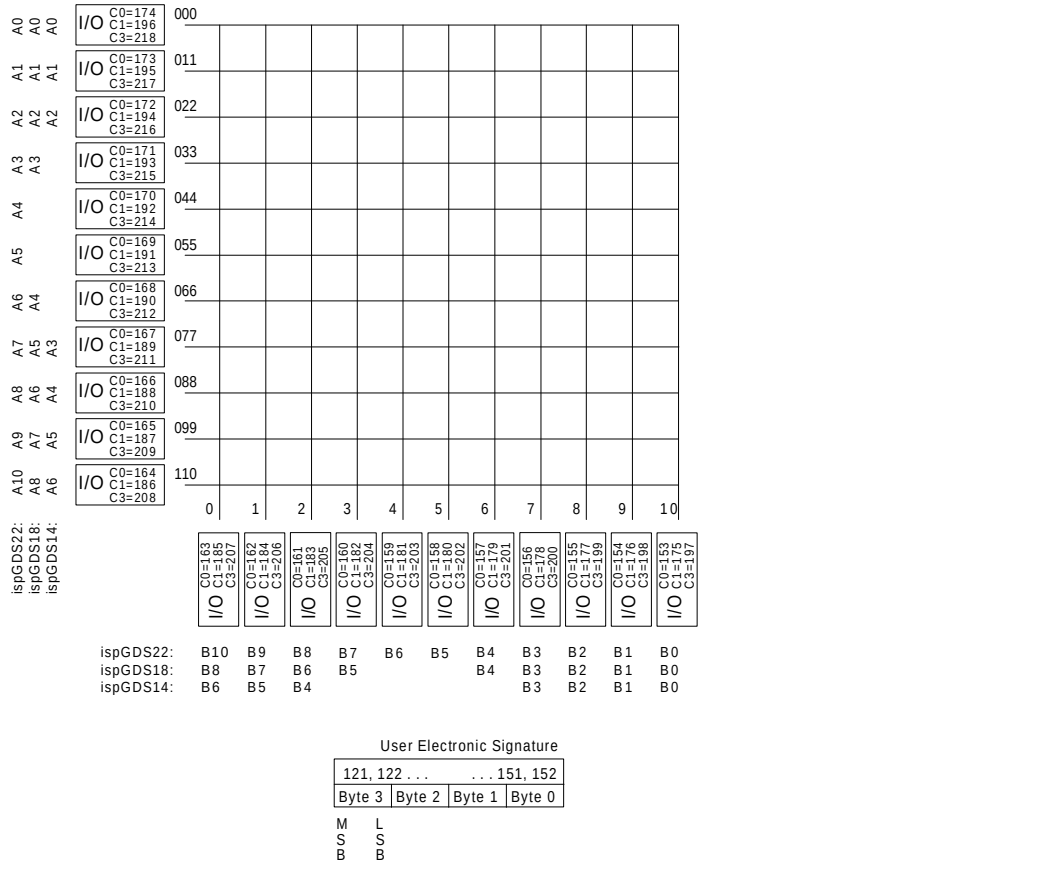
ispGDS ispSTREAM Format

To convert the information in a standard JEDEC file into the ispSTREAM format, add all of the addressing information and the placeholding bits (dummy bits). The objective is to include every bit needed for programming. For the three architecture rows, simply add the two address bits.

For the UES and Switch Matrix rows, there are eight bits to add. The first two bits are always 00, which distinguishes this area from the Architectural row. In addition, there are four bits needed to address the specific row, and two bits needed as placeholders. In the Switch Matrix rows, there are also 5 bits needed for placeholding at the end of the rows. The various placeholding bits are built into the device so that all rows appear to be the same length, thus simplifying programming operations.

The ispSTREAM uses one bit for each programmable cell. This means that each row includes 24 bits, or three *bytes* of storage. With three bytes of storage per row, and 16 rows per device, the ispSTREAM uses only 48 bytes of storage area. However, there is one extra byte used at the front of the file to store the device ID code, and a 32-bit checksum. The ID code is identical to the one that is hardwired into the device. This ID code ensures that the ispSTREAM type is the same as the device to be programmed. For example, if an ispSTREAM is stored in EPROM, it is stacked end to end. The ID code determines not only which device type the ispSTREAM belongs with, but its length, and thus, where the next pattern starts. All ispSTREAM formats, regardless of which Lattice In-System Programmable device they are intended for, contain this ID code in the first byte. See Figure 26 for details of the ispSTREAM format, and Figure 27 for the JEDEC map.

Figure 27. ispGDS JEDEC Fuse Map



Algorithms

ispGDS device programming is described as a hierarchical set of algorithms and functions. This section contains high-level algorithms for erasing, programming, verifying, and loading ispGDS devices. A universal set of functions is used to make up the algorithms and enable them to be written in a modular format. The individual functions are explained in the next section. Note that most procedures leave the device in the SHIFT state. These algorithms and functions closely follow the ispCODE source code library that Lattice Semiconductor provides.

To simplify the algorithms, all operations use an ispSTREAM format as the data structure from which to read and write. The ispSTREAM contains the address information and simplifies the operations considerably. Working from the ispSTREAM, the device appears as an array of 16 rows, each 24 bits long.

Program Algorithm

Before programming a device, it must be erased. Cells can be programmed (set to a JEDEC zero) using the programming command, but only an Erase procedure erases a cell (set a cell back to a JEDEC "1" (one)). In the algorithm in Listing 1, the entire device is erased (Bulk Erased), and then the entire device is programmed.

Listing 1. ispGDS Programming Algorithm

To program a device:

```
Call procedure: Get_ID ( to check device type)
Call procedure: Change_State ( from IDLE to SHIFT state)
(Erase entire device)
      Call procedure: Shift_Command, with command: ERASE
      Call procedure: Change_State (to EXECUTE State)
      Call procedure: Execute_Command (starts operation)
      Call procedure: Wait (Erase_Time)
      Call procedure: Change_State ( to SHIFT state)
Set row_count =0
Loop until row_count = 15
(Program one row on each loop)
      Call procedure: Shift_Command, with command: SHIFT_DATA
      Call procedure: Change_State (to EXECUTE State)
      Call procedure: Shift_Data_In, with data location in ispSTREAM at (row_count
      x 24)
      Call procedure: Change_State ( to SHIFT state)
      Call procedure: Shift_Command, with command: PROGRAM
      Call procedure: Change_State (to EXECUTE State)
      Call procedure: Execute_Command (starts operation)
      Call procedure: Wait (Program_Time)
      Call procedure: Change_State ( to SHIFT state)
End Loop
```

Load Algorithm

The load algorithm in Listing 2 is the same for all ispGDS devices. First, the 13 rows of array data (11 rows for the array matrix, and two for the UES) are read, and then the three rows of architectural information are read. After each row is read, it is stored in an ispSTREAM format.

In order to load each row's data into the shift register, it is necessary to load the address of the row into the appropriate area of the shift register. Because of the unique way the different areas of the device are addressed, the simplest way to get the addresses into the device in the proper order is to use an existing ispSTREAM to supply those addresses. In other words, the full data for each row is loaded from the ispSTREAM into the device. When a VERIFY command is executed, the device's data for the same row is then loaded into the shift register to be shifted out. This method will be used in this algorithm.

When using an existing ispSTREAM to supply the addresses, the data should not be the same as the expected data, or a failure to verify may not be detected. To avoid this possibility, a pattern that contains all "1s" (ones) for data can be used (and is supplied with the software tools provided by Lattice Semiconductor). This ispSTREAM still has the addresses intact, but all programmable cell data is set to a "1" (one) (erased state).

Listing 2. Load Algorithm

To load a device:

```
Call procedure: Get_ID ( to check device)
Call procedure: Change_State ( from IDLE to SHIFT state)
Set row_count =0
Loop until row_count = 15
      Call procedure: Shift_Command, with command: SHIFT_DATA
      Call procedure: Change_State (to EXECUTE State)
      Call procedure: Shift_Data_In, with data location in Source ispSTREAM at
(row_count x 24)
      Call procedure: Change_State ( to SHIFT state)
      Call procedure: Shift_Command, with command: PROGRAM
      Call procedure: Change_State (to EXECUTE State)
      Call procedure: Execute_Command (starts operation)
      Call procedure: Change_State ( to SHIFT state)
      Call procedure: Shift_Command, with command: SHIFT_DATA
      Call procedure: Change_State (to EXECUTE State)
      Call procedure: Shift_Data_Out, with data location in Target ispSTREAM at
      (row_count x 24)
      Call procedure: Change_State ( to SHIFT state)
End Loop
```

Verify Algorithm

A row by row verification procedure is used to verify the ispGDS device. This procedure is basically the same as the Load algorithm, except that each row is compared with (instead of stored in) an ispSTREAM as the data is shifted out of the device. Note that the special pattern used for verifying is used to load the addresses, as in the Load algorithm.

Listing 3. Verify Algorithm

To verify a device:

```
Call procedure: Get_ID (to check device type)
Call procedure: Change_State ( from IDLE to SHIFT state)
Set row_count =0
Loop until row_count = 15
      Call procedure: Shift_Command, with command: SHIFT_DATA
      Call procedure: Change_State (to EXECUTE State)
      Call procedure: Shift_Data_In, with data location in Source ispSTREAM at
(row_count x 24)
      Call procedure: Change_State ( to SHIFT state)
      Call procedure: Shift_Command, with command: VERIFY
      Call procedure: Change_State (to EXECUTE State)
      Call procedure: Execute_Command (starts operation)
      Call procedure: Wait (Verify_Time)
      Call procedure: Change_State ( to SHIFT state)
      Call procedure: Shift_Command, with command: SHIFT_DATA
      Call procedure: Change_State (to EXECUTE State)
      Call procedure: Shift_Data_Out, with data location a 24 bit temporary buffer
      Compare temp row buffer with data location in ispSTREAM to be verified
      against, at (row_count x 24) Verify Error if the 24 bits don't match
      Call procedure: Change_State ( to SHIFT state)
End Loop
```

ispGDS Procedures

This section describes the procedures that make up the program, verify, and load algorithms for the ispGDS family of devices. The procedures are written so that each algorithm may be written in a high-level modular format, calling one of the following procedures to actually change pin levels and handle timing.

Important: Notice that most of the procedures are written so that the state machine is left in the Shift State, ready to perform the next operation. This point is important in keeping all the routines compatible.

Goto_IDLE Procedure

The Goto_IDLE procedure resets the programming state machine to the IDLE state, regardless of which state it is in. Procedure steps:

set MODE pin High, and SDI pin Low

wait Tsu

bring SCLK pin High

wait Tclkh

bring SCLK pin Low

(END Procedure)

Get_ID Procedure

The 8-bit device ID codes identify the three different ispGDS devices (Table 12). The ID is read in the IDLE state by first loading the ID into the shift register and then clocking the data out. The ID is loaded by holding MODE high and SDI low and clocking the device. The ID is clocked out of the device by holding MODE low and clocking SCLK. Only seven clock cycles are required, since the first bit is available at SDO after the ID is loaded.

Table 13. ispGDS Device Codes

Device	Pins	Device ID
ispGDS22	28	0111 0010 (72 hex)
ispGDS18	24	0111 0001 (71 hex)
ispGDS14	20	0111 0000 (70 hex)

Procedure steps:

set MODE pin High, and SDI pin Low

wait Tsu

Set SCLK pin High

wait Tclkh

Set SCLK pin Low

set count =0

get value from SDO and store in temp_buffer[0]

set count = 1

loop until count == 7

    bring SCLK pin High

    wait Twh

    bring SCLK pin Low

    wait Twl

    get value from SDO and store in temp_buffer[count]

End loop

(Device ID code is now stored in the temp_buffer array)

(END procedure)

Change_State Procedure

The Change_State procedure changes the programming state machine to the next state, according to the state diagram. Procedure steps:

set MODE pin High, and SDI pin High

wait Tsu

bring SCLK pin High

wait Th

set MODE pin Low, and SDI pin Low

wait Tclkh

bring SCLK pin Low

(END Procedure)

Shift_ Command Procedure

The Shift_Command procedure shifts a five-bit command into the device's shift register. The various commands should be coded so the procedure can use a mnemonic (such as PROGRAM), and the controlling software can use the appropriate five-bit sequence for that command. Procedure steps:

set MODE pin Low

set count =0

loop until count == 4

get next bit of command code (count = bit number)

set SDI pin to bit value

wait Tsu

bring SCLK pin High

wait Tclkh

bring SCLK pin Low

count = count +1

End loop

(END Procedure)

Shift_ Data_In Procedure

The Shift_Data_In procedure explains the steps to clock a row of data into the device, reading the data from an ispSTREAM. This procedure shifts in 22 bits of data, and is used for all 16 rows. Procedure steps:

set MODE pin Low

set count =0

loop until count == 23

get next bit from ispSTREAM (bit number = count x row_number)

set SDI pin to bit value

wait Tsu

bring SCLK pin High

wait Tclkh

bring SCLK pin Low

End loop

(END Procedure)

Shift_ Data_Out Procedure

The Shift_Data_In procedure explains the steps to clock a row of data out of the device and store it in an ispSTREAM. This procedure shifts out 22 bits of data, and is used for all 16 rows. Procedure steps:

set MODE pin Low

wait Tsu

set count =0

loop until count == 23

bring SCLK pin High

wait Tclkh

bring SCLK pin Low

get value of SDO pin and store as next bit in ispSTREAM (bit number = count x row_number)

End loop

(END Procedure)

Execute_Command Procedure

The Execute_Command procedure causes many of the commands to begin executing after the state machine is in the EXECUTE state. Procedure steps:

set MODE pin Low, and SDI pin Low

wait Tsu

bring SCLK pin High

wait Twh

bring SCLK pin Low

(END Procedure)

Wait Procedure

The Wait procedure waits the indicated time to ensure that various timing parameters are met. This procedure is likely to be used when executing the PROGRAM and ERASE procedures, which need a long delay (tens of milliseconds). The other timing parameters may be guaranteed by the system timing. Various timing parameters should be coded so that a mnemonic may be passed to the procedure. Procedure steps:

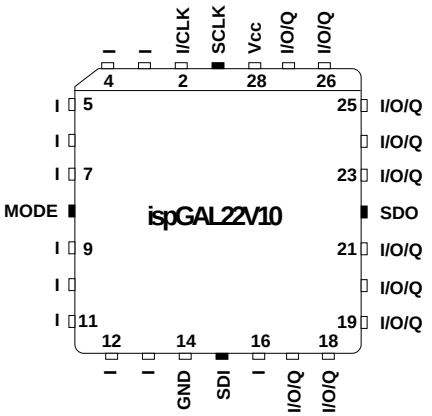
wait the indicated time

(END Procedure)

ispGAL Programming Details

The following sections describe the state machine instruction set, timing parameters, and device layout as they apply to ispGAL devices in general. Figure 28 shows the ispGAL22V10 28-pin device pinout.

Figure 28. ispGAL22V10 28-Pin PLCC Pinout Diagram



Shift Registers

The ispGAL device has four shift registers: Device ID, Instruction, Data, and Architecture. All shift registers operate on a First In-First Out (FIFO) basis, and are enabled by the programming state machine.

The Device ID shift register is only accessible in the IDLE state. It is eight bits long, and is only used to shift out the device ID. For the ispGAL22V10, the ID is defined to be 08 (hex). The Instruction shift register is only accessible in the SHIFT state. It is five bits long, and is only used to shift the Instruction Codes into the device. The Data and Instruction shift registers expect the LSB to be shifted in first. The Data shift register is 138 bits long, and is used to shift all addresses and data into or out of the device. The Data shift register is only accessible in the EXECUTE state when executing a SHIFT_DATA instruction. The Architecture shift register is 20 bits long and the Output Logic Macro Cell (OLMC) 1's S1 architecture bit is shifted in first and OLMC 10's S0 architecture bit is shifted in last. The Architecture shift register is accessed during the EXECUTE state, when the ARCH_SHIFT instruction is executed.

To program an ispGAL device, data is read from a serial bit stream and shifted into the shift registers. The data is read 138 bits at a time, shifted into the device, and then programmed into the device through a programming operation. Table 14 describes the instructions for the ispGAL state machine. The exact sequence and methods for converting a JEDEC map into a serial bit stream are explained in the Internal Architecture section.

Timing

Programming the ispGAL devices properly requires that a number of timing specifications be met. Most critical are the specifications relating to programming and erasing the E^2CMOS cells. In addition to a minimum pulse width, there is also a maximum specification for these parameters. Refer to the ispGAL programming mode timing specifications for the timing requirements (Table 12), which are identical to the ispGDS specifications. Diagrams for the programming mode specifications are shown in Figures 22, 23, and 24 of the ispGDS timing section.

Table 14. ispGAL Programming State Machine Instruction Set

Instruction	Operation	Description
00000	NOP	No operation performed.
00010	SHIFT_DATA	Clocks data into, or out of, the Data Shift Register.
00011	BULK_ERASE	Erases the entire device.
00101	ERASE_ARRAY	Erases everything except the Architecture rows.
00110	ERASE_ARCH	Erases the Architecture rows only
00111	PROGRAM	Programs the Serial Shift Register data into the addressed row
01010	VERIFY	Load data from the selected row into the Serial Shift Register.
01101	IOPRLD	Preload the I/O register with given data.
01110	FLOWTHRU	Disables the Shift Register (SDI=SDO).
10100	ARCH SHIFT	Enables the Architecture shift register for shifting data into or out of the register.

Securing an ispGAL Device

The ispGAL devices are not secured by an instruction. To secure ispGAL devices, row 61 must be programmed in the same manner that other data rows are programmed. When programming this security row, the data bits are "don't care."

Internal Architecture

This section describes the internal architecture of the device as it relates to programming.

This section covers details of constructing the ispSTREAM format. If you are using the supplied software tools, a conversion utility (complete with source code) is included to convert an industry-standard JEDEC file to ispSTREAM format. All of the Lattice Semiconductor software routines read and write the ispSTREAM format.

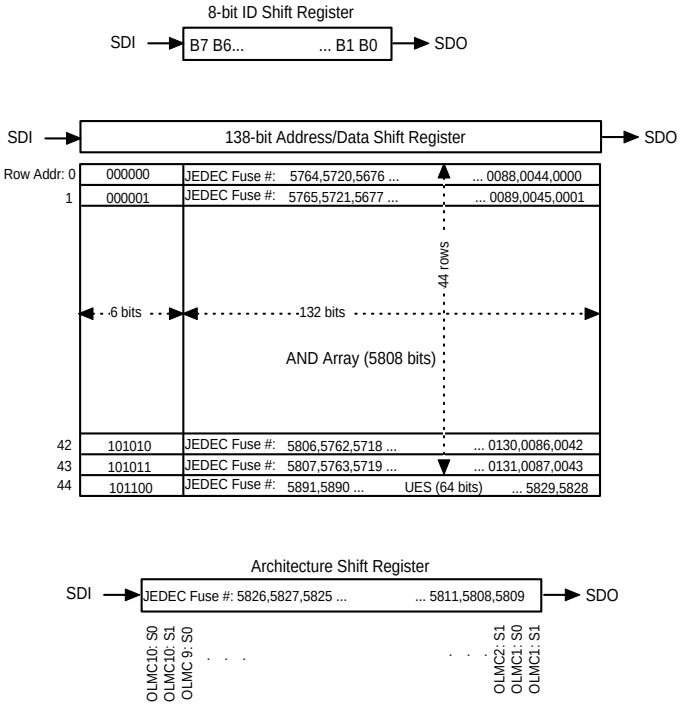
Three components comprise the ispGAL device programming architecture (Figure 29): 44, 132-bit rows of AND array, one 64-bit row of User Electronic Signature (UES), and one 20-bit row of architecture information.

The AND array section of the physical layout is organized so that each column of JEDEC fuse numbers shown in the logic diagram of the ispGAL22V10 corresponds to one row of shift register for the device layout. Each physical row is 132 bits long. With each row of AND array data, there is a 6-bit row address associated with it, which including the row address bits, makes the shift registers 138 bits long. The row address bits must be shifted into the shift register along with the AND array data. Executing a PROGRAM command following the combination of data and row address shift programs the row that is specified by the shift instruction.

The I/O preload (IOPRLD) is performed in the same order as the Architecture shift register shown in Figure 29. Once in I/O Preload, the length of the shift register is determined by the number of I/Os that are configured as registered output. The length of the shift register and the order must be determined before IOPRLD can be executed.

The UES row is unique in that it is only 64 bits long. When the row address bits are added to the row itself, the total shift register length required to fully specify the UES row is 70 bits long. In other words, only 70 bits out of the 132-bit shift register are used for the UES. The 20-bit Architecture shift register is selected when the ARCH_SHIFT instruction is executed. The OLMC 0, S1: OLMC 0, S0; OLMC 1, S1: OLMC 1, S0: etc. are shifted in order with the last bit of the shift register being OLMC 10, S0.

Figure 29. ispGAL Device Shift Register Layout



Algorithms and Procedures

The ispGAL's programming algorithm and programming procedure are very similar to the ispGDS. For the sake of brevity, please refer to the algorithm and procedures section in the ispGDS section if you are interested in this information. If you have further questions, please call the Lattice Semiconductor Hotline at 1-800-FASTGAL.

ISP Daisy Chain Details

This section provides a detailed look at the issues associated with daisy chain programming. Before examining the details, the reader should understand the differences between ISP devices. This section describes those differences and the unique programming features of each ISP device.

ISP Overview for Daisy Chain

Similarities and Differences Between Devices

For the purpose of cascading, ISP devices can be categorized into two device groups: ispLSI and ispGDS/ispGAL. Table 15 highlights the similarities between these device groups.

Using the same state machine controls makes it possible to program multiple ISP devices by operating all the cascaded devices' state machines in parallel. This synchronizes all the devices during programming within the daisy chain to a known state. However, having all ISP devices in the same state does not mean that all devices are executing the same instruction. The ability of each device in the daisy chain to execute a different instruction makes it possible to selectively program one or multiple ISP devices at a time.

For the ispLSI devices, the active $\overline{\text{ispEN}}$ signal enables the programming mode. By driving $\overline{\text{ispEN}}$ low, all of the device I/Os are put into a high-impedance state for programming and the programming functions for SDI, SDO, Mode and SCLK are enabled.

For the ispGDS and ispGAL devices, on the other hand, the I/Os are put into a high-impedance state when the programming state machine goes into the Command Shift State. The ispGDS and ispGAL devices do not use a dedicated $\overline{\text{ispEN}}$ pin for this function.

Most shift operations, such as ID shift and command shift, are the same for the ispLSI and the ispGDS/ispGAL devices. However, one difference exists in the way that the address and data are shifted into the devices. The ispLSI devices have separate address and data shift commands. The row(s) are selected by the address that is shifted-in prior to each programming command. The data can then be shifted with the data shift instruction. With ispGDS and ispGAL devices, both address and data are shifted-in with a single shift command (the address is part of the Data shift register). When executing commands that only require a row address, a dummy data stream or no data can be shifted in place of the data stream.

ISP Daisy Chain Programming

A specific illustration of multiple device programming in a daisy chained environment is shown in Figure 1. The example shows ISP programming aspects such as identifying the devices in the daisy chain, shifting commands, bypassing devices, and executing commands.

All of the programming state machines run in parallel which keeps the devices synchronized. The programming information for the ISP devices is summarized in Table 16. Similar details for any ISP device can be found

Table 15. Features of the ISP Device Families

		ispLSI	ispGDS/ispGAL
Common	ID shift register length	8-Bits	8-Bits
	Command shift register length	5-Bits	5-Bits
	Programming signals	MODE, SDI, SDO & SCLK	MODE, SDI, SDO & SCLK
	State machine	3-state with same MODE and SDI controls for state transitions	3-state with same MODE and SDI controls for state transitions
	FLOWTHRU instruction	Yes	Yes
Different	ispEN signal	Yes	No
	Address and data shift register	Different shift instructions for address and data	Both address and data is shifted with one shift command.
	Fuse map sizes	Varies for different high density devices	Varies for different low density devices.

in the ISP Architecture and Programming section of this Data Book and in the appropriate device data sheet.

The first procedure of the programming sequence identifies the devices in the ISP chain. The following procedure describes one way of reading the device IDs.

Load_ID Procedure

set $\overline{\text{ispEN}}$ = L

set MODE, SDI = H, L

clock SCLK (Load ID)

Continue to Shift_ID Procedure ...

At this point, the 8-bit ID registers are loaded with the hardwired device IDs. Figure 30 shows the configuration of the ID shift registers.

After the device ID has been loaded, the following shift ID procedure sequentially shifts the IDs through to the last device's SDO. While the ID is being shifted out, keep SDI at a known logic level so that the end of the ID stream can be identified. This is especially important when there are an unknown number of devices in the ISP daisy chain. By detecting a sequence of eight zeros or eight ones, the ISP controller can detect the end of the ID string.

Shift_ID Procedure

... Continued from Load_ID Procedure

set MODE, SDI = L, H

clock SCLK (Shift ID)

if last 8 SDO = H then go to End

else go to Shift_ID

End

Now, all of the devices within the ISP daisy chain and their order can be properly identified. The next step is to match the proper JEDEC fuse map file to the appropriate device. There are several programming options at this point. To simplify the programming routines however, this example programs the devices one at a time. In programming time critical applications, the daisy chained devices can be programmed in parallel. The parallel programming routines must keep track of the differences in the fuse map lengths between different ISP devices.

The following procedures illustrate how to shift commands, shift data, and execute commands to program the ispGAL22V10. Since the ispGAL22V10 is the second device in the ISP daisy chain, these procedures also illustrate how to put the other devices into flow-through mode. The following procedure shifts the SHIFT_DATA command into the ispGAL22V10 and the FLOWTHRU command into the rest of the ISP devices.

Load_Command Procedure

... Continued from end of Shift_ID Procedure

set MODE, SDI = H, H

clock SCLK (Shift State)

set MODE = L

Loop

set SDI = command stream (Figure 26B)

clock SCLK (Shift Command)

End Loop

End Procedure

Table 16. ISP Programming Information

Description	ispLSI 1032	ispGAL22V10	ispGDS22	ispLSI 2032
Device ID (8-bits)	0000 0011	0000 1000	0111 0010	0001 0101
Command Register	5 bits	5 bits	5 bits	5 bits
Address Shift Register	108 bits	n/a	n/a	102 bits
Data/Addr. & Data Shift Register	160 bits	(6+132) bits	(6+18) bits	40 bits

Execute_Command Procedure

set MODE, SDI = H, H

clock SCLK (Execute State)

set MODE = L

Loop 138 times

set SDI = data stream (Figure 26C)

clock SCLK (Execute SHIFT_DATA Command)

End Loop

set MODE, SDI = H, H

clock SCLK (Shift State)

End Procedure

At the end of the Execute_Command procedure, the state machine is returned to the Shift State. This readies the devices for another command shift procedure. For the ispGAL22V10, the DATA_SHIFT instruction of 138 bits includes the row address and the data associated with the row. Similar procedures can be used to complete the programming of the ispGAL22V10.

Figure 30a. ID Shift Register Configuration

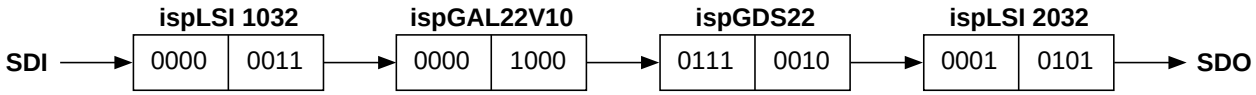


Figure 30b. ISP Command Stream

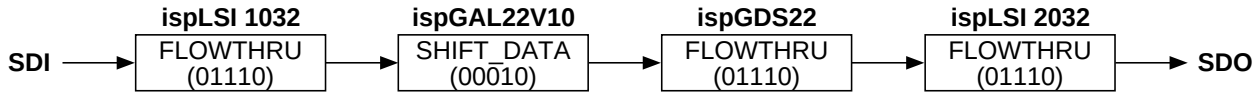
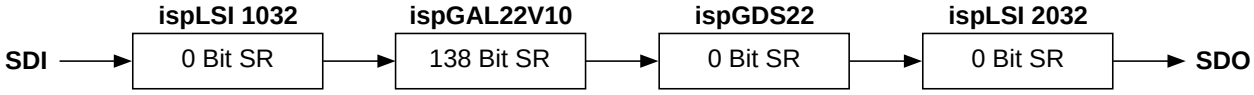


Figure 30c. ISP Data Stream



ISP™ Cost-of-Ownership Analysis

What is Cost-of-Ownership?

Cost-of-ownership is defined as the total of all costs incurred throughout the life and use of a component, that can be directly attributed to that component. The life of a programmable logic device (PLD) begins with the System Design Phase, extends through the System Manufacturing Phase, and goes beyond initial system shipments into the Field Repair and Update Phase. In most cases, the initial purchase price—the standard by which engineers and purchasing agents often judge component costs—is only a fraction of the total cost incurred by a component during its lifecycle.

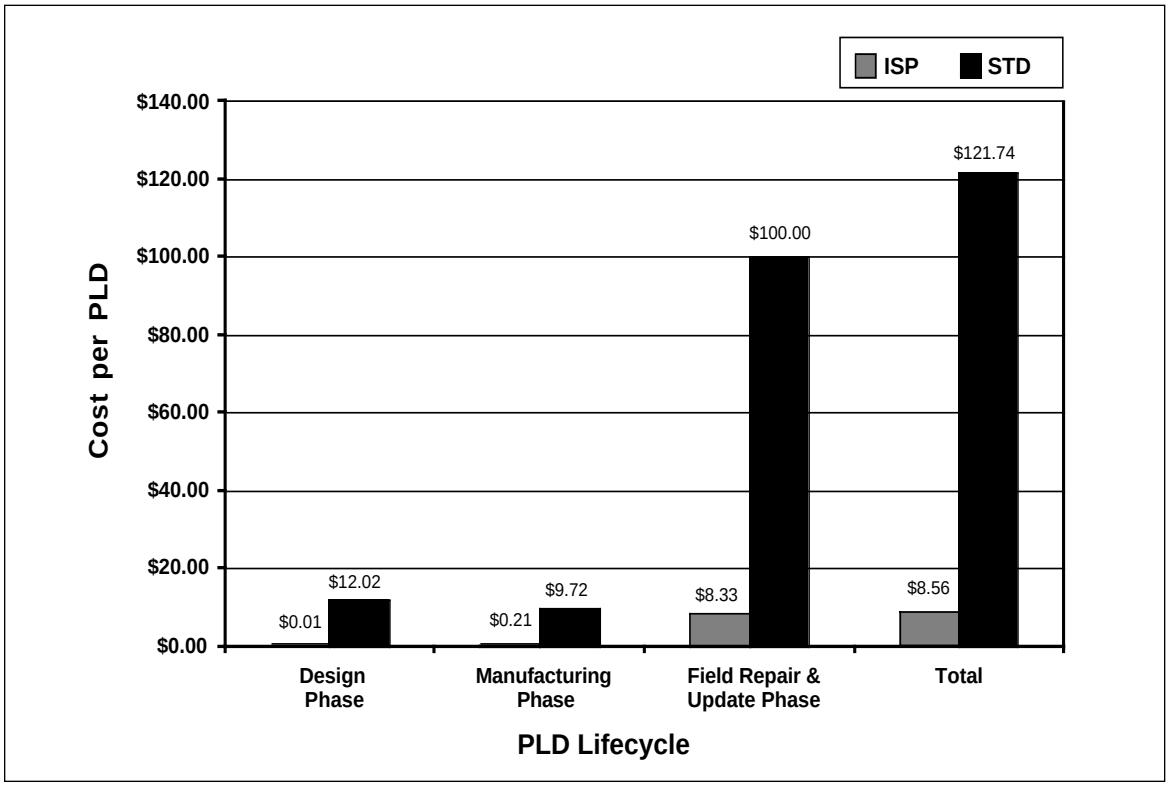
The ISP Cost-of-Ownership Model

This document uses the In-System Programmable™ (ISP™) Cost-of-Ownership Model (hereafter referred to as the "model") to compare the cost-of-ownership for ISP and standard PLDs at each stage of their lifecycles:

- During the **System Design Phase**, the model illustrates the direct costs of prototype PLDs and sockets as well as the associated prototype device programming costs. It also explores the less obvious, yet potentially more significant opportunity cost of time-to-market— the time it takes a product to move from idea to production.
- In the **System Manufacturing Phase**, the model describes five cost categories, including production programming, PLD inventory costs, obsolete PLD inventory costs, general manufacturing costs, and quality and reliability costs.
- The last phase of the model, the **Field Repair and Update Phase**, explores the cost of updating systems that use PLDs which have already been installed in the field.

This model has been developed largely from the input of Lattice Semiconductor Corporation (LSC) customers who have implemented ISP solutions in their systems and

Figure 1. Incremental PLD Cost-of-Ownership



manufacturing environments. The model describes the overall PLD costs involved in the lifecycle of an average or typical system. However, no system is average or typical. Thus, it is expected that the reader will assign different levels of importance to the various elements of cost described. The reader is also encouraged to calculate cost estimates based on his or her own situation using the model as a template.

The ISP Cost-of-Ownership Metric

Figure 1 (see page 1) summarizes the cost elements associated with each phase of a component's lifecycle and the impact of these elements on total PLD cost-of-ownership. This figure illustrates the difference in overall PLD cost structure associated with the two PLD types. The balance of the model will document these cost elements and their calculations. Some calculations presented may contain slight rounding errors when a fixed number of decimal places is used (generally two or three).

PLD Categories Compared

This model divides PLDs (both low- and high-density) into two basic categories—in-system programmable PLDs and standard PLDs:

- **In-System Programmable (ISP) PLDs—**This category features PLDs which can be configured and reconfigured electrically while "in-system." LSC offers three ISP product families: ispLSI®, ispGAL®, and ispGDS™. These families share the same non-volatile ISP E²CMOS™ process technology and ISP programming algorithm.
- **Standard PLDs (STD)—**Standard PLDs consist of conventional PLD technologies which do not support in-system programmability. Primarily, this covers erasable technologies such as EPROM and EEPROM, but also extends to one-time programmable (OTP) technologies such as bipolar and anti-fuse.

The specific cost examples discussed in this model generally focus on standard PLDs which are electrically erasable but do not support in-system programmability. OTP PLD technologies such as anti-fuse, bipolar and EPROM in OTP plastic packages are not featured for a number of reasons:

- The vast majority of new PLD designs use either ISP, EPROM or EEPROM technology.
- The cost-of-ownership for OTP-based PLDs is dramatically higher than for any of these erasable PLDs:
  - By definition, OTP PLDs cannot be reconfigured. Thus, any code changes result in device scrap.
  - Programming yields are much lower; OTP PLDs cannot be 100% tested prior to user configuration.
  - Programming times for OTP PLDs are typically much longer than for other PLDs.
  - OTP PLDs offer none of the benefits of ISP.

Model Assumptions

- The end equipment is an electronic system with an average selling price of $5,000.
- The lifetime (three-year) system volume is 15,000 systems ($75,000,000 total revenue).
- Five prototype systems are required prior to production release.
- One of the boards in the system contains three 6,000-gate high density PLDs or field programmable gate arrays (FPGAs). The model assumes two versions of this board, requiring two separate sets of interface logic.
- The PLDs use a high pin-count quad flat pack (QFP) package.
- The PLD purchase price is $30 for prototypes, $15 in volume.
- The system lifetime PLD usage is 45,000 units (15,000 systems at three PLDs per system).
- The design engineering pay rate is $12,000 per month (or $3,000 per week), including salary and benefits.
- Board rework labor costs are $300 per board.

System Design Phase

As stated earlier, the purchase price of a PLD should be viewed only as the starting point for calculating the total cost-of-ownership. A designer's PLD choice can have a dramatic impact on costs incurred—or avoided—during the System Design Phase.

Prototype Sockets

ISP PLDs can be soldered directly onto the prototype circuit board and still accommodate design iterations by simply reconfiguring the devices in-system, eliminating the need for prototype sockets.

Standard PLDs, however, require sockets on the circuit board which must be removed and reprogrammed for each design iteration. The model assumes that the board's production configuration includes surface mounted PLDs, versus socketed (see Table 1). Surface mounted PLDs require the use of socket adapters during prototyping which are footprint compatible with the surface mount PLD package (QFP assumed). These socket adapters cost approximately $500 each (source: 100pc pricing from Emulation Technology). Standard through-hole socket adapters can also be used at a cost of approximately $75 each. However, a final respin of the board is required after debug to remove the socket adapters and layout the board for the PLD footprint. The respin costs at least $3,000 and is not without risk of error and project delay.

Table 1. Prototype Socket Costs

Prototype Socket Costs	ISP	STD
Quantity of prototype sockets (five prototype systems)	N/A	15
Prototype socket cost (PLD footprint compatible)	N/A	$500
Total prototype socket costs	N/A	$7,500
Prototype socket costs per 45,000 production PLDs	$0.000	$0.167

There are many designs whose critical timing requirements make using prototype sockets unacceptable. Sockets add extra loading on signal paths reducing performance. For these designs, the use of standard PLDs forces the designer to solder and desolder the prototype PLD for each revision of code. After two or three cycles, the prototype board is unworkable and must be replaced with a new prototype board and the associated board components. These costs—all of which are avoided with ISP PLDs—are not included in the model.

The use of standard PLDs results in the expenditure of $7,500 for prototype sockets, which when amortized over the 45,000 system lifetime PLD usage, adds almost $0.17 to the purchase price of each PLD.

Prototype Silicon

The number of prototype ISP PLDs required can be calculated by simply multiplying the required prototype systems by the number of PLDs per system. These devices can be soldered to the circuit board and reconfigured in-system as needed as the design matures. As a result, there is no device scrap.

Standard PLDs require two socketings for each pattern iteration (one socketing at the programmer and a second on the circuit board). In higher pin-count QFP packages with their fragile leads, two pattern iterations can cause enough lead damage to make them unusable. The model assumes a conservative 33% yield loss (five devices) over the course of the prototype phase (see Table 2).

Table 2. Prototype Silicon Costs

Prototype Silicon Costs	ISP	STD
Quantity of prototype PLDs (five prototype systems)	15	15
Handling/socketing fallout rate (QFP package)	0%	33%
Replacement PLDs (handling damage)	0	5
Total prototype PLDs required	15	20
Prototype PLD costs	$450	$600
Prototype PLD costs per per 45,000 production PLDs	$0.010	$0.013

During prototyping, ISP PLD users can achieve a savings of $150 over standard PLD users.

Prototype Programming Costs

One of the major costs incurred during the System Design Phase is the cost of device programming. A designer using ISP technology simply solders an ISP device onto the prototype board and downloads design iterations via a download cable. LSC offers the

ispDOWNLOAD™ Cable for $65. This cable is also available at no cost with the purchase of any of LSC's Logic Development Systems.

With standard PLDs, a stand-alone, third-party PLD programmer (approximate cost, $5,000) is required to pattern the devices. The model assumes that the cost of the programmer will be depreciated over a five-year period (see Table 3).

Further, the model assumes that the programmer is shared by five designers, each working on four projects per year. The ISP designer is able to complete six projects per year, for reasons explained in the next section.

Table 3. Prototype Programming Costs

Prototype Programming Costs	ISP	STD
Programmer costs	$65.00	$5,000.00
Annual depreciation (assume five-year life)	$13.00	$1,000.00
Annual updates (15% of purchase price)	$0.00	$750.00
Programmer costs/year	$13.00	$1,750.00
Number of designers/programmer	1	5
Design projects/year/designer	6	4
Quantity of prototype PLDs/project	15	15
Total prototype PLDs/year	90	300
Programmer costs/prototype PLD	$0.14	$5.83
Programmer costs/project	$2.17	$87.50
Programmer costs per 45,000 production PLDs	$0.000	$0.002

With ISP, each designer is given his or her own $65.00 "programmer" at a per project cost of $2.17 versus the standard PLD approach costing over $87.00 per project.

"Time is money! With Lattice ispLSI devices, we are able to do our development in one-fifth the time it would take with competitive FPGA solutions."

—William A. Long, Vice President of Engineering, Micronet Corporation, winner of the 1990 and 1991 Storage Product of the Year Award from MacUser Magazine

"Prototyping with the ispLSI 1032 cut more than 50% off our development and debug time. Design changes that once took half a day are now handled in minutes!"

—Alan Beverly, Engineering Manager, Ziatech Corporation

Time-to-Market Opportunity Costs

The most significant advantage for ISP technology during the System Design Phase is its dramatic impact on reducing system design cycle time. Both Ziatech and Micronet can attest to this fact.

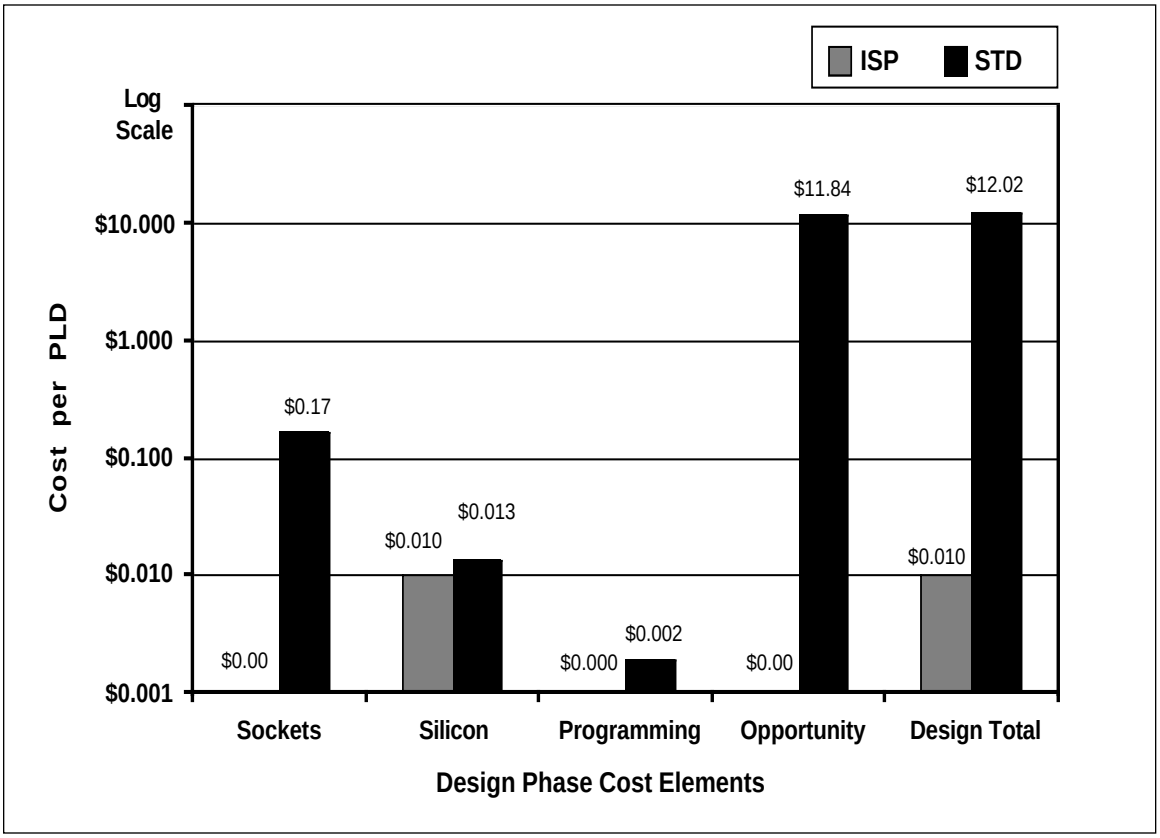
This model assumes a 33% ISP product development cycle time reduction from three months to two months, translating directly into a time-to-market advantage. Every day saved in system design equals a one-day gain in product availability, revenue generation, and corporate net margin contribution (assumed at 25% of revenue). With ISP, the system can be launched into the marketplace one month earlier than in the standard PLD scenario, resulting in $521,000 in incremental corporate profits. A decision to design with standard PLDs is a decision to forego these corporate profits.

Use of standard PLDs also requires a design engineer to remain on a project for an additional month (at a cost of $12,000), delaying his or her work on the next system generation.

Table 4. Time-To-Market Opportunity Cost

Time-to-Market Opportunity Cost	ISP	STD
Lifetime system revenue	$75,000,000	$75,000,000
System revenue/month	$2,083,833	$2,083,333
After tax contribution margin	25%	25%
Margin contribution/month	$520,833	$520,833
Design cycle time (months)	2	3
Product intro delay (months)	0	1
Cycle time opportunity cost	N/A	$520,833
Incremental engineering costs	N/A	$12,000
Total opportunity cost	N/A	$532,833
Opportunty cost per 45,000 production PLDs	$0.00	$11.84

Figure 2. System Design Cost-of-Ownership



The opportunity cost of choosing the standard PLD approach is $533,000, adding $11.84 to the original purchase price of the standard PLD.

System Design Phase Summary

As shown in Figure 2, the most significant component cost incurred by the standard PLD during the System Design Phase is the opportunity cost, which contributes $533,000—almost an additional $12 to the $15 original purchase price of the PLD—for an increase of 80%. The standard PLD component cost contributions (prototype sockets, silicon and programming) are relatively small by comparison, but each is dramatically higher than for the ISP PLD scenario, adding over $8,000 to the overall project development costs.

System Manufacturing Phase

In the system manufacturing arena, costs continue to escalate if PLDs which do not integrate smoothly into the board/system process flow are used. Failures after board/system assembly are very expensive to detect and repair.

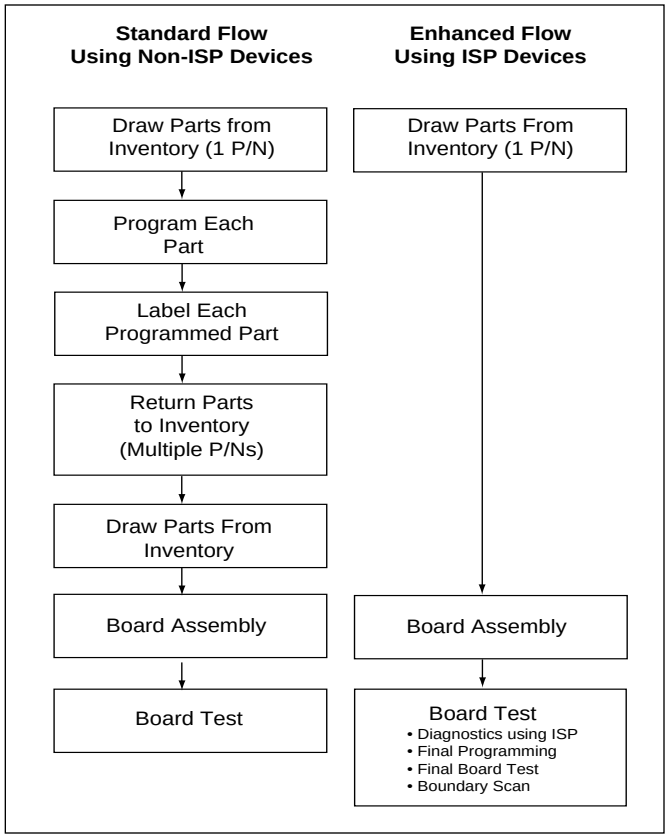
Programming Costs

One of the most exciting benefits of ISP PLDs is the ability to eliminate the stand-alone programming and mark steps from the manufacturing flow. As shown in Figure 3 (see next page), PLD device programming can be integrated into final board-level testing, thus eliminating the problems and expense inherent in the traditional PLD programming flow. Tables 5 through 9 outline the cost

Table 5. Base Programming/Mark Costs

Base Programming/ Mark Costs (QFP)	ISP	STD
Programming unit costs	$0.80	$0.50
Mark unit costs	$0.00	$0.15
Total program/mark costs per device	$0.80	$0.65

Figure 3. ISP Manufacturing Flow



elements associated with the production programming of ISP and standard PLDs.

The model establishes a base device programming and mark (or label) cost for ISP and standard PLDs (see Table 5, previous page). The standard PLD programming and mark costs were derived after consulting with a number of large electronics distributors. For high-density PLDs in QFP packages, the charges ranged from $0.50 to over $1.00. The model assumes a conservative $0.50 for programming and an additional $0.15 for marking a standard PLD.

For ISP PLDs, device programming occurs during final board testing using PC, workstation or standard ATE equipment (such as Hewlett Packard, Teradyne or GenRad). There is no need for device labeling since the blank ISP PLDs have already been soldered onto the board. ATE programming ensures that the correct device pattern is programmed into the correct PLD. An electrical device identification can be programmed into each device's user electronic signature (UES) for easy tracking of pattern revisions.

The model uses an $0.08 cost per device for programming ISP PLDs via ATE (see Table 6). A $200,000

Table 6. ATE Programming Costs

ATE Programming (QFP Package)	ISP
ATE board tester cost	$200,000
Annual depreciation (over five years)	$40,000
Annual maintenance (15% purchase price)	$30,000
Annual equipment/maintenance costs	$70,000
Base equipment cost/hour	$10.13
Operator wages/hour	$12.15
Total base programming costs	$22.28
Utilization cost adder (assume 80%)	$5.57
Efficiency cost adder (assume 80%)	$5.57
Net ATE programming costs/hour	$33.42
ATE programming costs/second	$0.0093
100-pin QFP programming time (seconds)	8.64
100-pin QFP programming cost	$0.080

combinational board tester (Hewlett Packard 3070 class) is assumed, depreciated over five years, including annual maintenance, for a total of $70,000 in annual equipment expenses. After adding operator wages, and utilization and efficiency adders (including tester "up time," shift changes, lunches, breaks etc.), the ATE costs $33.42 per hour. An ATE can program an ISP PLD in a little over eight seconds which drives the $0.08 per device ISP programming cost (*ISP Manual*, page 2-10) .

Table 7 documents the programming yield assumptions used in this cost analysis. The model recognizes that the 100% testability of both the ISP and electrically erasable standard PLD technologies makes programming and functional yield loss virtually nonexistent. This is not the case for OTP PLD technologies which cannot be fully tested prior to user programming. There is, however, a

Table 7. Programming Yield Assumptions

Programming Yield Assumptions	ISP	STD
Yield assumptions:		
First pass handling yield loss	0%	20%
Second pass handling yield loss (unrecoverable)	0%	30%
Net handling yield loss	0%	6%
Programming yield loss	0%	0%
Functional yield loss	0%	0%
Cumulative yield loss	0%	6%

significant element of programming yield loss associated with standard PLDs in QFP packages. With fragile leads requiring hand socketing in a stand-alone programmer, fallout rates of 30% and higher are common. The model assumes a 20% first pass handling yield loss with the further assumption that 70% of those failures can be successfully reworked and reprogrammed.

With these yield assumptions, the model examines the programming cycle costs, assuming a PLD quantity of 45,000 over the life of the system (see Table 8). The standard PLD scenario requires the purchase of an additional 2,700 devices to replace those irreparably damaged in handling. Programming and mark costs for standard PLDs are 10 times greater than for ISP PLDs ($31,000 vs. $3,600). The purchase of the extra 2,700 standard PLDs adds an additional $40,500 (2,700 units @ $15 per unit). The handling rework charges for the standard PLD approach add another $9,000 based on rescreening 9,000 devices, each incurring a $0.50 lead straightening and $0.50 programming charge.

Table 8. Program, Mark & Replacement Costs

Programming, Mark and Replacement PLD Costs	ISP	STD
First pass programming:		
Initial PLD quantity	45,000	45,000
Replacement PLDs (from yield loss)	0	2,700
Total quantity of PLDs required	45,000	47,700
Programming/mark costs	$3,608.93	$31,005.00
Incremental PLD purchase costs	$0.00	$40,500.00
Handling rework costs:		
Number of units needing rework	0	9,000
Lead straightening charge	N/A	$0.50
Programming charge	N/A	$0.50
Total rework charge/unit	N/A	$1.00
Total rework charges	$0.00	$9,000.00
Total programming/mark costs	$3,608.93	$80,505.00
Total programming costs per 45,000 production PLDs	$0.08	$1.79

Total programming costs for ISP PLDs add only $0.08 to overall cost-of-ownership, while programming costs for standard PLDs add an incremental $1.79 to the original component purchase price.

PLD Inventory Costs

ISP PLDs dramatically simplify PLD inventory strategies by requiring a single unprogrammed part number to be forecasted, ordered, received, inventoried and issued to manufacturing. When standard PLDs are procured in the pre-patterned state, six unique part numbers must be tracked from forecast through manufacturing. For standard PLDs programmed in-house, the single PLD part number becomes six separate part numbers after the programming step.

As illustrated in Figure 4 (see next page), ISP PLDs can reduce on-hand PLD inventories by half. For example, six weeks of standard PLD inventories can shrink to three weeks of ISP PLD inventories. And, ISP PLDs provide enhanced manufacturing flexibility since these inventories are not customized until final board test.

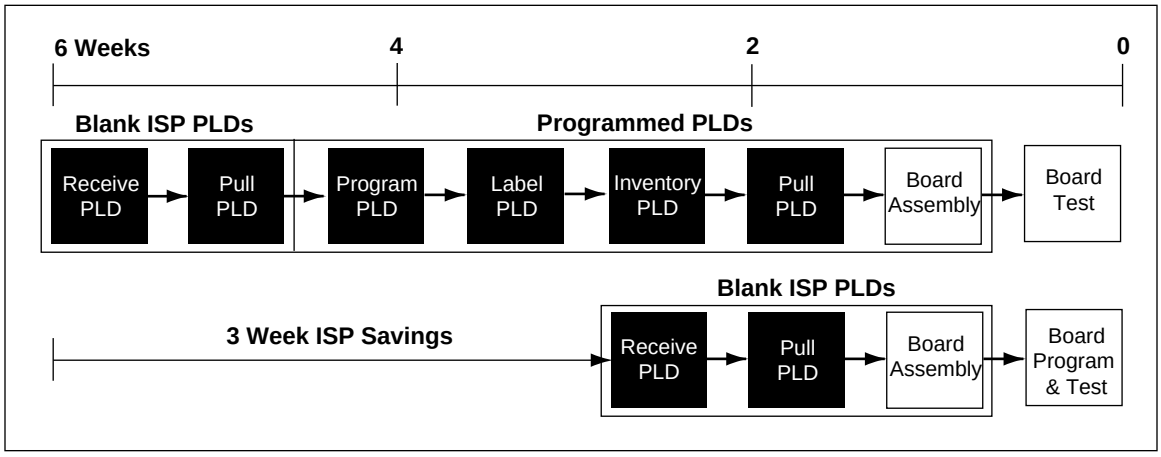
Table 9. PLD Inventory Costs

PLD Inventory Costs	ISP	STD
PLD consumption per week	288	288
Required weeks of PLD inventory	3	6
“On-hand” PLD inventory (units)	865	1,731
“On-hand” PLD inventory	$12,980.77	$25,961.54
Carrying cost rate (% per year)	15%	15%
System lifetime (years)	3	3
Total inventory carrying costs	$5,841.35	$11,682.69
Total carrying costs per 45,000 production PLDs	$0.13	$0.26

Needlessly carrying three weeks of standard PLD inventory represents an opportunity cost equal to the amount of interest those inventory dollars could have earned if they had been invested in other projects. Table 9 quantifies the on-hand inventory requirements and associated carrying costs for both ISP and standard PLDs (at the industry standard carrying cost of 15% for three years).

The inventory carrying costs for standard PLDs, at $0.26 per production device are twice that of ISP PLDs which add only $0.13 to the total cost-of-ownership.

Figure 4. Reduced PLD Inventory WIP



Obsolete PLD Inventory Costs

What happens to PLD inventories when the engineering department issues an emergency request requiring new PLD patterns, to the manufacturing floor? What happens when the marketing department informs manufacturing that the sales forecast is incorrect—the market is now demanding Version B of the system instead the Version A currently being built?

In systems designed with standard PLDs, the manufacturing floor now has programmed component PLD inventories needing to be reprogrammed and remarked, and board inventories needing to be reworked. If the system has been designed with ISP PLDs, the manufacturing floor is instantly retooled by calling up the board test program for Version B on the ATE tester. Any Version A board inventories can be easily converted to Version B by reconfiguring the ISP PLDs in-system. These costs are described in detail in Table 10.

The model assumes that during the three-year life of this system, there will be six "events" in which the on-hand programmed PLD inventories will need to be reworked. Further, it is assumed that at each event, there will be three weeks of programmed component inventories on-hand (standard PLDs only), and one week of PLDs soldered on boards (both standard and ISP PLDs), all of which will need to be reworked to incorporate the new Version B device codes.

The standard PLD component inventories will incur the $0.65 programming and mark costs. The board rework is more involved, since replacement standard PLDs will be necessary due to the package damage caused by the de-solder process (6 events x 288 PLDs/event x $15/PLD = $25,900). These replacement PLDs must be programmed

Table 10. Obsolete PLD Inventory Costs

Obsolete PLD Inventory Costs	ISP	STD
Assumptions:		
Number of code or mix change "events" during system life	6	6
Weeks of programmed component inventory	N/A	3
Weeks of PLD inventory per event	1	1
Compoment PLD inventory per event	0	865
Board level PLD inventory per event	288	288
Boards requiring rework per event	96	96
Component rework:		
Program and remark unit charges	$0.08	$0.65
Total component rework costs	$0.00	$3,375.00
Board rework:		
New device costs	$0.00	$25,961.54
Programming/mark costs	$138.80	$1,125.00
Board rework labor (per board)	$0.00	$300.00
Board rework costs	$0.00	$173,076.92
Total board rework costs	$138.80	$200,163.46
Total obsolete PLD inventory costs	$138.80	$203,538.46
Obsolete inventory costs per 45,000 production PLDs	$0.003	$4.52

and marked. The labor alone required to desolder, resolder and retest each circuit board can easily total $300 each.

For ISP PLDs, reprogramming the PLDs is the only effort in reworking. Table 10 shows the board rework cost of $0.00 for the ISP scenario since all ISP costs are covered by the $0.08 programming charge.

Obsolete PLDs add $204,000 to the total system cost over the three-year system life or an additional $4.52 to the original purchase price of every standard PLD.

General Manufacturing Costs (Labor and Equipment)

ISP PLDs allow for several manufacturing efficiences not possible with the use of standard PLDs:

- ISP PLDs support multi-function hardware whereby a single board design can be configured in "real time", to multiple board configurations. For this model, the use of standard PLDs requires manufacturing to manage two unique board designs (at half the volume each) and alternate the line between boards periodically. With ISP PLDs, the manufacturing floor performs 50% fewer product change-overs.
- With ISP, only a single device track is required for all pick-and-place locations, no matter the board revision or device pattern. With standard PLDs, three device tracks must be devoted to PLDs (one for each pattern). For many operations, this capability can help avoid the purchase of new pick-and-place equipment.

Table 11. General Manufacturing Costs

General Manufacturing Costs (Labor and Equipment)	ISP	STD
Number of boards manufactured	15,000	15,000
Number of unique board designs	1	2
Boards built per design (assume 50/50 split)	15,000	7,500
Baseline manufacturing cost per board	$50.00	$50.00
Manufacturing cost savings (%)	5%	0%
Actual board manufacturing cost per board	$47.50	$50.00
Total board manufacturing costs	$712,500.00	$750,000.00
Incremental costs	$0.00	$37,500.00
Incremental manufacturing cost per 45,000 production PLDs	$0.00	$0.83

Table 12. Quality and Reliability Costs

Quality and Reliability Costs	ISP	STD
Board fallout due to PLD coplanarity	0%	2%
Boards requiring rework	0	300
Replacement PLDs required (at $15 each)	0	900
Board rework:		
New device costs	$0.00	$13,500.00
Programming/mark costs	$0.00	$585.00
Board rework costs		$90,000.00
Total board rework costs	$0.00	$104,085.00
Board rework costs per 45,000 production PLDs	$0.00	$2.31

The model assumes a modest 5% savings in general manufacturing costs as a result of these efficiencies of scale (see Table 11).

The use of ISP saves $37, 500 over the standard PLD approach which adds an additional $0.83 to the standard PLD cost-of-ownership total.

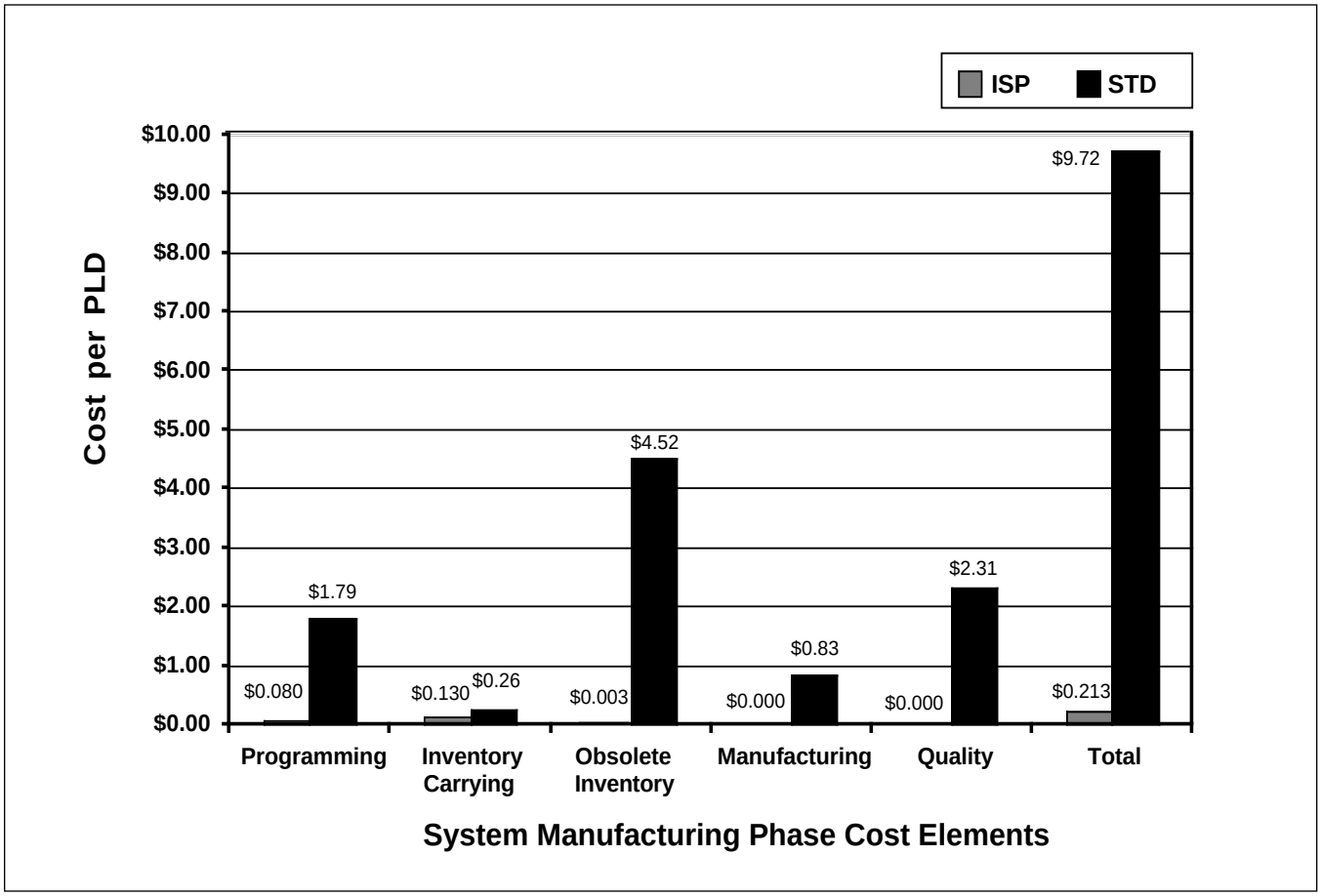
Quality and Reliability Costs

ISP PLDs can dramatically reduce board quality and reliability problems and costs. Two common causes of board rework are poor solder joints from bent leads and incorrect devices or device patterns on the board.

Both of these problems are eliminated with ISP PLDs, since the devices go from stock to circuit board without the handling-intensive, stand-alone programming steps required of standard PLDs that can cause coplanarity and bent leads. ISP programming not only significantly reduces these problems, but also eliminates the possibility of placing patterned PLDs in the wrong locations on the board.

The model (Table 12) assumes a 2% board fallout for standard PLDs with high pin-count QFP packages. The excessive handling associated with the programming operation causes lead damage which can result in poor solder joints on the PCB. The board rework cost model was discussed in the Obsolete PLD Inventory Costs section on page 8 and will not be discussed in detail here.

Figure 5. System Manufacturing Cost-of-Ownership



The standard PLD scenario adds $104,000 to the total system cost or an additional $2.31 to the standard PLD cost-of-ownership total.

System Manufacturing Summary

There are five areas in the System Manufacturing Phase in which the choice of PLD can have a significant impact on the overall PLD cost-of-ownership (see Figure 5). ISP PLDs offer consistently lower component costs across all five categories, and in two of the categories, add no incremental component costs to the cost-of-ownership totals.

In total, ISP PLDs add an additional $0.21 to the original $15.00 purchase price whereas standard PLDs add an additional $9.72 to the $15.00 purchase price.

Field Repair and/or Update Phase

This last phase of the System lifecycle highlights the ability of ISP PLDs to easily reconfigure system logic while the systems are installed in the field.

Field Repair Costs

Field replacement of defective PLDs is a rarity. ISP and electrically erasable standard PLDs enjoy 100% factory test coverage which eliminates infant mortality, unlike OTP PLDs which cannot be fully tested prior to user programming. Neither ISP nor electrically erasable standard PLDs incur field repair costs due to latent programming problems.

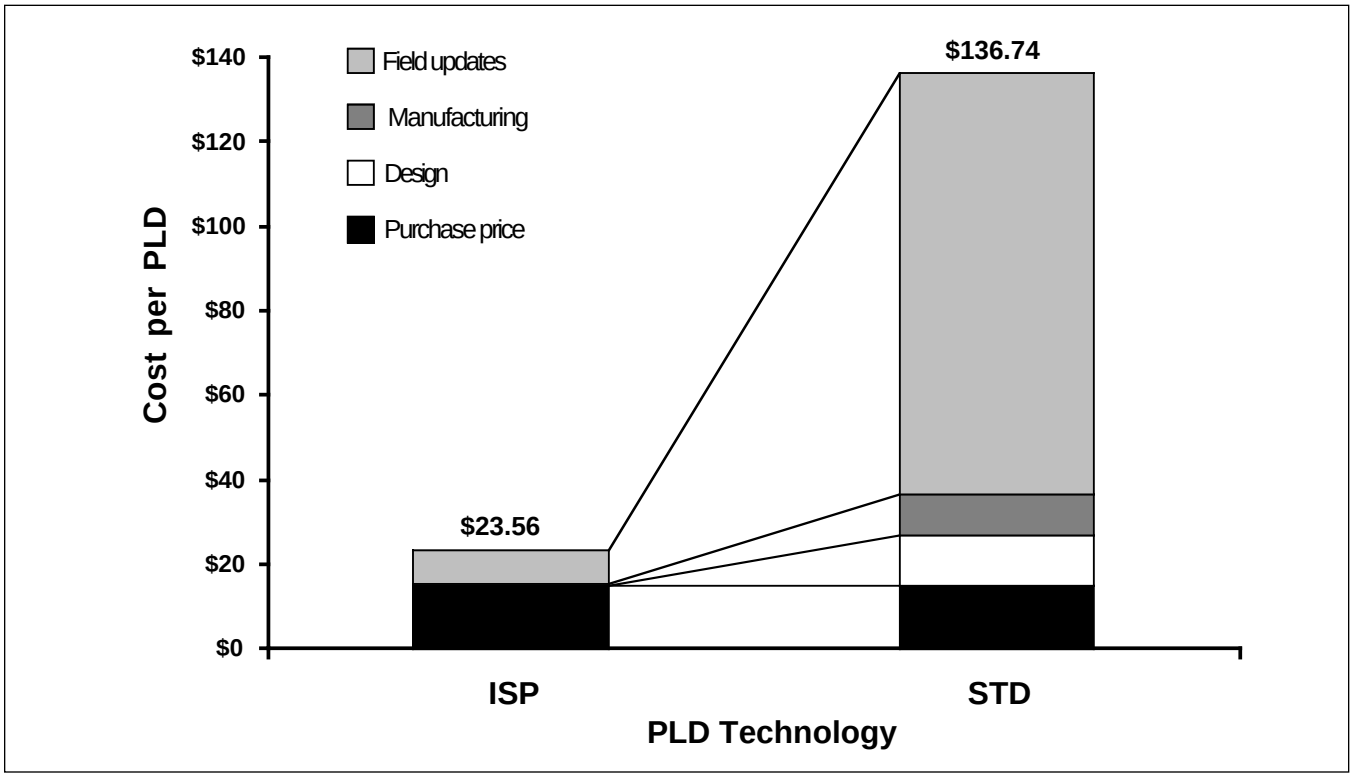
Table 14. Total Incremental Cost-of-Ownership (Over System Life)

Grand Total Costs over System Life Cycle	ISP	STD
System Design:		
Prototype socket costs	$0.00	$7,500.00
Prototype silicon costs	$450.00	$600.00
Prototype programming costs	$2.17	$87.50
Opportunity cost	$0.00	$532,833.33
System design subtotal	**$452.17**	**$541,020.83**
Manufacturing:		
Programming costs	$3,608.93	$80,505.00
PLD inventory costs	$5,841.35	$11,682.69
Obsolete PLD inventory costs	$138.80	$203,538.46
General board manufacturing costs	$0.00	$37,500.00
Quality and reliability costs	$0.00	$104,085.00
Manufacturing subtotal	**$9,589.08**	**$437,311.15**
Field Updates:		
Mass field update costs	$375,000.00	$4,450,000.00
Grand total ISP cost-of-ownership	**$385,041.24**	**$5,478,331.99**

Table 15. Total Incremental Cost-of-Ownership (per Production PLD)

Grand Total Costs per Production PLD	ISP	STD
System Design:		
Prototype socket costs	$0.000	$0.167
Prototype silicon costs	$0.010	$0.013
Prototype programming costs	$0.000	$0.002
Opportunity cost	$0.000	$11.841
System design subtotal	**$0.010**	**$12.023**
Manufacturing:		
Programming costs	$0.080	$1.789
PLD inventory costs	$0.130	$0.260
Obsolete PLD inventory costs	$0.003	$4.523
General board manufacturing costs	$0.000	$0.833
Quality and reliability costs	$0.000	$2.313
Manufacturing subtotal	**$0.213**	**$9.718**
Field Updates:		
Mass field update costs	$8.333	$100.000
Grand total ISP cost-of-ownership	**$8.56**	**$121.74**

Figure 6. Total Cost-of-Ownership



Field Upgrade/Update Costs

ISP is the only technology that makes mass hardware updates of installed systems practical. With ISP, installed systems can be upgraded by simply mailing a disk to the user, who downloads the upgrade code using the software provided (assume $25 per disk to generate and mail).

Update of a standard PLD-based systems require a board swap-out and at least a half day of a technician's time at a cost of $300 (not including the cost of the replacement circuit board). To update the entire installed system base of 15,000 systems would cost $375,000 with ISP PLD-based systems or $4.5 million for the standard PLD-based system (see Table 13). Field updates of standard PLD-based systems are simply cost-prohibitive and impractical. In short, ISP has emerged as the only technology which makes field updates and enhancements practical.

Table 13. Field Repair/Update Costs

Field Repair/Update Costs	ISP	STD
Total field repair costs	None	None
Number of updates	15,000	15,000
Cost/update	$25.00	$300.00
Total field update cost	$375,000.00	$4,500,000.00
Field repair/update cost per 45,000 production PLDs	$8.33	$100.00

Summary

ISP provides an overwhelming cost advantage over standard PLD-based designs when the total cost-of-ownership is examined. ISP PLDs provide the most cost competitive PLD solutions on the market today. ISP positively impacts every phase of the system lifecycle. Tables 14 and 15 (see page 11) summarize the total incremental cost-of-ownership incurred above and beyond the base purchase of the system lifetime requirement of 45,000 PLDs.

Figure 6 (page 11) demonstrates the impact of PLD programming technology on overall PLD cost-of-ownership. With ISP, the purchase price of $15 grew $8.56 for a total component cost of $23.56, whereas the cost of the standard PLD grew an astronomical $121.74 for a per device cost of $136.74.

As mentioned previously, it is expected that the reader may not find all elements of this model relevant to his or her situation, or may have different valuations for certain cost elements. However, portions of this analysis should be applicable to almost any PLD user. Examining a component's total cost-of-ownership is the best way to minimize overall cost. In-system programmable PLDs are clearly superior to standard PLDs in minimizing programmable logic costs and maximizing profits.

Copying PAL, EPLD & PEEL Patterns Into GAL® Devices

INTRODUCTION

The generic/universal architectures of Lattice Semiconductor Corporation (LSC) GAL devices are able to emulate a wide variety of PAL, EPLD and PEEL devices. GAL devices are direct functional and parametric replacements for most PLD device architectures. To use GAL devices in place of other PLD types, some conversion of the original device pattern may be needed. This conversion is not difficult, and can be accomplished at either the design or manufacturing level. The following sections describe several techniques available to convert PAL, EPLD and PEEL device patterns to LSC GAL device patterns.

CROSS PROGRAMMING: GAL16V8 AND GAL20V8

The GAL16V8 and GAL20V8 devices replace most standard 20-pin and 24-pin PAL devices. To simplify the conversion process, LSC has worked with programmer hardware manufacturers to provide the ability to program GAL devices directly from existing PAL JEDEC files, or master PAL devices. LSC qualified programmers can automatically configure the architecture of a GAL device to emulate the source PAL device.

To provide a conceptual framework for the conversion from PAL devices to GAL devices, a mythical device known as a RAL device was created. A RAL device is simply a GAL device configured to emulate a PAL. There is a one-to-one correspondence between the name of a PAL device and that of a RAL device. For example, a RAL16L8 is simply a GAL16V8 configured as a PAL16L8. Some programmers list the RAL device types as choices for cross-programming, while others specifically state that a cross-programming operation is to be performed using a PAL device type as the architecture type. Other programmers list devices such as a LSC 16L8. Even though LSC does not make a 16L8 device, choosing this selection allows the programmer to accept a 16L8 JEDEC file, and will program a GAL16V8 device to emulate a PAL16L8.

To program a GAL16V8 or GAL20V8 device from an existing PAL JEDEC file, simply select the appropriate device code (either RAL type, or PAL type to cross-program from), then download the PAL JEDEC file to the programmer. Insert the appropriate GAL device that can directly emulate the PAL device (according to the chart in the GAL16V8 or GAL20V8 data sheets). The programmer will automatically configure the GAL device to emulate the PAL device during programming. The resulting GAL device is 100% compatible with the original PAL device.

A GAL device may also be programmed from a master PAL device by reading the pattern of the master PAL into the programmer memory, then selecting the appropriate RAL device or PAL type to cross-program from. The GAL device can then be programmed from the programmer memory.

CROSS PROGRAMMING: GAL22V10/GAL20RA10

The GAL22V10 and GAL20RA10 are direct replacements for bipolar PAL devices, and are JEDEC fuse map compatible with these industry standard devices. To program a GAL22V10 or GAL20RA10 device from an existing PAL JEDEC file, simply select the appropriate GAL device code, then download the PAL JEDEC file to the programmer. The resulting GAL device is 100% compatible with the original PAL.

GAL devices also may be programmed from Master PAL devices by reading the pattern of the Master PAL into the programmer memory, then selecting the appropriate GAL device code. The GAL device can then be programmed from the programmer memory.

The GAL22V10 and GAL20RA10 also can store a User Electronic Signature (see the data sheets on these devices for more information). To use this feature, the JEDEC file must contain this information. To add the signature data to the JEDEC map, use the PALtoGAL conversion utility (see next section) or recompile the source equations for a LSC GAL device instead of a generic 22V10 type. Many programmers list two device types to differentiate between the two types of JEDEC files, and list both a GAL22V10 and a name such as GAL22V10-UES or GAL22V10-ES. Other programmers allow both types of JEDEC files to be accepted, and simply don't program the Signature fuses if they are not present in the file.

CROSS PROGRAMMING: GAL20XV10

The GAL20XV10 can be configured as a direct replacement for bipolar PAL20X10, 20X8, 20X4, and 20L10 devices. Many programmers provide cross-programming support similar to that provided for the GAL16V8/GAL20V8 devices. This allows the use of existing PAL device files to program the GAL20XV10 to emulate the PAL devices. The PALtoGAL conversion software (described below) also supports conversion of the PAL JEDEC files to a functionally equivalent GAL device file.

Copying PAL Patterns Into GAL Devices

PALTOGAL CONVERSION UTILITY SOFTWARE

Lattice Semiconductor has created a software utility that will convert an existing PAL device JEDEC file to the appropriate GAL device JEDEC format. Called PALtoGAL, this software utility can be used to convert PAL device files to GAL device files, add/or change the User Electronic Signature without changing device functionality, and reformat existing GAL JEDEC files for readability.

Since a few programmable logic devices have features that a GAL device cannot exactly emulate, the PALtoGAL utility will clearly describe the incompatibility but will not create an output file. GAL devices programmed using files converted by PALtoGAL will be 100% compatible with the original logic device. PALtoGAL is just another method of cross-programming, and should produce the same results as using a programmer. The advantage is that a full GAL device JEDEC map is created, meaning that the appropriate GAL device may then be selected on the programmer, which may simplify the manufacturing flow. Also, the PALtoGAL conversion software provides conversions that programmers do not.

A copy of the PALtoGAL conversion utility software can be obtained through your local LSC representative, or by contacting the GAL Applications Hotline at 1-800-FASTGAL (327-8425) or (503) 693-0201. The software also may be downloaded from LSC's Electronic Bulletin Board at (503) 693-0215; the file name is "PALTOGAL.EXE".

SOFTWARE COMPILER CONVERSION

If the equation source file is available for the PAL device, it can be converted by re-compiling using a suitable logic compiler that supports GAL devices. If there are any device incompatibilities (there shouldn't be in most cases), the compiler will describe the errors. The output of the compiler will be a GAL JEDEC file that can be used to program a GAL device directly. The resulting GAL device will be 100% functionally compatible with the original device.

Suitable logic compilers are listed in the Development Tools section. If additional questions arise, contact your compiler manufacturer or a LSC Applications Engineer by calling the GAL Applications Hotline at 1-800-FASTGAL or (503) 693-0201.

GAL Product Line Cross Reference

MANUFACTURER	PART #	LSC PART #
ALTERA	EP310 EP320 EP330	GAL16V8Z[1] GAL16V8[1] or... GAL18V10
	5C031 5C032 85C220	GAL16V8[1] or... GAL16V8Z or... GAL18V10
	85C224	GAL20V8[1] or... GAL22V10
	85C22V10	GAL22V10
AMD	PAL10H8 PAL10L8 PAL12H6 PAL12L6 PAL14H4 PAL14L4 PAL16H2 PAL16L2	GAL16V8
	PAL16L8 PAL16R4 PAL16R6 PAL16R8 PALC16L8 PALC16R4 PALC16R6 PALC16R8 AmPAL16L8 AmPAL16R4 AmPAL16R6 AmPAL16R8 PAL16P8 PAL16RP4 PAL16RP6 PAL16RP8	GAL16V8
	PALCE16V8	GAL16V8
	PALCE16V8Z	GAL16V8Z
	AmPAL18P8	GAL16V8[1] or... GAL18V10
	PAL14L8 PAL16L6 PAL18L4 PAL20L2	GAL20V8
	PAL20L8 PAL20R4	GAL20V8
	PAL20R6 PAL20R8 AmPAL20RP4 AmPAL20RP6 AmPAL20RP8	GAL20V8
	PALCE20V8	GAL20V8
AMD	PAL20RA10 AmPAL20RP10	GAL20RA10 GAL22V10
	PAL20S10 PAL20RS4 PAL20RS8 PAL20RS10	GAL6002[1] or... GAL22V10[1]
	PAL12L10 AmPAL20L10 PAL20L10 PAL20X4[2] PAL20X8[2] PAL20X10[2]	GAL20XV10
	AmPAL22V10 PAL22V10 PALC22V10 PALCE22V10	GAL22V10
	PALCE24V10 PALCE26V12	GAL26CV12[1]
	PLS167 PLS168	GAL6002[1]
ATMEL	AT22V10	GAL22V10
CYPRESS	PALC16L8 PALC16R4 PALC16R6 PALC16R8	GAL16V8
	PLDC18G8	GAL20XV10[1] or... GAL18V10
	PALC20G10 PALC22V10 PAL22V10	GAL16V8[1] or... GAL22V10
	PLD20RA10	GAL20RA10
HARRIS	HPL16LC8 HPL16RC4 HPL16RC6 HPL16RC8	GAL16V8

1) Conversion possible but not 100% compatible with this device.
2) PLCC pin-out may not be 100% compatible.

GAL Product Line Cross Reference

MANUFACTURER	PART #	LSC PART #
ICT	PEEL18CV8	GAL16V8[1] or... GAL18V10
	PEEL153 PEEL253	GAL16V8[1] or... GAL18V10[1]
	PEEL20CG10 PEEL22CV10A	GAL20V8[1] or... GAL22V10
NATIONAL	PAL10H8	GAL16V8
	PAL10L8 PAL12H6 PAL12L6 PAL14H4 PAL14L4 PAL16H2 PAL16L2	GAL16V8
	PAL16L8 PAL16R4 PAL16R6 PAL16R8	GAL16V8
	GAL16V8 GAL16V8A	GAL16V8
	GAL18V10	GAL18V10
	PAL14L8 PAL16L6 PAL18L4 PAL20L2	GAL20V8
	PAL20L8 PAL20P8 PAL20R4 PAL20RP4 PAL20R6 PAL20RP6 PAL20R8 PAL20RP8	GAL20V8
	PAL20RA10	GAL20RA10
	PAL20L10 PAL20X4 PAL20X8 PAL20X10	GAL20XV10
	GAL22V10	GAL22V10
	GAL26CV12	GAL26CV12
	GAL6001	GAL6001 or... GAL6002

MANUFACTURER	PART #	LSC PART #
SGS-THOMSON	GAL16V8	GAL16V8
	GAL20V8	GAL20V8
	GAL39V18	GAL6001 or... GAL6002
SIGNETICS	PLHS16L8 PLUS16L8 PLUS16R4 PLUS16R6 PLUS16R8	GAL16V8
	PLHS18P8	GAL16V8[1] or... GAL18V10
	PLS153 PHD16N8	GAL16V8[1] or... GAL18V10[1]
	PLUS20L8 PLUS20R4 PLUS20R6 PLUS20R8	GAL20V8
	PLUS168 PLUS173	GAL6002[1]
TI	TIBPAL16L8 TIBPAL16R4 TIBPAL16R6 TIBPAL16R8	GAL16V8
	TICPAL16L8 TICPAL16R4 TICPAL16R6 TICPAL16R8	GAL16V8
	EP330 TIBPAD16N8	GAL16V8[1] or... GAL18V10[1]
	TIBPAL20L8 TIBPAL20R4 TIBPAL20R6 TIBPAL20R8	GAL20V8
	TIBPAL20L10 TIBPAL20X4 TIBPAL20X8 TIBPAL20X10	GAL20XV10
	TIBPAL22V10 TICPAL22V10	GAL22V10
	TIBPLS506C TIBPLS507C TIB82S105 TIB82S167	GAL6002[1]

1) Conversion possible but not 100% compatible with this device.

Thermal Management

Introduction to Thermal Management

Thermal considerations are rarely an issue with low-density PLDs such as the Lattice Semiconductor GAL products, however, high-density PLDs often require consideration of thermal issues as part of any sound design methodology. To avoid reliability problems, Lattice Semiconductor specifies a maximum allowable junction temperature of 150 °C for its ispLSI and pLSI devices. The system designer should always complete a thermal analysis of their specific design to ensure that this temperature is not exceeded.

In addition to the device and package, the thermal characteristics of a circuit depend on the operating temperature, device power consumption, and the ability of the system to dissipate heat. The maximum junction temperature of a device can be calculated as shown:

$T_J = T_A + Power*\theta_{JA}$

or

$T_J = T_C + Power*\theta_{JC}$

Where :

- T_J = Junction Temperature of the Device
- T_A = Ambient Temperature
- T_C = Case Temperature
- θJ_A = Junction-to-Air Thermal Resistance (see table at the end of this section)
- θJ_C = Case-to-Air Thermal Resistance (see table at the end of this section)
- Power = $I_{CC} * V_{CC}$

Icc may be estimated as shown in the "Power Consumption" section of the individual data sheets. The parameters in the Icc equation may be found in the report file from the pDS or pDS+ development systems.

If the calculated T_J max exceeds 150°C, refer to the following hints to reduce overall power dissipation and package temperature.

Ways to Reduce Junction Temperature

1. Increase air flow in the system to reduce the case or ambient temperature.

2. Reduce power in one of the following ways:

    a. Reduce net utilization. Internal net utilization can be reduced by combining common input functions of the application into one logic block (GLB) The group feature of the pDS+ Fitter can be used to accomplish this task.

    b. Reduce the number of product terms (PT). The number of product terms can be reduced by either re-partitioning the device into multiple devices or carefully selecting how the logic function is implemented. For example, implementing a counter in a sum-of-product configuration will utilize more PT's than in an XOR implementation.

    c. Reduce the frequency of operation. ispLSI and pLSI architectures provide flexibility to control clock polarity to potentially reduce the overall clock speed.

3. Where possible, make use of the output slew rate control to reduce the output switching current of the device.

4. Make sure that programmable pull-ups are enabled to drive unused inputs to a proper logic level.

Package Thermal Resistance

The following tables provide information on the package thermal resistance of Lattice Semiconductor (LSC) commercial and industrial grade devices. For information on the package thermal resistance of LSC military grade devices, please refer to "MIL-M-38510, Appendix C."

Testing was performed per SEMI TEST METHOD G38-87: "Still and Forced-Air Junction-to-Ambient Thermal Resistance Measurements of IC Packages" with devices mounted on a thermal test board conforming to SEMI SPECIFICATION G42-88: "Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages."

Table 1. Package Thermal Resistance for ispLSI and pLSI Products

Package	Pin Count	θ_{JA} 2-Layer Board (Still Air)	θ_{JA} 2-Layer Board (225 lfpm)	θ_{JA} 4-Layer Board (Still Air)	θ_{JA} 4-Layer Board (225 lfpm)	θ_{JC}
PLCC	44-pin	50	42	42.5	35	16
	68-pin	45	37	38	31	13
	84-pin	42	34	36	29	12
JLCC	44-pin	69	—	—	—	4
	68-pin	52	—	—	—	3
PQFP	120-pin	40	32	32	26	15
	128-pin	40	32	32	26	15
TQFP	44-pin	80	70	65	57	19
	100-pin	64	53	52	43	22
	128-pin	60	50	51	42	24
	176-pin	45	35	35	28	8
MQFP	160-pin	—	—	20	—	2
	208-pin	—	—	17	—	2
	240-pin	—	—	16	—	2
CPGA	84-pin	38	—	—	—	3
	133-pin	26	—	—	—	2
	167-pin	25	—	—	—	2

Table 2. Package Thermal Resistance for GAL, ispGAL and ispGDS Products

Package	Pin Count	θ_{JA} 2-Layer Board (Still Air)	θ_{JC}
Plastic DIP	20-pin	67	30
	24-pin	65	25
	28-pin	52	23
PLCC	20-pin	67	25
	28-pin	56	23
SOIC	20-pin	85	18
SSOP	28-pin	105	—
Ceramic DIP	20-pin	62	10
	24-pin	60	10
	28-pin	58	10
LCC	20-pin	65	8
	28-pin	62	7

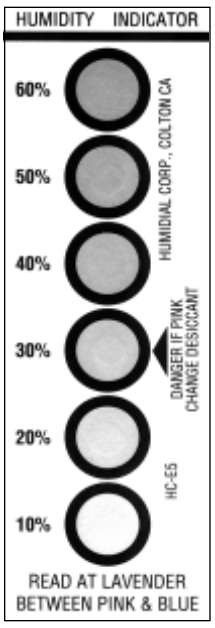
Handling Moisture Sensitive Packages

It is common knowledge throughout the electronics industry that high pin-count (≥44 pins) plastic packages are susceptible to moisture related failure mechanisms during board assembly. Excess moisture in these packages can turn to steam during the board solder process, causing package blistering and mechanical problems. This sensitivity to the moisture content of a plastic package led to the implementation of the industry standard practice known as Dry Pack**.**

Dry Pack is a process whereby plastic encapsulated semiconductors are first baked to drive all moisture out of the package and then vacuum-sealed in a waterproof bag by the manufacturer to prevent any subsequent absorption of moisture. As a further precaution, a desiccant (moisture absorbing) material and a Humidity Indicator Card (see figure 1) are sealed in the bag as well. The desiccant absorbs any residual moisture in the sealed bag. The Humidity Indicator Card indicates the relative humidity inside the sealed bag and provides an instant alert to any user who opens a sealed bag and finds a Humidity Indicator Card reading of 20% or higher.

Lattice Semiconductor Dry Packs all shipments of 44-pin and higher pin-count plastic packages in compliance with this industry standard practice. Unfortunately, Dry- Packed shipments alone can't guarantee trouble free use of these moisture sensitive packages. Special handling procedures must be followed by all who handle this product after initial shipment by Lattice Semiconductor. If these Dry-Pack handling procedures are followed, unwanted moisture will not be absorbed by the packages and a vapor-phase or infrared solder reflow process will not cause any moisture induced quality problems.

Figure 1. Humidity Indicator Card



Lattice Semiconductor documents proper Dry-Pack handling procedures on a label (see figure 2) placed on the outside of every Dry-Packed bag shipped. The text contained in the label is as follows:

1) Shelf life in the sealed bag is 12 months when stored at < 40°C and 90% relative humidity (RH) conditions.

2) After the bag is opened, devices that will be subjected to infrared reflow, vapor phase reflow, or equivalent processing (peak package body temperature of no more than 220°C) must be:
   a) Mounted within 48 hours at factory conditions of <30°C and 60% RH, or
   b) Stored at less than 20% RH.

3) Devices require baking before mounting if either:
   a) The Humidity Indicator Card is > 20% when read at 23°C +/- 5°C, or if
   b) Items 2a or 2b are not met.

4) If baking is required, devices may be baked for:
   a) 192 hours at 40°C + 5° /- 0°C and <5% RH for low temperature device containers, or
   b) 24 hours at 125°C +/- 5°C for high-temperature device containers.

Figure 2. Dry-Pack Label

Tape and Reel Specifications

A tape-and-reel packing container is available for plastic leaded chip carriers to protect the product from mechanical/ electrical damage and to provide an efficient method for handling. Lattice Semiconductor's tape-and-reel containers are shipped in full compliance with Electronics Industry Association Standard EIA-RS481.

The tape-and-reel packing system consists of a pocketed carrier tape loaded with one device per pocket. A protective cover tape seals the carrier tape and holds the devices in the pockets. A full reel holds a maximum quantity of devices depending on the package size. Lattice Semiconductor requires ordering in full reel quantities. Once loaded, the tape is wound onto a plastic reel for labeling and packing.

Any GAL or pLSI device (non-ISP) must be factory programmed (pre-patterned). Custom marking of devices prior to mounting on tape-and-reel is available upon request.

TAPE-AND-REEL QUANTITIES AND DIMENSIONS

Package	Pin Count	Carrier Tape Dimensions		Quantity Per 13 Inch Reel
		Width	Pitch	
PLCC	20-pin	16mm	12mm	1000
	28-pin	24mm	16mm	750
	44-pin	32mm	24mm	500
	68-pin	44mm	32mm	250
	84-pin	44mm	36mm	250

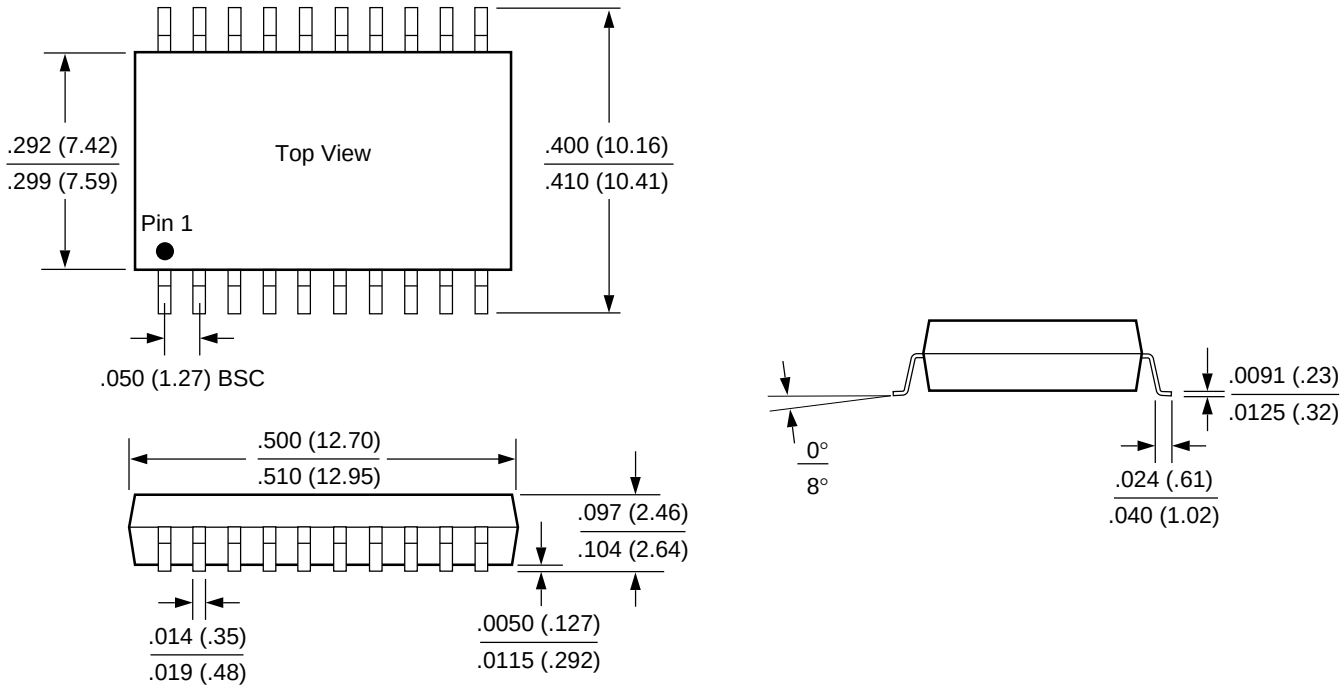
Package Diagrams

Index of Package Diagrams

20-PinSOICPackage

Dimensions in Inches MIN. / MAX.

(Dimensions in millimeters, shown in parentheses, are for reference only)

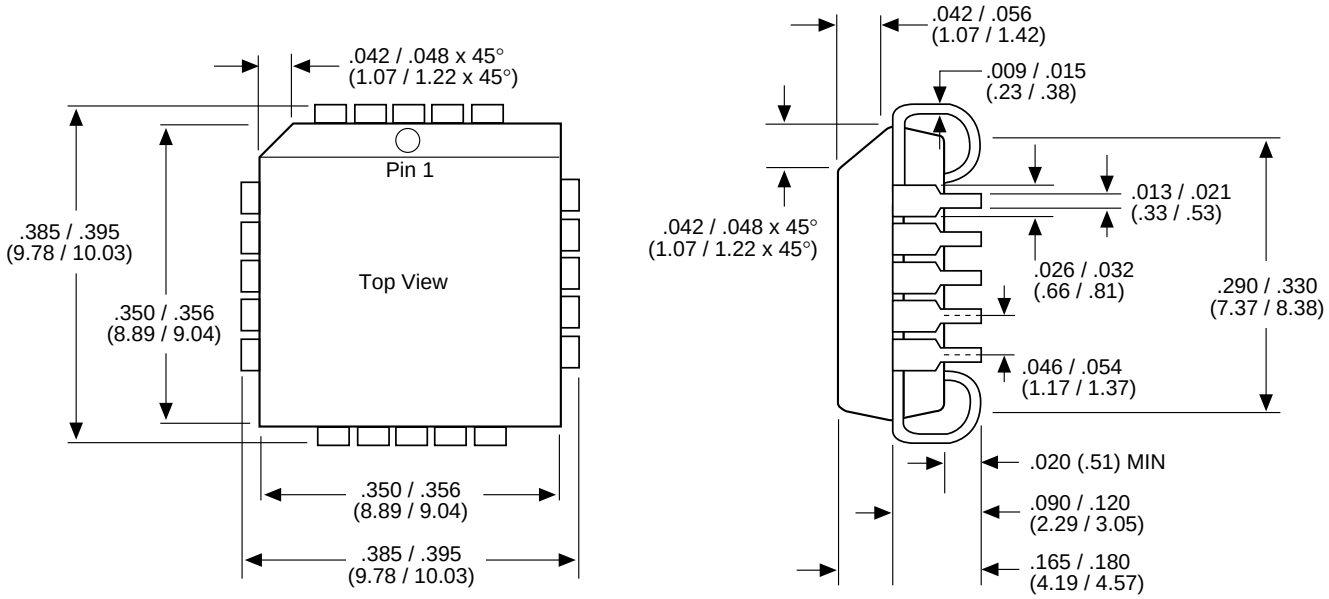


Package Diagrams

20-PinPLCCPackage

Dimensions in Inches MIN. / MAX.

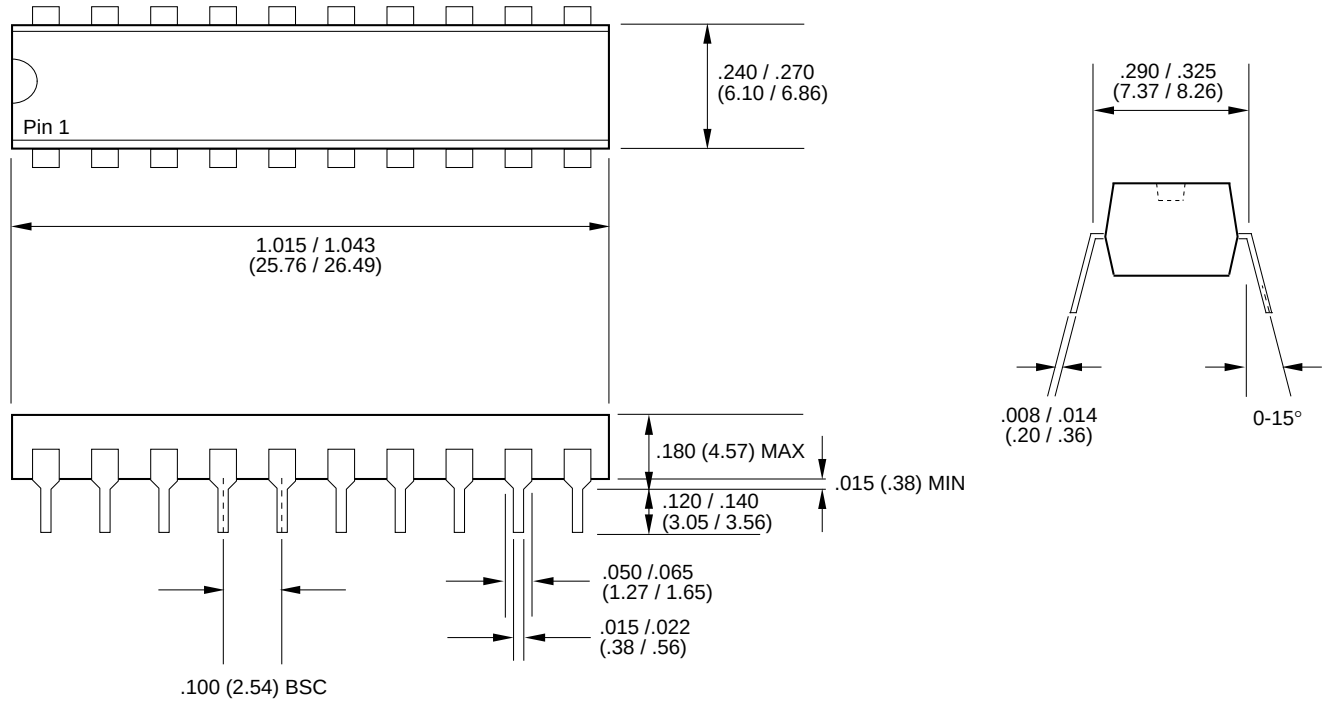
(Dimensions in millimeters, shown in parentheses, are for reference only)



20-PinPlasticDIP

Dimensions in Inches MIN. / MAX.

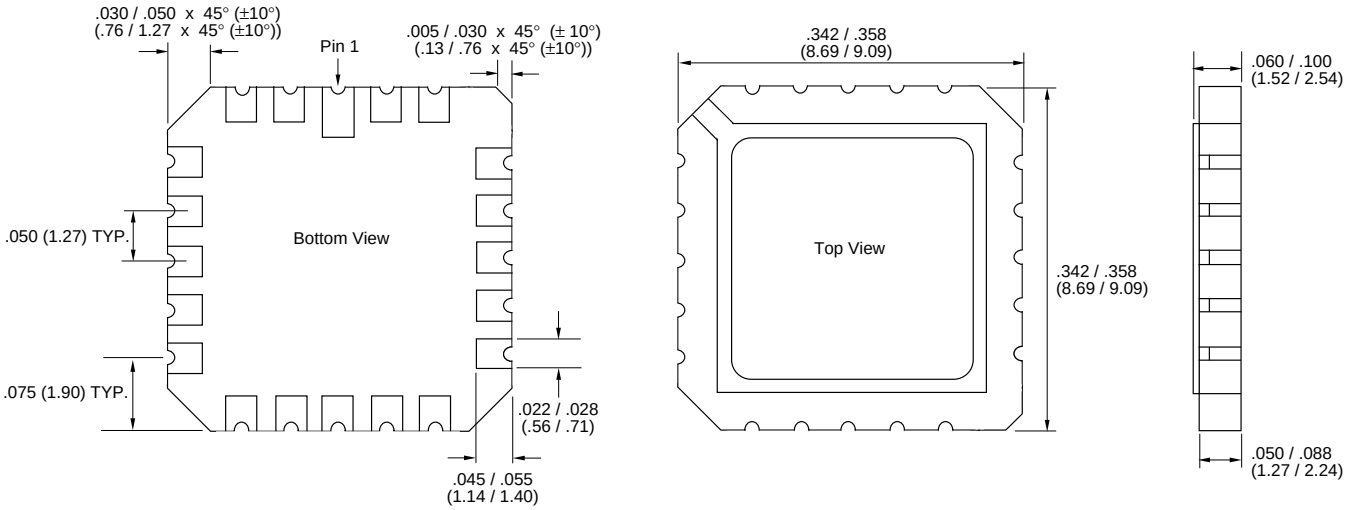
(Dimensions in millimeters, shown in parentheses, are for reference only)



20-PinLCC

Dimensions in Inches MIN. / MAX.

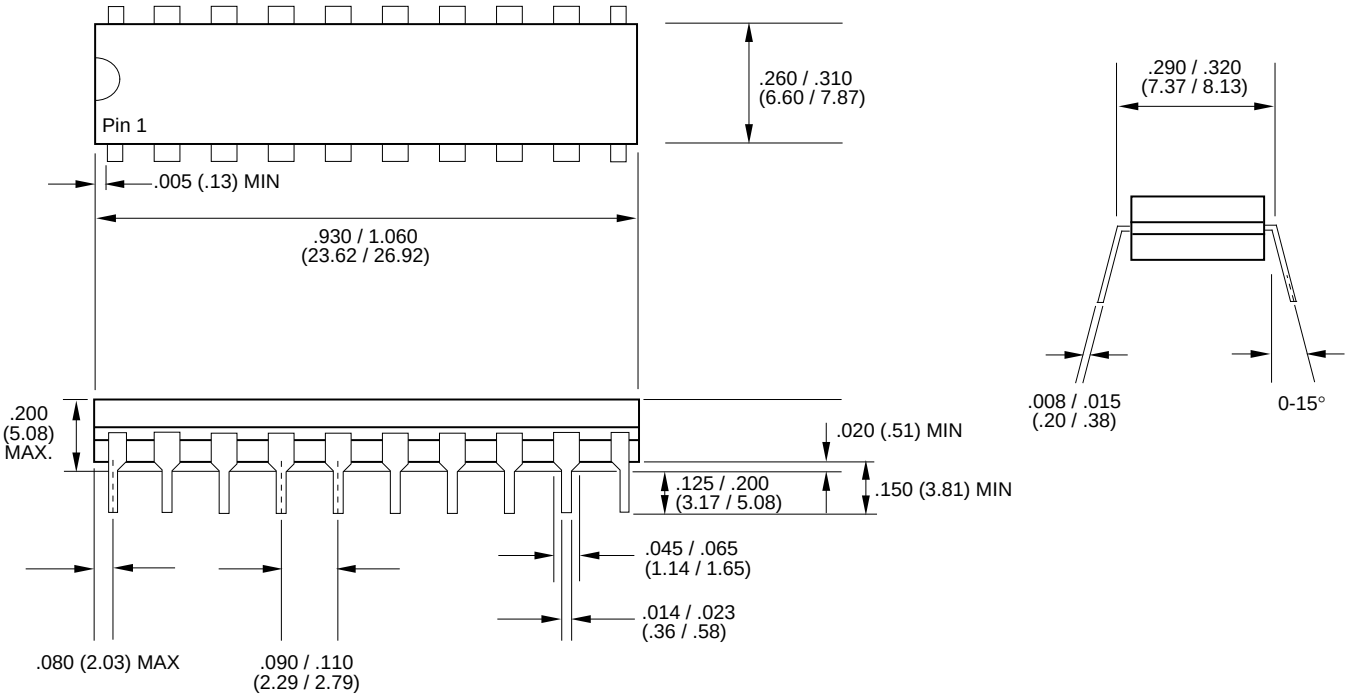
(Dimensions in millimeters, shown in parentheses, are for reference only)



20-Pin(300-Mil)CERDIP

Dimensions in Inches MIN. / MAX.

(Dimensions in millimeters, shown in parentheses, are for reference only)

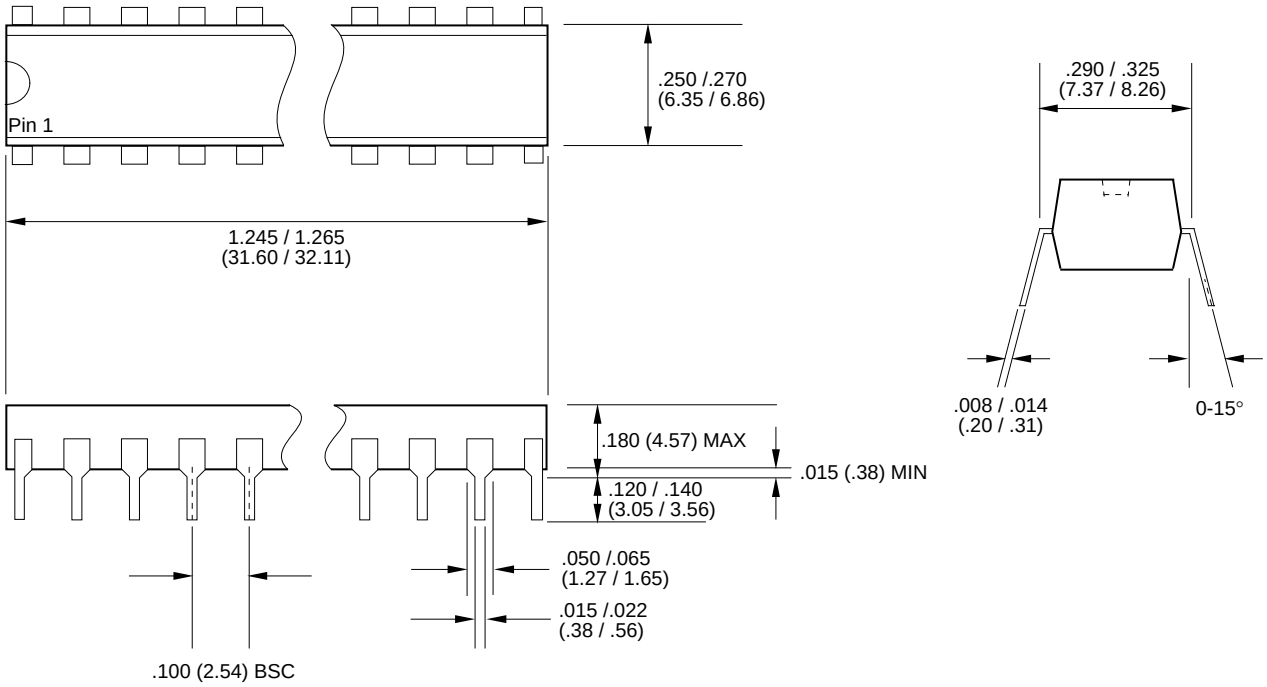


Package Diagrams

24-PinPlasticDIP

Dimensions in Inches MIN. / MAX.

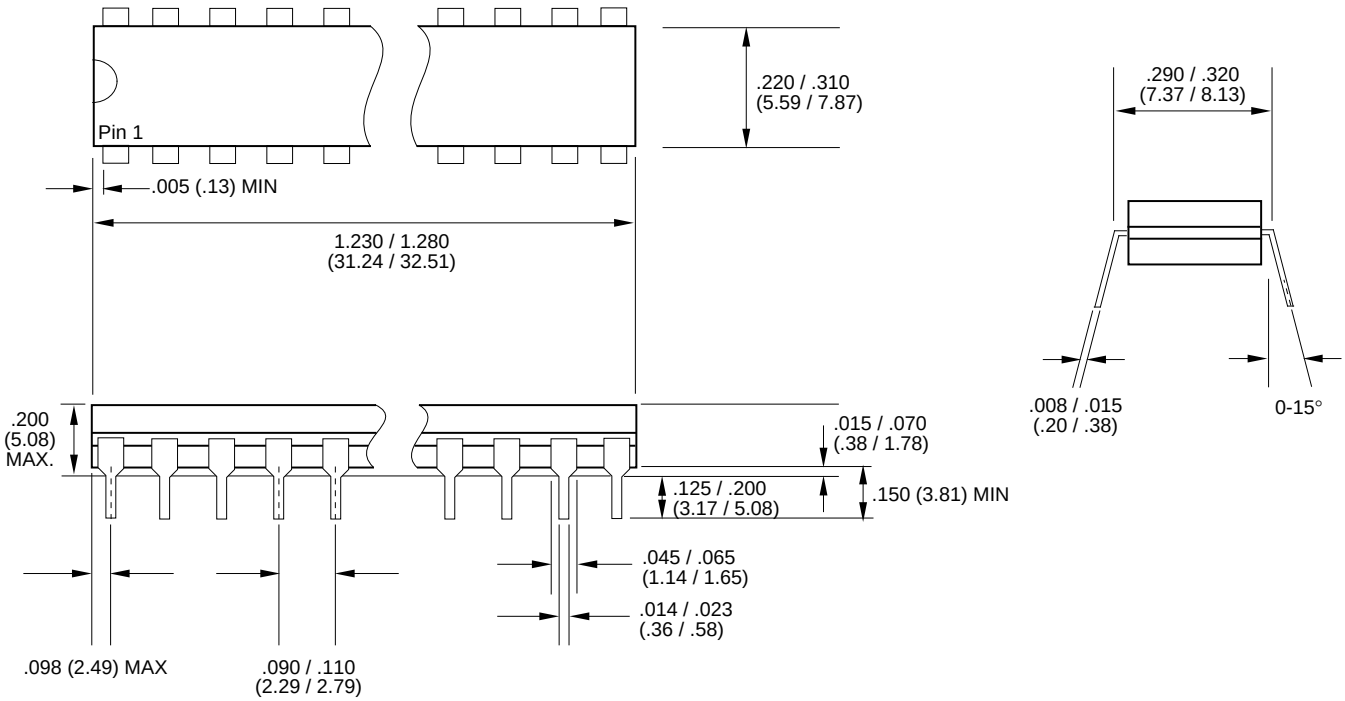
(Dimensions in millimeters, shown in parentheses, are for reference only)



24-Pin(300-Mil)CERDIP

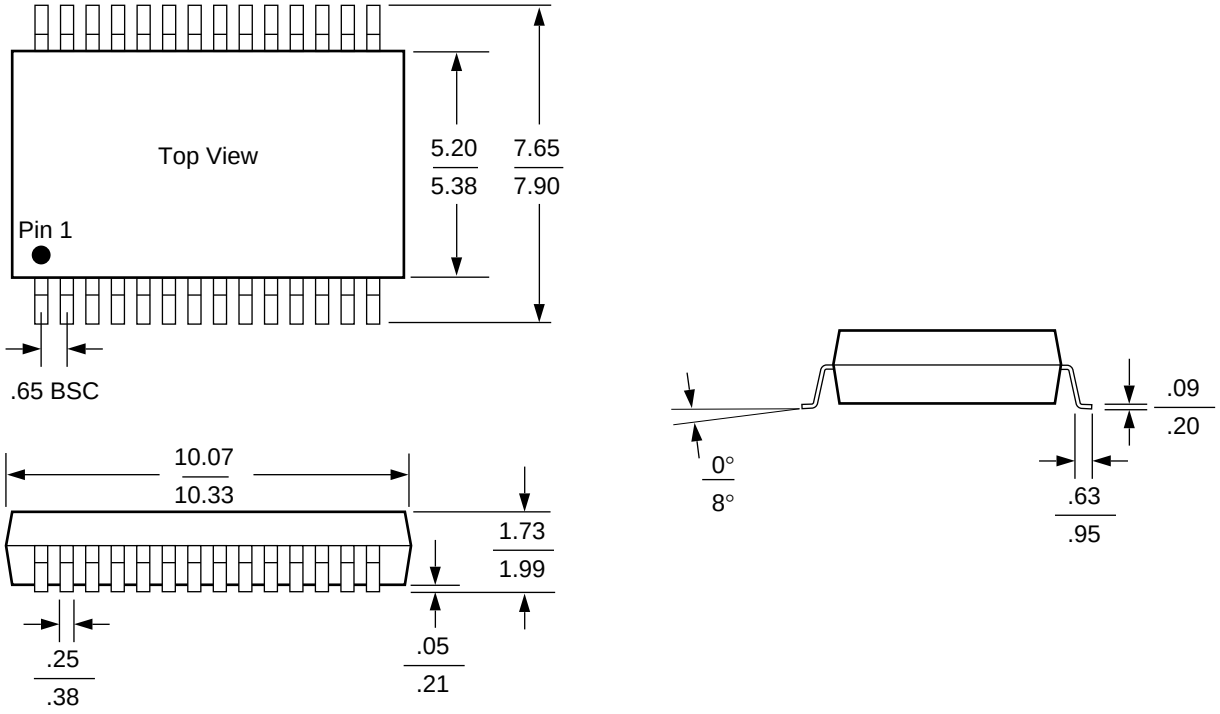
Dimensions in Inches MIN. / MAX.

(Dimensions in millimeters, shown in parentheses, are for reference only)



28-PinSSOP

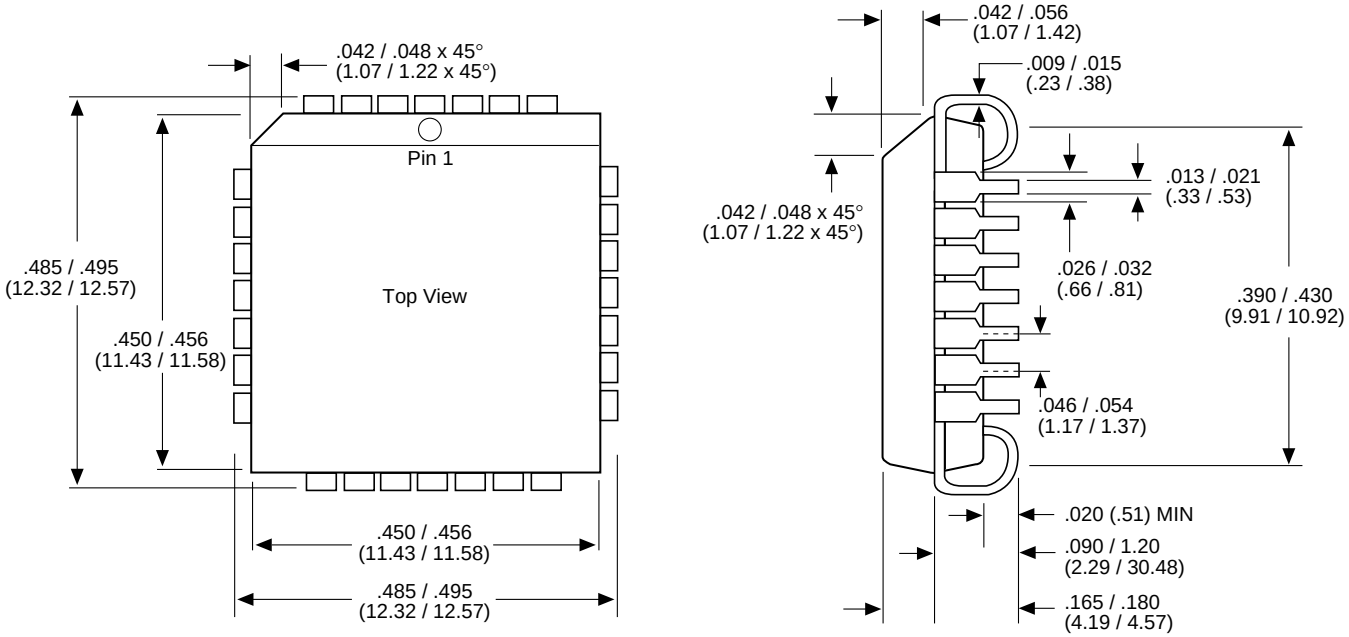
Dimensions in Millimeters MIN. / MAX.



28-PinPLCCPackage

Dimensions in Inches MIN. / MAX.

(Dimensions in millimeters, shown in parentheses, are for reference only)

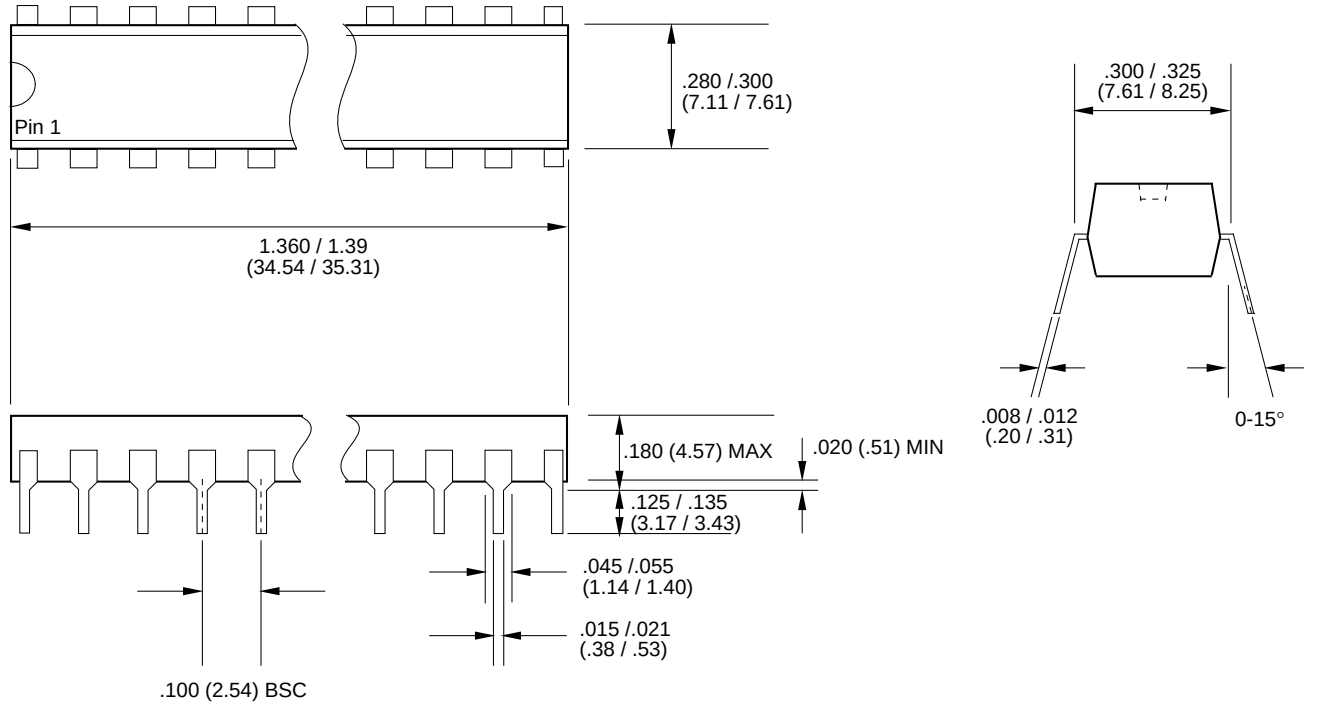


Package Diagrams

28-PinPlasticDIP

Dimensions in Inches MIN. / MAX.

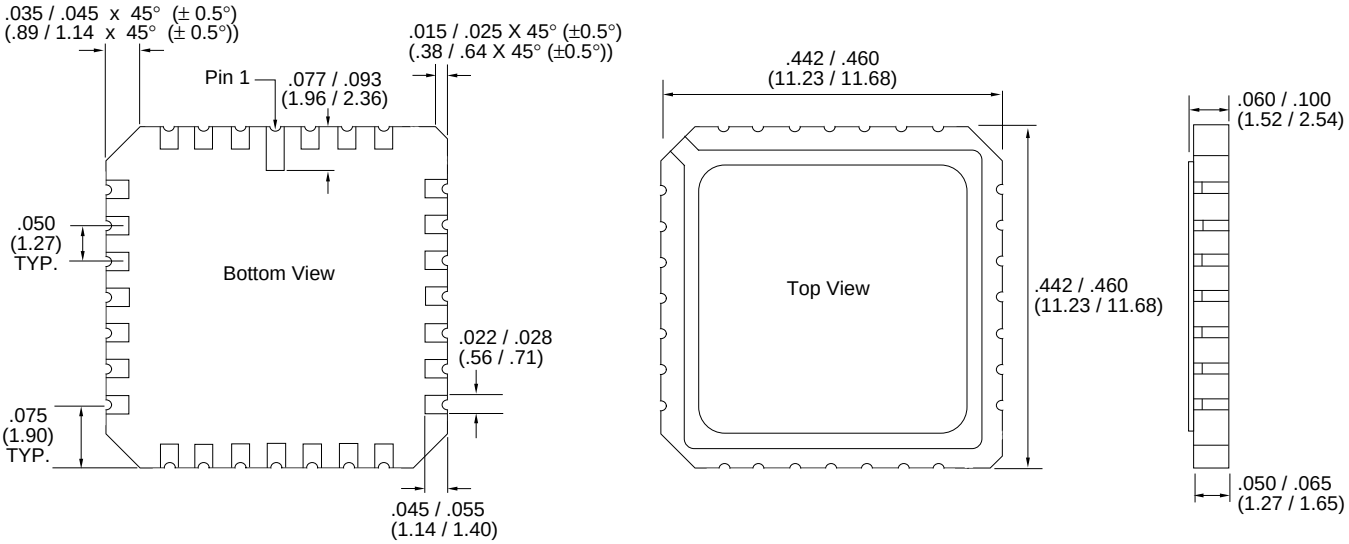
(Dimensions in millimeters, shown in parentheses, are for reference only)



28-PinLCC

Dimensions in Inches MIN. / MAX.

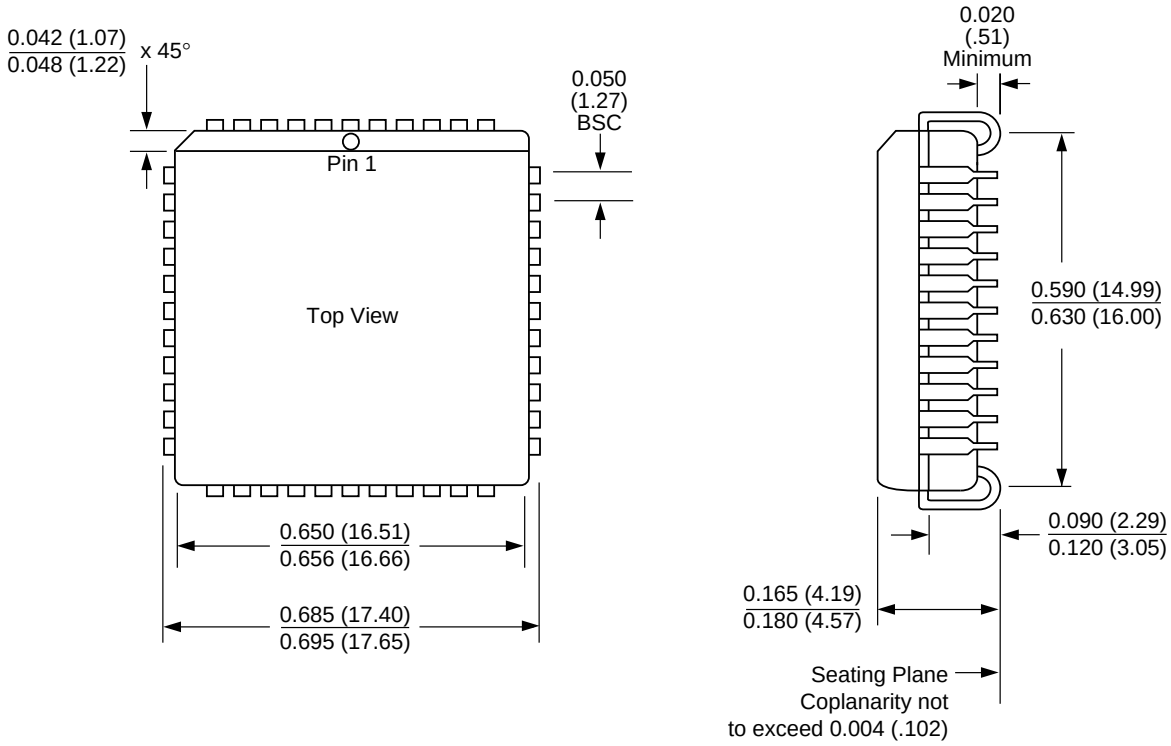
(Dimensions in millimeters, shown in parentheses, are for reference only)



44-PinPLCCPackage

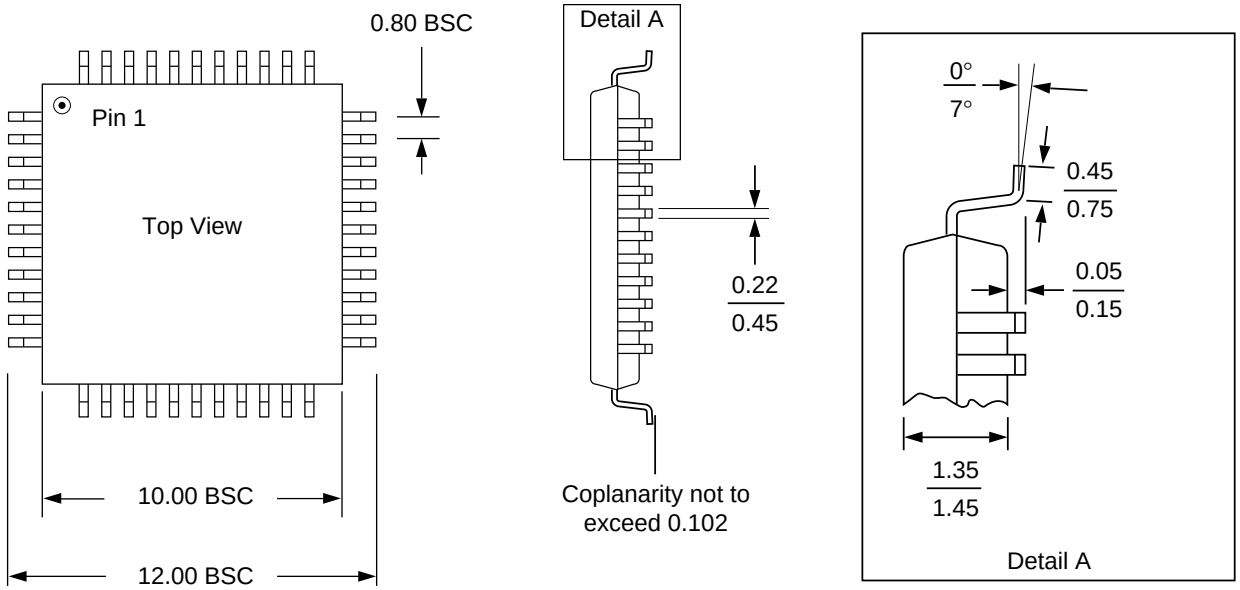
Dimensions in Inches MIN. / MAX.

(Dimensions in millimeters, shown in parentheses, are for reference only)



44-PinTQFPPackage(T44)

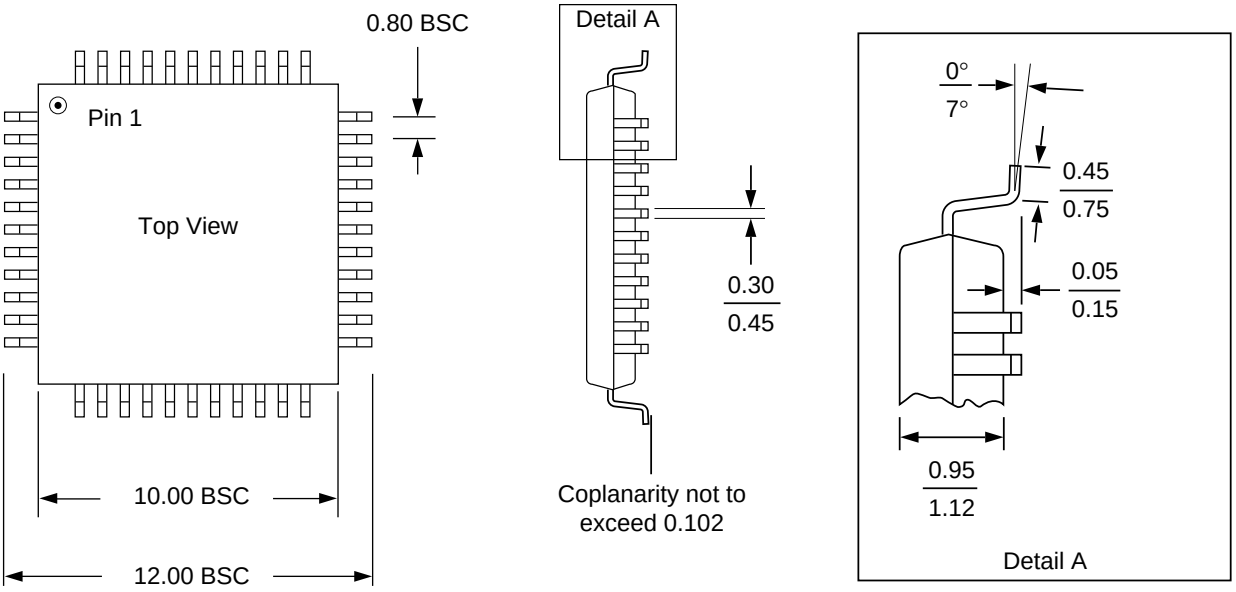
Dimensions in Millimeters MIN. / MAX.



Package Diagrams

44-PinTQFPPackage(T)

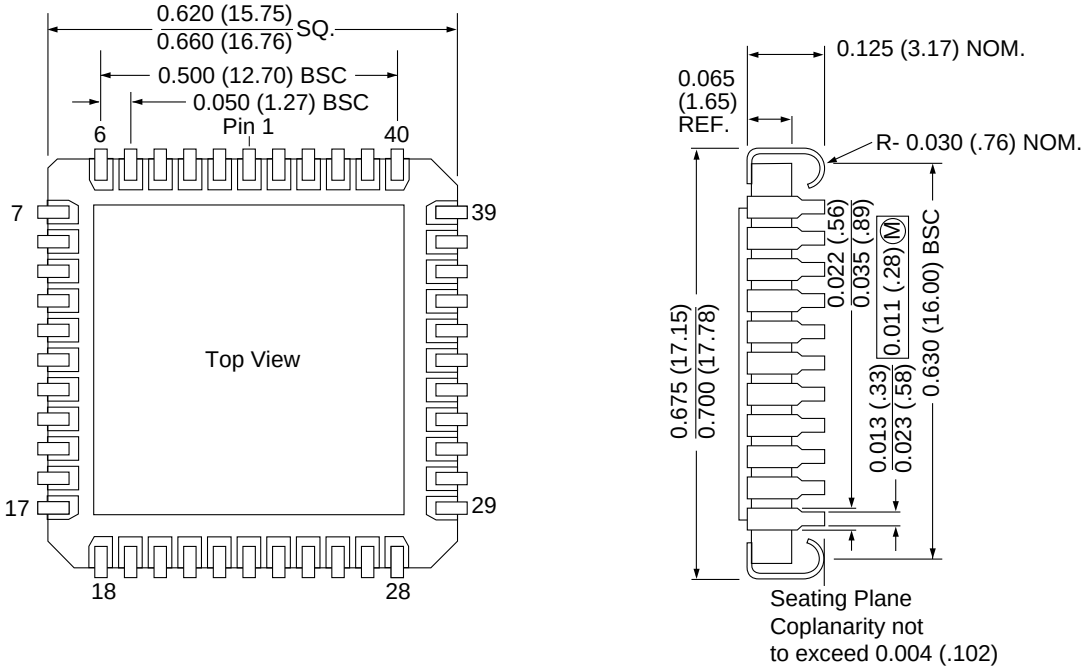
Dimensions in Millimeters MIN. / MAX.



44-PinJLCCPackage

Dimensions in Inches MIN. / MAX.

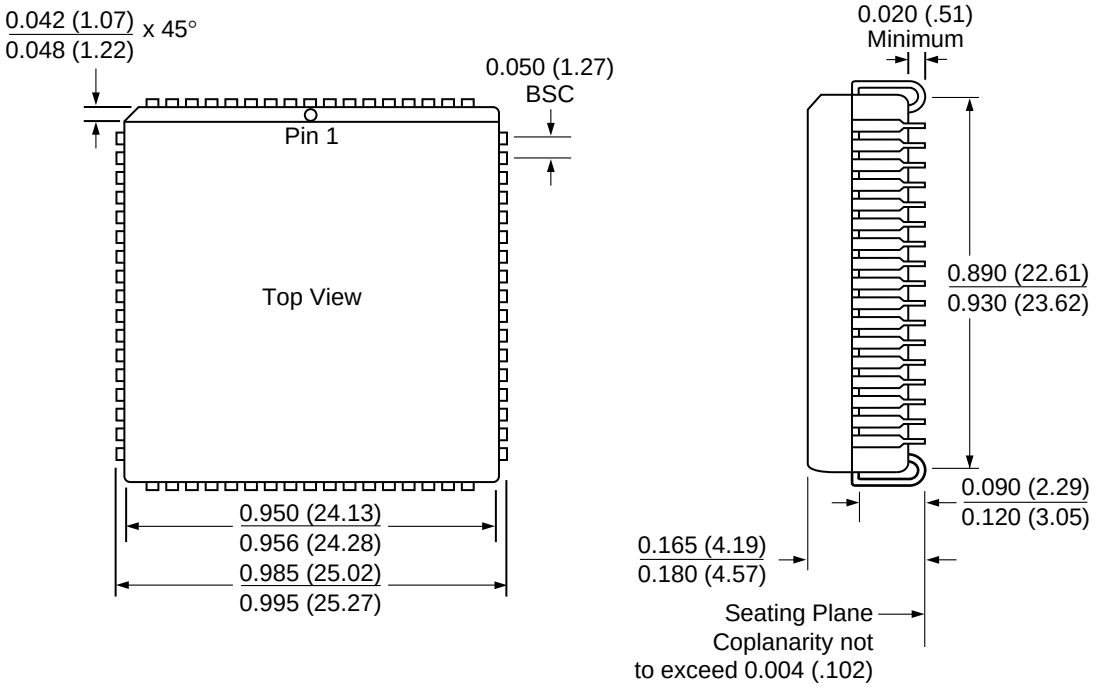
(Dimensions in millimeters, shown in parentheses, are for reference only)



68-PinPLCCPackage

Dimensions in Inches MIN. / MAX.

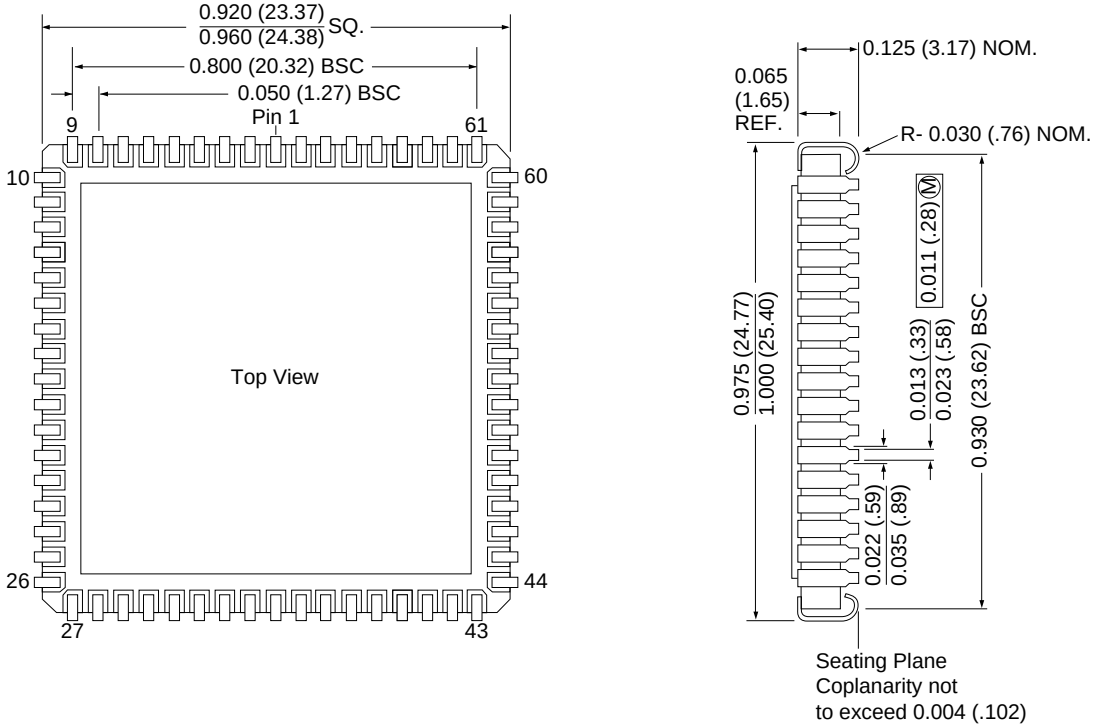
(Dimensions in millimeters, shown in parentheses, are for reference only)



68-PinJLCCPackage

Dimensions in Inches MIN. / MAX.

(Dimensions in millimeters, shown in parentheses, are for reference only)

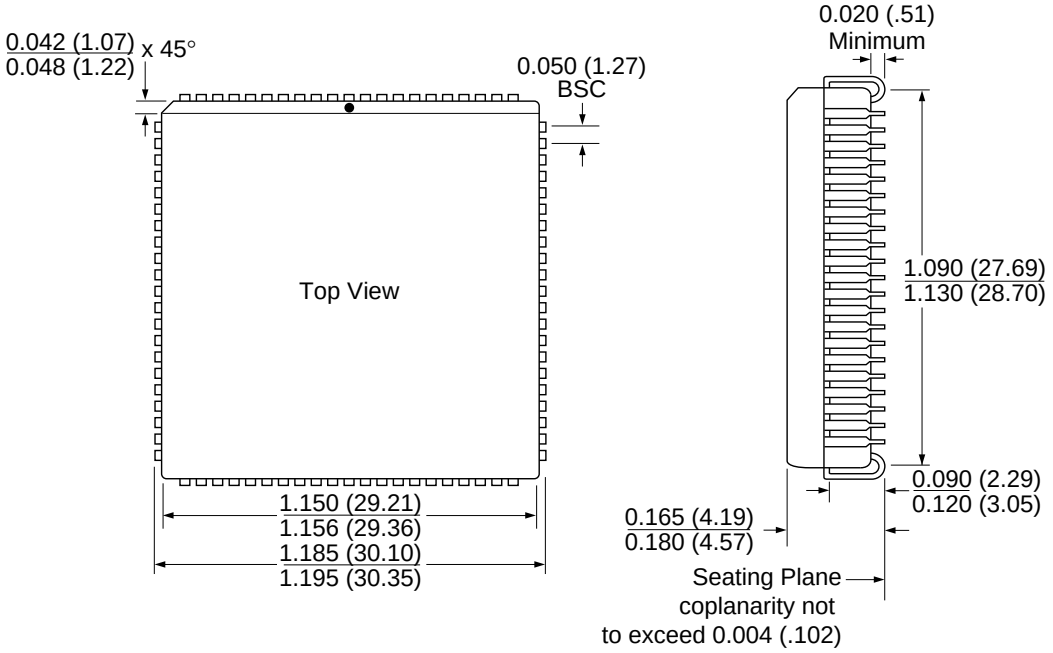


Package Diagrams

84-PinPLCCPackage

Dimensions in Inches MIN. / MAX.

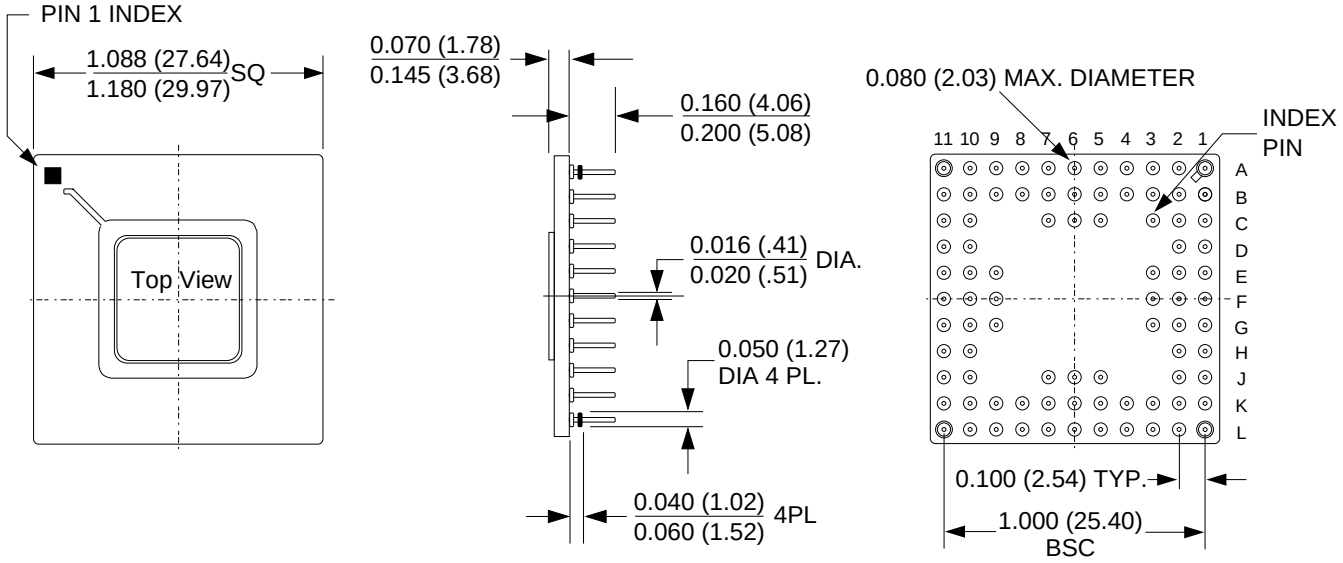
(Dimensions in millimeters, shown in parentheses, are for reference only)



84-PinCPGAPackage

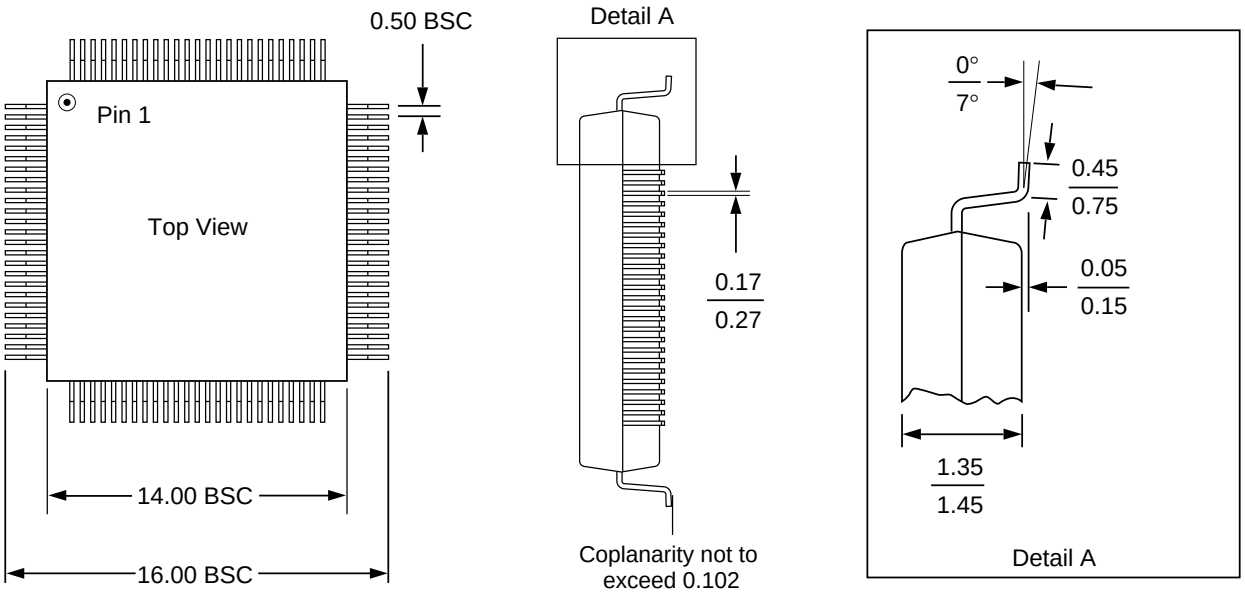
Dimensions in Inches MIN. / MAX.

(Dimensions in millimeters, shown in parentheses, are for reference only)



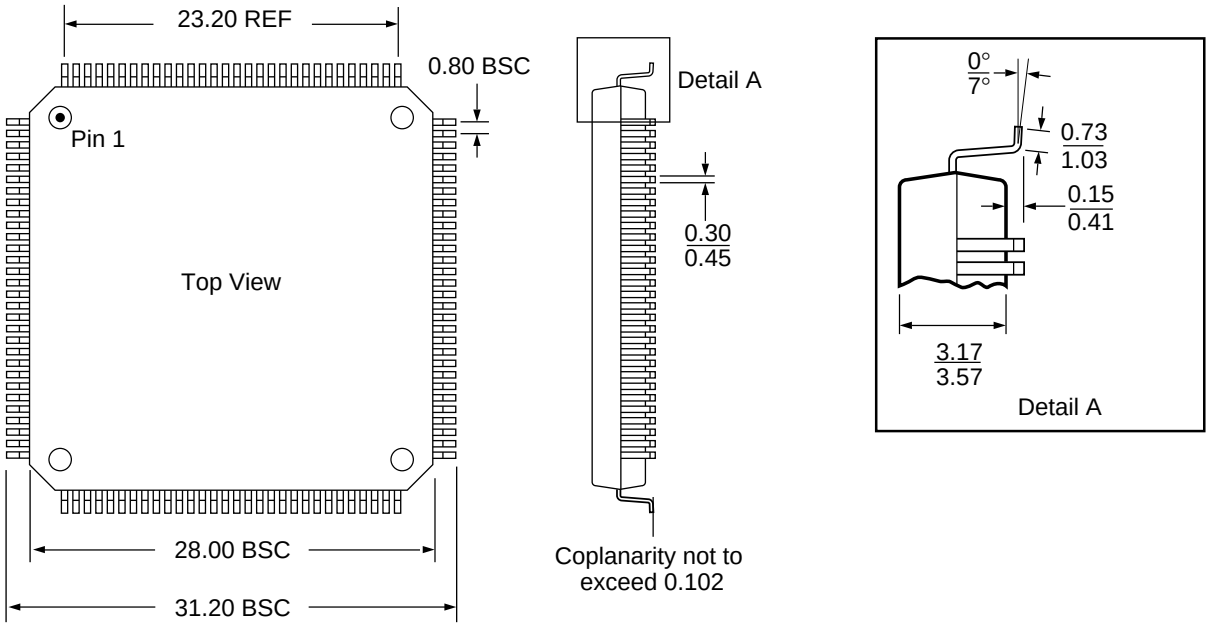
100-PinTQFPPackage

Dimensions in Millimeters MIN. / MAX.



120-PinPQFPPackage

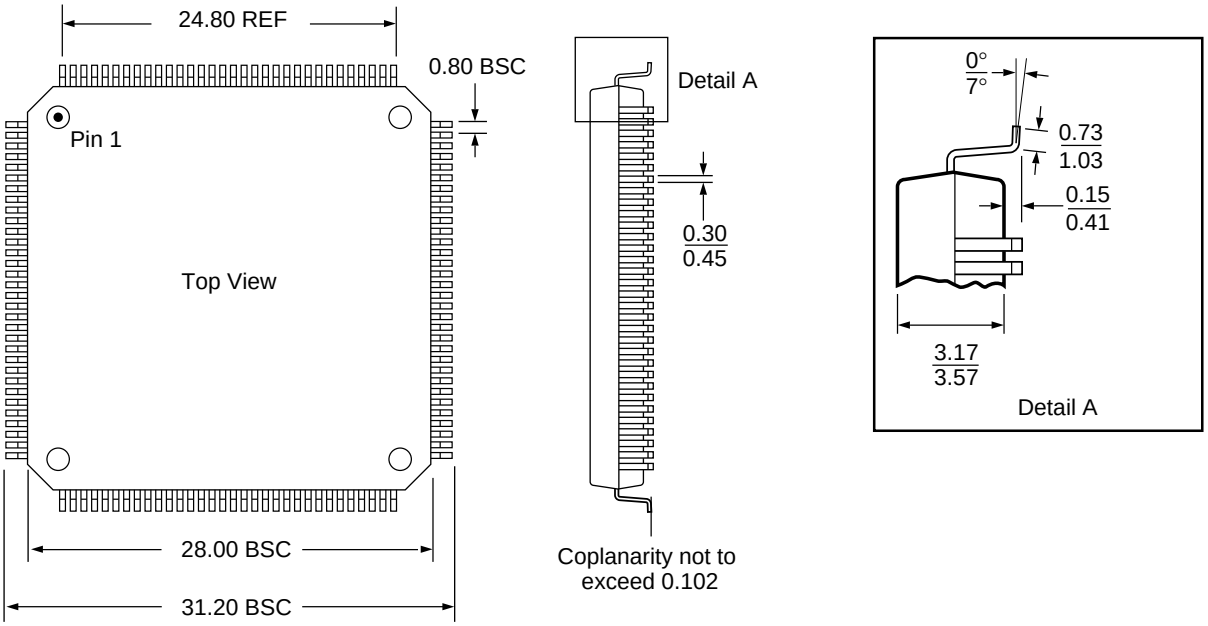
Dimensions in Millimeters MIN. / MAX.



Package Diagrams

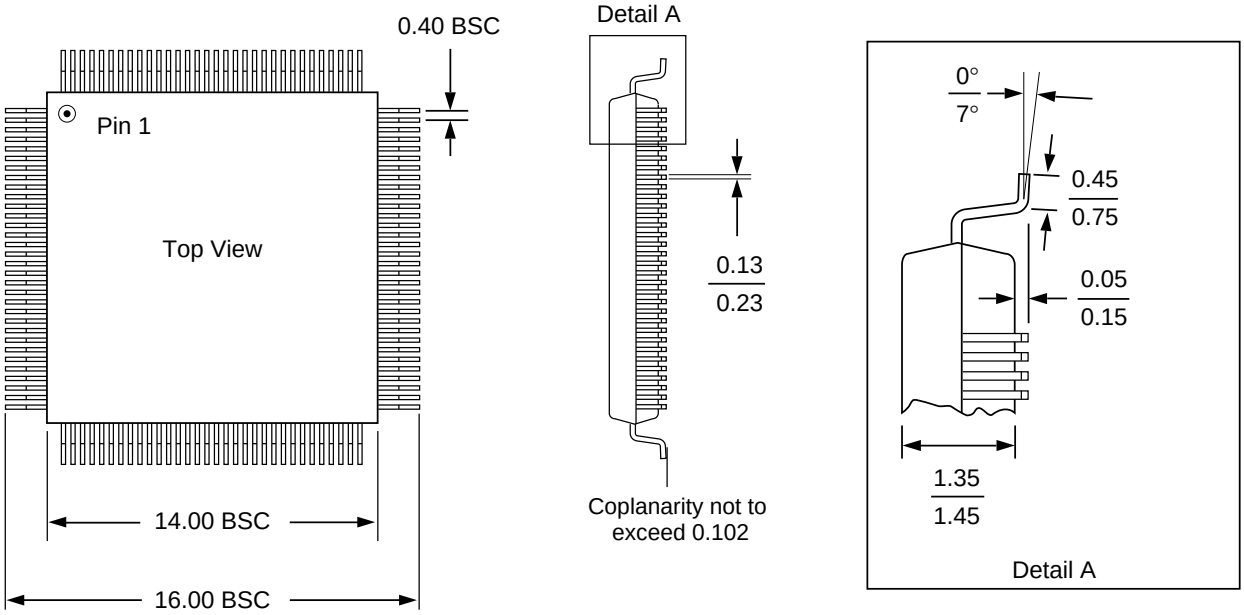
128-PinPQFPPackage

Dimensions in Millimeters MIN. / MAX.



128-PinTQFPPackage

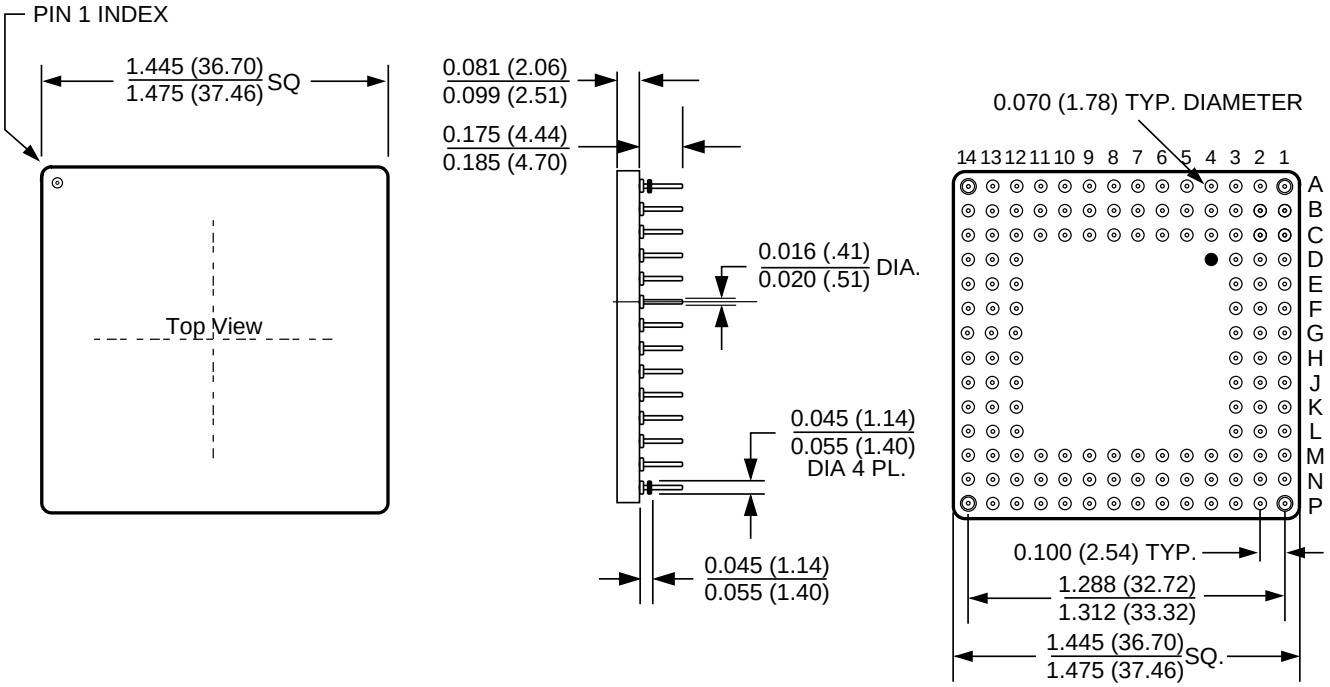
Dimensions in Millimeters MIN. / MAX.



133-PinCPGAPackage

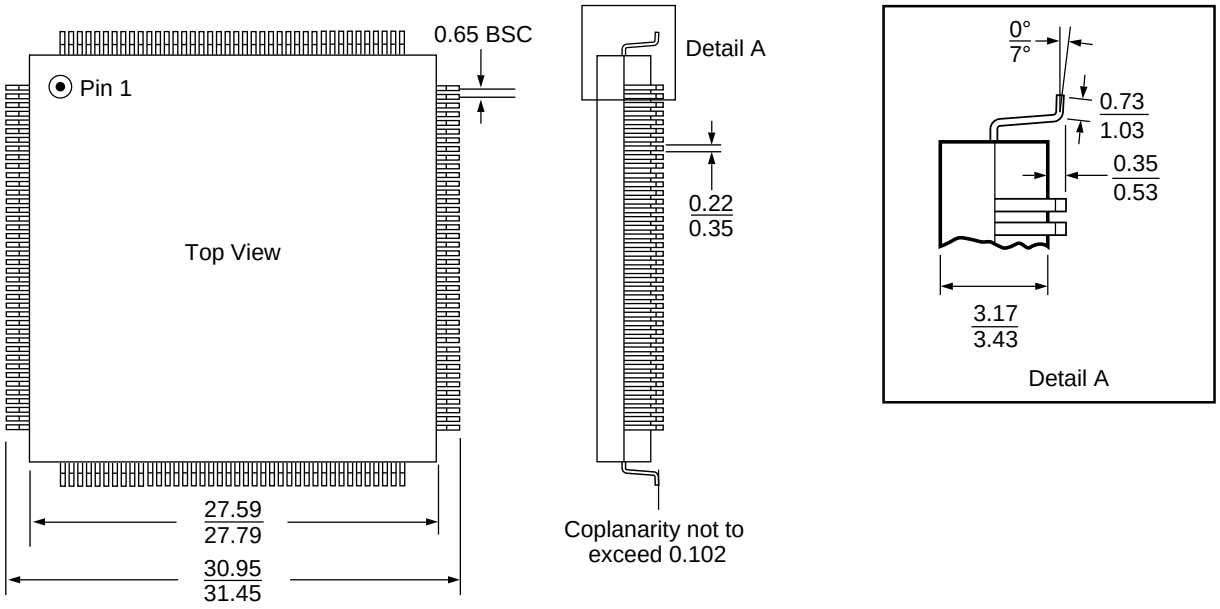
Dimensions in Inches MIN. / MAX.

(Dimensions in millimeters, shown in parentheses, are for reference only)



160-PinMQFPPackage

Dimensions in Millimeters MIN. / MAX.

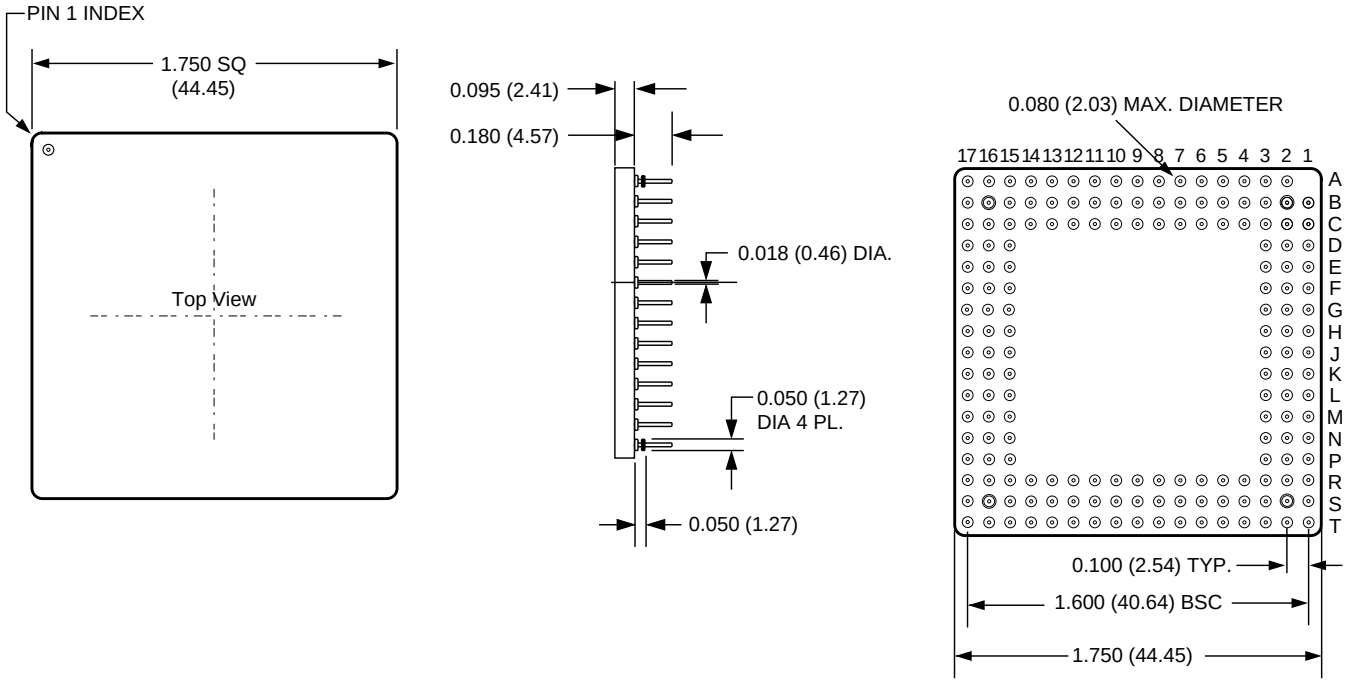


Package Diagrams

167-PinCPGAPackage

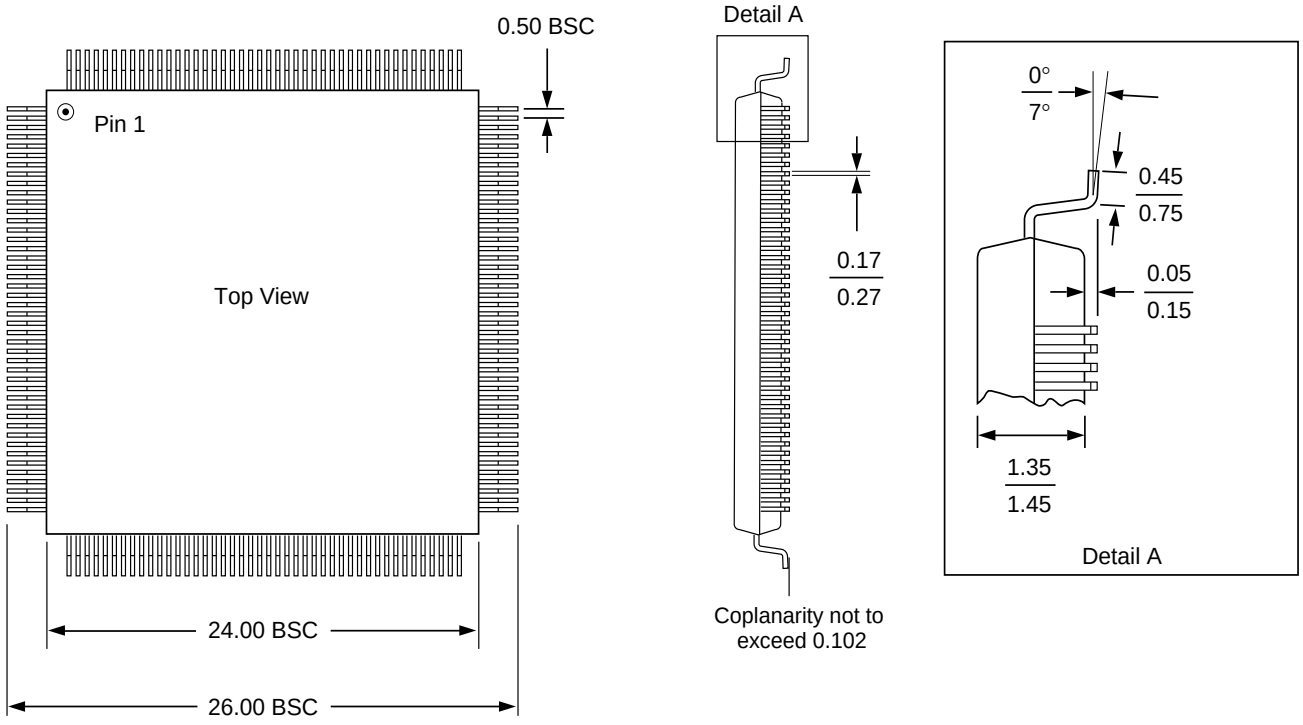
Dimensions in Inches MIN. / MAX.

(Dimensions in millimeters, shown in parentheses, are for reference only)



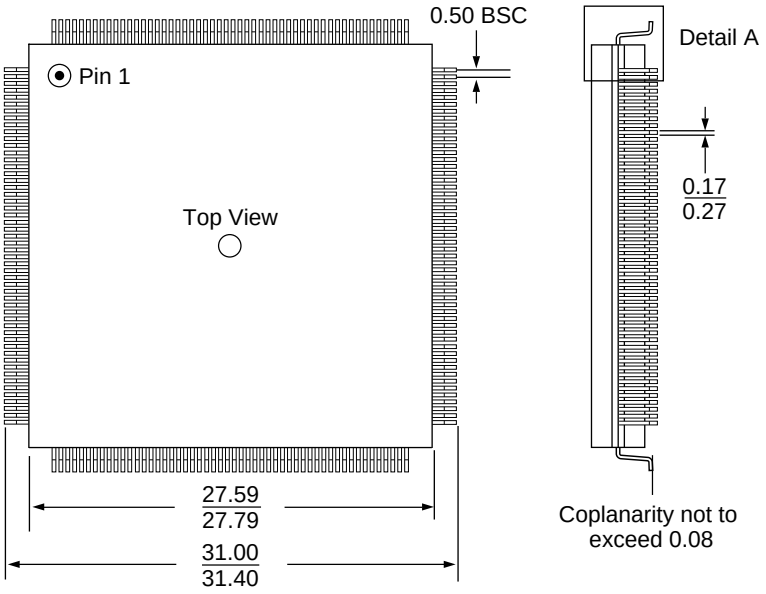
176-PinTQFPPackage

Dimensions in Millimeters MIN. / MAX.



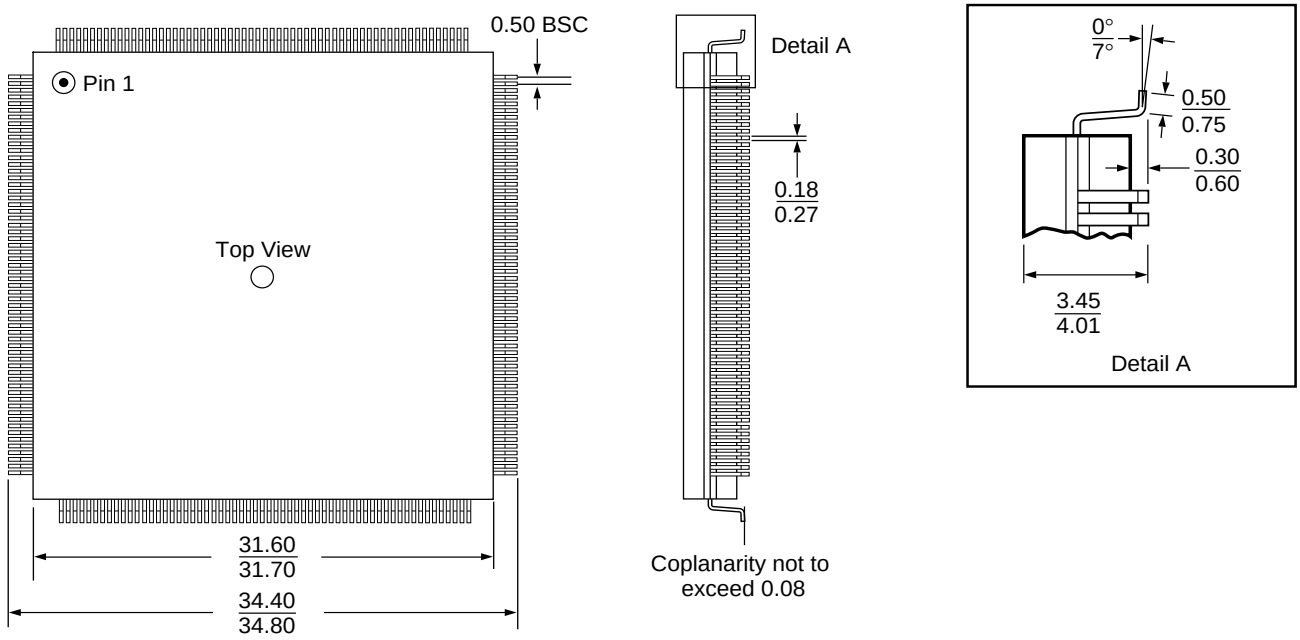
208-PinMQFPPackage

Dimensions in Millimeters MIN. / MAX.



240-PinMQFPPackage

Dimensions in Millimeters MIN. / MAX.



Technical Support

Introduction

Lattice Semiconductor Corporation (LSC) is dedicated to providing customers with comprehensive technical support. LSC Applications Engineers may be reached, via telephone, FAX or electronically.

Telephone and FAX Resources

Technical Support Hotline
Customers can receive direct technical support for all LSC products by calling LSC Applications during the hours of 8 am. to 5 p.m. Pacific Time.

LSC Literature Department
The LSC Literature Department offers a variety of technical literature to help customers select and design with programmable logic, including application notes, application briefs, data sheets, and a quarterly newsletter.

Electronic Resources

Bulletin Board Service
LSC maintains a 24-hour bulletin board service (BBS) for instant access to the latest product information. On-line versions of application notes and briefs, recent quarterly newsletters, and software utility programs are available from the BBS. The BBS can also be used to transfer files to and from the Applications Department for technical support and review. To connect to the BBS via modem, the following equipment and configuration is required: Bell Standard 212A, ccm standard, or compatible modem, up to 14,400 baud rate, 8 data bits, 1 stop bit, no parity. The following file transfer protocols are supported: ASCI1 (Non-Binary), Xmodem (Checksum), Xmodem (CRC), lK-Xmodem, Ymodem (Batch U/L and D/L), Zmodem (Batch U/L and D/L), and Kermit.

E-Mail
Customers can use E-mail to send technical questions to LSC Applications (applications@latticesemi.com or gal@latticesemi.com). E-mail is checked regularly throughout the day and is given the same priority as telephone calls. However, since E-mail delivery through the internet can be delayed, please use either the technical support hotline or fax for urgent issues.

FTP Site
Lattice Semiconductor provides a 24-hour file transfer protocol (FTP) site for instant internet access to the latest product information. On-line versions of application notes, application briefs, recent quarterly newsletters, and software utilities are available at http://www.latticesemi .com/ftp/index.html

Information Need	Customer Resource	USA & Canada	Other Locations
ispLSI® / pLSI® Applications Support	Telephone Hotline	1-800-LATTICE	(408) 428-6414
	FAX	(408) 944-8450	
	Bulletin Board System	(408) 428-6417	
	E-Mail	applications@latticesemi.com	
	FTP Site	http://www.latticesemi.com/ftp/index.html	
	World Wide Web	http://www.latticesemi.com	
GAL® / ispGAL® / ispGDS™ Applications Support	Telephone Hotline	1-800-FASTGAL	(503) 681-0118
	FAX	(503) 681-3037	
	Bulletin Board System	(503) 693-0215	
	E-Mail	gal@latticesemi.com	
	FTP Site	http://www.latticesemi.com/ftp/index.html	
	World Wide Web	http://www.latticesemi.com	
Literature	Telephone Hotline	1-800-327-8425	(503) 681-0118
	FAX	(503) 681-3037	
	E-Mail	gal@latticesemi.com	
	FTP Site	http://www.latticesemi.com/ftp/index.html	

Sales Offices

Lattice Semiconductor Sales Offices

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Notes

1996 Data Book Updates

The 1996 Lattice Semiconductor Data Book on CD-ROM includes new products and information added since the original version was printed. Below is a listing of the updates included on the CD-ROM version.

To view one of the listed documents, click on the hypertext link.

New Product Datasheets

Datasheet	Description
GAL22LV10Z/ZD	New GAL device: Zero-power, 3.3V, 22V10 architecture.
ispLSI 3256E	New ispLSI device: 256 I/O, 256 macrocells, ispLSI 3000 architecture.
pDS+ CUPL	New datasheet for pDS+ CUPL design software.

Updates to Existing Datasheets

Datasheet	Description of Update
ispGAL22V10C	Addition of new 28-pin SSOP package to commercial speed grades (ispGAL22V10C-xxLK) and new industrial grade devices (ispGAL22V10C-15LJI and ispGAL22V10C-15LKI)
ispLSI 1016	Addition of new industrial grade device (ispLSI 1016-60LT44I)
ispLSI 1024	Addition of new industrial grade device (ispLSI 1024-60LTI)
ispLSI 1032	Addition of new industrial grade device (ispLSI 1032-60LTI)
ispLSI 2032	Addition of new 48-pin TQFP packaging to commercial speed grades (ispLSI 2032-xxLT48) and new industrial grade devices (ispLSI 2032-80LJI, ispLSI 2032-80LT44I and ispLSI 2032-80LT48I)
ispLSI 2064	Addition of new industrial grade devices (ispLSI 2064-80LJI and ispLSI 2064-80LTI)
ispLSI 2096	Addition of new industrial grade devices (ispLSI 2096-80LQI and ispLSI 2096-80LTI)
ispLSI 2128	Addition of new industrial grade device (ispLSI 2128-80LTI)
ispLSI 2032LV	Change in datasheet status from Preliminary to Final and addition of new industrial grade devices (ispLSI 2032LV-60LJI and ispLSI 2032LV-60LT44I)
ispLSI 3192	Addition of new industrial grade device (ispLSI 3192-70LMI)
ispLSI 1032E	Addition of new 125MHz speed grade (ispLSI 1032E-125LT and ispLSI/pLSI 1032E-125LJ)

New Package Diagrams (Mechanical Drawings)

Package
28-pin SSOP
48-Pin TQFP
304-Pin MQFP

GAL22LV10Z
GAL22LV10ZD

Low Voltage, Zero Power E²CMOS PLD

FEATURES

- **3.3V LOW VOLTAGE, ZERO POWER OPERATION**
  - **— Interfaces with Standard 5V TTL Devices**
  - **— 50μA Typical Standby Current (100μA Max.)**
  - **— 40mA Typical Active Current (55mA Max.)**
  - **— Input Transition Detection on GAL22LV10Z**
  - **— Dedicated Power-down Pin on GAL22LV10ZD**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 15 ns Maximum Propagation Delay**
  - **— Fmax = 71.4MHz**
  - **— UltraMOS® Advanced CMOS Technology**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
  - **— Fully Function/Fuse-Map/Parametric Compatible with Bipolar and CMOS 22V10 Devices**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— Battery Powered Systems**
  - **— DMA Control**
  - **— State Machine Control**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

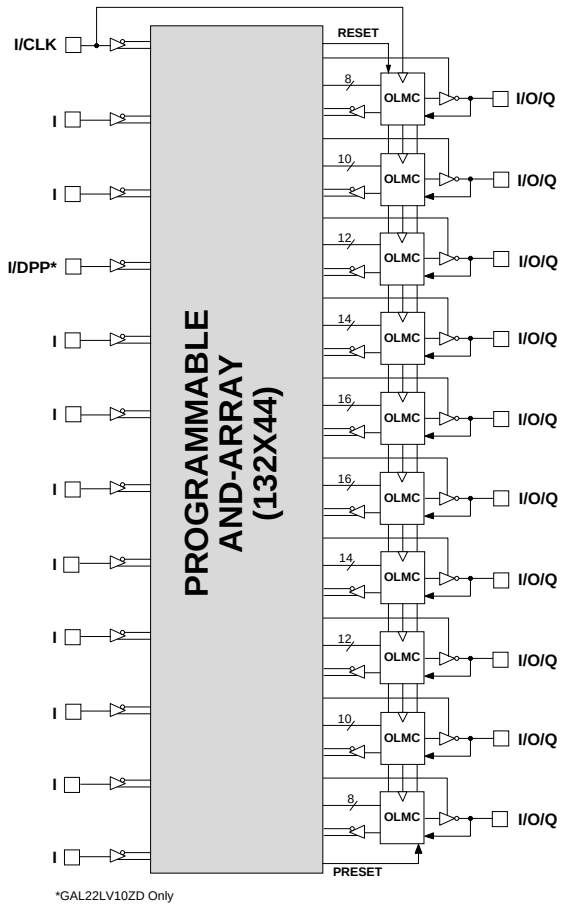
DESCRIPTION

The GAL22LV10Z and GAL22LV10ZD, at 15ns maximum propagation delay time and 100μA standby current, combine 3.3V CMOS process technology with Electrically Erasable (E^2) floating gate technology to provide the best PLD solution to support today's new 3.3V systems. E^2 technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

The generic 22V10 architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22LV10Z uses Input Transition Detection (ITD) to put the device into standby mode and is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices. The GAL22LV10ZD utilizes a Dedicated Power-down Pin (DPP) to put the device into standby mode.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor is able to guarantee 100% field programmability and functionality of all GAL® products. In addition,100 erase/rewrite cycles and data retention in excess of 20 years are guaranteed.

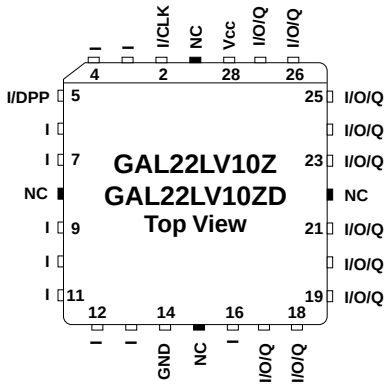
FUNCTIONAL BLOCK DIAGRAM



*GAL22LV10ZD Only

PACKAGE DIAGRAMS

PLCC



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June 1996
Order #: DS0085

GAL22LV10Z AND GAL22LV10ZD ORDERING INFORMATION

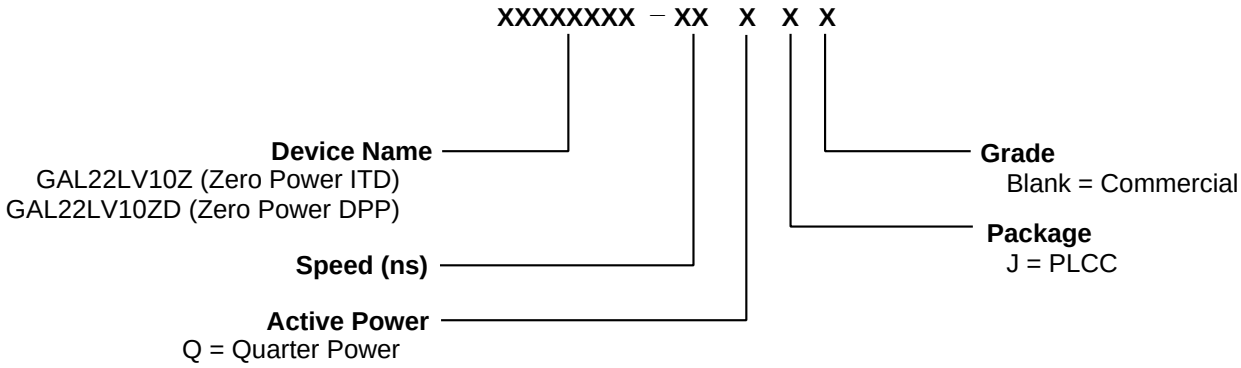
GAL22LV10Z: Commercial Grade Specifications

Tpd (ns)	Tsu1 (ns)	Tco (ns)	Icc (mA)	Isb (μA)	Ordering #	Package
15	10	10	55	100	GAL22LV10Z-15QJ	28-Lead PLCC
25	15	15	55	100	GAL22LV10Z-25QJ	28-Lead PLCC

GAL22LV10ZD: Commercial Grade Specifications

Tpd (ns)	Tsu1 (ns)	Tco (ns)	Icc (mA)	Isb (μA)	Ordering #	Package
15	10	10	55	100	GAL22LV10ZD-15QJ	28-Lead PLCC
25	15	15	55	100	GAL22LV10ZD-25QJ	28-Lead PLCC

PART NUMBER DESCRIPTION



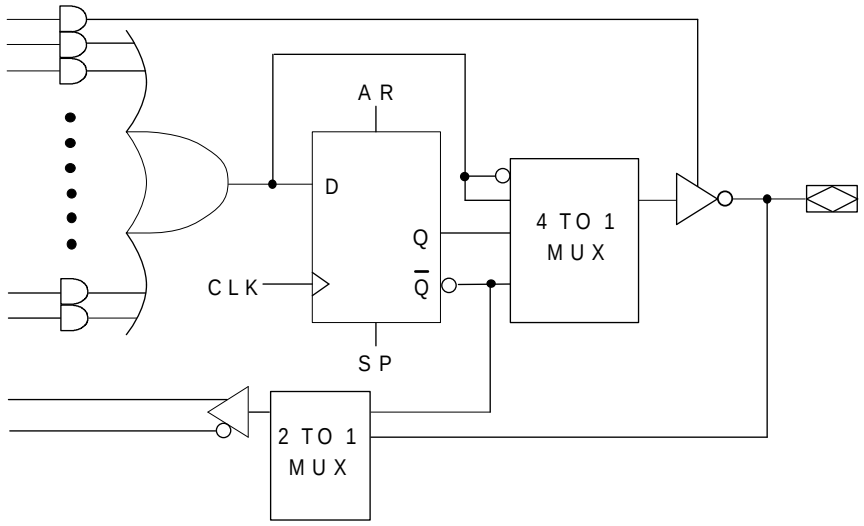
OUTPUT LOGIC MACROCELL (OLMC)

The GAL22LV10Z and GAL22LV10ZD have a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 17 and 27), two have ten product terms (pins 18 and 26), two have twelve product terms (pins 19 and 25), two have fourteen product terms (pins 20 and 24), and two OLMCs have sixteen product terms (pins 21 and 23). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL22LV10Z and GAL22LV10ZD have a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL22LV10Z AND GAL22LV10ZD OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL22LV10Z and GAL22LV10ZD have two primary functional I/O modes: registered, and combinatorial. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

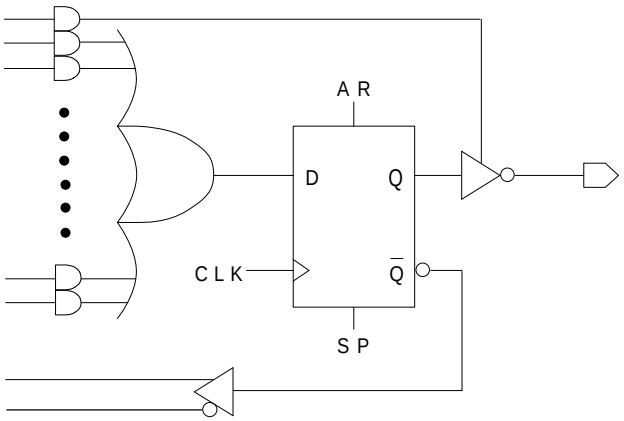
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's $\overline{Q}$ output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the $\overline{Q}$ output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

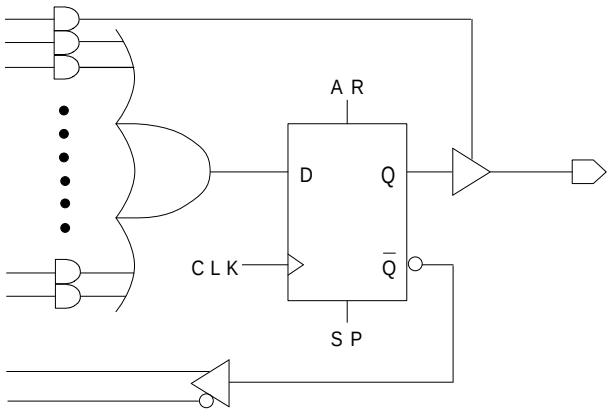
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

REGISTERED MODE



ACTIVE LOW

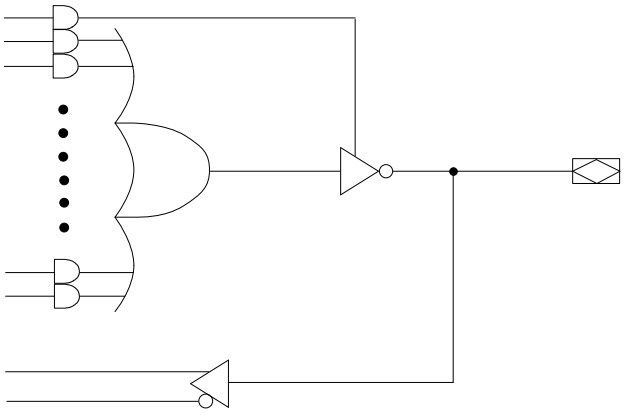
S_0 = 0
S_1 = 0



ACTIVE HIGH

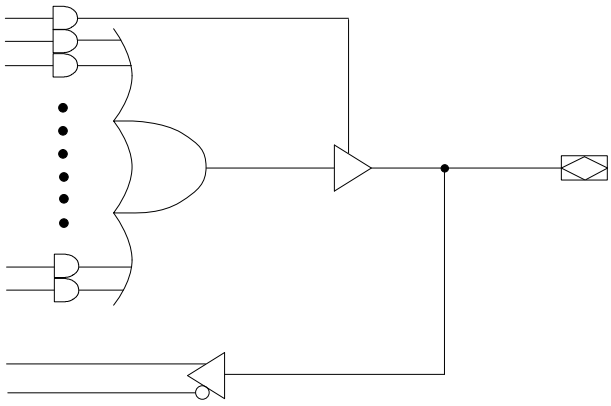
S_0 = 1
S_1 = 0

COMBINATORIAL MODE



ACTIVE LOW

S_0 = 0
S_1 = 1

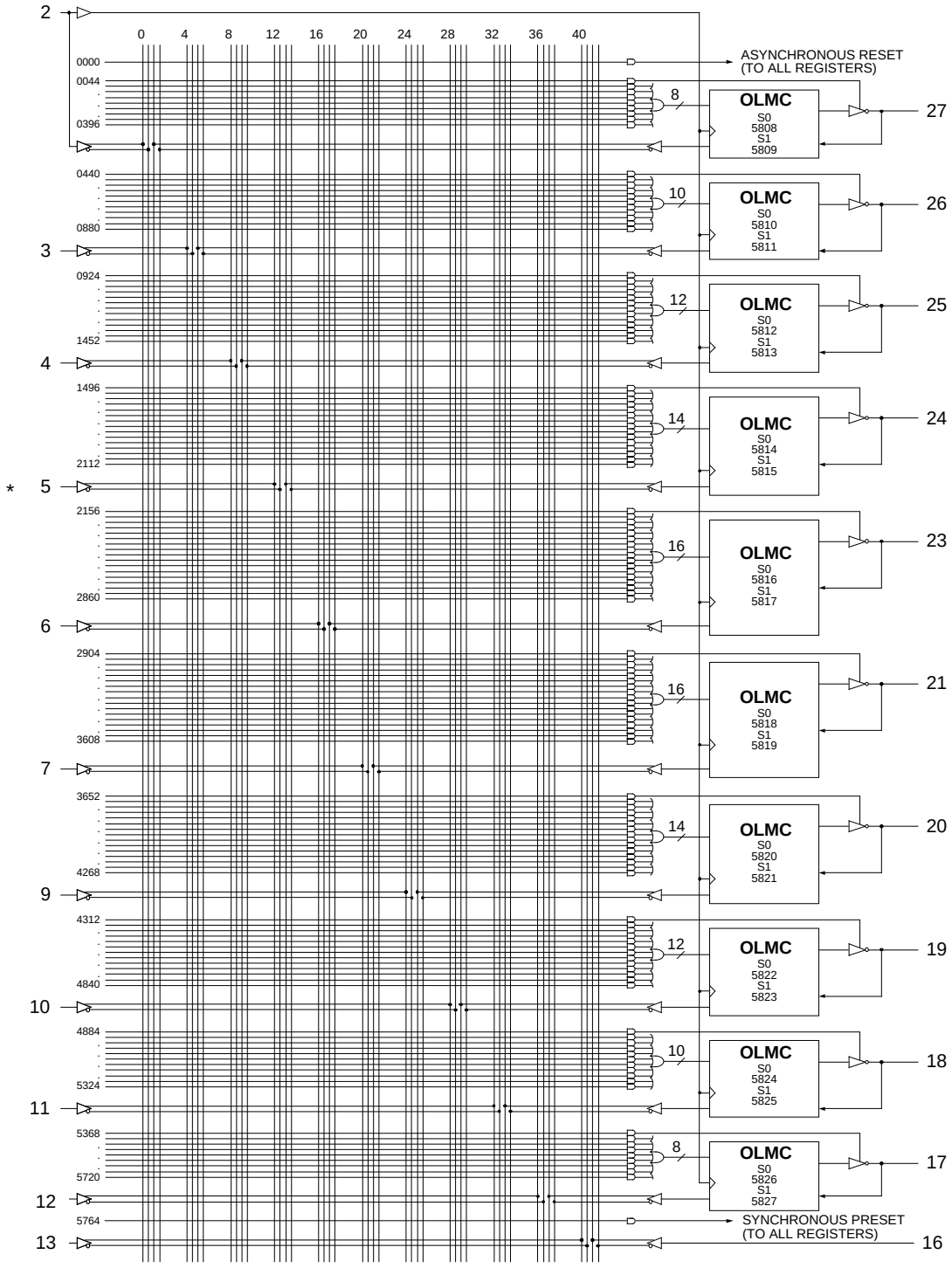


ACTIVE HIGH

S_0 = 1
S_1 = 1

GAL22LV10Z AND GAL22LV10ZD LOGIC DIAGRAM / JEDEC FUSE MAP

PLCC Package



5828, 5829 ... Electronic Signature ... 5890, 5891							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
MSB							LSB

* Note: Input not available on GAL22LV10ZD

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... -0.5 to +5.6V

Input voltage applied ..... -0.5 to +5.6V
Off-state output voltage applied ..... -0.5 to +5.6V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	5.25	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CC} - 0.2)V \le V_{IN} \le V_{CC}$	—	—	10	µA
		$V_{CC} \le V_{IN} \le 5.25V$	—	—	1	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
		I_{OL} = 0.5 mA Vin = V_{IL} or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -0.5 mA Vin = V_{IL} or V_{IH}	Vcc-0.45	—	—	V
		I_{OH} = -100 µA Vin = V_{IL} or V_{IH}	Vcc-0.2	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-8	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = 0.5V T_A = 25°C	-30	—	-130	mA

COMMERCIAL

I_{SB}	Stand-by Power Supply Current	V_{IL} = GND V_{IH} = Vcc Outputs Open	Z -15/-25 ZD -15/-25	—	50	100	µA
I_{CC}	Operating Power Supply Current	V_{IL} = GND V_{IH} = 3.0V f_{toggle} = 5 MHz Outputs Open	Z -15/-25 ZD -15/-25	—	40	55	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 3.3V and T_A = 25 °C

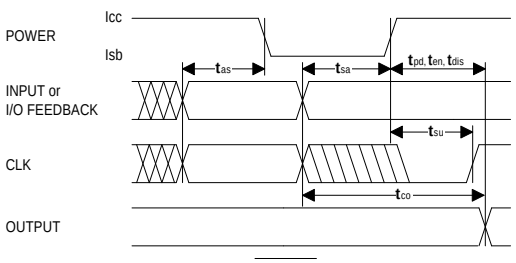
AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM	TEST COND.[1]	DESCRIPTION	COM -15 MIN.	COM -15 MAX.	COM -25 MIN.	COM -25 MAX.	UNITS
tpd	A	Input or I/O to Combinatorial Output	3	15	3	25	ns
tco	A	Clock to Output Delay	2	10	2	15	ns
tcf[2]	—	Clock to Feedback Delay	—	10	—	10	ns
tsu1	—	Setup Time, Input or Fdbk before Clk↑	10	—	15	—	ns
tsu2	—	Setup Time, SP before Clk↑	14	—	20	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	50	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	50	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	71.4	—	50	—	MHz
twh	—	Clock Pulse Duration, High	6	—	10	—	ns
twl	—	Clock Pulse Duration, Low	6	—	10	—	ns
ten	B	Input or I/O to Output Enabled	3	15	3	25	ns
tdis	C	Input or I/O to Output Disabled	3	15	3	25	ns
tar	A	Input or I/O to Asynch. Reset of Reg.	3	20	3	25	ns
tarw	—	Asynch. Reset Pulse Duration	15	—	25	—	ns
tarr	—	Asynch. Reset to Clk↑ Recovery Time	10	—	25	—	ns
tspr	—	Synch. Preset to Clk↑ Recovery Time	10	—	15	—	ns
tas	A	Last Active Input to Standby	100	250	100	250	ns
tsa[4]	A	Standby to Active Output	—	15	—	20	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.
4) Add **t**sa to **t**pd, **t**su, **t**ar, **t**en and **t**dis when the device is transitioning from standby state to active state.

STANDBY POWER TIMING WAVEFORMS



AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAM	TEST COND.[1]	DESCRIPTION	COM -15 MIN.	COM -15 MAX.	COM -25 MIN.	COM -25 MAX.	UNITS
tpd	A	Input or I/O to Combinatorial Output	3	15	3	25	ns
tco	A	Clock to Output Delay	2	10	2	15	ns
tcf[2]	—	Clock to Feedback Delay	—	10	—	10	ns
tsu1	—	Setup Time, Input or Fdbk before Clk↑	10	—	15	—	ns
tsu2	—	Setup Time, SP before Clk↑	14	—	20	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	50	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	50	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	71.4	—	50	—	MHz
twh	—	Clock Pulse Duration, High	6	—	10	—	ns
twl	—	Clock Pulse Duration, Low	6	—	10	—	ns
ten	B	Input or I/O to Output Enabled	3	15	3	25	ns
tdis	C	Input or I/O to Output Disabled	3	15	3	25	ns
tar	A	Input or I/O to Asynch. Reset of Reg.	3	20	3	25	ns
tarw	—	Asynch. Reset Pulse Duration	15	—	25	—	ns
tarr	—	Asynch. Reset to Clk↑ Recovery Time	10	—	25	—	ns
tspr	—	Synch. Preset to Clk↑ Recovery Time	10	—	15	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

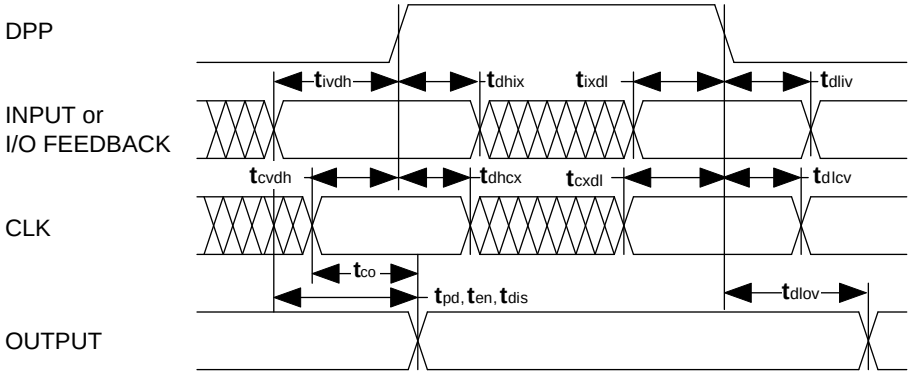
DEDICATED POWER-DOWN PIN SPECIFICATIONS

Over Recommended Operating Conditions

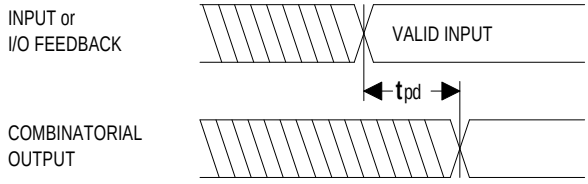
PARAMETER	TEST COND[1].	DESCRIPTION	COM -15		COM -25		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{whd}	—	DPP Pulse Duration High	40	—	40	—	ns
t_{wld}	—	DPP Pulse Duration Low	30	—	40	—	ns
ACTIVE TO STANDBY							
t_{ivdh}	—	Valid Input before DPP High	0	—	0	—	ns
t_{cvdh}	—	Valid Clock Before DPP High	0	—	0	—	ns
t_{dhix}	—	Input Don't Care after DPP High	—	15	—	25	ns
t_{dhcx}	—	Clock Don't Care after DPP High	—	15	—	25	ns
STANDBY TO ACTIVE							
t_{ixdl}	—	Input Don't Care before DPP Low	—	0	—	0	ns
t_{cxdl}	—	Clock Don't Care before DPP Low	—	0	—	0	ns
t_{dliv}	—	DPP Low to Valid Input or I/O	20	—	25	—	ns
t_{dlcv}	—	DPP Low to Valid Clock	30	—	35	—	ns
t_{dlov}	A	DPP Low to Valid Output	5	35	5	45	ns

1) Refer to **Switching Test Conditions** section.

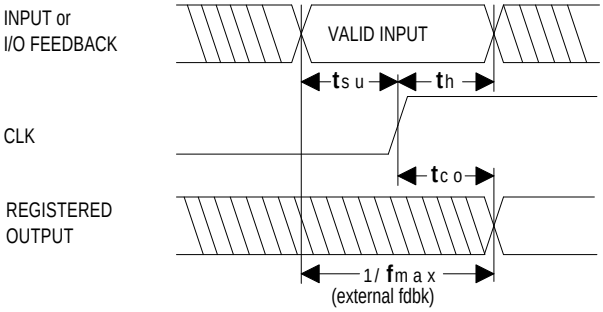
DEDICATED POWER-DOWN PIN (DPP) TIMING WAVEFORMS



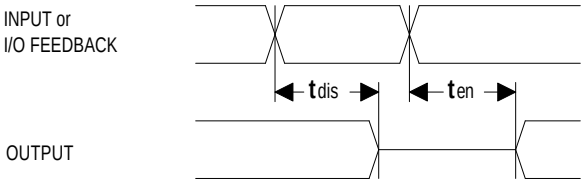
SWITCHING WAVEFORMS



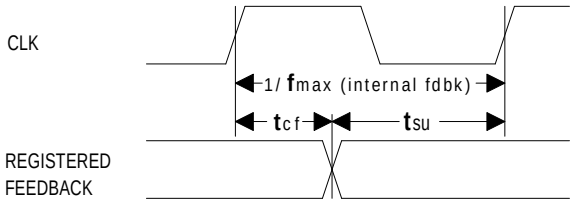
Combinatorial Output



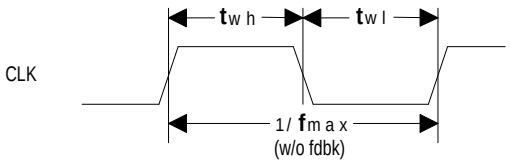
Registered Output



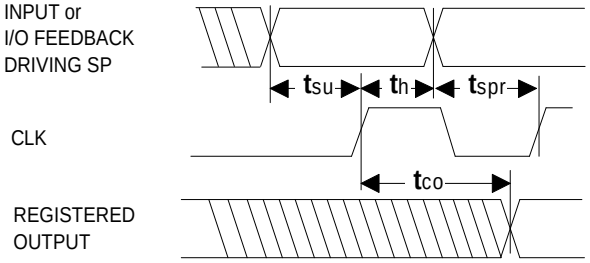
Input or I/O to Output Enable/Disable



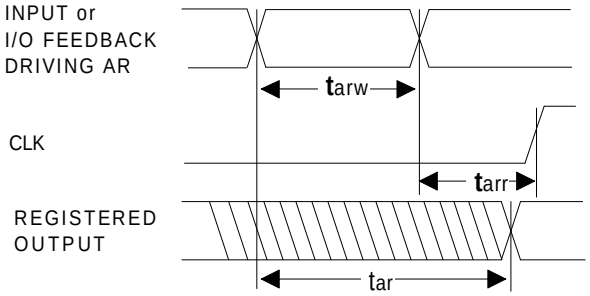
fmax with Feedback



Clock Width



Synchronous Preset



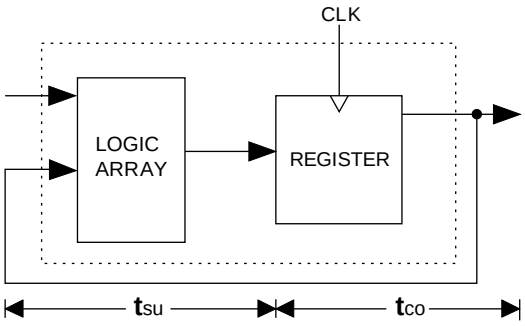
Asynchronous Reset

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TYPICAL*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 3.3V, V_I = 0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 3.3V, $V_{I/O}$ = 0V

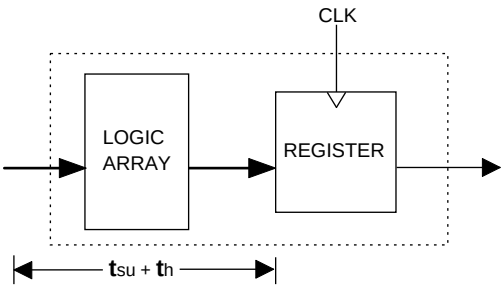
*Guaranteed but not 100% tested.

fmax DESCRIPTIONS



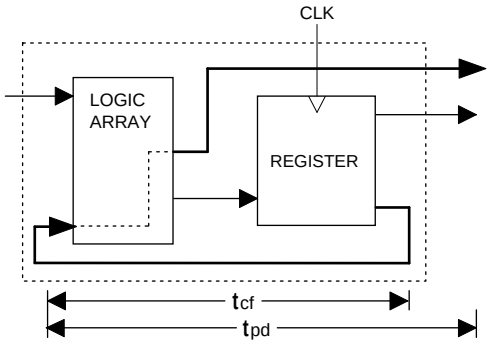
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

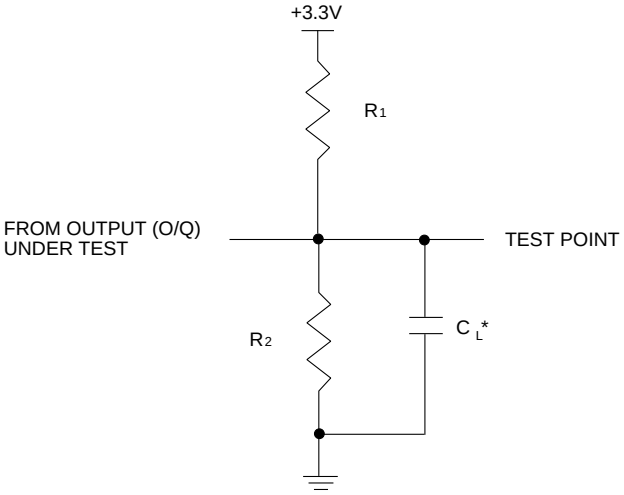
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	2ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

All 3-state levels are measured at (Voh - 0.5) V and (Vol + 0.5) V.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		270Ω	220Ω	35pF
B	Active High	270Ω	220Ω	35pF
	Active Low	270Ω	220Ω	35pF
C	Active High	270Ω	220Ω	5pF
	Active Low	270Ω	220Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided in every GAL22LV10Z and GAL22LV10ZD device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

The electronic signature is an additional feature not present in other manufacturers' 22V10 devices. To use the extra feature of the user-programmable electronic signature it is necessary to choose a Lattice Semiconductor 22LV10 device type when compiling a set of logic equations. In addition, many device programmers have two separate selections for the device, typically a GAL22LV10 and a GAL22LV10-UES (UES = User Electronic Signature). This allows users to maintain compatibility with existing 22V10 designs, while still having the option to use the GAL device's extra feature.

The JEDEC map for the GAL22LV10Z and GAL22LV10ZD contains the 64 extra fuses for the electronic signature, for a total of 5892 fuses. However, GAL22LV10Z and GAL22LV10ZD devices can still be programmed with a standard 22V10 JEDEC map (5828 fuses) with any qualified device programmer.

SECURITY CELL

A security cell is provided in every GAL22LV10Z and GAL22LV10ZD device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

DEVICE PROGRAMMING

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

GAL22LV10Z and GAL22LV10ZD devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

INPUT BUFFERS

GAL22LV10Z and GAL22LV10ZD devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

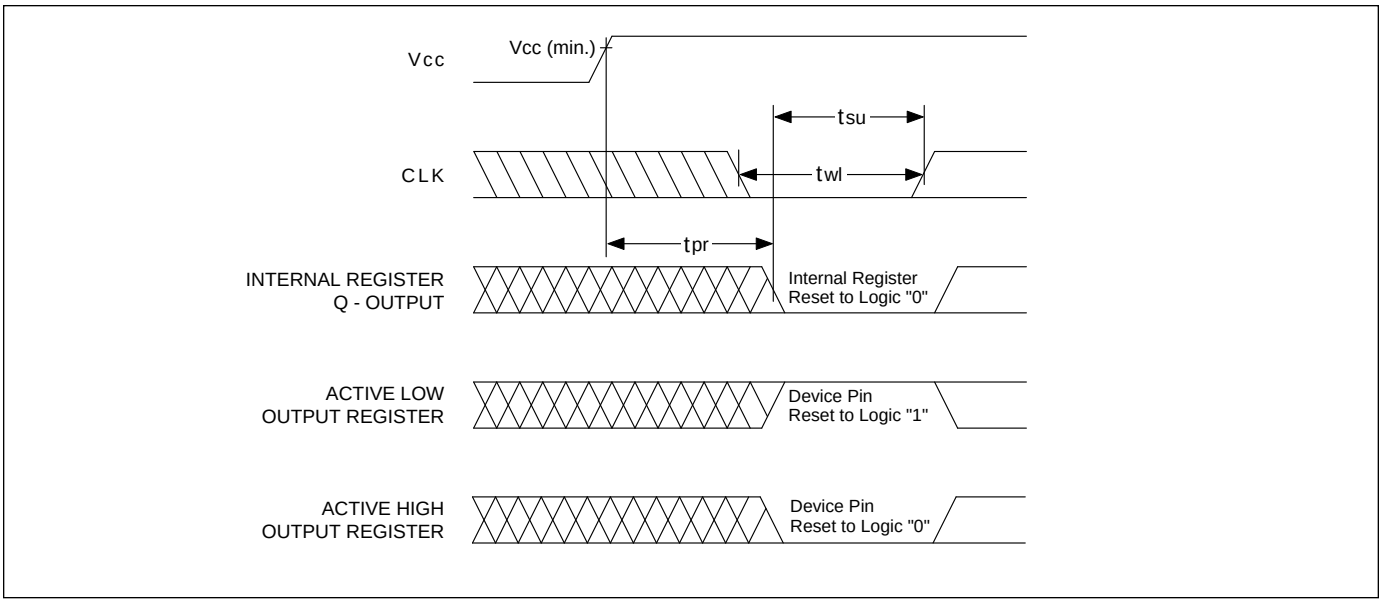
INPUT TRANSITION DETECTION (ITD)

The GAL22LV10Z relies on its internal input transition detection circuitry to put the device into power down mode. If there is no input transition for the specified period of time, the device will go into the power down state. Transition detection on any input or I/O will put the device back into the active state. Any input pulse widths greater than 5ns at an input transition voltage level of 1.5V will be detected as an input transition. The device will not detect input pulse widths less than 1ns measured at an input transition voltage level of 1.5V as an input transition.

DEDICATED POWER-DOWN PIN (DPP)

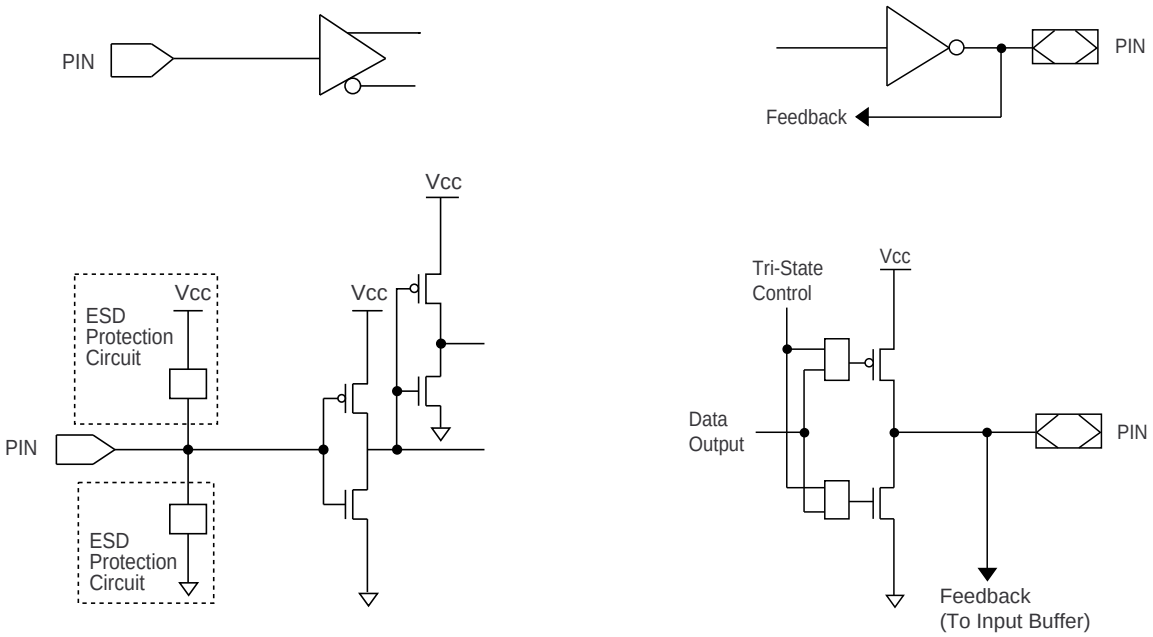
The GAL22LV10ZD uses pin 5 as the dedicated power-down signal to put the device into the standby state. DPP is an active high signal. A logic high driven onto this signal puts the device into the standby state. Input pin 5 cannot be used as a logic function input on this device.

POWER-UP RESET



Circuitry within the GAL22LV10Z and GAL22LV10ZD provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 10µs MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the device. First, the V_{CC} rise must be monotonic. Second, the clock input must be at a static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

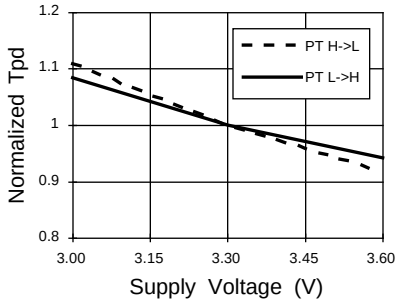
INPUT/OUTPUT EQUIVALENT SCHEMATICS



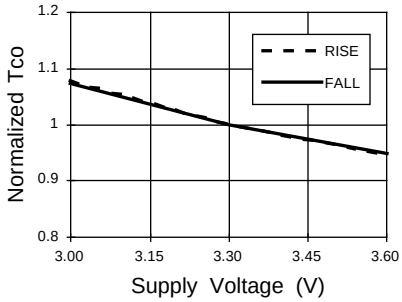
Typical Input **Typical Output**

GAL22LV10Z/ZD: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

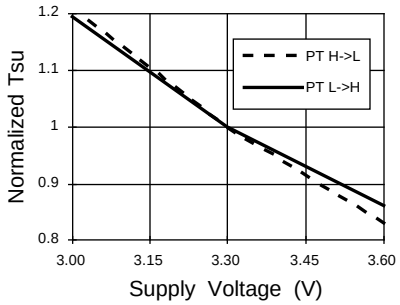
Normalized Tpd vs Vcc



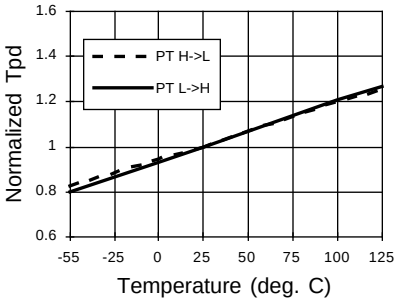
Normalized Tco vs Vcc



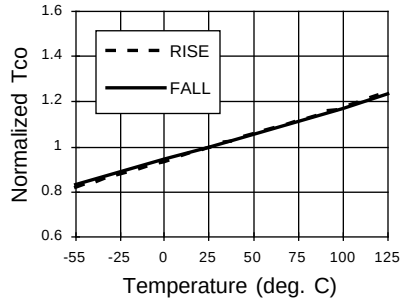
Normalized Tsu vs Vcc



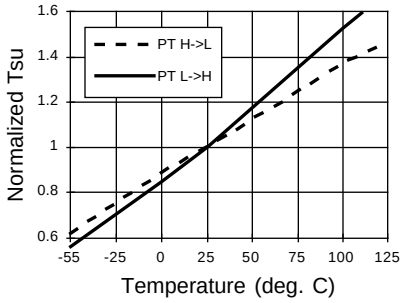
Normalized Tpd vs Temp



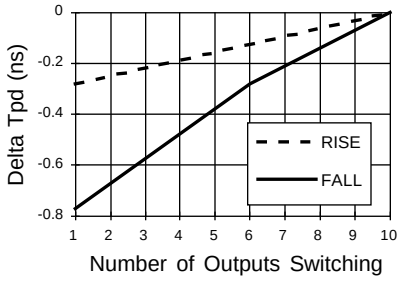
Normalized Tco vs Temp



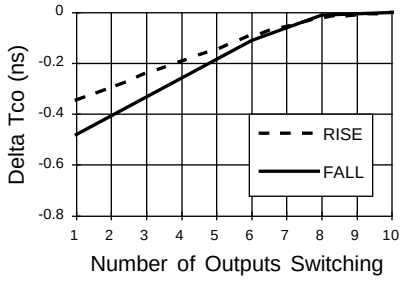
Normalized Tsu vs Temp



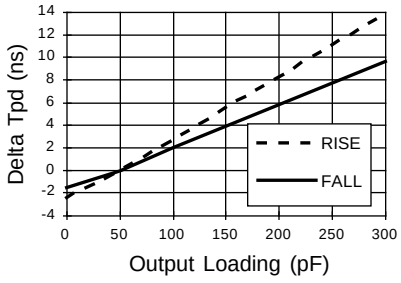
Delta Tpd vs # of Outputs Switching



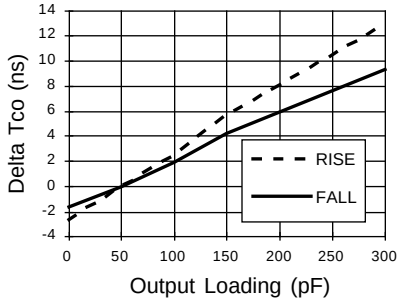
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

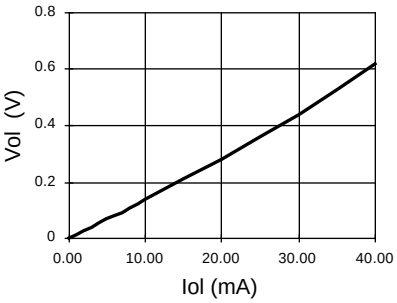


Delta Tco vs Output Loading

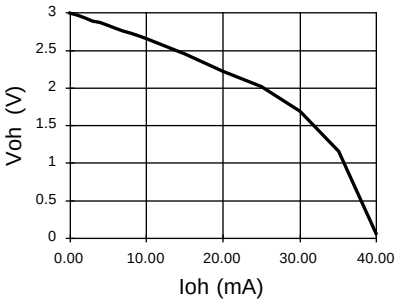


GAL22LV10Z/ZD: TYPICAL AC AND DC CHARACTERISTIC DIAGRAMS

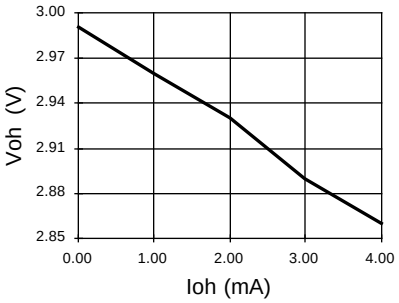
Vol vs Iol



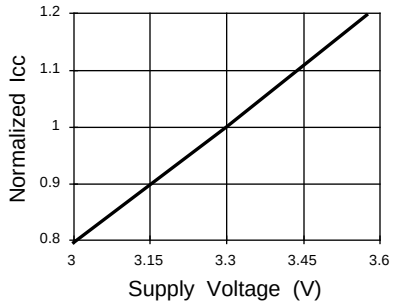
Voh vs Ioh



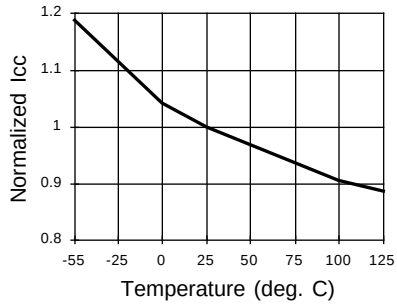
Voh vs Ioh



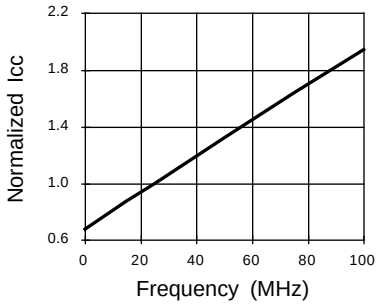
Normalized Icc vs Vcc



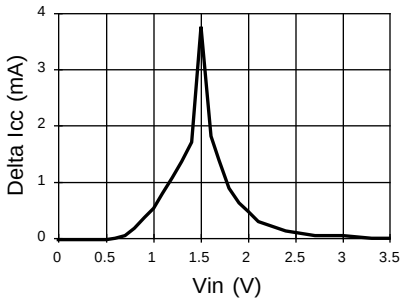
Normalized Icc vs Temp



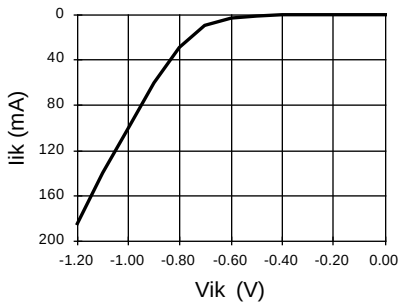
Normalized Icc vs Freq.



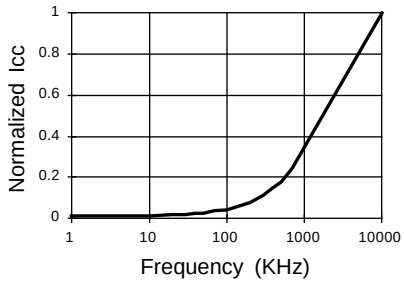
Delta Icc vs Vin (1 input)



Input Clamp (Vik)



Normalized Icc vs Freq. (ITD)



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  - **— 256 I/O Pins**
  - **— 11000 PLD Gates**
  - **— 512 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 100 MHz Maximum Operating Frequency**
  - **— t_{pd} = 10 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
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  - **— 100% Tested at Time of Manufacture**
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  - **— Reprogram Soldered Devices for Faster Debugging**
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  - **— Automatic Partitioning and Place and Route**
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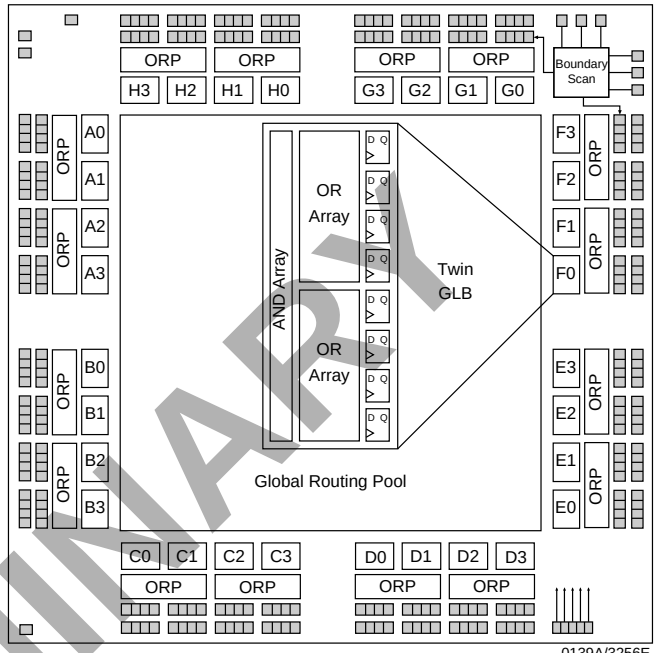
  - **— PC and Workstation Platforms**

Functional Block Diagram



0139A/3256E

Description

The ispLSI and pLSI 3256E are High Density Programmable Logic Devices which contain 512 Registers, 256 Universal I/O pins, five Dedicated Clock Input Pins, sixteen Output Routing Pools (ORP), and a Global Routing Pool (GRP) which allows complete inter-connectivity between all of these elements. The ispLSI 3256E features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 3256E offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 3256E devices.

The basic unit of logic on the ispLSI and pLSI 3256E devices is the Twin Generic Logic Block (Twin GLB) labelled A0, A1...H3. There are a total of 32 of these Twin GLBs in the ispLSI and pLSI 3256E devices. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays, and eight outputs which can be configured to be either combinatorial or registered. All Twin GLB inputs come from the GRP.

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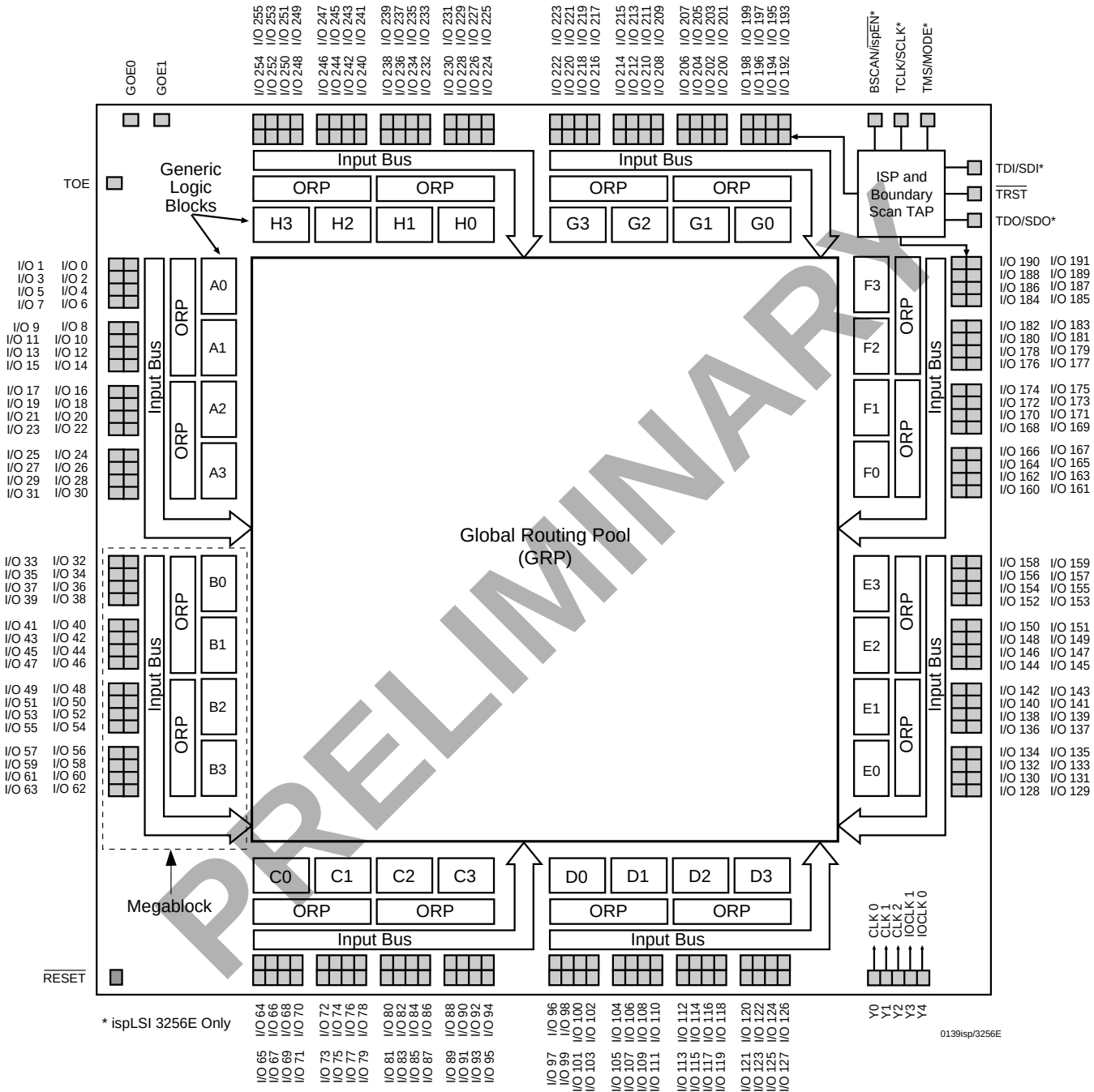
Order #: DS0087

Functional Block Diagram

Figure 1. ispLSI and pLSI 3256E Functional Block Diagram



Description (continued)

All local logic block outputs are brought back into the GRP so they can be connected to the inputs of any other logic block on the device. The device also has 256 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a registered input, a latched input, an output or a bidirectional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

The 256 I/O Cells are grouped into sixteen sets of 16 bits. Pairs of these I/O groups are associated with a logic Megablock through the use of the ORP. Each Megablock is able to provide one Product Term Output Enable (PTOE) signal which is globally distributed to all I/O cells. That PTOE signal can be generated within any GLB in the Megablock. Each I/O cell can select either a Global OE or a PTOE.

Four Twin GLBs, 32 I/O Cells and two ORPs are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of the four Twin GLBs are connected to a set of 32 I/O cells by the ORP. The ispLSI and pLSI 3256E device contains eight of these Megablocks.

The GRP has as its inputs the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the ispLSI and pLSI 3256E devices are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

The table below lists key attributes of the device along with the number of resources available.

An additional feature of the ispLSI and pLSI 3256E is the Boundary Scan capability, which is composed of cells connected between the on-chip system logic and the device's input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one.

The ispLSI and pLSI 3256E supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

Key Attributes of the ispLSI and pLSI 3256E

Attribute	Quantity
Twin GLBs	32
Registers	512
I/O Pins	256
Global Clocks	5
Global OE	2
Test OE	1

Table - 003/3256E

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied .... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2 - 0005/3256

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL [1]	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	15	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2 - 0006/3192

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2- 0008B

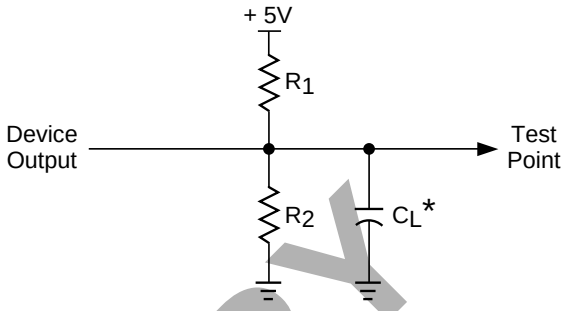
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Ouput Timing Reference Levels	1.5V
Output Load	See figure 2

Table 2 - 0003

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A

Output Load conditions (See figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
I_{IL-isp}	Bscan/ispEN Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V f_{TOGGLE} = 1 MHz	–	300	–	mA

Table 2 - 0007isp/3256E

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using sixteen 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of the 1996 Lattice Semiconductor Data Book to estimate maximum I_{CC}.

External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-100		-70		UNITS
				MIN.	MAX.	MIN.	MAX.	
tpd1	A	1	Data Prop. Delay, 4PT Bypass, ORP Bypass	—	10	—	15	ns
tpd2	A	2	Data Propagation Delay	—	13	—	18	ns
fmax	A	3	Clock Frequency with Internal Feedback[3]	100	—	70	—	MHz
fmax (Ext.)	—	4	Clock Freq. with Ext. Feedback,1/(tsu2 + tco1)	77	—	50	—	MHz
fmax (Tog.)	—	5	Clock Frequency, Max Toggle[4]	100	—	83	—	MHz
tsu1	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	5.5	—	9	—	ns
tco1	A	7	GLB Reg. Clock to Output Delay, ORP bypass	—	6.5	—	9	ns
th1	—	8	GLB Reg. Hold Time after Clock, 4PT bypass	0	—	0	—	ns
tsu2	—	9	GLB Reg. Setup Time before Clock	6.5	—	11	—	ns
tco2	—	10	GLB Reg. Clock to Output Delay	—	7	—	10	ns
th2	—	11	GLB Reg. Hold Time after Clock	0	—	0	—	ns
tr1	A	12	Ext. Reset Pin to Output Delay	—	13.5	—	15	ns
trw1	—	13	Ext. Reset Pulse Duration	6.5	—	12	—	ns
tptoeen	B	14	Input to Output Enable	—	16	—	19	ns
tptoedis	C	15	Input to Output Disable	—	16	—	19	ns
tgoeen	B	16	Global OE Output Enable	—	9	—	12	ns
tgoedis	C	17	Global OE Output Disable	—	9	—	12	ns
ttoeen	—	18	Test OE Output Enable	—	12	—	15	ns
ttoedis	—	19	Test OE Output Disable	—	12	—	15	ns
twh	—	20	Ext. Sync. Clock Pulse Duration, High	5	—	6	—	ns
twl	—	21	Ext. Sync. Clock Pulse Duration, Low	5	—	6	—	ns
tsu3	—	22	I/O Reg. Setup Time before Ext. Sync. Clock (Y3, Y4)	4.5	—	5	—	ns
th3	—	23	I/O Reg. Hold Time after Ext. Sync. Clock (Y3, Y4)	0	—	0	—	ns

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Timing Ext.3256E.eps

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-100		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
tiobp	24	I/O Register Bypass	—	2.4	—	4.0	ns
tiolat	25	I/O Latch Delay	—	4.4	—	7.0	ns
tiosu	26	I/O Register Setup Time before Clock	3.9	—	4.4	—	ns
tioh	27	I/O Register Hold Time after Clock	-0.7	—	-1.1	—	ns
tioch	28	I/O Register Clock to Out Delay	—	6.7	—	8.9	ns
tior	29	I/O Register Reset to Out Delay	—	5.8	—	7.5	ns
GRP							
tgrp	30	GRP Delay	—	2.3	—	3.2	ns
GLB							
t4ptbp	31	4 Product Term Bypass Path Delay (Comb.)	—	3.2	—	3.6	ns
t4ptbr	32	4 Product Term Bypass Path Delay (Reg.)	—	3.1	—	4.8	ns
t1ptxor	33	1 Product Term/XOR Path Delay	—	4.0	—	5.1	ns
t20ptxor	34	20 Product Term/XOR Path Delay	—	4.1	—	5.2	ns
txoradj	35	XOR Adjacent Path Delay[3]	—	4.3	—	5.7	ns
tgbp	36	GLB Register Bypass Delay	—	1.5	—	1.6	ns
tgsu	37	GLB Register Setup Time before Clock	0.3	—	1.2	—	ns
tgh	38	GLB Register Hold Time after Clock	5.0	—	7.6	—	ns
tgco	39	GLB Register Clock to Output Delay	—	1.6	—	3.0	ns
tgro	40	GLB Register Reset to Output Delay	—	5.2	—	5.2	ns
tptre	41	GLB Product Term Reset to Register Delay	—	4.0	—	4.4	ns
tptoe	42	GLB Product Term Output Enable to I/O Cell Delay	—	6.5	—	6.9	ns
tptck	43	GLB Product Term Clock Delay	3.0	3.6	3.4	4.2	ns
ORP							
torp	44	ORP Delay	—	1.2	—	1.9	ns
torpbp	45	ORP Bypass Delay	—	0.7	—	0.9	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Timing Int.3256E.eps

Internal Timing Parameters[1]

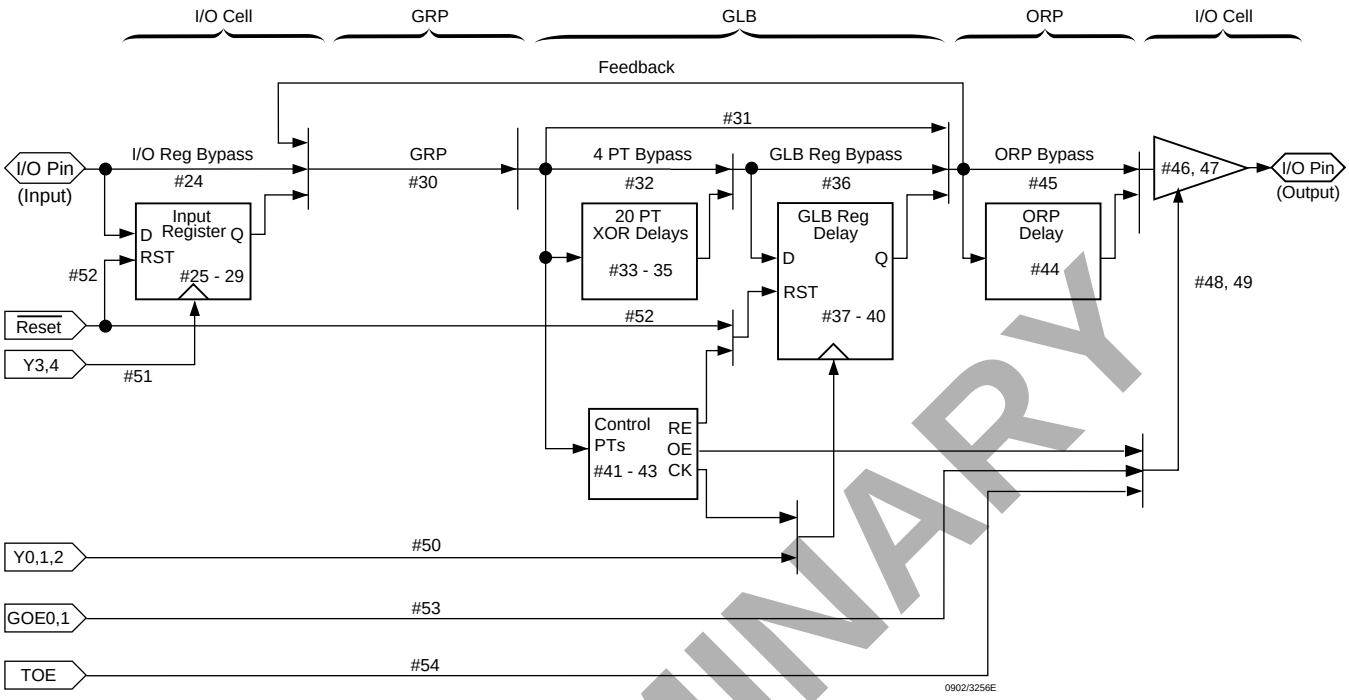
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-100		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
tob	46	Output Buffer Delay	—	2.6	—	3.3	ns
tobs	47	Output Buffer Delay, Slow Slew	—	17.6	—	18.3	ns
toen	48	I/O Cell OE to Output Enabled	—	5.5	—	5.7	ns
todis	49	I/O Cell OE to Output Disabled	—	5.5	—	5.7	ns
Clocks							
tgy0/1/2	50	Clock Delay, Y0 or Y1 or Y2 to Global GLB Clk Line	1.6	1.6	1.8	1.8	ns
tioy3/4	51	Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line	0.3	1.6	0.8	2.5	ns
Global Reset							
tgr	52	Global Reset to GLB and I/O Registers	—	4.5	—	4.6	ns
tgoe	53	Global OE Pad Buffer	—	5.9	—	7.5	ns
ttoe	54	Test OE Pad Buffer	—	6.1	—	8.9	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

Timing Int.2.3256E.eps

ispLSI and pLSI 3256E Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**iobp + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp + **t**ptck(min))
	=	(#24+ #30+ #34) + (#37) - (#24+ #30+ #43)
1.4 ns	=	(2.4 + 2.3 + 4.1) + (0.3) - (2.4 + 2.3 + 3.0)
th	=	Clock (max) + Reg h - Logic
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp + **t**20ptxor)
	=	(#24+ #30+ #43) + (#38) - (#24+ #30+ #34)
4.5 ns	=	(2.4 + 2.3 + 3.6) + (5.0) - (2.4 + 2.3 + 4.1)
tco	=	Clock (max) + Reg co + Output
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#24 + #30 + #43) + (#39) + (#44 + #46)
13.7 ns	=	(2.4 + 2.3 + 3.6) + (1.6) + (1.2 + 2.6)

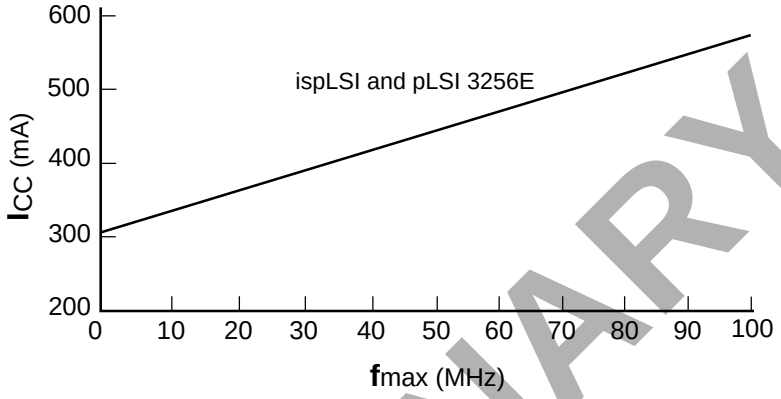
Table 2- 0042-3256E

Note: Calculations are based upon timing specifications for the ispLSI and pLSI 3256E-100L.

Power Consumption

Power Consumption in the ispLSI and pLSI 3256E device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of 16 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI and pLSI 3256E using the following equation:

I_{CC} = 60 + (# of PTs * 0.48) + (# of nets * Max. freq * 0.0106) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127/3256E

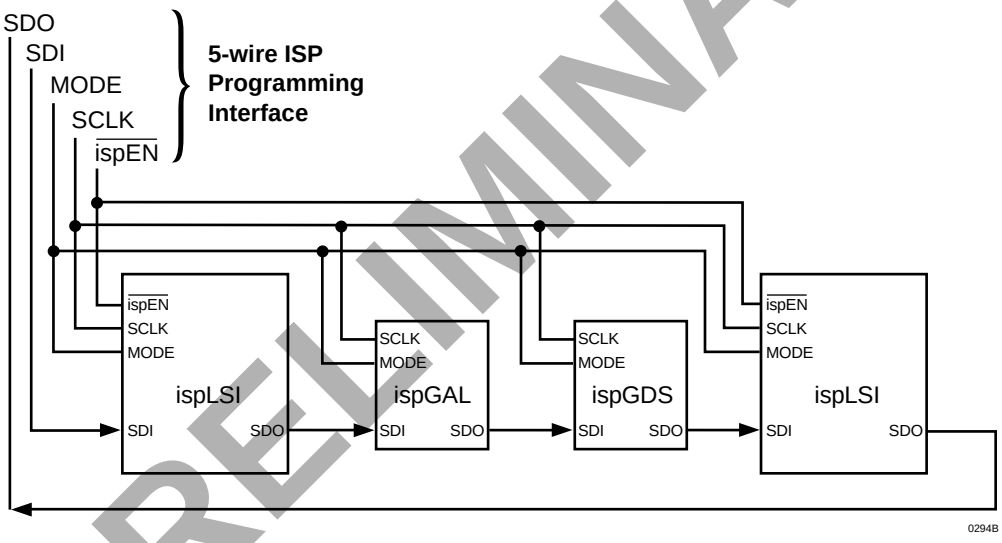
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

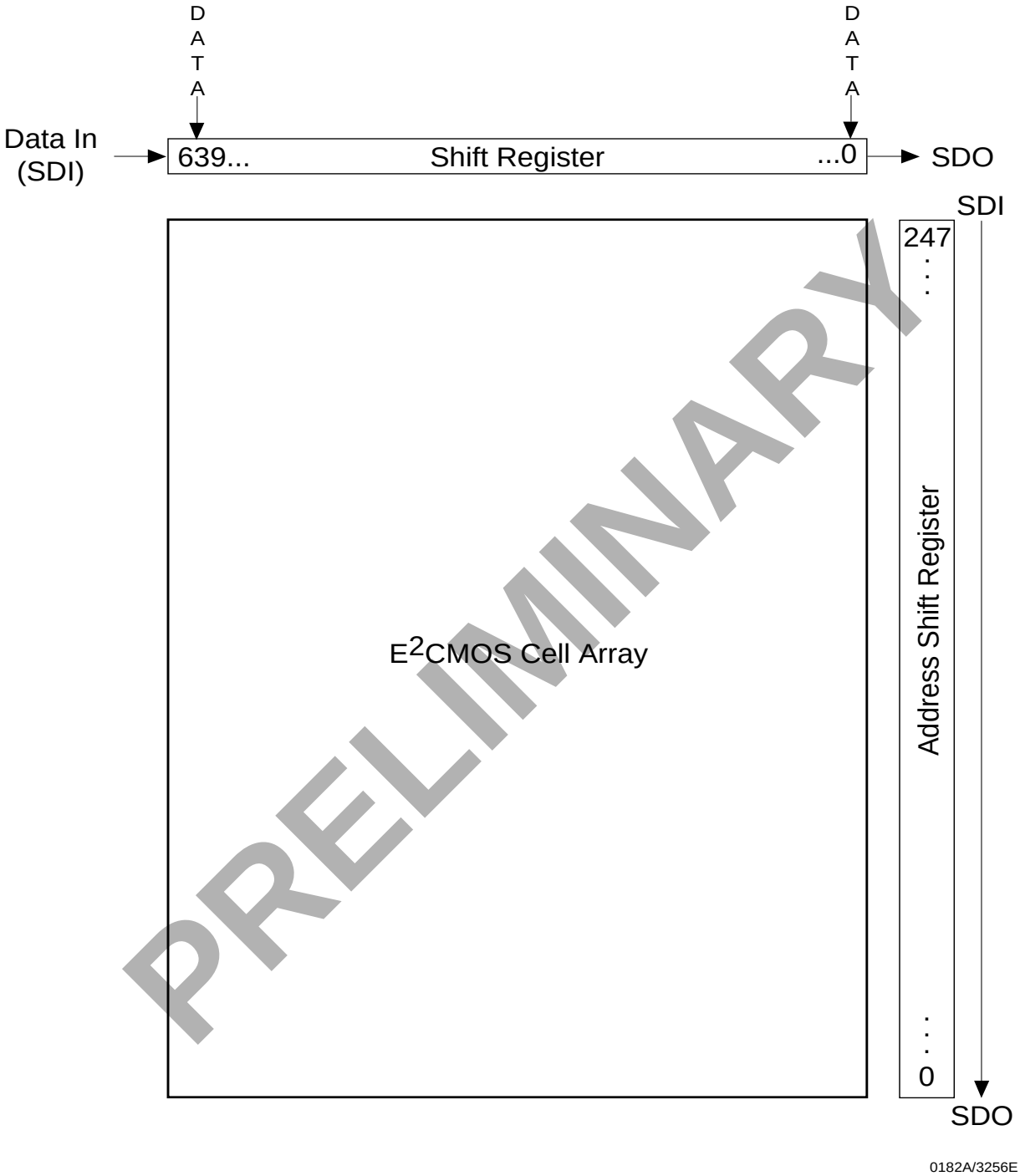
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for interface include isp™ Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section in the 1996 Lattice Semiconductor Data Book.

The device identifier for the ispLSI 3256E is 0010 0011 (23 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 3256E Shift Register Layout



Note: A logic “1” in the address shift register enables the row for programming or verification. A logic “0” disables it.

Boundary Scan

Lattice Semiconductor offers support for the IEEE 1149.1 Boundary Scan specification on the 3000 Family of devices.

The user interfaces to the boundary scan circuitry through the Test Access Port (TAP). The TAP consists of a control state machine, instruction decoder and instruction register.

The TAP is controlled using the test control lines: Test Data IN (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Reset ($\overline{TRST}$) and Test Clock (TCK).

All of the input cells and I/O cells are serially connected together in a long chain. The scan out of one cell is connected to the scan in of the next cell. The cells are connected in the following order: TDI to GOE0, GOE1, Y0, Y1, Y2, Y3, Y4, TOE, $\overline{RESET}$, I/O127 thru I/O0 to I/O128 thru I/O255 to TDO.

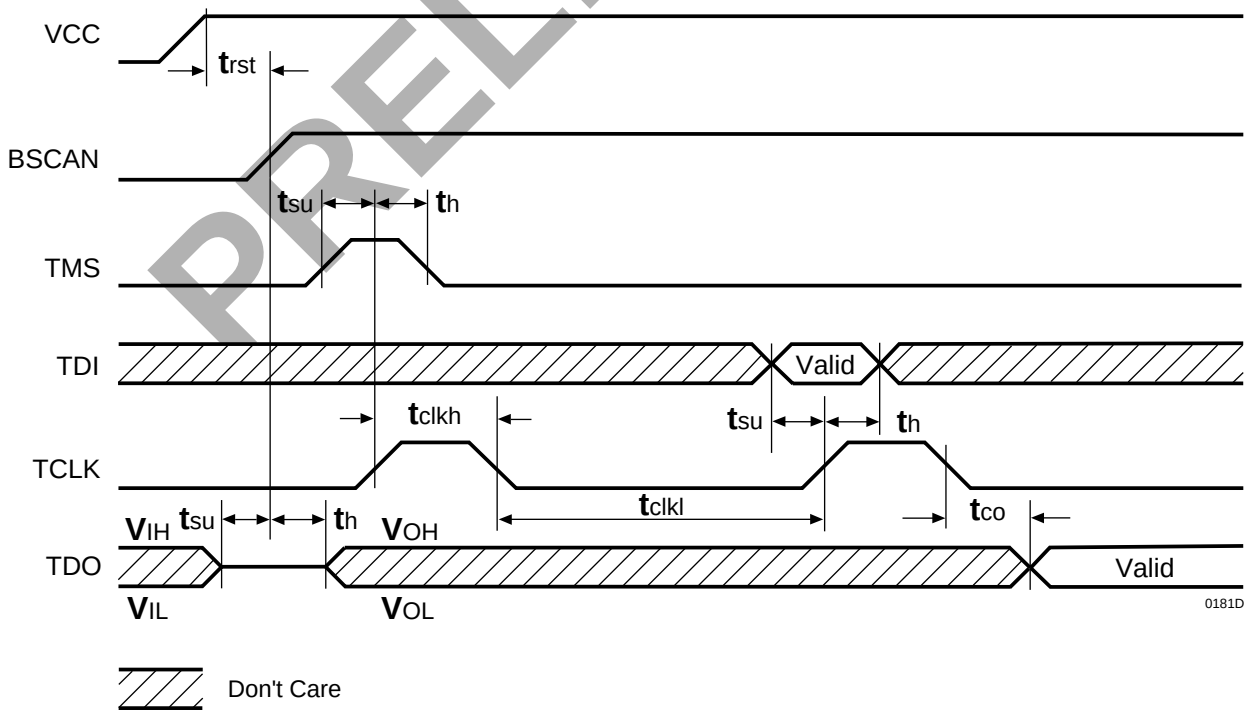
The timing specifications for Boundary Scan are listed below. The waveforms are shown in figure 5.

Boundary Scan Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
t_{rst}	Reset Time from Valid V_{CC}		100	–	–	µs
t_{su}	Setup Time		60	–	–	ns
t_h	Hold Time		10	–	–	ns
t_{co}	Clock to Output		–	–	60	ns
t_{clkh}	Clock Pulse Duration, High		60	–	–	ns
t_{clkl}	Clock Pulse Duration, Low		60	–	–	ns

Table 2 - 0028Aisp-3192

Figure 5. Boundary Scan Waveforms



Pin Description

NAME	MQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 7	40 41 42 44 45 46 47 48	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
I/O 8 - I/O 15	50 51 52 54 55 56 57 58	
I/O 16 - I/O 23	60 61 62 64 65 66 67 68	
I/O 24 - I/O 31	70 71 72 74 75 76 78 79	
I/O 32 - I/O 39	80 81 82 83 84 86 87 88	
I/O 40 - I/O 47	89 90 91 92 93 94 96 97	
I/O 48 - I/O 55	98 99 100 101 102 103 104 106	
I/O 56 - I/O 63	107 108 109 110 111 112 113 114	
I/O 64 - I/O 71	116 117 118 119 120 121 122 123	
I/O 72 - I/O 79	124 126 127 128 129 130 131 132	
I/O 80 - I/O 87	133 134 136 137 138 139 140 141	
I/O 88 - I/O 95	142 143 144 146 147 148 149 150	
I/O 96 - I/O 103	151 152 154 156 157 158 159 160	
I/O 104 - I/O 111	162 163 164 166 167 168 169 170	
I/O 112 - I/O 119	172 173 174 176 177 178 179 180	
I/O 120 - I/O 127	182 183 184 186 187 188 189 190	
I/O 128 - I/O 135	192 193 194 196 197 198 199 200	
I/O 136 - I/O 143	202 203 204 206 207 208 209 210	
I/O 144 - I/O 151	212 213 214 216 217 218 219 220	
I/O 152 - I/O 159	222 223 224 226 227 228 230 231	
I/O 160 - I/O 167	232 233 234 235 236 238 239 240	
I/O 168 - I/O 175	241 242 243 244 245 246 248 249	
I/O 176 - I/O 183	250 251 252 253 254 255 256 258	
I/O 184 - I/O 191	259 260 261 262 268 264 265 266	
I/O 192 - I/O 199	268 269 270 271 272 273 274 275	
I/O 200 - I/O 207	276 278 279 280 281 282 283 284	
I/O 208 - I/O 215	285 286 288 289 290 291 292 293	
I/O 216 - I/O 223	294 295 296 298 299 300 301 302	
I/O 224 - I/O 231	303 2 3 4 5 6 7 8	
I/O 232 - I/O 239	10 11 12 14 15 16 17 18	
I/O 240 - I/O 247	20 21 22 24 25 26 27 28	
I/O 248 - I/O 255	30 31 32 34 35 36 37 38	
GOE0 and GOE1	195 and 185	Global Output Enable input pins.
TOE	215	Test output enable pin.
$\overline{\text{RESET}}$	53	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0, Y1 and Y2	43, 33, 205	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device.
Y3 and Y4	175, 165	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the I/O cells in the device.
BSCAN/$\overline{\text{ispEN}}$**	63	Boundary Scan Enable. Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
TDI/SDI*	23	Input - This pin performs two functions. It is the Test Data input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the isp state machine.
TCLK/SCLK*	73	Input - This pin performs two functions. It is the Test Clock input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
TMS/MODE*	13	Input - This pin performs two functions. It is the Test Mode Select input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine.
$\overline{\text{TRST}}$	225	Input - Test Reset, active low to reset the Boundary Scan State Machine.
TDO/SDO*	155	Output - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the isp data. When $\overline{\text{ispEN}}$ is high it functions as Test Data Out.
GND	9, 19, 39, 49, 69, 85, 95, 115, 125, 145, 161, 171, 191, 201, 221, 237, 247, 267, 277, 297	Ground (GND)
VCC	1, 29, 59, 77, 105, 135, 153, 181, 211, 229, 257, 287, 304	V_{CC}

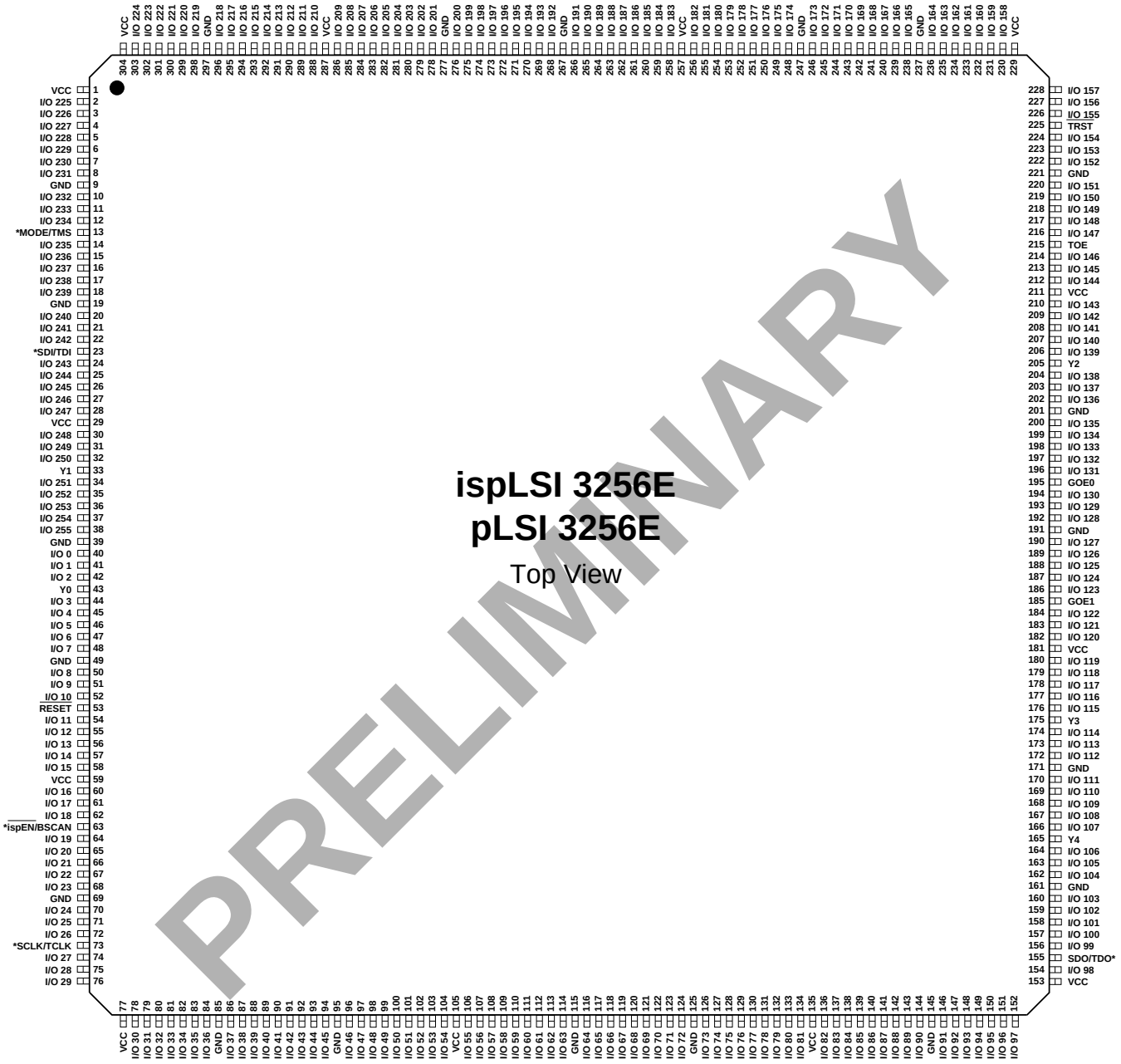
Table 2 - 0002/3256E

* ispLSI 3256E only

** $\overline{\text{ispEN}}$ for ispLSI 3256E only, NC for pLSI 3256E must be left floating or tied to Vcc, must not be grounded or tied to any other signal.

Pin Configuration

ispLSI and pLSI 3256E 304-pin MQFP



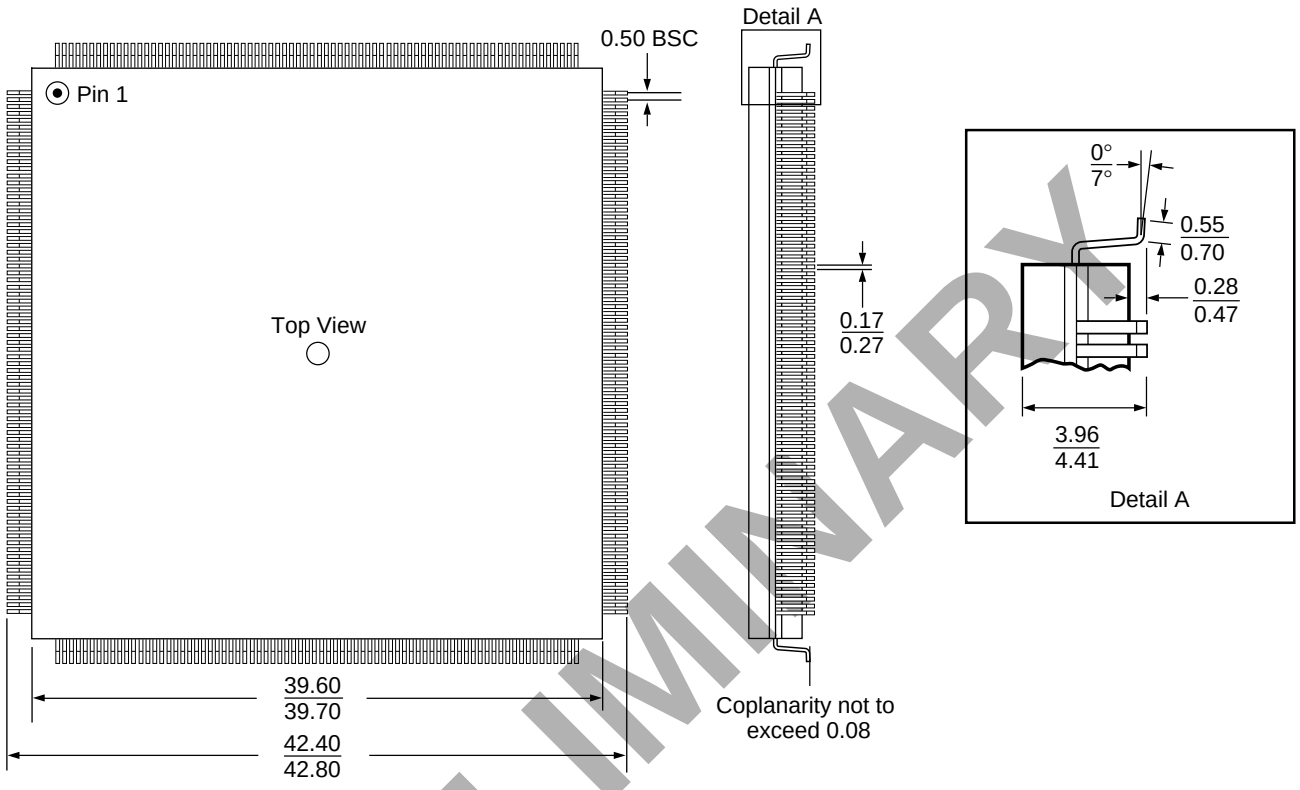
*Pins have dual function capability for ispLSI 3256E only.

304MQFP.3256E

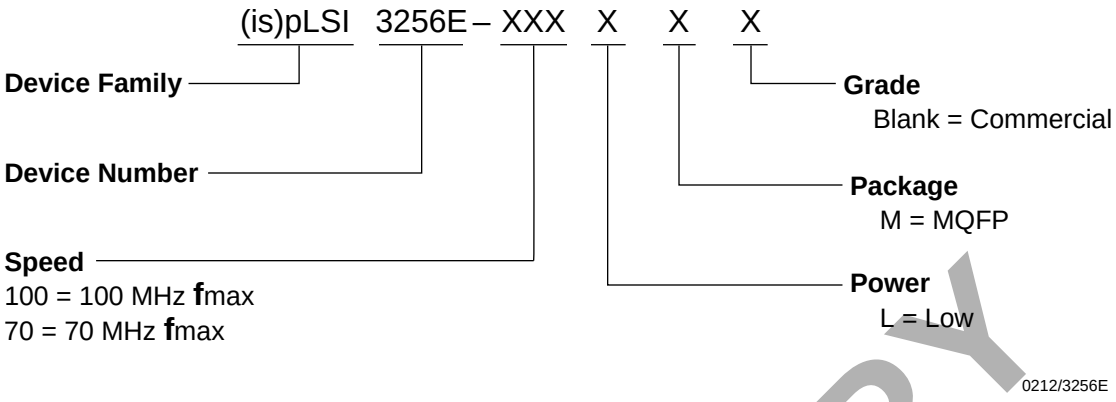
Package Diagram

304-Pin MQFP Package

Dimensions in Millimeters Min./Max.



Part Number Description



Ordering Information

Family	fmax	tpd	Ordering Number	Package
ispLSI	100	10	ispLSI 3256E-100LM	304-Pin MQFP
	70	15	ispLSI 3256E-70LM	304-Pin MQFP
pLSI	100	10	pLSI 3256E-100LM	304-Pin MQFP
	70	15	pLSI 3256E-70LM	304-Pin MQFP

Table 2- 0041/3256E

pDS+™ CUPL Software

Features

- **ispLSI® AND pLSI® DEVELOPMENT SYSTEM**
  - **— Supports ispLSI and pLSI 1000/E and 2000**
  - **— Upgrade to Support ispLSI and pLSI 3000**
- **INTEGRATED DEVELOPMENT ENVIRONMENT FOR MIXED-MODE DESIGN ENTRY**
  - **— CUPL Hardware Description Language (CUPL-HDL) Syntax Supports Boolean Equations, Truth Tables and State Machine Entry**
- **pDS+ CUPL FITTER**
  - **— Multi-Level Logic Synthesis**
  - **— Efficient Design Optimization and Minimization**
  - **— Automatic Mapping and Device Fitting**
  - **— Automatic Partitioning with High Utilization**
  - **— Predictable Performance**
- **INDUSTRY STANDARD PROGRAMMING FILE GENERATION**
  - **— Standard JEDEC Device Fuse Map**
- **PLATFORMS SUPPORTED**
  - **— Windows 3.1/Windows 95/Windows NT**
- **IN-SYSTEM PROGRAMMING SUPPORT**
  - **— ispCODE™ C Source Routines Included**
  - **— ISP Daisy Chain Download (PC Versions)**
  - **— ispATE™ Board Test Programming Utility**

Introduction

The pDS+ CUPL software from Lattice Semiconductor offers a powerful solution to fit high-density logic designs into Lattice's ispLSI and pLSI devices.

Design entry is made simple by using CUPL software from Logical Devices together with the pDS+ CUPL Fitter for design implementation. The CUPL software and pDS+ CUPL Fitter offer high-level, device independent design entry with efficient logic compilation, delivering unprecedented performance for the most complex designs.

Logical Devices

The easy-to-use, menu-driven CUPL software packages provide a complete pre-fit design environment. Using CUPL-HDL from Logical Devices, Inc., complex designs can be quickly and efficiently described using a combination of Boolean Equations, Truth Tables, State Machine syntax or other HDL descriptions. The HDL syntax allows design creation without regard to any specific device dependencies. The built-in functional simulator allows designs to be fully verified before device fitting. The menu driven environment makes design implementation as easy as clicking a mouse button.

pDS+ CUPL Fitter

The pDS+ CUPL Fitter for ispLSI and pLSI devices is completely integrated within the CUPL Software environment. The pDS+ CUPL Fitter provides hands-off design implementation through intelligent design optimization, logic partitioning, automatic place and route and fusemap generation with optional test vectors, in standard JEDEC format. Extensive top level design control is provided to optimize design implementation for speed and/or high device resource utilization.

Design Optimization & Logic Minimization

The pDS+ CUPL Fitter uses proprietary algorithms targeted for device specific features. The Fitter optimizes the design thoroughly, utilizing logic minimization, product term sharing and XOR functions whenever possible. In addition, the pDS+ CUPL Fitter supports multiple fitting strategies to obtain the best device utilization and performance.

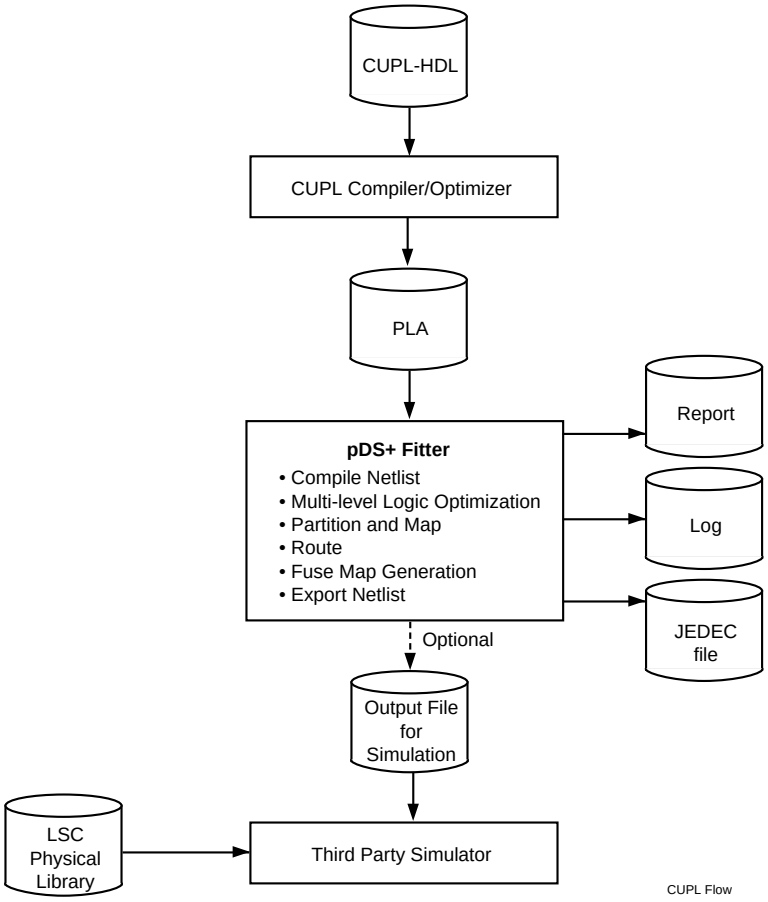
Automatic Partitioning

The pDS+ CUPL Fitter incorporates a powerful Automatic Partitioner for hands-free synthesis of a design into Generic Logic Blocks (GLBs). The partitioner takes full advantage of the device's powerful features such as the hard XOR function and product term sharing. The internal XOR can be utilized for Arithmetic functions, T-Type flip-flops, and on & off set optimization functions. The partitioner also makes extensive use of product term sharing. Product term sharing allows the fitter to efficiently use device resources by sharing product terms across multiple logic functions. These features combine to maximize device resource utilization and increase design performance.

LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-LATTICE; FAX (503) 681-3037; http://www.latticesemi.com

1996 Data Book.CD 7/96

Figure 1. pDS+ CUPL Fully Integrated Design Environment



Automatic Place and Route

Automatic place and route eliminates the need for manual editing and accelerates the design cycle. The Router automatically generates pinouts based on the optimal design implementation or user assigned pinouts.

The Router optimally interconnects signals between I/O cells and GLBs through the Global Routing Pool (GRP) and Output Routing Pool (ORP). It also performs GLB splitting and GLB output duplication to enhance routing.

The Extended Route option performs a comprehensive route to maximize device resource utilization and ensure efficient design implementation. The result is that small design changes won't cause expensive PC board re-work.

Design Parameter Control

Extensive design parameter control at the design entry level is possible with the pDS+ CUPL Fitter giving the user the option to optimize the design for maximum utilization and speed. Controls are specified using "Property" statements in the CUPL design file. These controls fall into two categories:

- — Fitter Controls
- — Design Implementation Controls
  - — Net Attributes
  - — Pin Attributes
  - — Path Attributes
  - — Symbol Attributes

Fitter Controls

Special properties can be passed to the pDS+ CUPL Fitter providing complete control over critical design considerations. Fitter control over design partitioning and routing optimizes the design for speed and/or device utilization. Here are a few of the powerful features:

Feature	Description
PART	Determines device type to be used.
PARAM_FILE	Allows user to specify attributes in a text file.
STRATEGY	Choice of AREA (default), DELAY or NO_OPTIMIZE. AREA optimizes device space, DELAY keeps GLB levels to a minimum and NO_OPTIMIZE does not reduce equations.
USE_GLOBAL_RESET	Causes global reset to use dedicated routing for reset.
MAX_GLB_OUT	Specifies maximum number of outputs from a GLB. Default is 4.
MAX_GLB_IN	Controls maximum number of inputs to a GLB. Default is 16 for 1K and 2K devices and 24 for 3K devices.
EFFORT	Controls optimization of partitioner.
EXTENDED_ROUTE	Choice of OFF (fixed) or ON (extended, default).
PIN_FILE	Specifies locked pin assignments.

Design Implementation Controls

Device controls are used for changing design parameters such as security. Some of these implementation controls are:

Feature	Description
ISP	Instructs Router to reserve in-system programming pins.
ISP_EXCEPT_Y2	Reserves all ISP pins except Y2 (ispLSI and pLSI 1016/E and 2032 only).
Y1_AS_RESET	Uses Y1 clock pin on ispLSI and pLSI 1016/E and 2032 as a global reset pin.
SECURITY	Sets the device security cell to prevent unauthorized fuse map read back.

Net Attributes

These properties control how the design is mapped into the specified features of the target device:

Feature	Description
CLK0-CLK2	Assigns a CLK signal to a dedicated CLK line.
IOCLK0-IOCLK1	Assigns a CLK signal to a dedicated IOCLK line if single fanout input pin.
FASTCLK	Fitter assigns CLK signal to CLK0-CLK2 or IOCLK0-IOCLK1.
SLOWCLK	Assigns the CLK signal to a GLB product term CLK.
PRESERVE	Prevents logic minimization on specified nets.
GROUP	Suggests grouping of functions in a GLB.

Pin Attributes

Feature	Description
CRIT	Specifies Output Routing Pool Bypass to minimize delay.
SLOWSLEW	Assigns slow slew rate on a specific I/O cell.
LOCK	Assigns device I/O pins to design I/O ports.
PULLUP	Specifies internal pull-up resistors.

Path Attributes

Feature	Description
SAP/EAP	Defines asynchronous paths to prevent signal duplication.
SCP/ECP	Defines critical paths to reduce delays.
SNP/ENP	Defines logic paths for no logic minimization.

Symbol Attributes

Feature	Description
REGTYPE	Determines where a register is to be placed (IOC or GLB).
PROTECT	Prevents removal of a primitive or a macro during minimization.
OPTIMIZE	Selects either hard or soft macros.

Parameter File

The pDS+ CUPL Fitter provides a parameter file feature which helps designers eliminate guesswork and optimizes the design for the right device. It allows the user to try a number of design implementation options using the design implementation controls in batch mode. The parameter file instructs the partitioner and the router on how to maximize both device utilization and performance.

The pDS+ CUPL Fitter also provides post-route equations showing exactly how the design is implemented in the selected device.

Fuse Map Generation

The pDS+ CUPL Fitter supports a device fusemap in standard JEDEC format. A security feature gives protection of proprietary designs from unauthorized duplication. The fitter also appends any design test vectors in JEDEC format to the device fusemap thus facilitating a quick, easy functional verification of a programmed device.

Design Verification

The pDS+ CUPL software supports functional simulation of all ispLSI and pLSI designs using the built-in CUPL functional simulator. The simulation test vectors can be combined into the JEDEC file for device testing in a programmer.

Complete post route design verification can also be performed using optional Viewlogic Viewsim, PROsim, or other third-party timing simulators. The pDS+ CUPL software generates the output file required for third-party simulation. Simulation libraries are available from Lattice Semiconductor for various PC and Sun-based CAE vendor tools. The Viewlogic PROsim simulator and Synario simulator are available from Lattice Semiconductor for the PC platform.

System Requirements (PC Platform)

- 486/Pentium™ IBM Compatible PC
- Operating System
  - MSDOS Version 4.x or Later
  - Windows 3.1
  - Windows NT
  - Windows 95
- 16 MB RAM with 30MB Hard Disk Space
- CUPL 4.4b or Later
- Parallel Printer Port for Software Key

Programmer Support

All devices in the ispLSI device families can be programmed while installed on the target circuit board. In-system programming can be performed using an ispDOWNLOAD™ Cable and PC, by an on-board microprocessor or by ATE systems during final board test.

All ispLSI and pLSI devices can also be programmed using third-party PLD programmers. The devices are currently supported by programmers from the following vendors:

Programmer Vendor	Model
Advin Systems	Pilot-U84
	Pilot-U40
	Pilot-GL/GCE
BP Microsystems	PLD-1128
	CP-1128
Data I/O	2900
	3900
	Unisite 40/48
Logical Devices	Allpro 40
	Allpro 88
SMS Micro Systems	Sprint Expert
Stag	System 3000
	ZL30A/B
System General	TURPRO-1/FX

High-pin count socket adapters are available from Emulation Technology, EDI Corporation and PROCON.

Product Ordering Information

Product Code	Description
pDS2190-PC1	Fitter for Logical Devices CUPL on PC Platform
pDS2190-3UP/PC1	3000 Family Upgrade for pDS2190-3UP/PC1
pDS1102-PC2	Viewlogic Library and Interface for PC
pDS3302-PC2	PROSim Simulator with Libraries
pDS1120-PC1	Synario Libraries and Interface
pDS1170-PC1	OrCAD Simulator Library and Interface

Maintenance*

pDS2190M-PC1	Maintenance for pDS2190-PC1
pDS1102M-PC2	Maintenance for pDS1102-PC2
pDS3302M-PC2	Maintenance for pDS3302-PC2
pDS1120M-PC1	Maintenance for pDS1120-PC1
pDS1170M-PC1	Maintenance for pDS1170-PC1

*One year of maintenance is provided with every product purchase.

Warranty/Update Service

- 90-day warranty on disk media
- One-year maintenance support included with purchase
- Annual maintenance agreement available

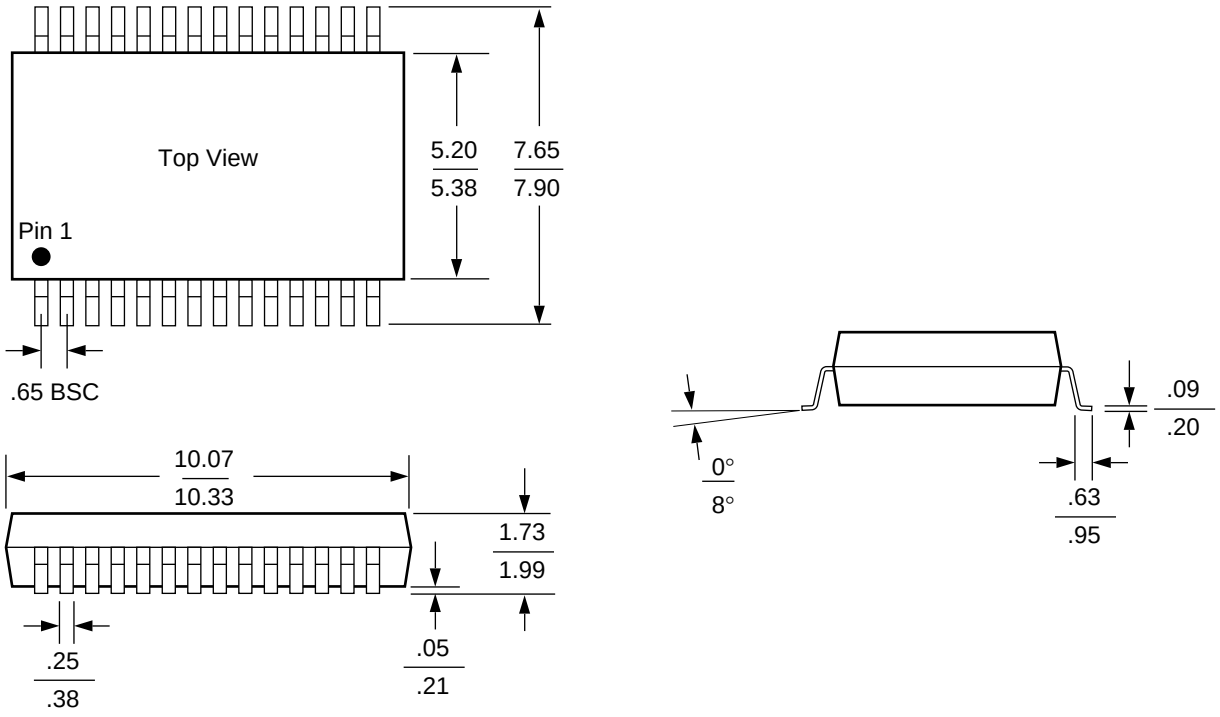
Technical Support Assistance

Hotline:	1-800-LATTICE (Domestic) 1-408-428-6414 (International)
BBS:	1-408-428-6417
FAX:	1-408-944-8450
email:	apps@latticesemi.com

Package Diagrams

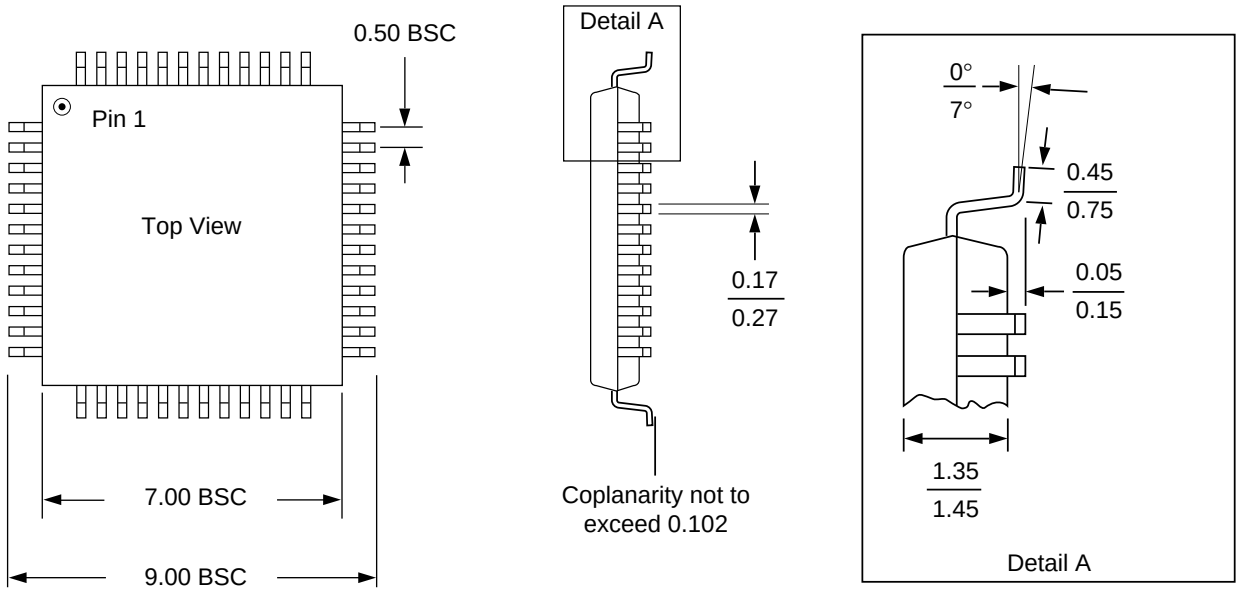
28-Pin SSOP Package

Dimensions in Millimeters MIN. / MAX.



48-Pin TQFP Package

Dimensions in Millimeters MIN. / MAX.



Package Diagrams

304-Pin MQFP Package

Dimensions in Millimeters MIN. / MAX.